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FPGA LUT delay degradation due to HCI: Experiment and simulation results

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ABSTRACT

Reliability of advanced VLSI circuits becomes more and more important as both product designers and manufactures relentlessly pursue technology advantages and stretch device physical limits to capitalize the consumer electronic market. In this paper, we focus on aging degradation of the Look-Up Table (LUT) on FPGAs. We have characterized the delay degradation of LUT dependent on the duty cycle and the frequency of stress signal. We have identified that the HCI degradation mechanism affects the fall delay more than the rise delay, it is related directly to the frequency stress and independent from the duty cycle. In addition, we built a model of the delay degradation due to HCI depending on switching frequency of stress signal and the aging time. Furthermore, we identified the relation between the effect of each aging transistor and the LUT delay for the HCI aging mechanism. This work is ideal for modelling the LUT aging mechanisms in FPGA.

1. Introduction

Reliability of advanced VLSI circuits becomes more and more important as both product designers and manufactures relentlessly pursue technology advantages and stretch device physical limits to capitalize the consumer electronic market. The most important aging mechanisms of a transistor are Negative/Positive Bias Temperature Instability (N/PBTI and Hot Carrier Injection (HCI). These mechanisms lead to device aging resulting in performance degradation and eventually design failure during the expected system lifetime [1,2].

Hot Carrier Injection (HCI) stress induces a degradation of the electrical parameters of MOSFETs under a dynamic stress mode [3]. Recent works have presented the main parameters and phenomena such as signal probability and frequency influencing the performance degradation of FPGAs [4]. Performance degradation of FPGAs due to HCI has been analyzed in [5] and some load balancing and alternate routing techniques have been proposed to improve the reliability of the FPGA chip. [6] gives an impact analysis of two different types of hard errors on FPGAs and a study of the performance degradation of FPGAs over time caused by Hot Carrier Effect (HCE) and NBTI. Stott et al. performed accelerated aging experiments on a pair of Altera Cyclone III FPGAs to estimate the impact of aging on FPGAs [7]. Using measurement technique from [8], they tested chips overvolted from 1.2 to 2.2 V and heated to 150 °C.

In this paper, we focus on HCI aging mechanism on FPGA. An analysis of experimental results to study the effect of aging on Look-Up Tables (LUTs) is presented in the following sections, then, an empirical model of HCI aging mechanism depending on the time of stress an,d the switching frequency is explained. Finally, we simulated this aging mechanism in order to model it on transistor level. This work is a basis in modelling the degradation of FPGAs depending on process operation.

2. Test set-up and circuits

A low cost auto-characterization test bench has been implemented on Altera Cyclone III 65 nm FPGAs [9]. This approach consists mainly of many Circuits Under Test (CUTs) and measuring circuits. A CUT has two phases of operation controlled by Mode input (Fig. 1):

1) *Mode* = 0: CUT operates in measure mode. During this mode, CUT makes a ring oscillator, and sends the output signal to the measuring circuit.
2) *Mode* = 1: CUT operates in stress mode, which takes the most of the experimental time. During this mode, the inputs of LUTs under test take the same state of the electrical stress signal, and the timing cannot be measured.

In this work, the test bench is turned under 1.8 V of core voltage (50% of the nominal voltage) to accelerate the aging of component, and about 316 K of junction temperature during 3000 h. We used the middle temperature because HCI is negatively correlated with temperature as carrier mobility decreases as temperature increases [10].

We tested 120 circuits that each one contains 9 LUTs configured as buffers. Three frequencies were applied as stress vectors: Low Frequency (*LF* = 25 Hz), Moderate Frequency (*MF* = 100 MHz) and High Frequency (*HF* = 402 MHz). For each frequency, input signal has a duty

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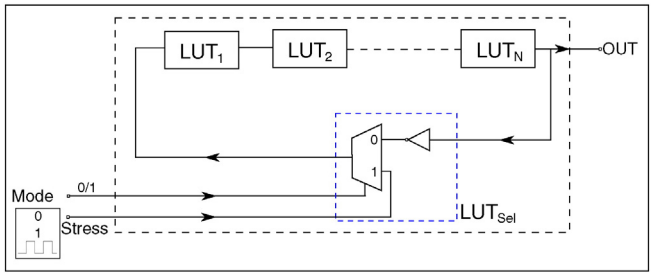

Fig. 1. Architecture of Circuit Under Test (CUT). Each CUT consists of 9 LUTs configured as buffers and implemented on a Logic Array Block (LAB) in the FPGA to reduce the impact of interconnection.

cycle from 10% to 90% with step of 20%. Two other static signals *GND* (DC0) and V_{DD} (DC1) were applied on other CUTs. Thus, 15 different types of stress signals were applied on 120 CUTs with 8 CUTs by stress type. As detailed in [9], we measure the CUT timing each 10 min and monitor the results in real-time.

The general architecture of our experimental methodology to characterize the degradation of LUT into FPGAs is given in Fig. 2.

Our test bench allows us to measure the duty cycle (α_m) and the frequency (f_m) of CUTs. Using these two parameters, we distinguish the fall and the rise delay of each CUT by the following expressions:

$$t_{Fall} = \frac{1-\alpha_m}{f_m} \quad (1)$$

$$t_{Rise} = \frac{\alpha_m}{f_m} \quad (2)$$

3. Experimental results

Figs. 3 and 4 illustrate the measured delay degradations of CUT stressed by different frequencies signals and duty cycles. It shows that HF increases the fall delay and the rise delay degradation for CUTs respectively about 20 ps and 14 ps. These figures show that HF stress signal affects the fall delay more than the rise delay. Actually, HCI is the responsible of this degradation.

TDDB was discounted as an active effect in these experiments because no hard failure of individual test cells was observed, and timing degradation levels are very repeatable across the many test cells (see error bars in Fig. 3).

A normal circuit will undergo both BTI and HCI under standard voltage switching conditions, so the circuits-based HCI/BTI measurement design must focus on isolating the effects of these two mechanisms, in order to examine the contributions of HCI to circuit degradation.

HCI is related to the current flowing through a transistor. In CMOS circuit the current flow only during switching, so HCI depends on switching frequency. Fig. 4a shows the degradation of fall delay of CUTs stressed by LF signal with different duty cycles. HCI aging

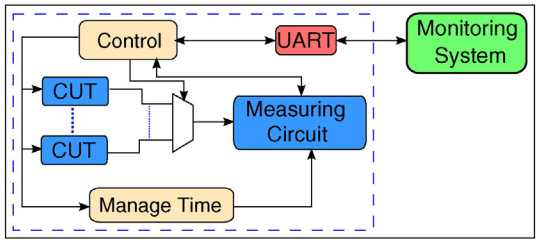

Fig. 2. General structure of our test set-up implemented on FPGA, which communicate with monitoring system using Universal Asynchronous Receiver Transmitter (UART) protocol.

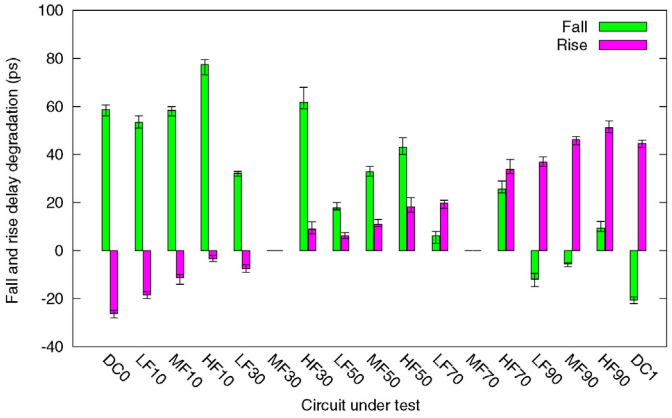

Fig. 3. Fall and rise delay degradation of CUTs after 3000 h of stress by different frequencies ($LF = 25$ Hz, $MF = 100$ MHz and $HF = 402$ MHz) and different values of α. DC0 and DC1 are static stress signals with respectively low and high level state.

mechanism can not be responsible of this degradation because the frequency of stress vectors is very low. Delay degradation can be explained by BTI aging who is sensitive to duty cycle but not to stress frequency. Thus, we used LF results as the reference of our measurement to determine the effect of HCI aging mechanism.

By subtracting the degradation due to stresses having the same duty cycles but different frequencies (Fig. 4b–a), we can extract the degradation due to frequency stress. Fig. 5 shows that the fall delay degradation due to frequency stress of the CUTs stressed by different duty cycle are approximately similar. Therefore, HCI is independent from the duty cycle of stress signal. The y axes of Fig. 6 represents in log scale the measured fall and rise delay degradation of CUTs turned under two frequencies HF and LF, while the x axis represents the stress time by hour in log scale. Based on these figures, we carried out the fitting model of the degradation due to HCI for 65 nm technology depending on the switching frequency and the aging time by using the power law expression:

$$\Delta t_{fall/rise} = A \times T^n \quad (3)$$

According to our results the power low exponents n equal 0.60 and 0.50 for the fall delay degradation of CUTs stressed by LF and HF signals respectively as shown in Fig. 6a. And n equal 0.57 and 0.48 for the rise delay degradation of these stressed by LF and HF respectively as observed in Fig. 6b.

These values are very close to the values given in [10] for the same technology: 0.44 for 470 MHz and 0.67 for 120 MHz.

4. Aging model for HCI

In digital circuit, for given voltage and temperature, the effects of HCI are generally considered as depending only on the number of switching cycles. For this reason, we draw the fall and rise delay degradation as a function of the number of cycle in Fig. 7a and b. We observe in these figures that the degradation of timing follows approximately a single power law for the two stress frequencies. Consequently, we propose a model of delay degradation due to HCI depending on the number of cycle ($f \times T$).

The fitting model of the fall delay degradation is determined using the following expression:

$$\Delta t_{Fall} = X \times (f \times T)^m \quad (4)$$

based on our experimental results we extract:

$$X = 4.6 \times 10^{-9}$$
$$m = 0.6$$

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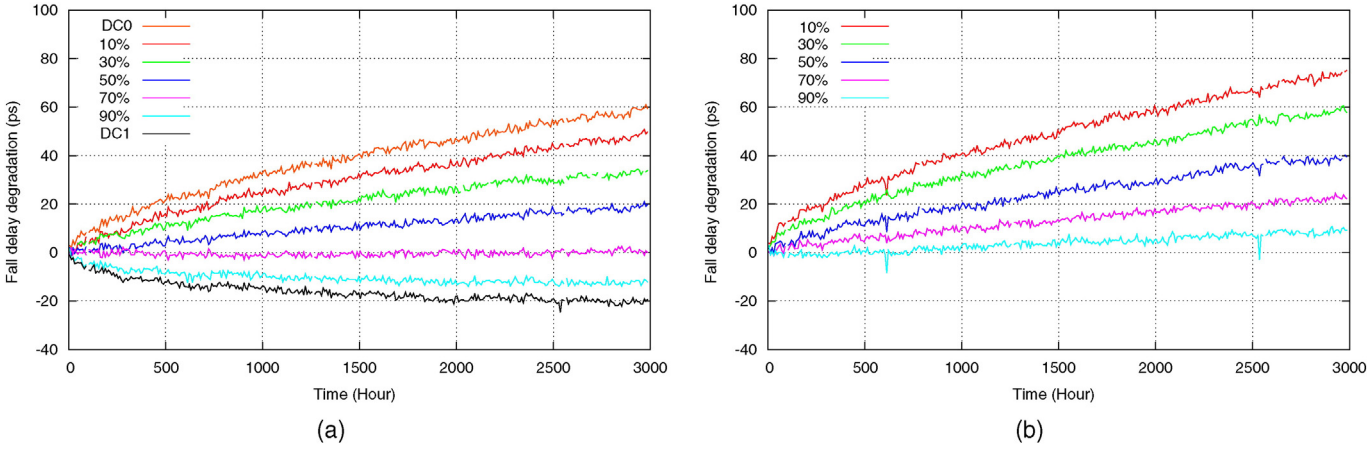

Fig. 4. Fall delay degradation of CUTs under low frequency stress ($f = 25$ Hz), with different values of duty cycle (0% to 100%), b) under high frequency stress ($f = 402$ MHz), with different values of duty cycle (10% to 90%).

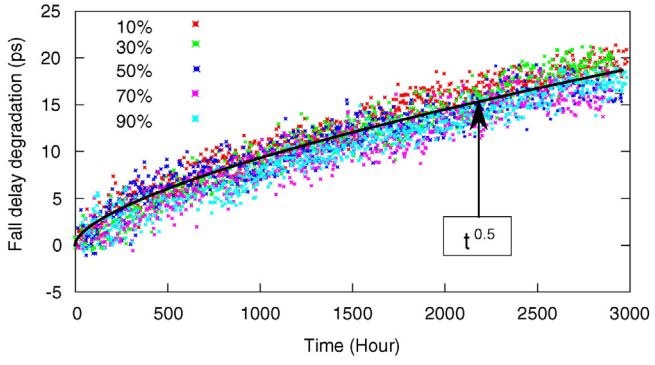

Fig. 5. Fall delay degradation due to HCI results for high frequency stress with different values of duty cycle. It shows that the HCI aging mechanism is independing from the duty cycle of stress signal.

The fitting model of the rise delay degradation due to HCI is:

$$\Delta t_{Rise} = Y \times (f \times T)^{m'} \tag{5}$$

where

$Y = 3.45 \times 10^{-9}$
$m' = 0.6$

5. Simulation

For HCI aging, as the trapped charge in the interface region of transistors increases, the threshold voltage V_{th} increases and the channel mobility μ decreases, resulting in an increase in gate propagation delay. These parameter shifts are calculated thus [2]:

$$\mu = \frac{\mu_0}{1 + \alpha \Delta N_{it}}; \tag{6}$$

$$\Delta V_{th} = \frac{q}{C_{ox}} \Delta N_{it} \tag{7}$$

where $\alpha = 2.4.10^{-12} cm^2$ according to [11].

From the two expression above, we determine the relation between the variation of the mobility μ and the degradation of threshold voltage using the formula:

$$\Delta V_{th} = f\left(\frac{\mu_0}{\mu}\right) = \frac{q}{\alpha C_{ox}}\left(\frac{\mu_0}{\mu} - 1\right) \tag{8}$$

A 2-inputs transmission gate LUT (Fig. 8) was modelled as it is a widespread circuit in FPGAs. A normal model BSIM4 of 65 nm CMOS technology [12] is used to simulate the transistor.

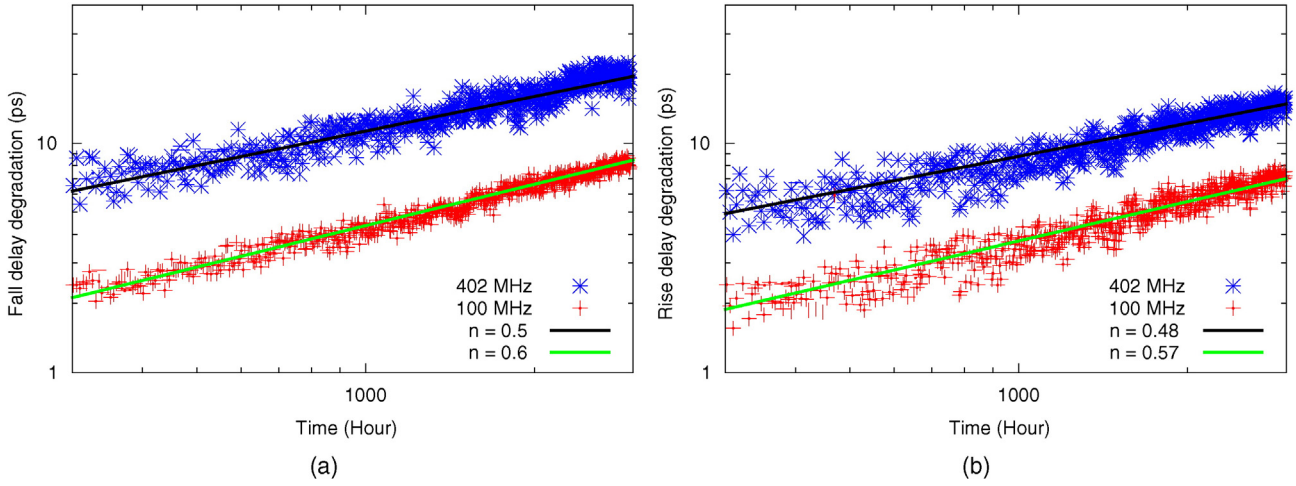

Fig. 6. Measured a) fall and b) rise delay degradation due to HCI results for two stress frequencies, with power law exponents (n). The decreasing exponent with increasing stress frequency is attributed to a faster saturation of the frequency degradation.

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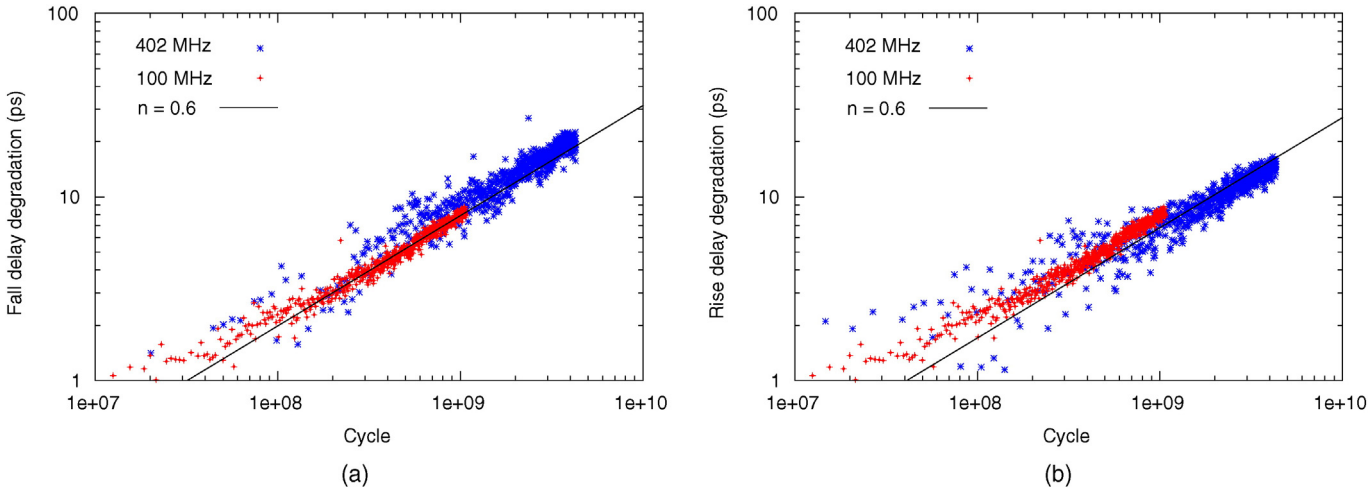

Fig. 7. Measured a) fall and b) rise delay degradation due to HCI results for two stress frequencies depending to the number of cycles. The cycle is calculate by multiplying the frequency stress and the aging time. The difference between the power law model (the line) and the measurements (the points) is clearly smaller than the measurement noise.

In a first group of simulations, we shifted the mobility of NMOS and PMOS transistors about 10%, ($\frac{\mu_0}{\mu} = 1.1$), which causes a shifting in the threshold voltage of NMOS and PMOS transistors about 3.58 mV and −3.77 mV in order to extract the influence of each transistors on the LUT timing. We analyzed the transistors effects on the delay from $IN1 \rightarrow OUT$ for different configurations of LUT. So, the first input $IN0$ is fixed as in the Table 1:

$IN1$ is switching to measure the fall and the rise delay of LUT.

When an input value is 0 ($IN1 = 0$), the upper gate TG4 will be opened as the value 0 is applied on the gate of PMOS transistor of TG4 and the value 1 is applied on the gate of its NMOS transistor through the inverter gate $INV1$. Consequently, $OUT0$ will propagate to the input of $INVOUT$ through the PMOS device of TG4, then to the output OUT through the NMOS of $INVOUT$.

Switching the input $IN1$ value to 1, the lower gate TG5 will be opened. Consequently, OUT_1 will propagate to the input of INV_{OUT} through the NMOS device of TG5, then to the output OUT through the PMOS of $INVOUT$.

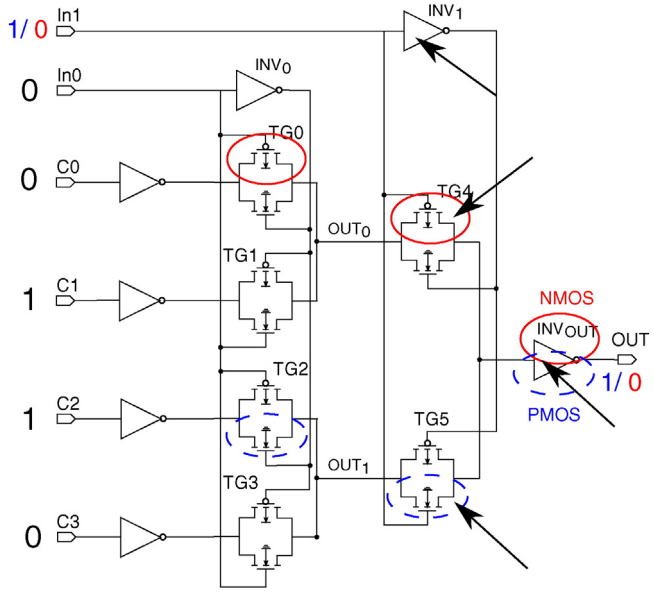

Fig. 8. 2-inputs LUT based on Transmission Gate (TG), configured as *XOR*. $IN0$ is set at low-state, thus the relation between $IN1$ and OUT is like a Buffer. The continous red circles represent which transistors are responsible to transmit a fall delay, while discontinous blue one represent these of the rise delay. Arrows represents the transistors are in HCI stress conditions.

When $IN1$ is switching, the current through NMOS and PMOS transistors of INV_1 change quickly, Thus a HCI stress is applied on both transistors. PMOS transistor of TG4 is in stress when the input of this transmission gate is on high-state ($OUT_0 = 1$), while the opposite case for the NMOS of TG5. No stress are applied on NMOS of TG4 and PMOS of TG5 because no current flows through these two transistors. HCI stress is applied on both transistors of INV_{OUT} as INV_1. These stressed transistors are represented by the arrows on the Fig. 8.

The timing results of LUT with different configurations are given in Fig. 9. Considering the configuration as *XOR BUFF*, this figure shows that the PMOS of TG4 and NMOS of INV_{OUT} affect strongly the fall delay degradation. However, this delay upgraded when PMOS of INV_{OUT} has a lower mobility μ, which causes a lower (more negative) threshold voltage.

The results obtained by the simulations show that the transistors which affect significantly the timing are those who transmitted the signal.

As mentioned in Section 3, the CUTs ware configured as *XOR* buffer, so the propagation delay is related to the second stage (TG4 and TG5) of LUT and the inverter INV_{OUT}. PMOS of TG4 and NMOS of INV_{OUT} are responsible to transmit a fall delay.

Based on this explanation we can relate the degradations obtained by simulations and the experiments using the following expression:

$$\Delta t_{fall} = \Delta t_{(PMOS\ \ TG4)} + \Delta t_{(NMOS\ \ INV_{OUT})} \tag{9}$$

where $\Delta t_{(X)}$ is the delay produced by the transistor X. Assuming the power law, we obtained:

$$\Delta t_{fall} = C \times \Delta P_{(PMOS\ \ TG4)} \times T^n + D \times \Delta P_{(NMOS\ \ INV_{OUT})} \times T^m \tag{10}$$

where, ΔP is the variation of the parameters of transistor such as the mobility μ and the threshold voltage V_{th}. Considering the rise delay

Table 1
OUT of LUT depends on their two inputs and the logic configuration.

$OUT = f(IN0, IN1)$	$IN0$	$OUT = g(IN1)$
XOR	0	Buffer
	1	Inverter
$\overline{XOR}$	0	Inverter
	1	Buffer

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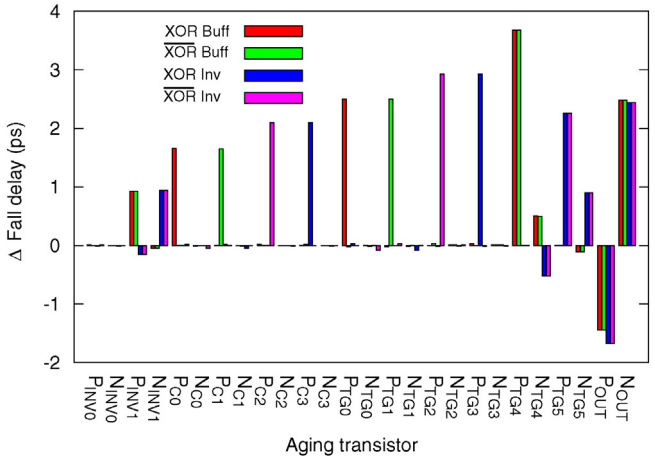

Fig. 9. Fall delay degradation of LUT ($IN1 \rightarrow OUT$) due to HCI of each transistor with different configurations. ($Buff : OUT = IN1; Inv : OUT = \overline{IN1}$).

degradation we focus on the NMOS of TG5 and PMOS of INV_{OUT} instead of PMOS of TG4 and NMOS of INV_{OUT} for the fall delay. So, the general form of the rise delay degradation due to HCI aging mechanism is:

$$\Delta t_{rise} = C' \times \Delta P_{(NMOS\ \ TG5)} \times T^{n'} + D' \times \Delta P_{(PMOS\ \ INV_{OUT})} \times T^{m'} \qquad (11)$$

Unfortunately, BTI stresses are not identical on PMOS of TG4 and of INV_{OUT}, because the first is in a transmission gate and the other in an inverter. The same situation occurs for the NMOS of TG5 and INV_{OUT}. Consequently, we cannot separate the variation in the parameters of the degraded transistors on the basis of the measurements.

6. Conclusion

Experimental and simulation results presented in this paper identify the effects of HCI aging mechanism to the LUT timing. We have identified that HCI aging mechanism depend on the frequency of input signals. This mechanism affects the fall delay more than the rise delay and it is independent from the duty cycle of the stress vector. A model of the delay degradation has been proposed in this paper depending on the switching frequency and the aging time.

Transient simulations have been made to extract the effects of each aging (HCI) transistor to the LUT timing, in order to model this mechanism at transistor level. However, we are not able to compute the transistors aging parameters values. Nevertheless, this work can be a help to model the degradation of LUT in FPGA at transistor level if the real structure of LUT is available.

References

[1] A.B. Kahng, Design challenges at 65 nm and beyond, Proceedings of the Conference on Design, Automation and Test in Europe, EDA Consortium 2007, pp. 1466–1467.
[2] X. Li, J. Qin, J.B. Bernstein, Compact modeling of MOSFET wearout mechanisms for circuit-reliability simulation, IEEE Trans. Device Mater. Reliab. 8 (1) (2008) 98–121.
[3] A. Bravaix, C. Guerin, V. Huard, D. Roy, J.-M. Roux, E. Vincent, Hot-carrier acceleration factors for low power management in DC-AC stressed 40 nm NMOS node at high temperature, Reliability Physics Symposium, 2009 IEEE International, IEEE 2009, pp. 531–548.
[4] Abdulazim Amouri, Florent Bruguier, Saman Kiamehr, Pascal Benoit, Lionel Torres, and Mehdi Tahoori. Aging effects in FPGAs: an experimental analysis. In Field Programmable Logic and Applications (FPL), 2014 24th International Conference, on pages 1–4. IEEE, 2014.
[5] S. Srinivasan, P. Mangalagiri, Y. Xie, N. Vijaykrishnan, K. Sarpatwari, FLAW: FPGA lifetime awareness, Proceedings of the 43rd Annual Design Automation Conference, ACM 2006, pp. 630–635.
[6] S. Srinivasan, R. Krishnan, P. Mangalagiri, Y. Xie, V. Narayanan, M.J. Irwin, K. Sarpatwari, Toward increasing FPGA lifetime, IEEE Trans. Dependable Secure Comput. 5 (2) (2008) 115–127.
[7] E.A. Stott, J.S.J. Wong, P. Sedcole, P.Y.K. Cheung, Degradation in fpgas: measurement and modelling, Proceedings of the 18th Annual ACM/SIGDA International Symposium on Field Programmable Gate Arrays, ACM 2010, pp. 229–238.
[8] Justin SJ Wong, Pete Sedcole, and Peter YK Cheung. A transition probability based delay measurement method for arbitrary circuits on fpgas. In ICECE Technology, 2008. FPT 2008. International Conference, on pages 105–112. IEEE, 2008.
[9] M. Naouss, F. Marc, Design and implementation of a low cost test bench to assess the reliability of FPGA, Microelectron. Reliab. 55 (9) (2015) 1341–1345.
[10] J. Keane, T.-h. Kim, X. Wang, C.H. Kim, On-chip reliability monitors for measuring circuit degradation, Microelectron. Reliab. 50 (8) (2010) 1039–1053.
[11] N. Hwang, L. Forbes, Hot-carrier induced series resistance enhancement model (hisrem) of nmosfet's for circuit simulations and reliability projections, Microelectron. Reliab. 35 (2) (1995) 225–239.
[12] Predictive technology model (ptm)[online] available: http://ptm.asu.edu.

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