HAOCHENG XIAO

1315 W. Dayton St
(+1)6083359975 ⋄ hxiao55@wisc.edu

EDUCATION

University of Wisconsin, Madison *Sept. 2019 - Present*
Research Master, Department of Electrical and Computer Engineering
Current GPA: 3.81

University of Science and Technology of China *Aug. 2015 - Jun. 2019*
Bachelor of Physics

PROJECTS IN PROGRESS

Surf-Pre: a Non-interfernce Routing for High-bandwidth Energy-Efficient NoCs *gem5/ garnet2.0/Parallel Benchmark* *March 2020 - Present*
Advisor: Prof. Joshua San Miguel
Providing strong performance isolation of applications with low fault-tolerance has been critical, and even gaining more attention when more and more hardware loopholes have been discovered recently. Previous work such as SurfNoc(Wassel et al., ISCA 13) could achieve non-interference communication across different domains with reasonable zero-load latency. However, those physical links are under-utilized, resulting a low saturation throughput. By enabling congested path to move in advance, our method achieved 20% bandwidth improvement with little area cost on a 8x8 mesh with 1VC/vnet/domain.

Global-Secure: Non-interference Routing with Global Information *gem5/ garnet2.0/Parallel Benchmark* *March 2020 - Present*
Advisor: Prof. Joshua San Miguel
This work is an extension of Surf-Pre. Since waves are adopted to be the traffic pattern of SurfNoc to ensure non-interference, global information could be transmitted with waves to help the routing decision and resource allocation. Surf-Pre is one specific instance of this method, which proves it's efficiency. With a redesign of both virtual channels(VC) and routing algorithm, a higher utilization of network resource is expected be achieved.

A Non-interfering Routing Design for Chiplet-based NoC System *gem5/garnet2.0/Java March 2020 - Present*
Advisor: Prof. Joshua San Miguel
Recently the popularity of breaking an SoC into smaller chiplets has been increasing due to SoC's increasing complexity and costs. A routing methodology for such system was proposed by Yin et al. in ISCA 18, ensuring deadlock-free routing in multi-chiplet systems. We added non-interference property into this system, and optimized the latency and path diversity of this network by generating new boundary router placement with an updated objective function.

SELECTED PAST PROJECTS

Mitigation of GPGPU L1D Cache Covert Channel Attack *CUDA/Microbenchmark/C++/ GPGPU-sim* *Fall 2019 CS 758*
This project aims at first reverse engineering L1D cache structure of GTX 1080 and then simulating the hardware mitigation mechanism on GPGPU-sim. I ran some micro-benchmarks on the real hardware and found L1D cache per SM to be non-linear mapped sector cache with 48 ways, 4 sets and 128-byte

cache line. I also implemented a naive mitigation mechanism based on run time performance counter and bypassing L1D cache.

Optimization of a Spectre Attack Mitigation *C++/Python/gem5* *Fall 2019 ECE/CS 752*
A Spectre attack mitigation, called InvisiSpec, was proposed by Yan et al. in MICRO 18. InvisiSpec stores speculative cache update in buffer until the validation point to mitigate Spectre attack. I proposed an improved mitigation that could enable speculative load/store operation result fill in cache before they are validated to avoid MSHR block and burst of cache eviction.

RISC-V based FPGA Simulation Platform for memory optimization *Verilog/Chisel*
Research Internship, University of Wisconsin, Madison *Jul.-Sept.,2018*
Advisor: Prof. Jing Li (now in University of Pennsylvania)
· Modified and mapped the RISC-V core Freedom to an FPGA
· Compared the memory access performance between this hardware platform with DDR4 and gem5 simulation result

SKILLS

Tools & Software	gem5, garnet2.0, GPGPU-sim, Vivado, Modelsim, PyTorch
Programming Languages	Proficient in C, C++, CUDA, Verilog, Java, Bash Familiar with Python, Matlab