HAOCHENG XIAO

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EDUCATION

The University of Edinburgh *Aug. 2021 -*
Ph.D., Computer Science *Advisor: Nigel Topham & Sam Ainsworth*
University of Wisconsin, Madison *Sept. 2019 - May. 2021*
Research Master, Electrical and Computer Engineering
Teaching Assistant *Aug. 2020 - Dec. 2020*
University of Science and Technology of China *Aug. 2015 - Jun. 2019*
Bachelor of Physics

PUBLICATION

Haocheng Xiao, Sam Ainsworth. Hacky Racers: Exploiting Instruction-Level Parallelism to Generate Stealthy Fine-Grained Timers. Proceedings of the Twenty-Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2023

PAST PROJECTS

A Non-Interfering Lookahead Routing for Secure Networks-On-Chip(NoC) *gem5/ garnet2.0/Parallel Benchmark* *March 2020 - April 2021*
◦ Implemented SurfNoc(ISCA 13), the non-interference routing scheme on gem5-garnet2.0 as baseline
◦ Proposed zebra system to efficiently arrange non-interference flit traffic wave
◦ Devised multiple schemes within zebra to in advance release and bypass the virtual channels on congested path, and achieve fully adaptive routing
◦ Achieved a 20% bandwidth improvement with little area cost on a 8x8 mesh with 1VC/vnet/domain.

A Non-interfering Routing Design for Chiplet-based NoC *gem5/garnet2.0/Java*
March 2020 - April 2021
◦ Implemented non-interference property to a multi-chiplet NoC
◦ Optimized the boundary router and turn restriction placement algorithm introduced by Yin et al. in ISCA 18, exploring more path diversity
◦ Introduced a scheme to choose path dynamically based on some global information

Mitigation of GPU Cache Covert Channel Attack *CUDA/Microbenchmark/C++/ GPGPU-sim* *Fall 2019 CS 758*
◦ Reverse Engineered L1 data cache in NVIDIA GTX1080 using micro-benchmarking
◦ Established a covert channel based on L1-D cache contention on both real hardware and GPGPU-sim
◦ Implemented a naïve protection mechanism on GPGPU-sim

Optimization of a Spectre Attack Mitigation *C++/Python/gem5* *Fall 2019 ECE/CS 752*
◦ Replicated the spectre attack on gem5
◦ Implemented a mitigation that enables speculative load/store operation result fill in cache before they are validated to avoid MSHR block and burst of cache eviction

SKILLS

Tools & Software	gem5, garnet2.0, GPGPU-sim, Vivado, Modelsim, PyTorch
Programming Languages	Proficient in C, C++, CUDA, Verilog, Java, Bash Familiar with Rust, Python, Matlab
Relevant Courses	Advanced Comp Arch(I & II), Advanced Topics on Comp Arch, Intro-Progm Langs&Compilers, Operating System, Database