HAOCHENG XIAO

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EDUCATION

University of Wisconsin, Madison *Sept. 2019 - Present*
Research Master, Department of Electrical and Computer Engineering
Current GPA: 3.72

University of Science and Technology of China *Aug. 2015 - Jun. 2019*
Bachelor of Physics

PROJECTS IN PROGRESS

Surf-Pre: a Non-interfernce Routing for High-bandwidth Energy-Efficient NoCs *gem5/garnet2.0/Parallel Benchmark* *March 2020 - Present*
- Implemented SurfNoc(Wassel et al., ISCA 13), the non-interference routing scheme on gem5-garnet2.0
- Devised a scheme to release the virtual channels on congested path in advance
- Achieved a 20% bandwidth improvement with little area cost on a 8x8 mesh with 1VC/vnet/domain.

A Non-interfering Routing Design for Chiplet-based NoC System *gem5/garnet2.0/Java*
March 2020 - Present
- Implemented non-interference property to a multi-chiplet NoC
- Optimized the boundary router and turn restriction placement algorithm introduced by Yin et al. in ISCA 18, exploring more path diversity
- Introduced a scheme to choose path dynamically based on some global information

SELECTED PAST PROJECTS

Mitigation of GPGPU L1D Cache Covert Channel Attack *CUDA/Microbenchmark/C++/GPGPU-sim* *Fall 2019 CS 758*
- Reverse Engineered L1 data cache in NVIDIA GTX1080 using micro-benchmarking
- Established a covert channel based on L1-D cache contention on both real hardware and GPGPU-sim
- Implemented a naïve protection mechanism on GPGPU-sim, and measured performance variation with and without protection

Optimization of a Spectre Attack Mitigation *C++/Python/gem5* *Fall 2019 ECE/CS 752*
- Replicated the spectre attack on gem5
- Implemented a mitigation that enables speculative load/store operation result fill in cache before they are validated to avoid MSHR block and burst of cache eviction

RISC-V based FPGA Simulation Platform for memory optimization *Verilog/Chisel*
Research Internship, University of Wisconsin, Madison *Jul.-Sept.,2018*
- Modified and mapped the RISC-V core Freedom to an FPGA
- Compared the memory access performance between this hardware platform with DDR4 and gem5 simulation result

SKILLS

Tools & Software	gem5, garnet2.0, GPGPU-sim, Vivado, Modelsim, PyTorch
Programming Languages	Proficient in C, C++, CUDA, Verilog, Java, Bash Familiar with Python, Matlab
Relevant Courses	Advanced Computer Architecture(I & II), Advanced Topics on Computer Architecture, Intro-Progm Langs&Compilers