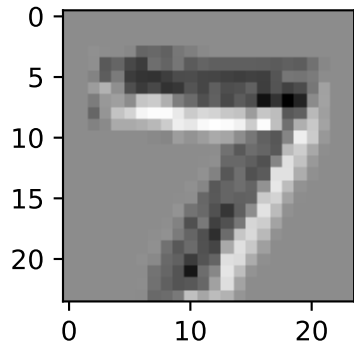
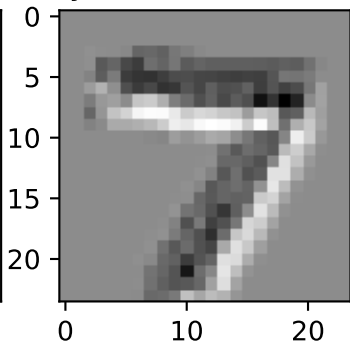


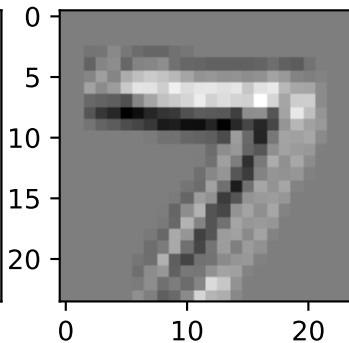
VHDL, Channel=0



Python, Channel=0



VHDL, Channel=31



Python, Channel=31

