Designing resistor for f1 and f2 values,

for a $f_1 = 1500\,Hz$

assume, $C = 10nF$

$$f_1 = \frac{1.45}{(R_A + 2R_B)C}$$

let $R_A = 48k$, $R_B = 24k$

$$f_1 = \frac{1.45}{(48k + 2 \times 24k)10n}$$

$f_1 = 1.51\,Hz \simeq 1.5Hz$

Thus, $\boxed{R_A = 24k\Omega}$ $\boxed{R_B = 48k\Omega}$

for $f_2 = 3000Hz$

assume $C = 10nF$

$$f_2 = \frac{1.45}{[(R_A \| R_C) + 2R_B]C}$$

$R_A = 24k\Omega$, $R_B = 48k\Omega$

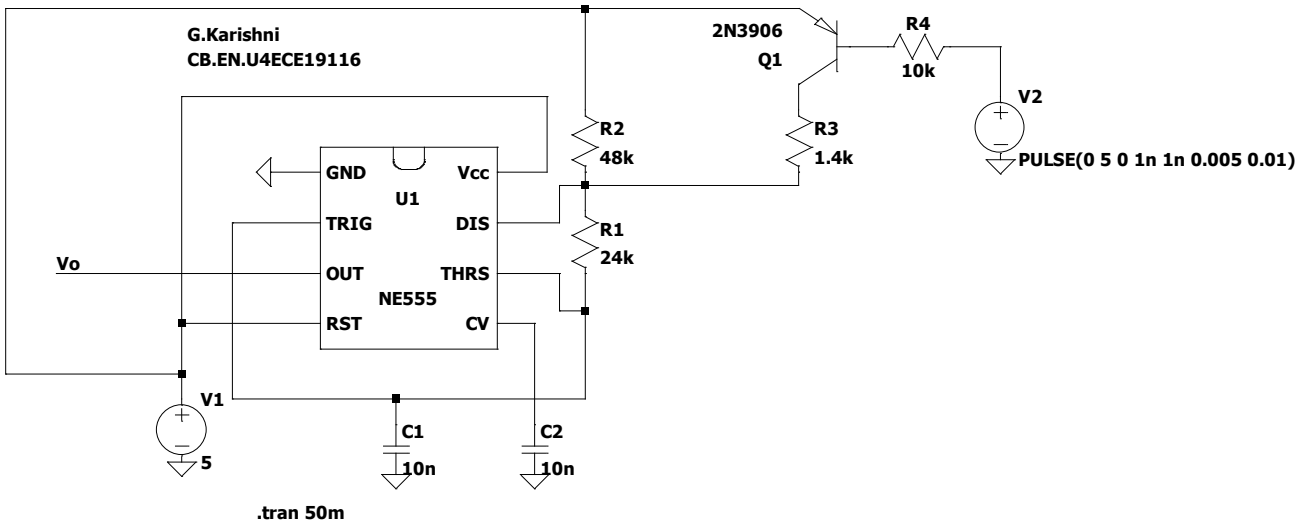
let $R_C = 1.4\,k\Omega$

$$f_2 = \frac{1.45}{[(24k \| 1.4k) + 2 \times 24k]\,10n}$$

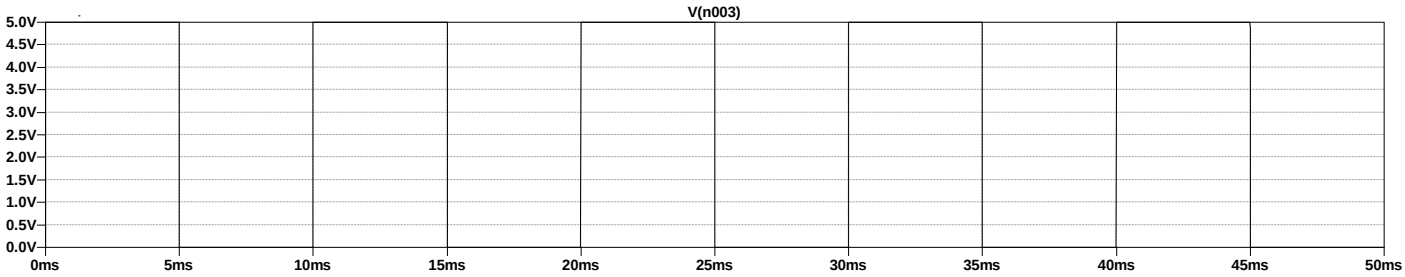
$f_2 = 2.93 \simeq 3Hz.$

Thus, $\boxed{R_C = 1.4\,k\Omega}$

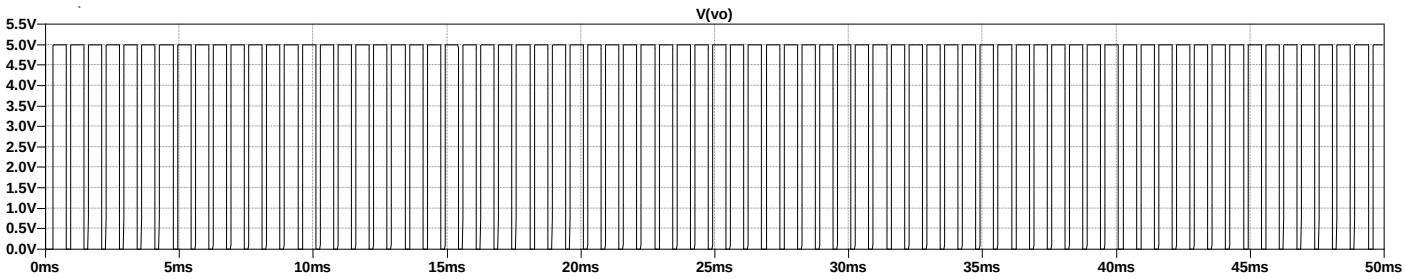
Frequency Shift Keying Modulation circuit



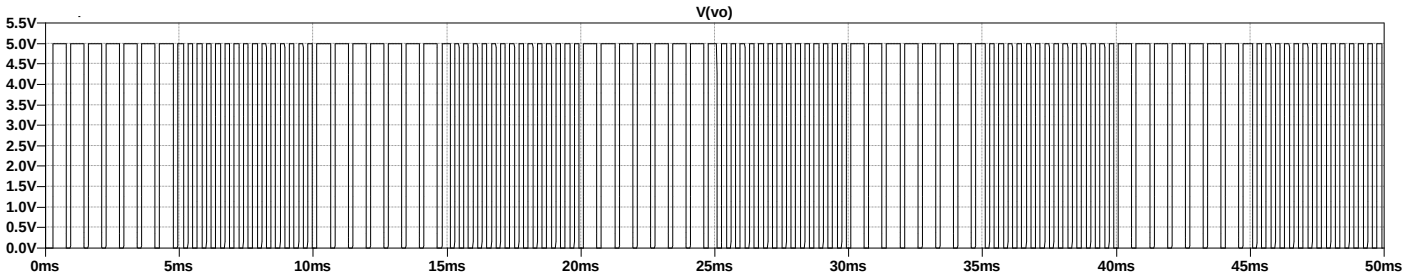
Message signal



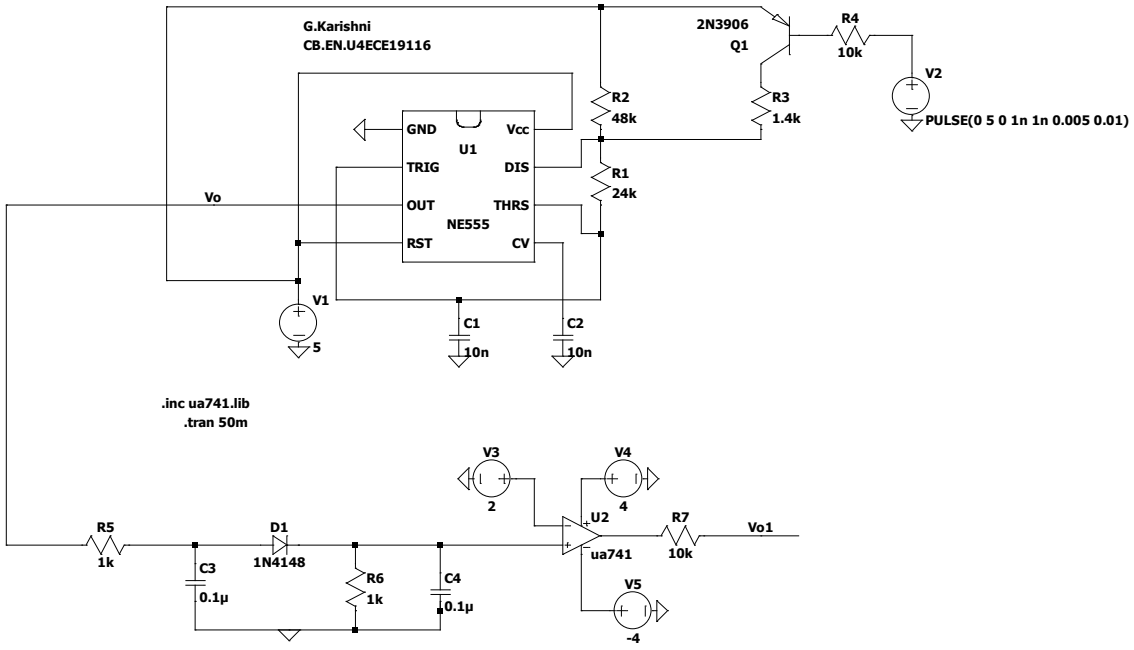
Carrier signal



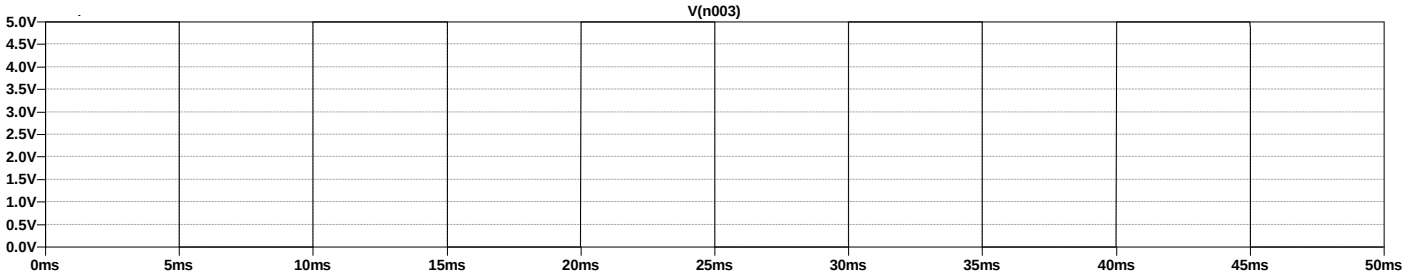
FSK output



Frequency Shift Keying Demodulation circuit



Message signal



Demodulated signal