Embedded Computer Architecture 2 - Filters

Gonçalo Camelo Neves Pereira - s2203731 Remi Jonkman - s1563599

February 2, 2019

Assignment 1

In this Assignment a general parallel FIR filter was designed. The system accepts parallel input and outputs serially.

Source Code 1: General FIR filter

```
-------------------------------------------------------------------------------
-- Assignment 1, Parallel FIR filter with N=6
-------------------------------------------------------------------------------
fir h x = foldl (+) 0 (zipWith (*) x h)
```

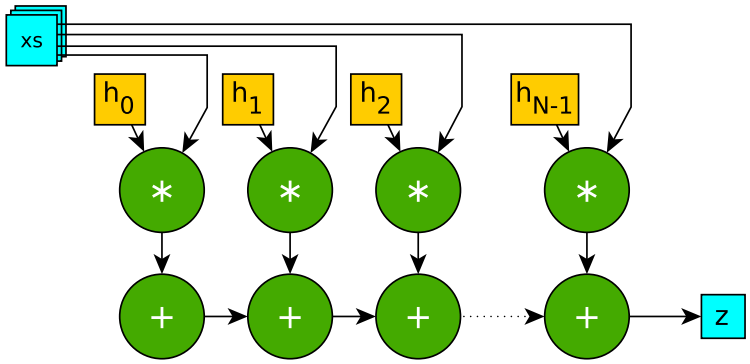


Figure 1: Structure of a general FIR filter

In Figure 1 is the expected RTL schematic for this filter and in Figure 2 is the obtained RTL schematic. It can be seen 6 outputs being loaded into multipliers which have on the other end its coefficient and after that the output of the multipliers is then summed, which translates to the desired architecture.

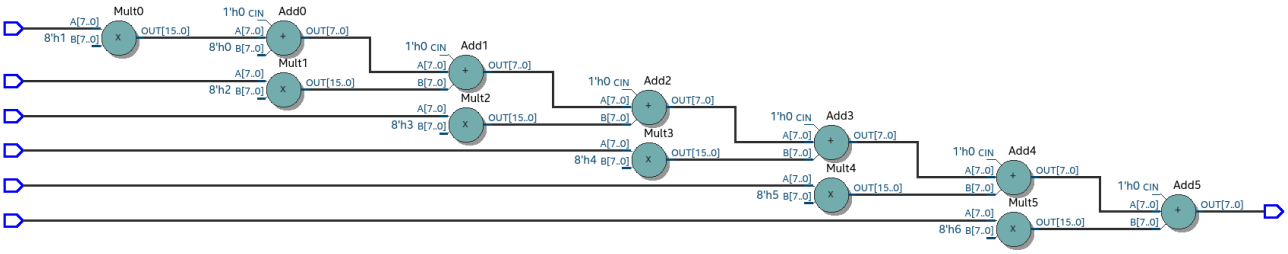
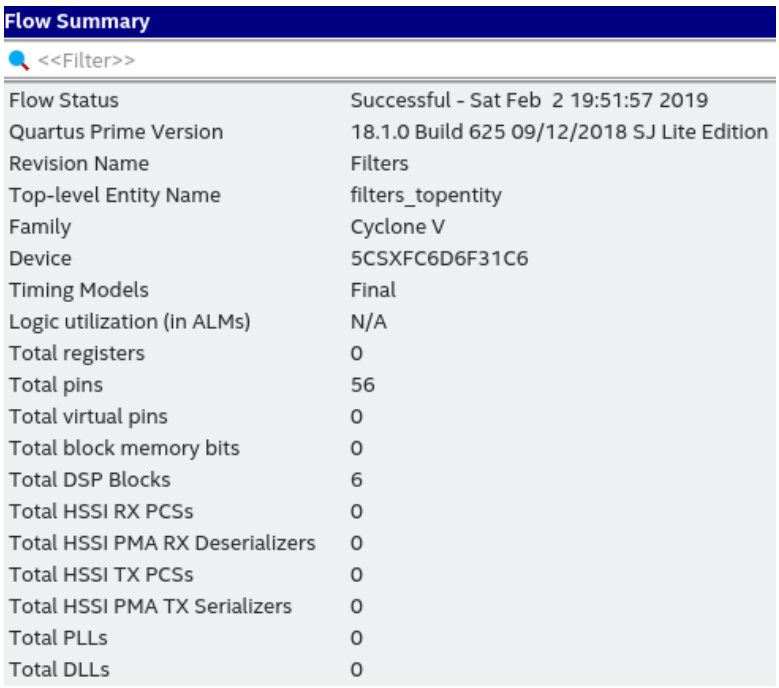


Figure 2: RTL Schematic

Then in Figure 3 it can be confirmed that 6 DSP blocks (multipliers) were used and 56 pins which translates to 6 inputs of 8 bits = 48 pins and 8 bits output which sums to 56 pins.



Flow Summary

<<Filter>>

Flow Status	Successful - Sat Feb 2 19:51:57 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	0
Total pins	56
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	6
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 3: Flow Summary

Assignment 2

In this assignment a larger low-pass filter is implemented that works with decimal numbers. Since the previous design was type independent, the same structure could be used so it was just a matter of using the provided decimal coefficients and the system scaled well.

Source Code 2: Larger FIR filter using Assignment 1 architecture

```
-------------------------------------------------------------------------------
-- Assignment 2, Larger General FIR filter with N=100 and decimal
-------------------------------------------------------------------------------
fir1_100 = fir filterCoef
```

For the Flow Summary on Figure 4 it can be seen that since there are now 100 coefficients there are also 100 DSP Blocks (multipliers) also the number of pins can be noted to be an extremely high quantity which leads to implemntation issues that will be solved in the next assignment.

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Feb 1 19:30:38 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	0
Total pins	1,818
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	100
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 4: Flow Summary

This time the RTL schematic, present in Figures 5 and 6, is not as straight-foward to analyse as the previous assignment that is due to the fact that decimal numbers are in play but it carries the same computation, so it's not relevant to analyse. Key point to note is the redundant component usage.

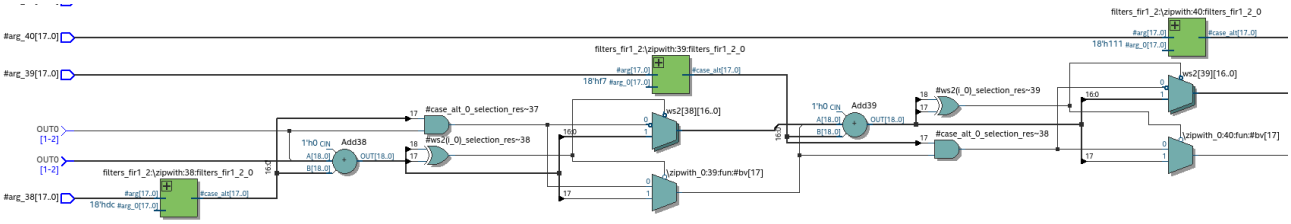


Figure 5: RTL Schematic - Top View

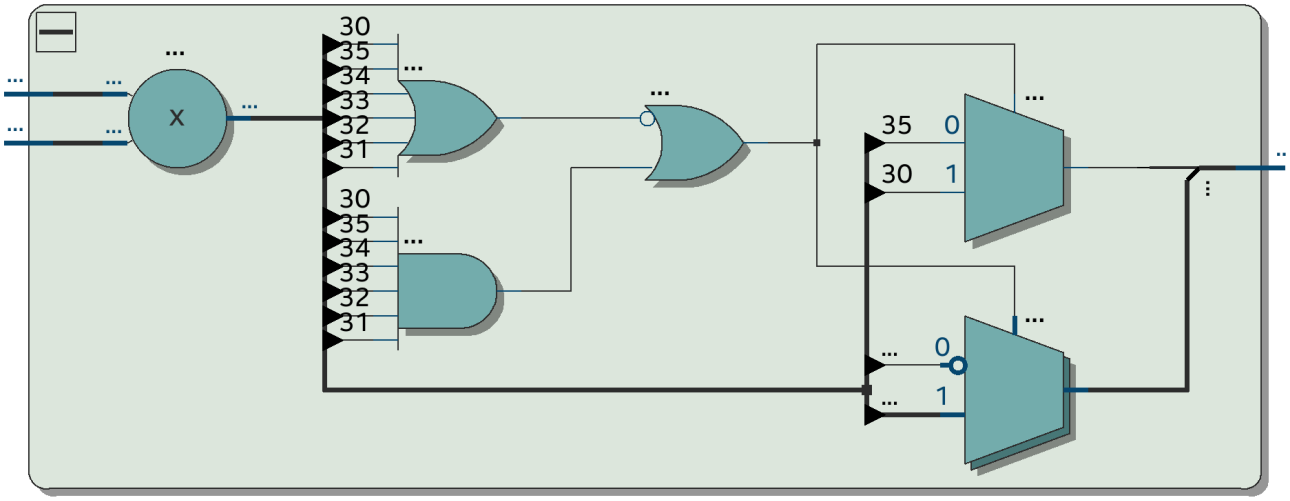


Figure 6: RTL Schematic - Sub Components (marked as green on Top View)

Assignment 3

In previous assignments it can be seen that when scaling the filter size the number of pins grows linearly and that can become difficult to implement and to manage. In this assignment the input is taken one at a time to reduce the pin number. A representation of the new architecture is depicted on Figure 7.

Source Code 3: FIR filter with serial input

```
--------------------------------------------------------------------------------
-- Assignment 3, A serial input FIR filter (using registers)
--------------------------------------------------------------------------------
fir_reg h u x = (u', z) where
    u' = x +>> u
    z = fir h u
```

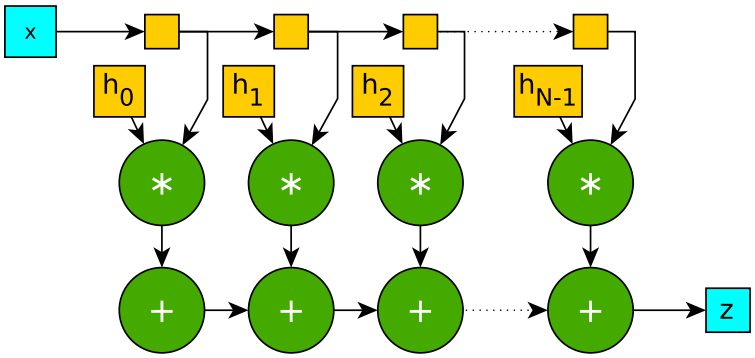


Figure 7: Filter Structure

In this case a Mealy machine is designed in order to store previous input values that are taken as the machine state and those are shifted every time a new value comes in.

Using this new architecture it can be seen that the number of pins was reduced. In the Flow Summary on Figure 8 it can be observed the reduction of pin number to 18 compared to assignment 1 which had 56. This is due to the input and out put signals which have 8 bits each and two new signals that are intrinsic to the behavior of this implementation. This new signals are *clock* and *reset*, the first sets the pace of the mealy machine and the second allows the reset of the system to its original state. The number of registers can be also easily understood since there are 6 inputs of 8 bits each which evaluates to 48 bits and thus 48 registers.

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Feb 1 21:02:40 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	48
Total pins	18
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	6
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 8: Flow Summary

In Figures 9 and 10 it can be noted that the system is identical other than the added registers successfully solving the issue with high pin numbers, however this comes at the cost of area and component number.

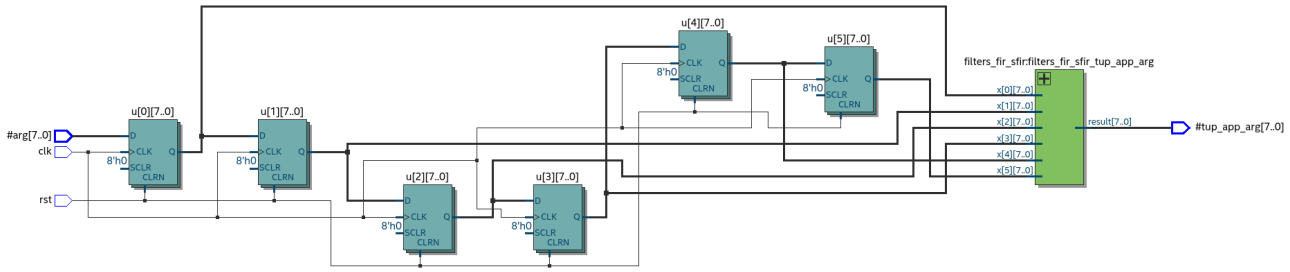


Figure 9: RTL Schematic - Top View

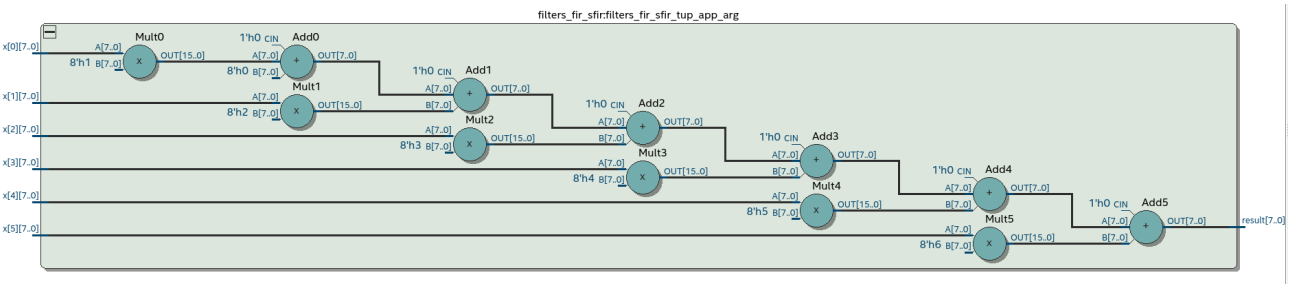


Figure 10: RTL Schematic - Sub Component (marked as green on Top View)

Assignment 4

Similar to assignment 2 the design used in assignment 3 will be scaled to analyse possible issues with its structure when up-scaled.

Source Code 4: FIR filter with serial input

```
-------------------------------------------------------------------------------
-- Assignment 4, A Larger serial input FIR filter
-------------------------------------------------------------------------------
fir2_100 = mealy (fir_reg filterCoef) (repeat 0)
```

In Source Code 4 the larger system is defined using the structure from the previous assignment and using the provided 100 decimal values like before.

In the Flow Summary present in Figure 11 it can be seen a high amount of registers which are avoiding the high pin number of the design however this is not ideal also. The multiplier number is also high, as expected, 100. However the pin number is at a reasonable number, 38 which is easily manageable.

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Feb 1 23:03:11 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	1800
Total pins	38
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	100
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 11: Flow Summary

In Figures 12 and 13 it can be seen that there is a high quantity of registers in the design which has the same issues discussed before about the high number of multipliers and adders.

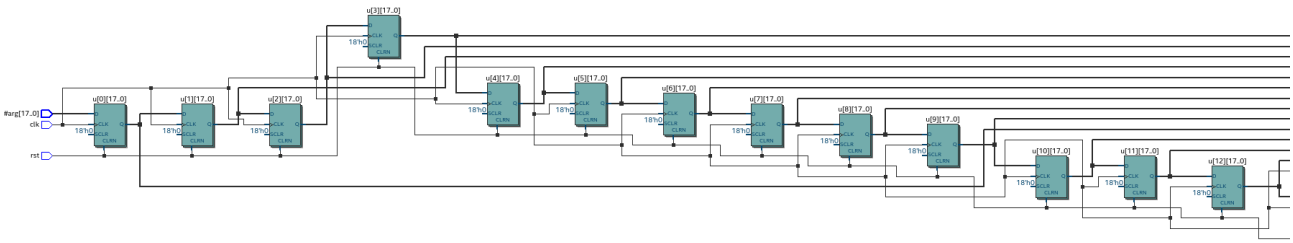


Figure 12: RTL Schematic - Top View (Cutted)

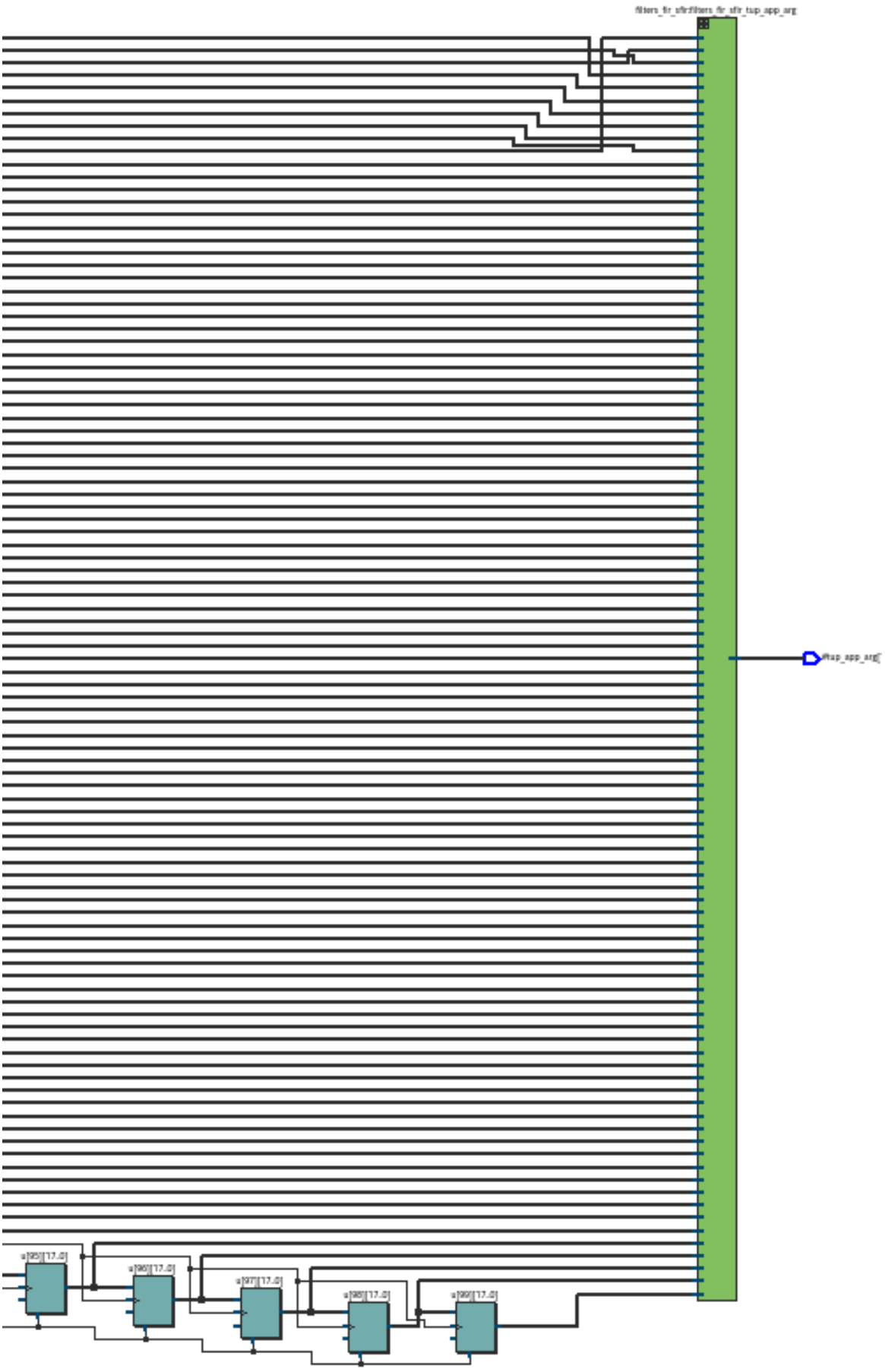


Figure 13: RTL Schematic - Register connections to the FIR filter

In Figure 14 it can be seen that the structure is the same compared to assignment 2 although it also has the same issue, a high component number.

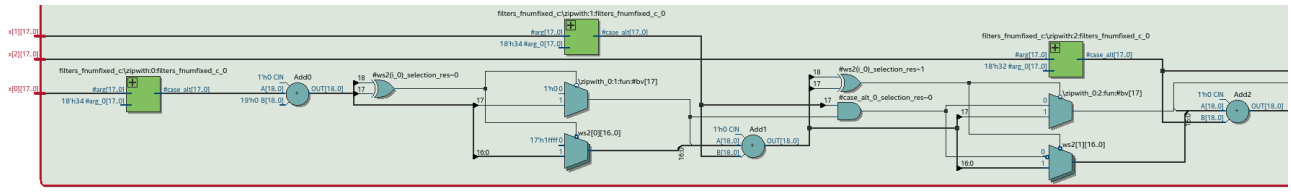


Figure 14: RTL Schematic - Sub Component (marked as green on Top View)

In Figure 15 it can be seen the output of the system when applied a sine wave which two visible different frequency components, and it can be seen that the high frequency components were filtered.

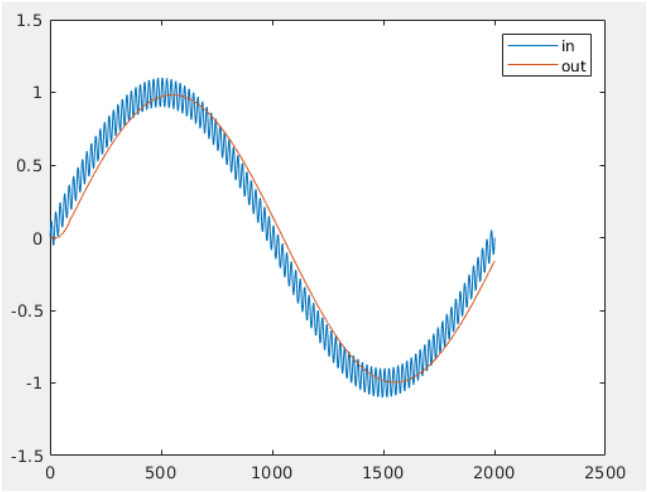


Figure 15: Input and output signals

Assignment 5

In this assignment the number of components will be halved since it can be seen that the given coefficients are symmetric. The first half of coefficients can be used to compute the second half of the output and thus the same multipliers can be used by summing values which are being multiplied by the same coefficient.

Source Code 5: FIR filter with symmetric coefficients

```
-------------------------------------------------------------------------------
-- Assignment 5, A Symmetric serial input FIR filter
-------------------------------------------------------------------------------
fir_sym h u x = (u', z) where
    u' = x +>> u
    w = zipWith (+) (takeI u) (takeI (reverse u))
    z = fir h w
```

In Source Code 5 a similar architecture is used than before other than the fact that the input is being taken as reversed to sum the first to the second half.

It can be seen in Figure 16 that the number of DSP blocks has halved as expected.

Flow Summary	
<<Filter>>	
Flow Status	Successful - Fri Feb 1 22:57:45 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	48
Total pins	18
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	3
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 16: Flow Summary

The same structure is present in Figure 12 and 18 except for the adders that are used to sum the first to the second half of the input and the number of multipliers.

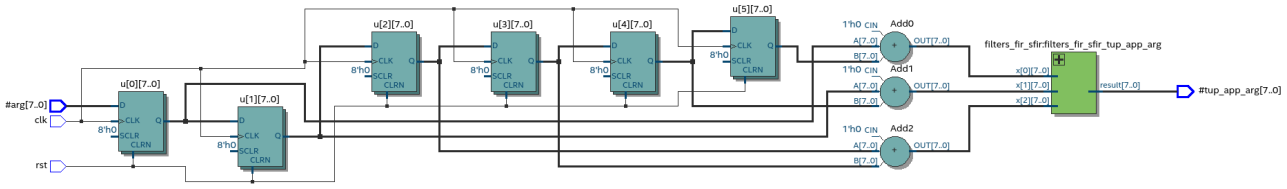


Figure 17: RTL Schematic - Top View

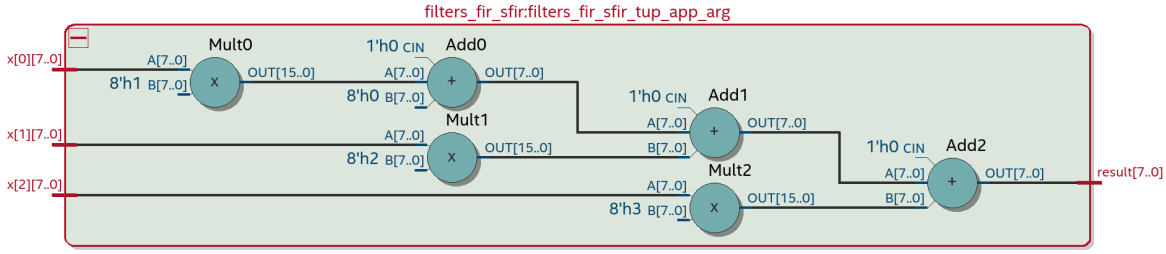


Figure 18: RTL Schematic - Sub-Component

Moreover the combinational path is reduced comparing to assignment 1 since the data is computed in parallel.

Assignment 6

In this assignment the previous structure is scaled up like it was done with previous designs.

Source Code 6: FIR filter with symmetric coefficients

```
-------------------------------------------------------------------------------
-- Assignment 6, A Larger Symmetric serial input FIR filter
-------------------------------------------------------------------------------
fir3_100 = mealy (fir_sym (takeI filterCoef)) (repeat 0)
```

Like before, longer numbers were loaded.

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Feb 1 23:54:29 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	1800
Total pins	38
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	50
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 19: Flow Summary

And it can be seen again that the component number was greatly reduced.

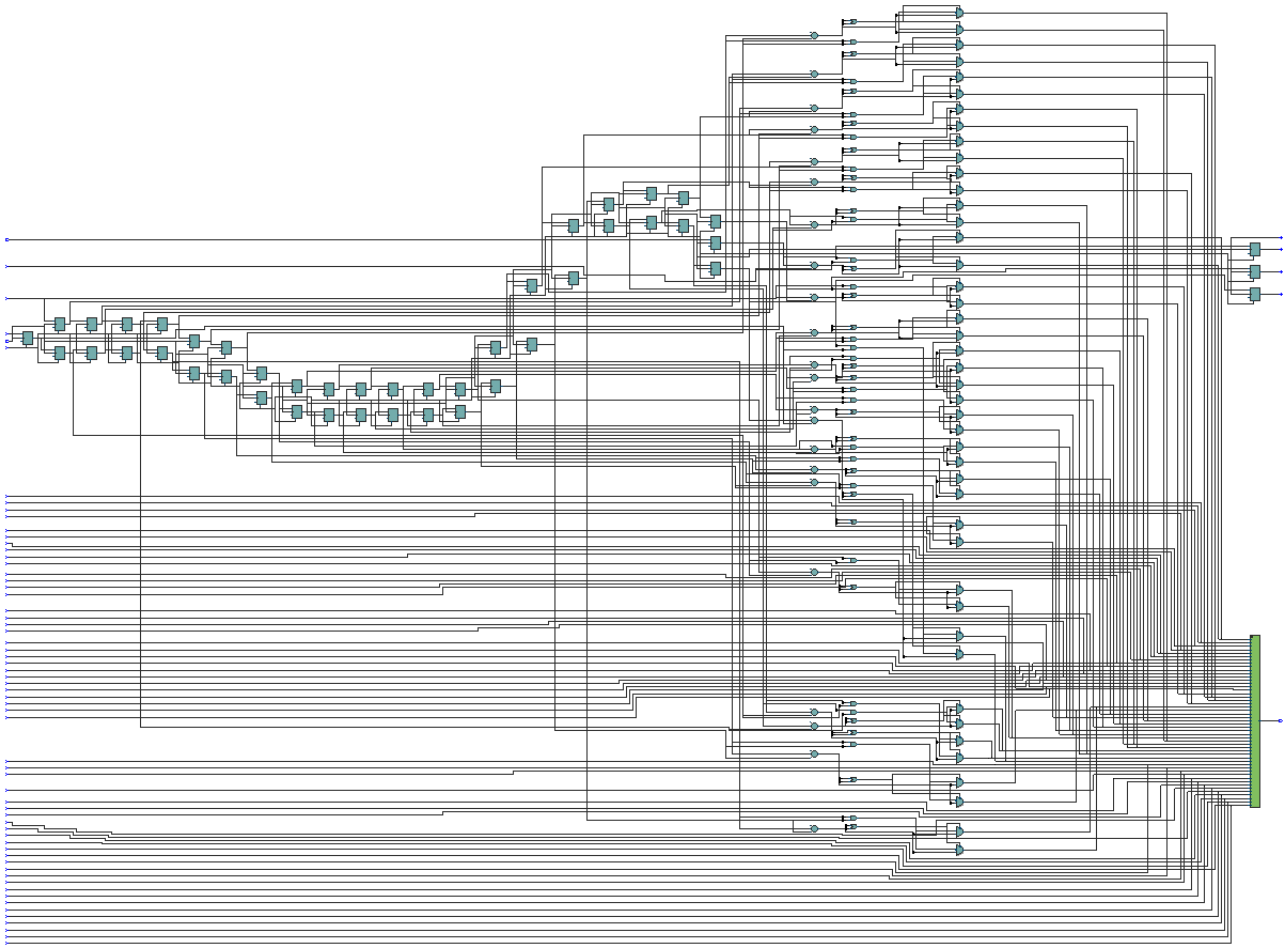


Figure 20: RTL Schematic - Top View

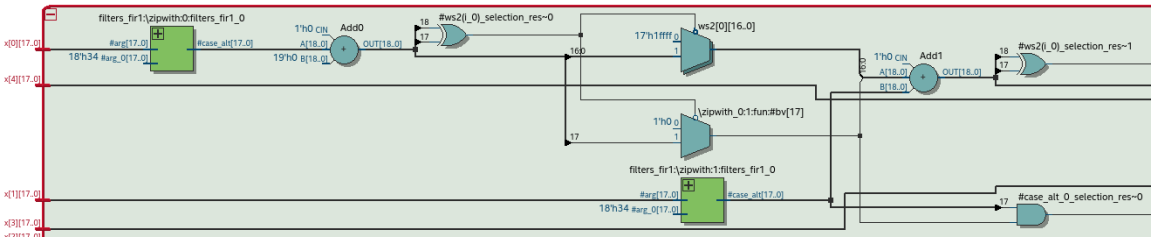


Figure 21: RTL Schematic - Structure of FIR filter

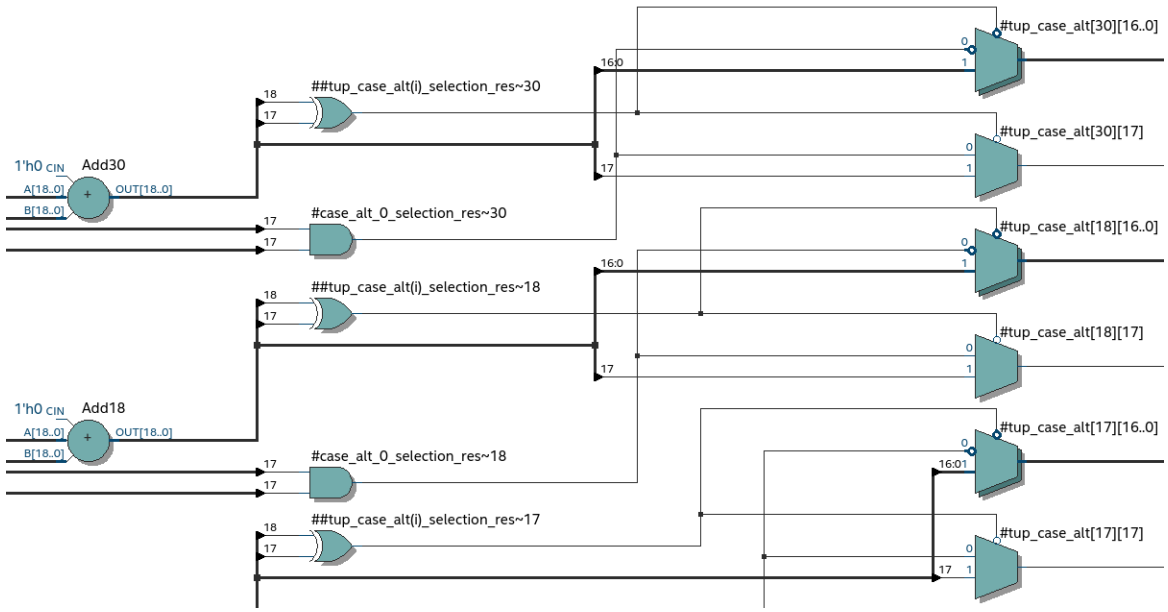


Figure 22: RTL Schematic - Inner Structure

Assignment 7

In this assignment the previous the aim is to reduce the combinational path by moving the registers to the end of the structure.

Source Code 7: Transformed FIR filter with symmetric coefficients

```
-------------------------------------------------------------------------------
-- Assignment 7, A Transformed Symmetric serial input FIR filter
-------------------------------------------------------------------------------
fir_sym_t h u x = (u', z) where
    m = map (*x) h
    w = m ++ (reverse m)
    s = (zipWith (+) (init w) (tail u)) ++ ((last w):>Nil)
    u' = s
    z = head u
```

To accomplish this the direction of all lines were reversed, the input and the output were interchanged and every junction was replaced by an adder and vice versa.

Flow Summary

<<Filter>>

Flow Status	Successful - Sat Feb 2 23:53:52 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	Filters
Top-level Entity Name	filters_topentity
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	48
Total pins	18
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	3
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Figure 23: Flow Summary

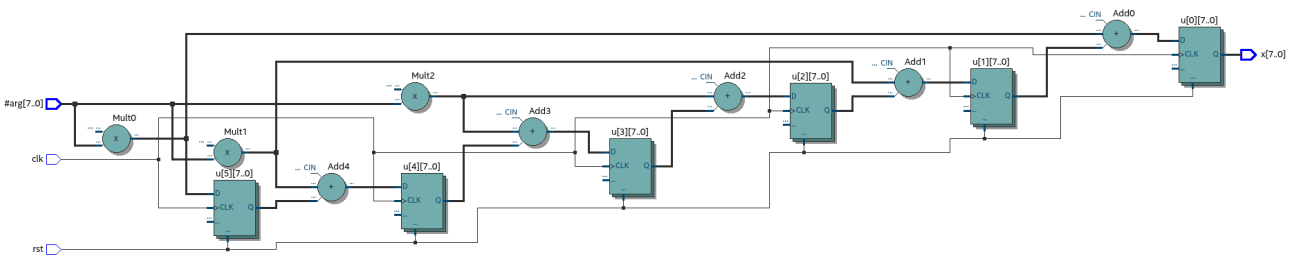


Figure 24: RTL Schematic - Top View