Jig Tests

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The Jig Tests are used with the IC Test Jig inserted in the UUT socket of the Flip Chip Test System. The jig is a short single-width PCB with a ZIF IC socket to hold digital ICs up to 28 pins that are 0.3 to 0.6 inches wide. On-board headers and power pin selection jumpers allow VCC and GND to be connected directly to the power and ground pins of the IC being tested.

Special test files having the prefix "JIG" have been created to test SN7400-series ICs that are commonly used in PDP-8/L and PDP-8/I computers. This document provides a brief description of each "JIG74xx.TST" file.

Test File	Latest Version	Description
JIG7400.TST	v00	SN7400N test vectors to individually test each of the four 2-input NAND gates. Based on Vince's original 74H00.TST file. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7402.TST	v00	SN7402N test vectors to individually test each of the four 2-input NOR gates. The test concept is based on the JIG7400 test but modified for a NOR gate logic function. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7404.TST	v00	SN7404N test vectors to individually test each of the six inverters. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7408.TST	v00	SN7408N test vectors to individually test each of the four 2-input AND gates. Based on the 7400.TST file but with opposite outputs. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7410.TST	v00	SN7410N test vectors to individually test each of the three 3-input NAND gates. Concept is like the 7400.TST file. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7432.TST	v00	SN7432N test vectors to individually test each of the four 2-input OR gates. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7440.TST	v00	SN7440N test vectors to individually test each of the two 4-input NAND gates. Based on Vince's original 7440.TST file. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7453.TST	v00	SN7453N test vectors to individually test each of the four AND gates within the AND-OR-INVERT structure. The expander pins are not tested. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7453A.TST	v00	SN7453N test vectors to test the AND-OR-INVERT structure using all 256 possible input permutations. The expander pins are not tested. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7474.TST	v00	SN7474N test vectors to individually test all functions of each of the two D-Type Edge-Triggered Flip-Flops. Insert the VCC jumper at 28 & GND jumper at 7.
JIG7493.TST	v00	SN7493N test vectors to individually test the 1-bit counter (QA) and 3-bit counter (QD, QC, QB) separately. **Insert the VCC jumper at 5 & GND jumper at 24**.