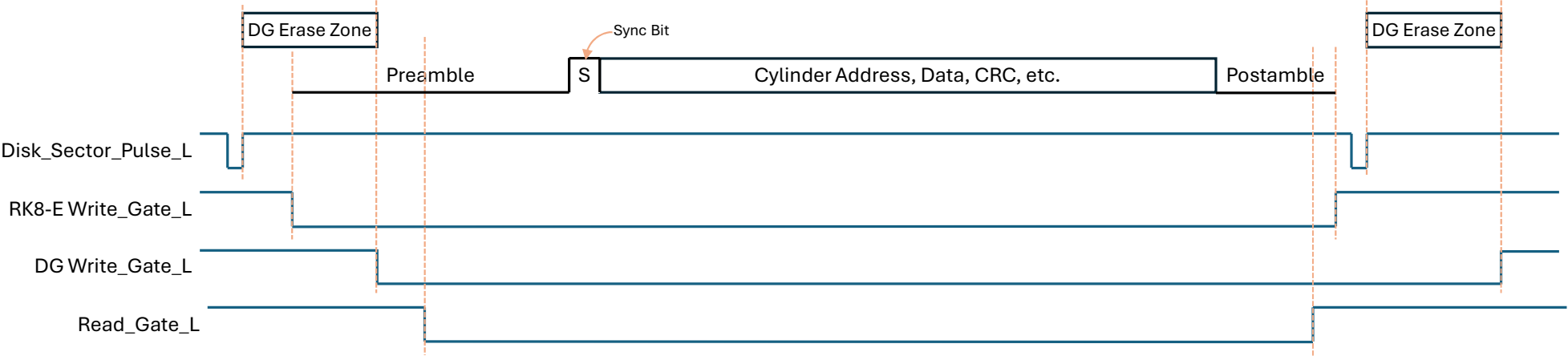
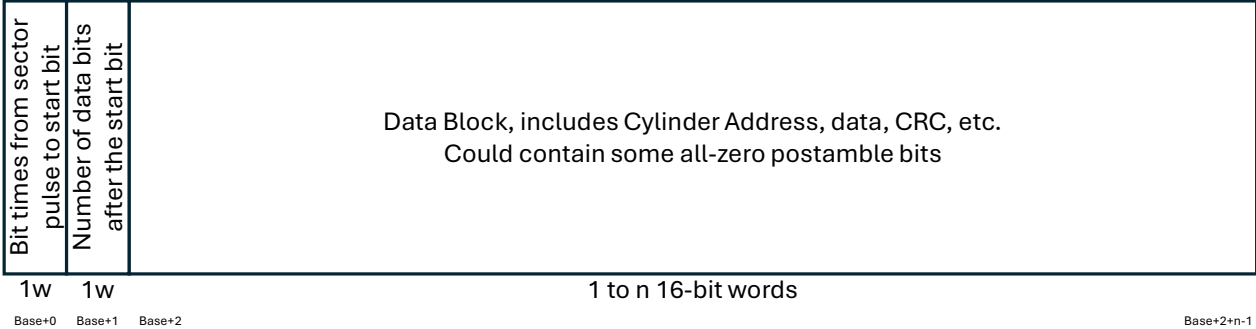
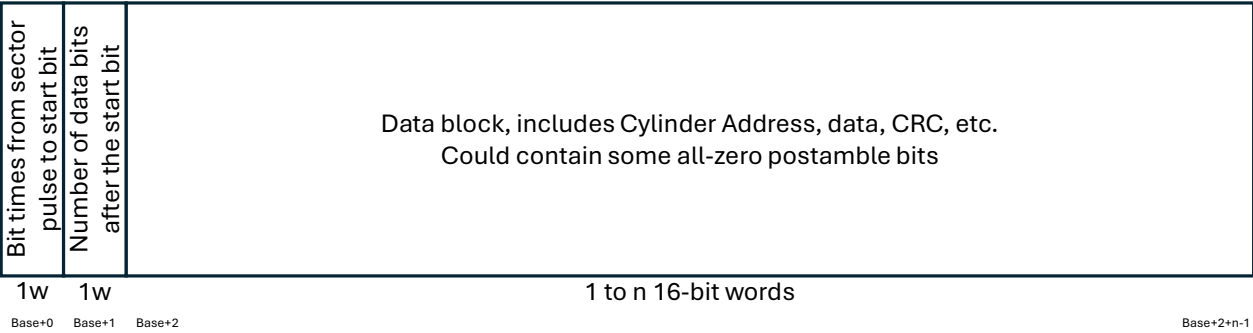


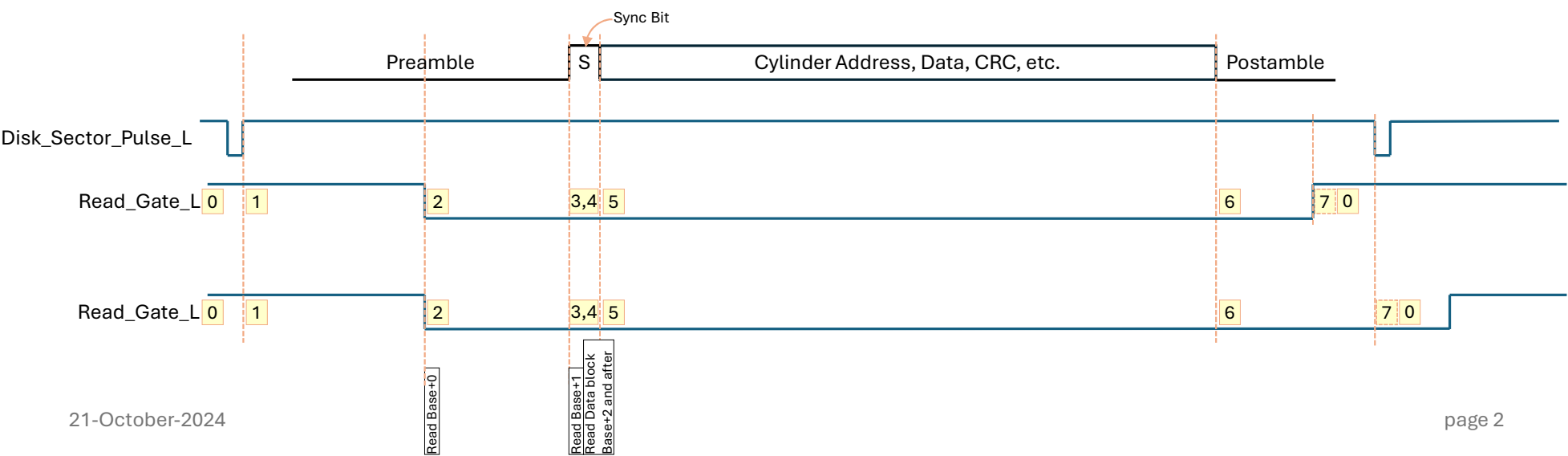
DRAM Internal Sector Block



DRAM Internal Sector Block



Sector Read Timing



Bit times from sector pulse to start bit	Number of data bits after the start bit	<p>Data block, includes Cylinder Address, data, CRC, etc. Could contain some all-zero postamble bits</p>
1w	1w	

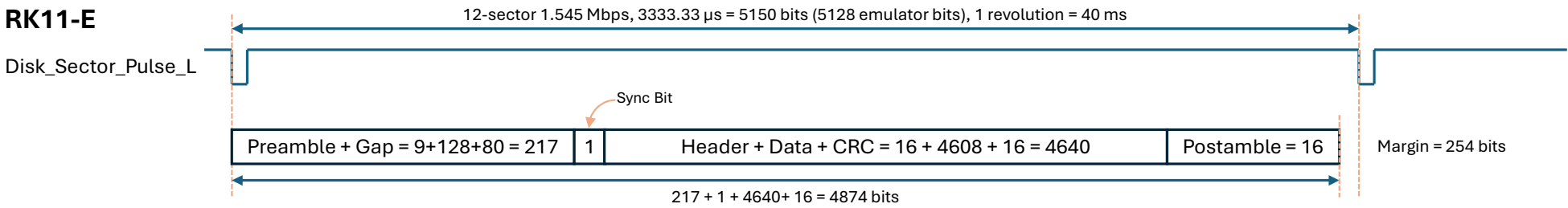
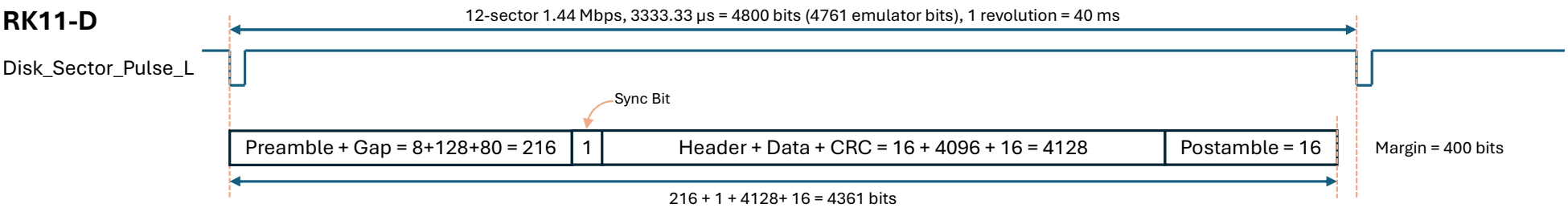
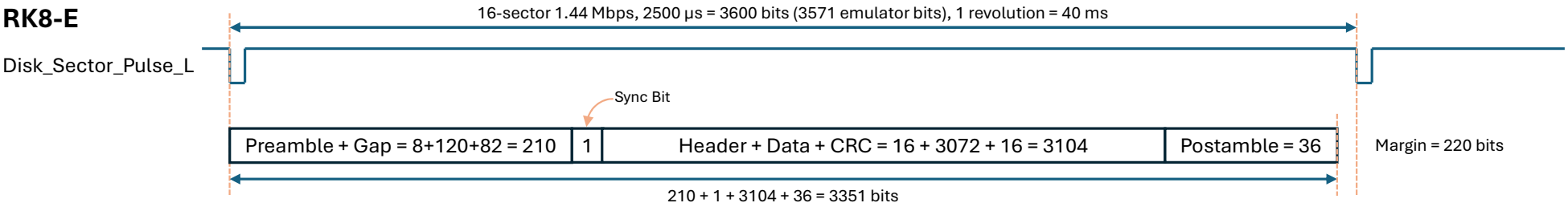
1 to 510 16-bit words

Base+0 Base+1 Base+2 Base+511

Timing diagram for Sector Write. The diagram shows the relationship between the Disk_Sector_Pulse_L, RK8-E Write_Gate_L, and DG Write_Gate_L signals. The timeline is divided into sections: DG Erase Zone, Preamble, Sync Bit, Cylinder Address, Data, CRC, etc., Postamble, and another DG Erase Zone. The signals show specific bit patterns (0, 1, 2, 3, 4, 12, 11, 5, 6, 7, 8, 9) during the write gate pulses. Annotations include 'load_address_buswrite', 'Write Base+0 dram_addr_incr_buswrite', 'Write Data block Base+2 and after', 'Write last word load_address_buswrite dram_addr_incr_buswrite Write Base+1', and 'Write last word load_address_buswrite dram_addr_incr_buswrite Write Base+1'.

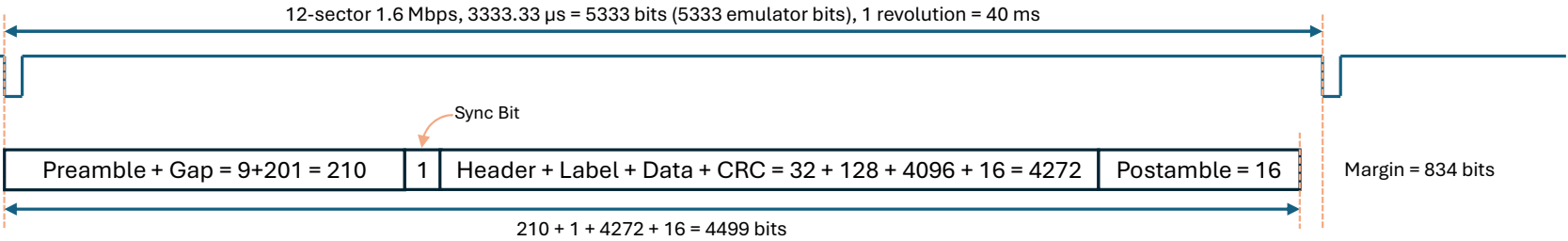
21-October-2024

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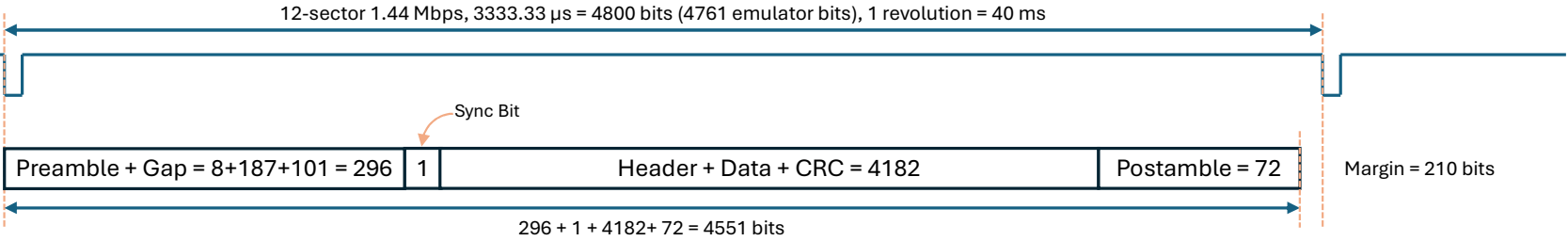
Xerox Alto

Disk_Sector_Pulse_L



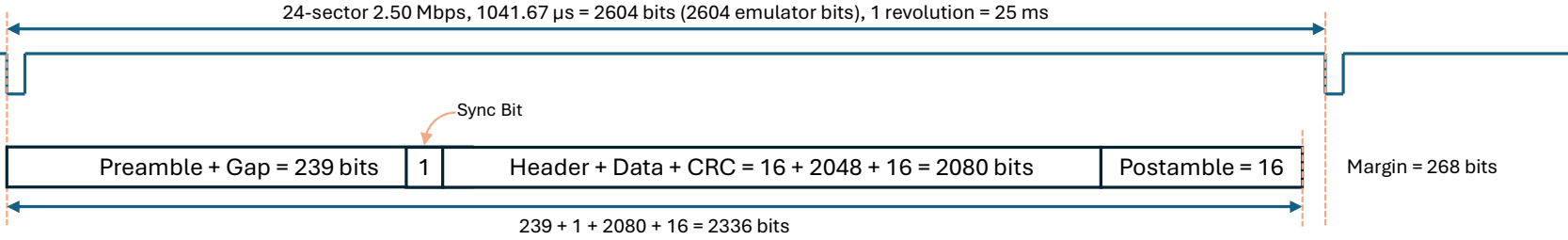
Data General

Disk_Sector_Pulse_L

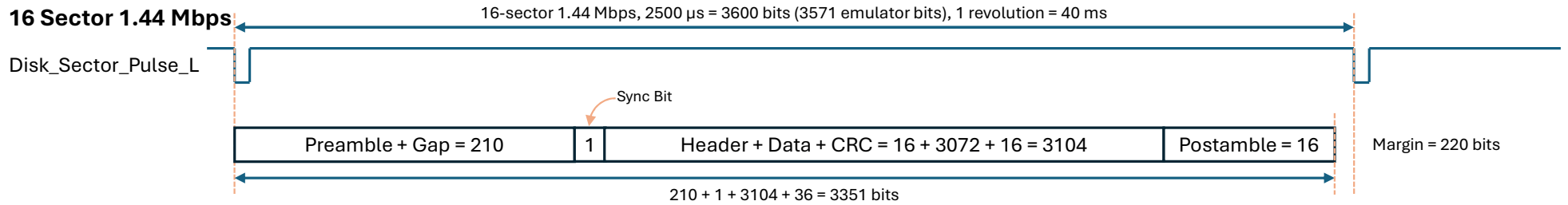


HP2100, 13210A

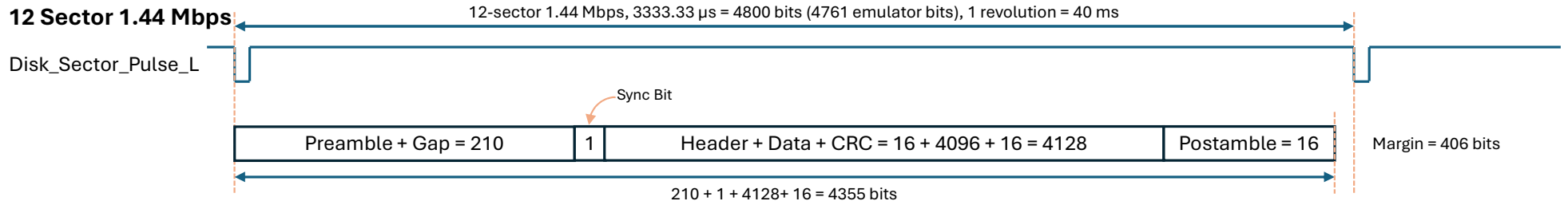
Disk_Sector_Pulse_L



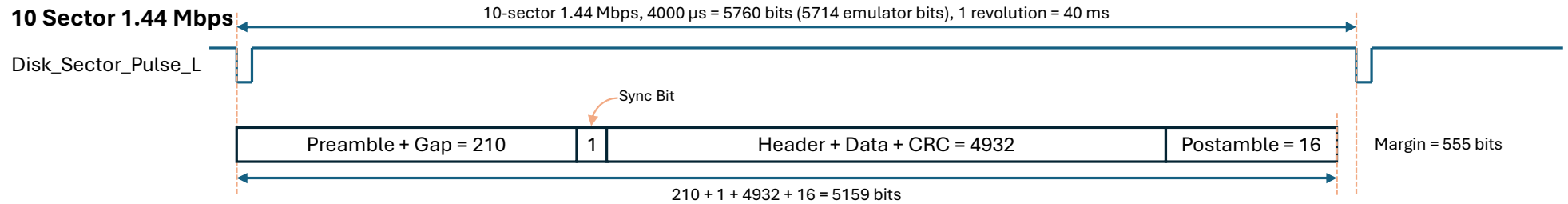
16 Sector 1.44 Mbps



12 Sector 1.44 Mbps

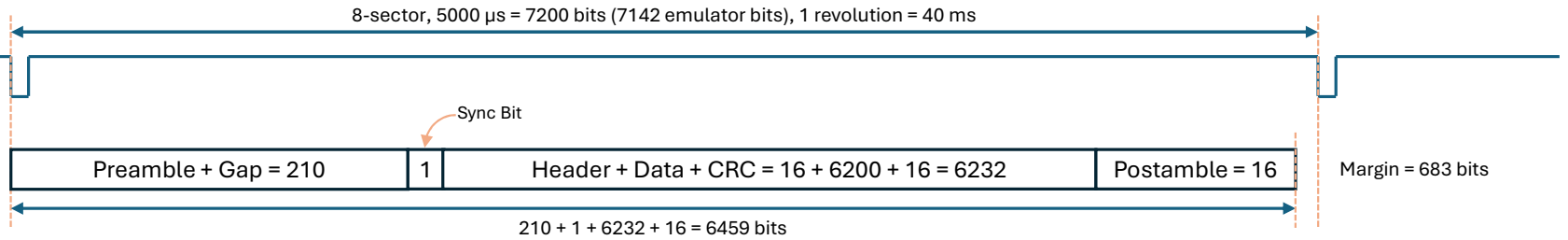


10 Sector 1.44 Mbps



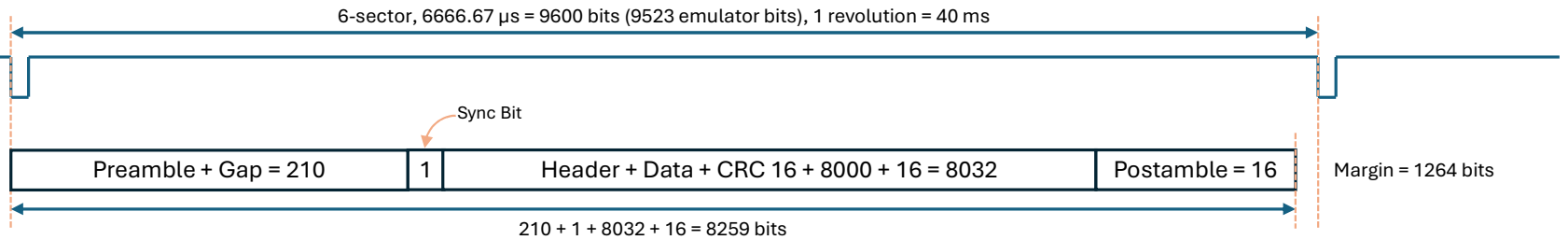
8 Sector 1.44 Mbps

Disk_Sector_Pulse_L



6 Sector 1.44 Mbps

Disk_Sector_Pulse_L



4 Sector 1.44 Mbps

Disk_Sector_Pulse_L

