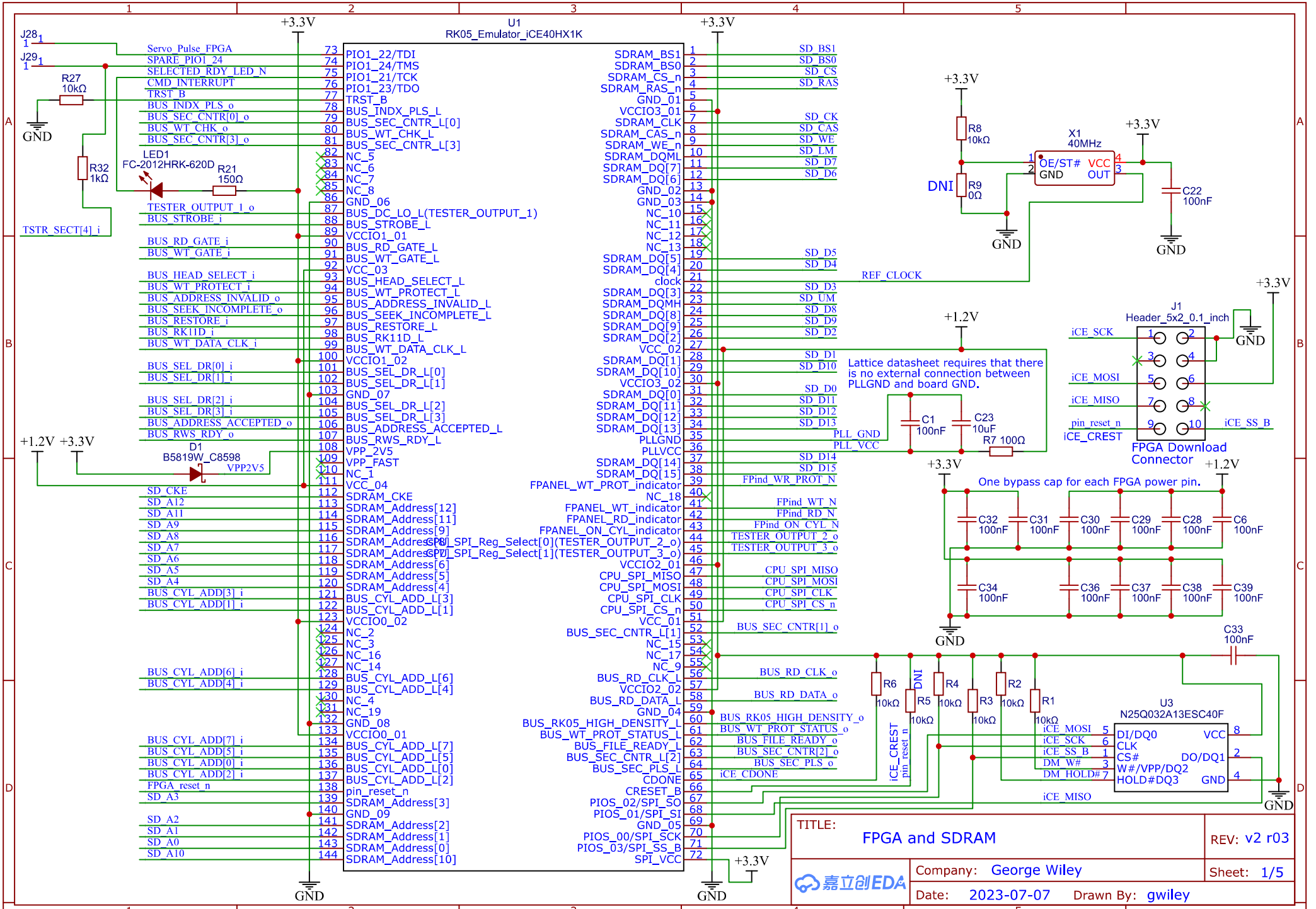
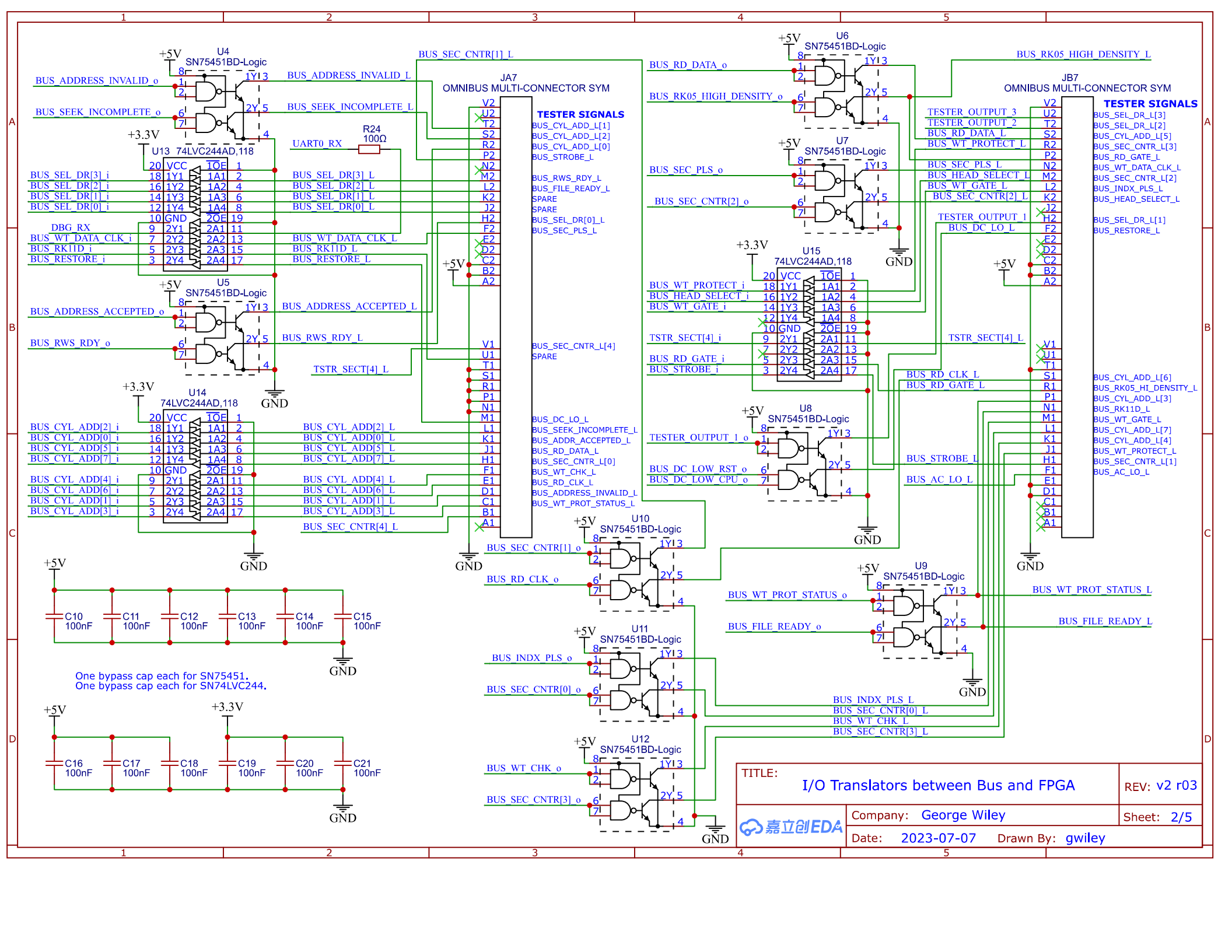
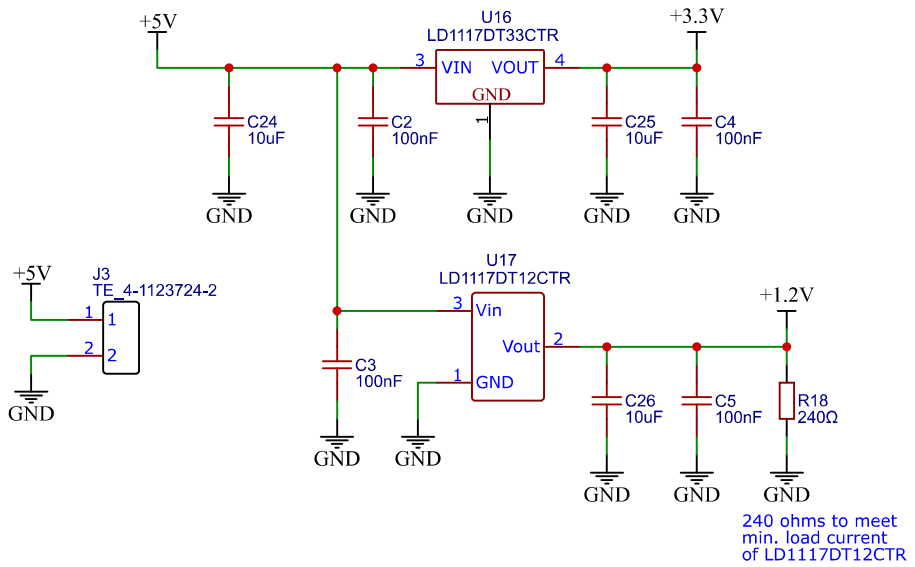
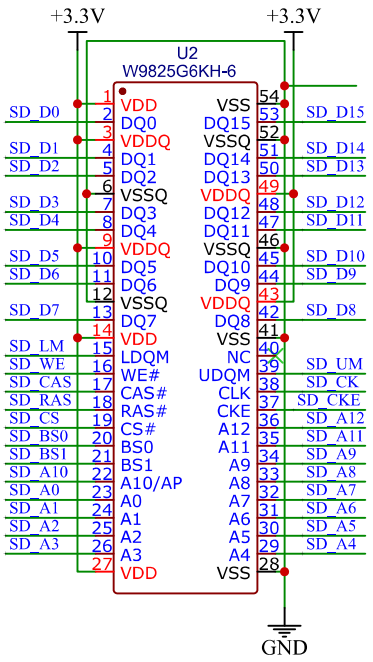
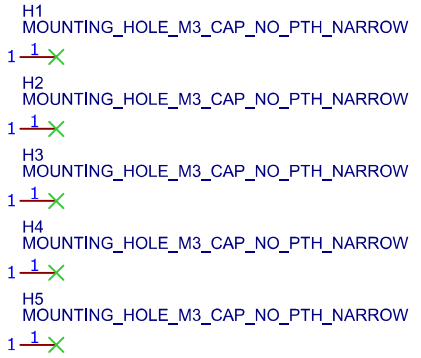
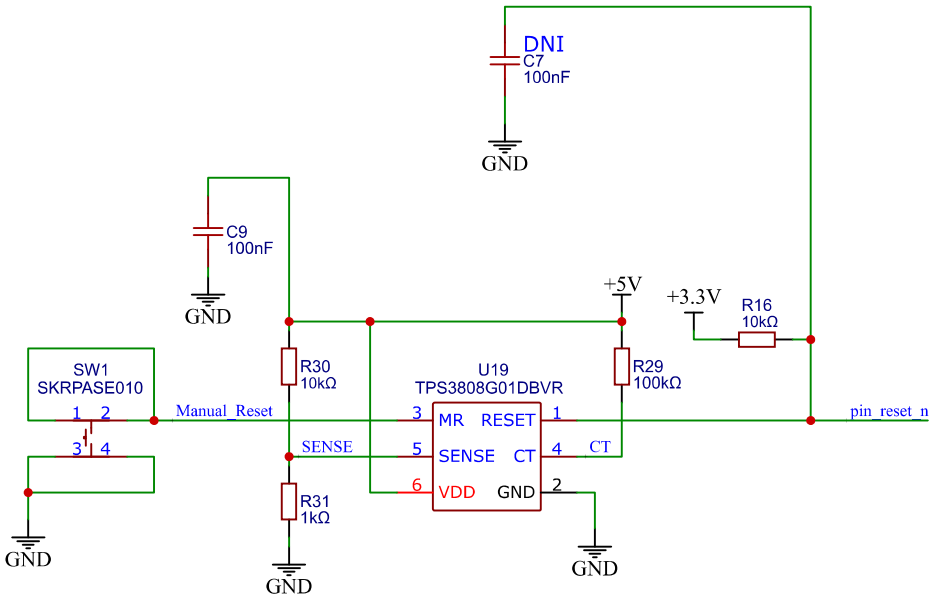

U1
RK05_Emulator_iCE40HX1K
PIO1_22/TDI
PIO1_24/TMS
PIO1_21/TCK
PIO1_23/TDO
TRST_B
BUS_INDX_PLS_L
BUS_SEC_CNTR_L[0]
BUS_WT_CHK_L
BUS_SEC_CNTR_L[3]
NC_5
NC_6
NC_7
NC_8
GND_06
BUS_DC_LO_L(TESTER_OUTPUT_1)
BUS_STROBE_L
VCCIO1_01
BUS_RD_GATE_L
BUS_WT_GATE_L
VCC_03
BUS_HEAD_SELECT_L
BUS_WT_PROTECT_L
BUS_ADDRESS_INVALID_L
BUS_SEEK_INCOMPLETE_L
BUS_RESTORE_L
BUS_RK11D_L
BUS_WT_DATA_CLK_L
VCCIO1_02
BUS_SEL_DR_L[0]
BUS_SEL_DR_L[1]
GND_07
BUS_SEL_DR_L[2]
BUS_SEL_DR_L[3]
BUS_ADDRESS_ACCEPTED_L
BUS_RWS_RDY_L
VPP_2V5
VPP_FAST
NC_1
VCC_04
SDRAM_CKE
SDRAM_Address[12]
SDRAM_Address[11]
SDRAM_Address[9]
SDRAM_Address[8]
SDRAM_Address[7]
SDRAM_Address[6]
SDRAM_Address[5]
SDRAM_Address[4]
BUS_CYL_ADD_L[3]
BUS_CYL_ADD_L[1]
VCCIO0_02
NC_2
NC_3
NC_16
NC_14
BUS_CYL_ADD_L[6]
BUS_CYL_ADD_L[4]
NC_4
NC_19
GND_08
VCCIO0_01
BUS_CYL_ADD_L[7]
BUS_CYL_ADD_L[5]
BUS_CYL_ADD_L[0]
BUS_CYL_ADD_L[2]
pin_reset_n
SDRAM_Address[3]
GND_09
SDRAM_Address[2]
SDRAM_Address[1]
SDRAM_Address[0]
SDRAM_Address[10]
SDRAM_BS1
SDRAM_BS0
SDRAM_CS_n
SDRAM_RAS_n
GND_01
VCCIO3_01
SDRAM_CLK
SDRAM_CAS_n
SDRAM_WE_n
SDRAM_DQML
SDRAM_DQ[7]
SDRAM_DQ[6]
GND_02
GND_03
NC_10
NC_11
NC_12
NC_13
SDRAM_DQ[5]
SDRAM_DQ[4]
clock
SDRAM_DQ[3]
SDRAM_DQMH
SDRAM_DQ[8]
SDRAM_DQ[9]
SDRAM_DQ[2]
VCC_02
SDRAM_DQ[1]
SDRAM_DQ[10]
VCCIO3_02
SDRAM_DQ[0]
SDRAM_DQ[11]
SDRAM_DQ[12]
SDRAM_DQ[13]
PLLGND
PLLVCC
SDRAM_DQ[14]
SDRAM_DQ[15]
FPANEL_WT_PROT_indicator
NC_18
FPANEL_WT_indicator
FPANEL_RD_indicator
FPANEL_ON_CYL_indicator
SPI_SPI_Reg_Select[0](TESTER_OUTPUT_2_o)
SPI_SPI_Reg_Select[1](TESTER_OUTPUT_3_o)
VCCIO2_01
CPU_SPI_MISO
CPU_SPI_MOSI
CPU_SPI_CLK
CPU_SPI_CS_n
VCC_01
BUS_SEC_CNTR_L[1]
NC_15
NC_17
NC_9
BUS_RD_CLK_L
VCCIO2_02
BUS_RD_DATA_L
GND_04
BUS_RK05_HIGH_DENSITY_L
BUS_WT_PROT_STATUS_L
BUS_FILE_READY_L
BUS_SEC_CNTR_L[2]
BUS_SEC_PLS_L
CDONE
CRESET_B
PIOS_02/SPI_SO
PIOS_01/SPI_SI
GND_05
PIOS_00/SPI_SCK
PIOS_03/SPI_SS_B
SPI_VCC
J28
J29
Servo_Pulse_FPGA
SPARE_PIO1_24
SELECTED_RDY_LED_N
CMD_INTERRUPT
TRST_B
BUS_INDX_PLS_o
BUS_SEC_CNTR[0]_o
BUS_WT_CHK_o
BUS_SEC_CNTR[3]_o
R27
10kΩ
R32
1kΩ
LED1
FC-2012HRK-620D
R21
150Ω
TESTER_OUTPUT_1_o
BUS_STROBE_i
TSTR_SECT[4]_i
BUS_RD_GATE_i
BUS_WT_GATE_i
BUS_HEAD_SELECT_i
BUS_WT_PROTECT_i
BUS_ADDRESS_INVALID_o
BUS_SEEK_INCOMPLETE_o
BUS_RESTORE_i
BUS_RK11D_i
BUS_WT_DATA_CLK_i
BUS_SEL_DR[0]_i
BUS_SEL_DR[1]_i
BUS_SEL_DR[2]_i
BUS_SEL_DR[3]_i
BUS_ADDRESS_ACCEPTED_o
BUS_RWS_RDY_o
D1
B5819W_C8598
VPP2V5
SD_CKE
SD_A12
SD_A11
SD_A9
SD_A8
SD_A7
SD_A6
SD_A5
SD_A4
BUS_CYL_ADD[3]_i
BUS_CYL_ADD[1]_i
BUS_CYL_ADD[6]_i
BUS_CYL_ADD[4]_i
BUS_CYL_ADD[7]_i
BUS_CYL_ADD[5]_i
BUS_CYL_ADD[0]_i
BUS_CYL_ADD[2]_i
FPGA_reset_n
SD_A3
SD_A2
SD_A1
SD_A0
SD_A10
SD_BS1
SD_BS0
SD_CS
SD_RAS
SD_CK
SD_CAS
SD_WE
SD_LM
SD_D7
SD_D6
SD_D5
SD_D4
REF_CLOCK
SD_D3
SD_UM
SD_D8
SD_D9
SD_D2
SD_D1
SD_D10
SD_D0
SD_D11
SD_D12
SD_D13
PLL_GND
PLL_VCC
SD_D14
SD_D15
FPind_WR_PROT_N
FPind_WT_N
FPind_RD_N
FPind_ON_CYL_N
TESTER_OUTPUT_2_o
TESTER_OUTPUT_3_o
CPU_SPI_MISO
CPU_SPI_MOSI
CPU_SPI_CLK
CPU_SPI_CS_n
BUS_SEC_CNTR[1]_o
BUS_RD_CLK_o
BUS_RD_DATA_o
BUS_RK05_HIGH_DENSITY_o
BUS_WT_PROT_STATUS_o
BUS_FILE_READY_o
BUS_SEC_CNTR[2]_o
BUS_SEC_PLS_o
iCE_CDONE
+3.3V
+1.2V
GND
R8
10kΩ
DNI
R9
0Ω
X1
40MHz
OE/ST#
GND
VCC
OUT
C22
100nF
Lattice datasheet requires that there is no external connection between PLLGND and board GND.
C1
100nF
C23
10uF
R7 100Ω
J1
Header_5x2_0.1_inch
iCE_SCK
iCE_MOSI
iCE_MISO
pin_reset_n
iCE_CREST
iCE_SS_B
FPGA Download Connector
One bypass cap for each FPGA power pin.
C32
C31
C30
C29
C28
C6
C34
C36
C37
C38
C39
C33
R6
R5
R4
R3
R2
R1
U3
N25Q032A13ESC40F
DI/DQ0
CLK
CS#
W#/VPP/DQ2
HOLD#DQ3
DO/DQ1
TITLE:
FPGA and SDRAM
REV: v2 r03
Company: George Wiley
Sheet: 1/5
Date: 2023-07-07
Drawn By: gwiley
嘉立创EDA


U4
SN75451BD-Logic
U5
SN75451BD-Logic
U6
SN75451BD-Logic
U7
SN75451BD-Logic
U8
SN75451BD-Logic
U9
SN75451BD-Logic
U10
SN75451BD-Logic
U11
SN75451BD-Logic
U12
SN75451BD-Logic
U13 74LVC244AD,118
U14
74LVC244AD,118
U15
74LVC244AD,118
JA7
OMNIBUS MULTI-CONNECTOR SYM
JB7
OMNIBUS MULTI-CONNECTOR SYM
TESTER SIGNALS
TESTER SIGNALS
R24
100Ω
+5V
+3.3V
GND
BUS_ADDRESS_INVALID_o
BUS_SEEK_INCOMPLETE_o
BUS_ADDRESS_ACCEPTED_o
BUS_RWS_RDY_o
BUS_RD_DATA_o
BUS_RK05_HIGH_DENSITY_o
BUS_SEC_PLS_o
BUS_SEC_CNTR[2]_o
TESTER_OUTPUT_1_o
BUS_DC_LOW_RST_o
BUS_DC_LOW_CPU_o
BUS_SEC_CNTR[1]_o
BUS_RD_CLK_o
BUS_INDX_PLS_o
BUS_SEC_CNTR[0]_o
BUS_WT_CHK_o
BUS_SEC_CNTR[3]_o
BUS_WT_PROT_STATUS_o
BUS_FILE_READY_o
UART0_RX
DBG_RX
BUS_SEL_DR[3]_i
BUS_SEL_DR[2]_i
BUS_SEL_DR[1]_i
BUS_SEL_DR[0]_i
BUS_WT_DATA_CLK_i
BUS_RK11D_i
BUS_RESTORE_i
BUS_CYL_ADD[2]_i
BUS_CYL_ADD[0]_i
BUS_CYL_ADD[5]_i
BUS_CYL_ADD[7]_i
BUS_CYL_ADD[4]_i
BUS_CYL_ADD[6]_i
BUS_CYL_ADD[1]_i
BUS_CYL_ADD[3]_i
BUS_WT_PROTECT_i
BUS_HEAD_SELECT_i
BUS_WT_GATE_i
TSTR_SECT[4]_i
BUS_RD_GATE_i
BUS_STROBE_i
BUS_ADDRESS_INVALID_L
BUS_SEEK_INCOMPLETE_L
BUS_ADDRESS_ACCEPTED_L
BUS_RWS_RDY_L
BUS_SEC_CNTR[1]_L
TSTR_SECT[4]_L
BUS_SEC_CNTR[4]_L
BUS_SEL_DR[3]_L
BUS_SEL_DR[2]_L
BUS_SEL_DR[1]_L
BUS_SEL_DR[0]_L
BUS_WT_DATA_CLK_L
BUS_RK11D_L
BUS_RESTORE_L
BUS_CYL_ADD[2]_L
BUS_CYL_ADD[0]_L
BUS_CYL_ADD[5]_L
BUS_CYL_ADD[7]_L
BUS_CYL_ADD[4]_L
BUS_CYL_ADD[6]_L
BUS_CYL_ADD[1]_L
BUS_CYL_ADD[3]_L
BUS_RK05_HIGH_DENSITY_L
TESTER_OUTPUT_3
TESTER_OUTPUT_2
BUS_RD_DATA_L
BUS_WT_PROTECT_L
BUS_SEC_PLS_L
BUS_HEAD_SELECT_L
BUS_WT_GATE_L
BUS_SEC_CNTR[2]_L
TESTER_OUTPUT_1
BUS_DC_LO_L
TSTR_SECT[4]_L
BUS_RD_CLK_L
BUS_RD_GATE_L
BUS_STROBE_L
BUS_AC_LO_L
BUS_WT_PROT_STATUS_L
BUS_FILE_READY_L
BUS_INDX_PLS_L
BUS_SEC_CNTR[0]_L
BUS_WT_CHK_L
BUS_SEC_CNTR[3]_L
BUS_SEL_DR[3]_L
BUS_SEL_DR[2]_L
BUS_CYL_ADD_L[5]
BUS_SEC_CNTR_L[3]
BUS_RD_GATE_L
BUS_WT_DATA_CLK_L
BUS_SEC_CNTR_L[2]
BUS_INDX_PLS_L
BUS_HEAD_SELECT_L
BUS_SEL_DR_L[1]
BUS_RESTORE_L
BUS_CYL_ADD_L[6]
BUS_RK05_HI_DENSITY_L
BUS_CYL_ADD_L[3]
BUS_RK11D_L
BUS_WT_GATE_L
BUS_CYL_ADD_L[7]
BUS_CYL_ADD_L[4]
BUS_WT_PROTECT_L
BUS_SEC_CNTR_L[1]
BUS_AC_LO_L
BUS_CYL_ADD_L[1]
BUS_CYL_ADD_L[2]
BUS_SEC_CNTR_L[0]
BUS_WT_CHK_L
BUS_ADDR_ACCEPTED_L
BUS_RD_DATA_L
BUS_WT_PROT_STATUS_L
BUS_RD_CLK_L
BUS_ADDRESS_INVALID_L
BUS_WT_PROT_STATUS_L
BUS_SEC_CNTR_L[4]
SPARE
BUS_SEL_DR[0]_L
BUS_SEC_PLS_L
BUS_RWS_RDY_L
BUS_FILE_READY_L
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 100nF
C19 100nF
C20 100nF
C21 100nF
One bypass cap each for SN75451.
One bypass cap each for SN74LVC244.
TITLE:
I/O Translators between Bus and FPGA
REV: v2 r03
Company: George Wiley
Sheet: 2/5
Date: 2023-07-07
Drawn By: gwiley
嘉立创EDA

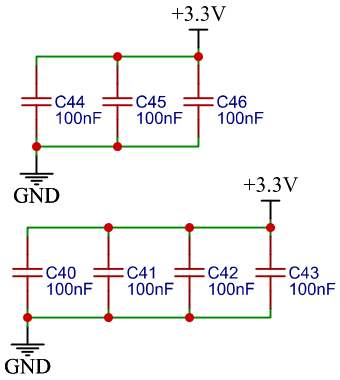




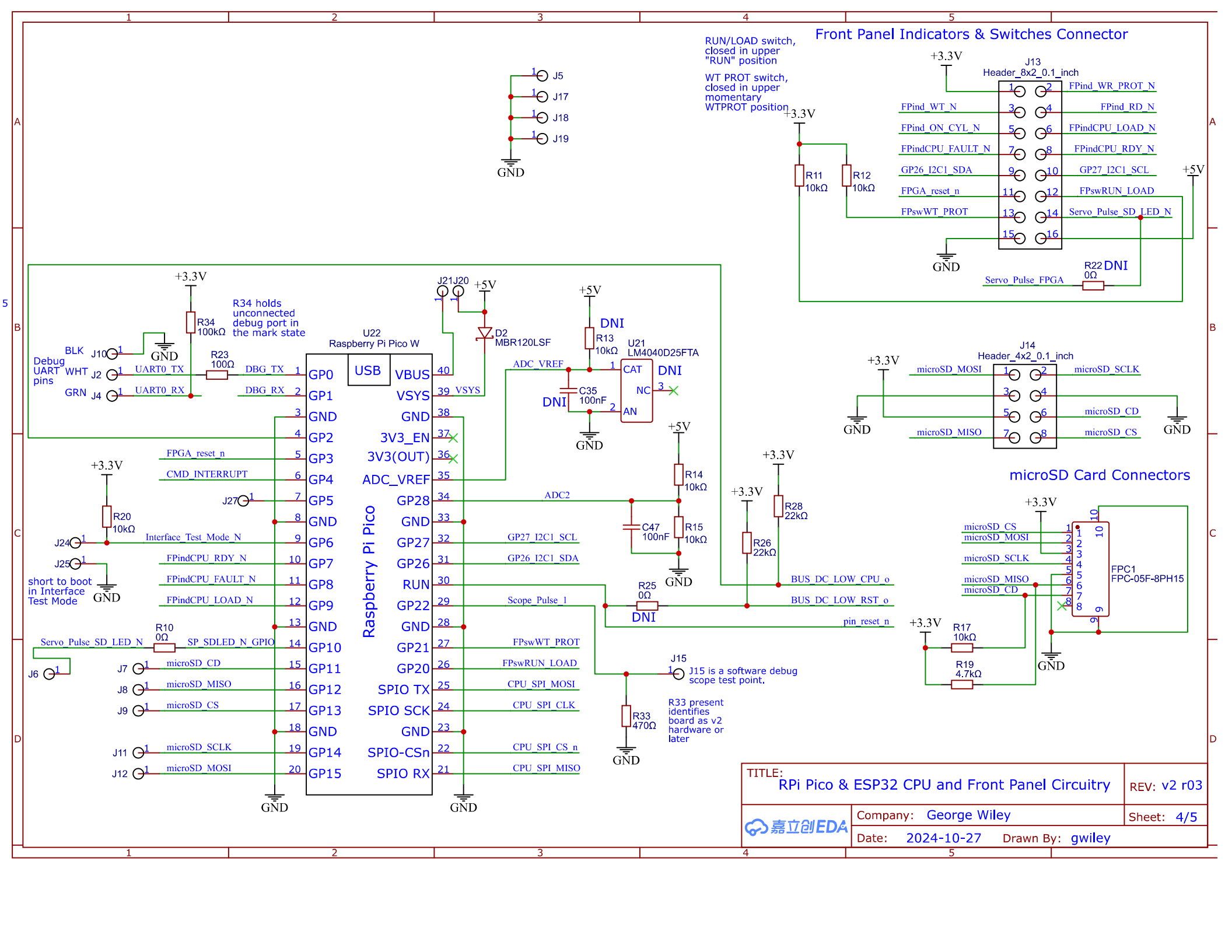


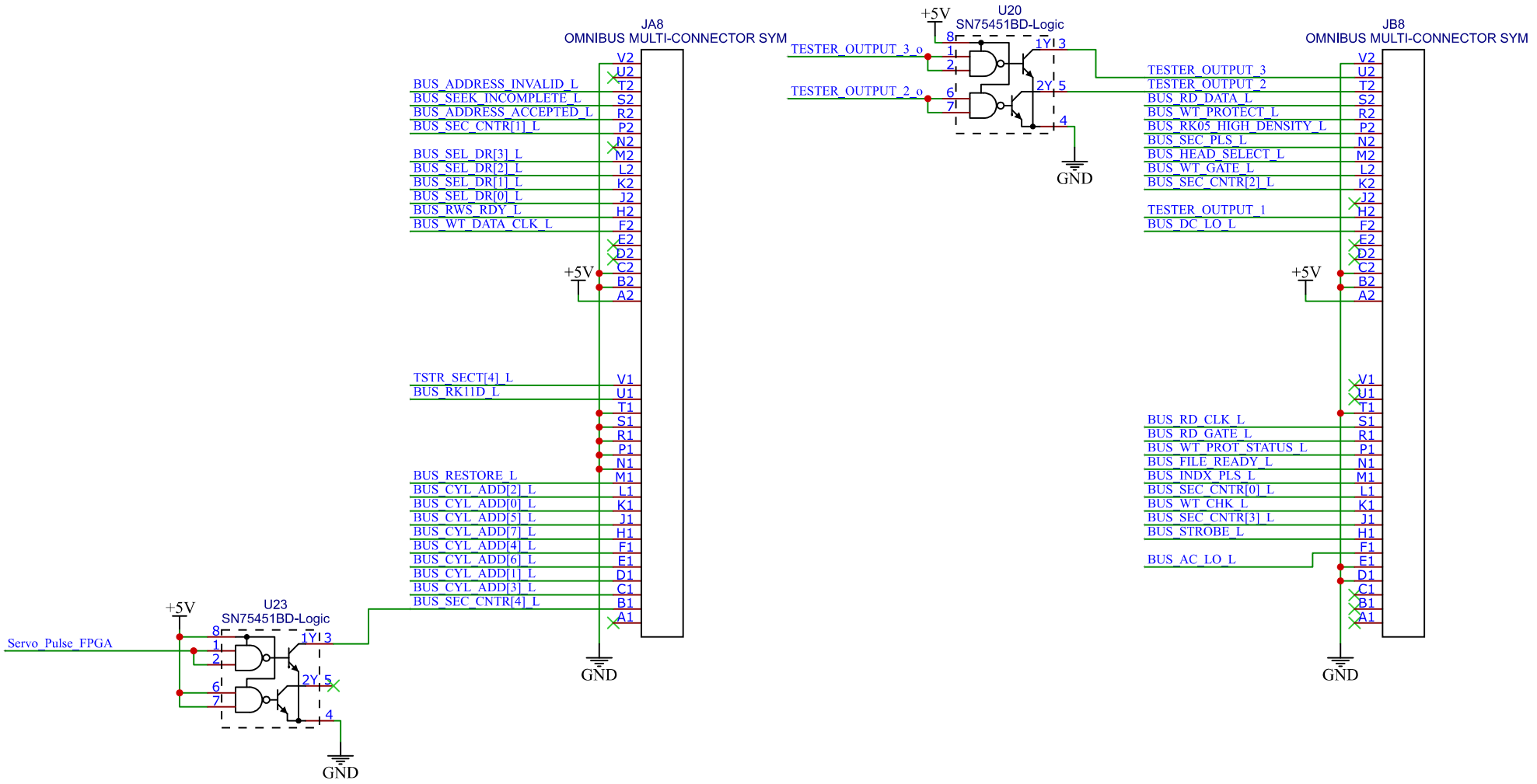


One bypass cap for each DRAM power pin.



TITLE: Voltage Regulators and Reset		REV: v2 r03
嘉立创EDA	Company: George Wiley	Sheet: 3/5
	Date: 2023-07-07 Drawn By: gwiley	


Front Panel Indicators & Switches Connector
RUN/LOAD switch, closed in upper "RUN" position
WT PROT switch, closed in upper momentary WTPROT position
J13
Header_8x2_0.1_inch
FPind_WT_N
FPind_WR_PROT_N
FPind_RD_N
FPind_ON_CYL_N
FPindCPU_LOAD_N
FPindCPU_FAULT_N
FPindCPU_RDY_N
GP26_I2C1_SDA
GP27_I2C1_SCL
FPGA_reset_n
FPswRUN_LOAD
FPswWT_PROT
Servo_Pulse_SD_LED_N
Servo_Pulse_FPGA
R11 10kΩ
R12 10kΩ
R22 DNI 0Ω
+3.3V
+5V
GND
J5
J17
J18
J19
R34 holds unconnected debug port in the mark state
Debug UART pins
BLK J10
WHT J2
GRN J4
UART0_TX
UART0_RX
R34 100kΩ
R23 100Ω
DBG_TX
DBG_RX
U22
Raspberry Pi Pico W
USB
Raspberry Pi Pico
GP0
GP1
GP2
GP3
GP4
GP5
GP6
GP7
GP8
GP9
GP10
GP11
GP12
GP13
GP14
GP15
VBUS
VSYS
3V3_EN
3V3(OUT)
ADC_VREF
GP28
GP27
GP26
RUN
GP22
GP21
GP20
SPIO TX
SPIO SCK
SPIO-CSn
SPIO RX
J21J20
D2 MBR120LSF
R13 10kΩ DNI
U21 LM4040D25FTA
CAT
AN
NC
C35 100nF DNI
ADC_VREF
ADC2
R14 10kΩ
R15 10kΩ
C47 100nF
R28 22kΩ
R26 22kΩ
BUS_DC_LOW_CPU_o
BUS_DC_LOW_RST_o
pin_reset_n
R25 0Ω DNI
Scope_Pulse_1
J15
J15 is a software debug scope test point.
R33 470Ω
R33 present identifies board as v2 hardware or later
FPGA_reset_n
CMD_INTERRUPT
Interface_Test_Mode_N
FPindCPU_RDY_N
FPindCPU_FAULT_N
FPindCPU_LOAD_N
short to boot in Interface Test Mode
R20 10kΩ
J24
J25
J27
R10 0Ω
Servo_Pulse_SD_LED_N
SP_SDLED_N_GPIO
J6
J7
J8
J9
J11
J12
microSD_CD
microSD_MISO
microSD_CS
microSD_SCLK
microSD_MOSI
GP27_I2C1_SCL
GP26_I2C1_SDA
FPswWT_PROT
FPswRUN_LOAD
CPU_SPI_MOSI
CPU_SPI_CLK
CPU_SPI_CS_n
CPU_SPI_MISO
J14
Header_4x2_0.1_inch
microSD Card Connectors
FPC1
FPC-05F-8PH15
R17 10kΩ
R19 4.7kΩ
TITLE:
RPi Pico & ESP32 CPU and Front Panel Circuitry
REV: v2 r03
Company: George Wiley
Sheet: 4/5
Date: 2024-10-27
Drawn By: gwiley
嘉立创EDA



TITLE: RK05 Bus Connectors		REV: v2 r03
嘉立创EDA	Company: George Wiley	Sheet: 5/5
	Date: 2023-07-07 Drawn By: gwiley	