RK05 Disk Drive Maintenance Manual, page 3-1

Interface cable connection of the RK05 Disk Drive is made to card position 7 or 8 of the electronic module. These card positions are parallel-wired so that several drives may be daisy-chained in a multi-drive configuration; that is, card position 7 or 8 of the first drive is connected to card position 7 or 8 of the succeeding drive, etc. (By convention, card position 7 is used for input signals; card position 8 is used for output signals.) If there is only one drive in the system, an M930 terminator card must be installed in the unused interface card position; if there is more than one drive in the system, only the last drive on the bus must have the M930 terminator card in the unused interface card position. The interface signal levels are determined by the M930 terminator card. An assertion, or logic 1, is approximately +0.5 Vdc, and a negation, or logic 0, is approximately +3.5 Vdc.

page 3-3

3.2.5 Head Select

BUS SEL UPPER HD L transmits a signal that determines which of the two read/write heads is to be selected. The controller places a logical 1 on this line to select the upper head, and a logical 0 to select the lower head. Either signal remains on the line throughout the entire read or write operation.

PDP-8e/f/m Maintenance Manual, volume 3, 2nd printing 1973, page 11-7

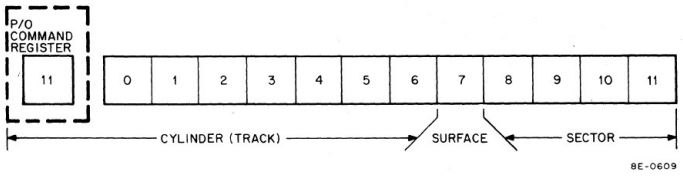


Figure 11-5 Disk Address Register

Based on the schematic, the disk address doesn't have a hardware-based auto-increment feature.

- SURFACE = 0 (lower head)
- SURFACE = 1 (upper head)

RK11-D Disk Drive Controller Manual, page 3-8

DISK ADDRESS REGISTER (RKDA)
Address = 777412

DRIVE SELECT			CYLINDER ADDRESS								SUR	SECTOR ADDRESS			
2	1	0	7	6	5	4	3	2	1	0		3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTE
This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the Control Ready (RDY – bit 07 of the RKCS) state, and are cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.

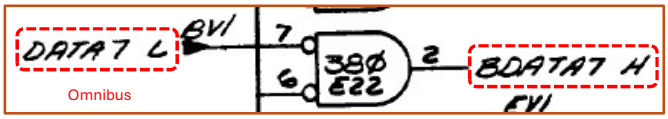
Bit	Designation	Description and Operation
00–03	Sector Address (SA)	Binary representation of the disk sector to be addressed for the next function.
04	Surface (SUR)	When active, enables the lower disk head so that operation is performed on the lower surface; when inactive, enables the upper disk head.
05–12	Cylinder Address (CYL ADDR)	Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312_8.
13–15	Drive Select (DR SEL)	Binary representation of the logical drive number currently being selected.

Based on the schematic, in hardware, the surface and cylinder addresses increment in the sequence:

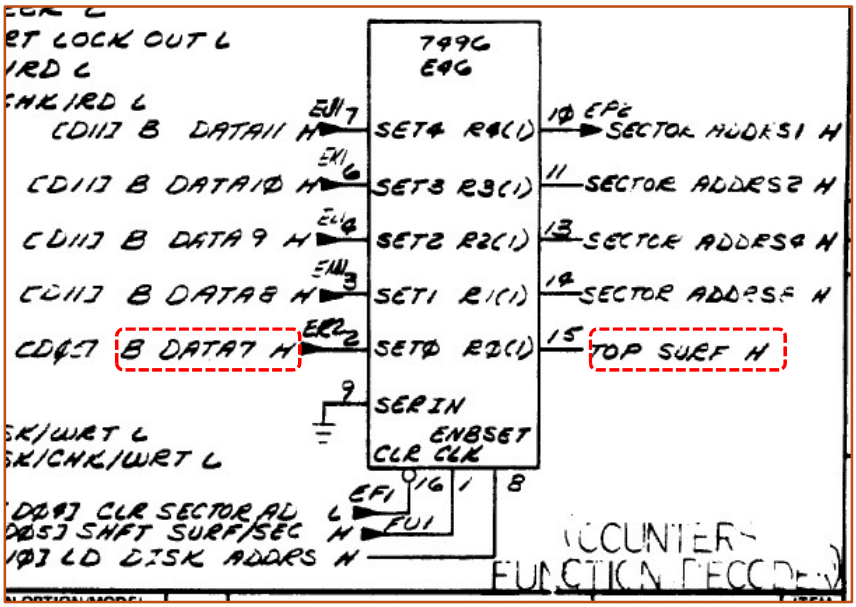
- $CYLINDER\_ADDRESS_n$, SUR = 0 (upper head)
- $CYLINDER\_ADDRESS_n$, SUR = 1 (lower head)
- $CYLINDER\_ADDRESS_{n+1}$, SUR = 0 (upper head)
- $CYLINDER\_ADDRESS_{n+1}$, SUR = 1 (lower head)

RK8-E Head Select Path:

M7105, sheet 4, receives Omnibus active-low data bit 7 on connector pin BV1



M7106, sheet 3



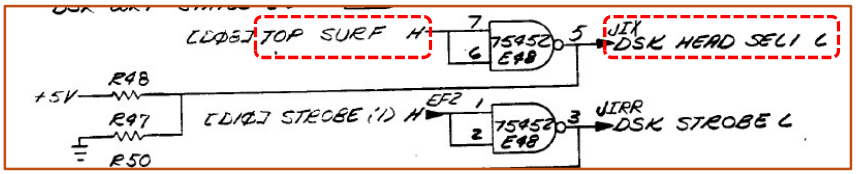
Register output E46 pin 15:

- Low selects lower head
- High selects upper head

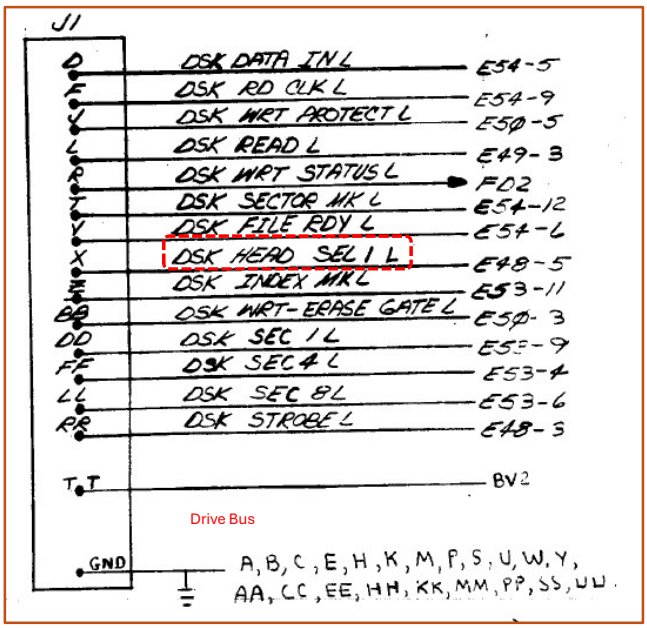
Logic state is the same as the Disk Address Register:

- Low → 0
- High → 1

M7106, sheet 6

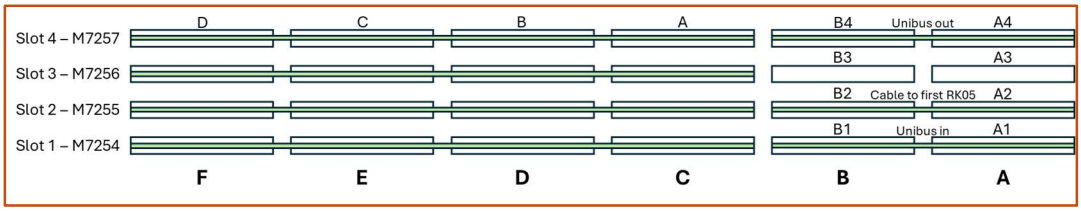


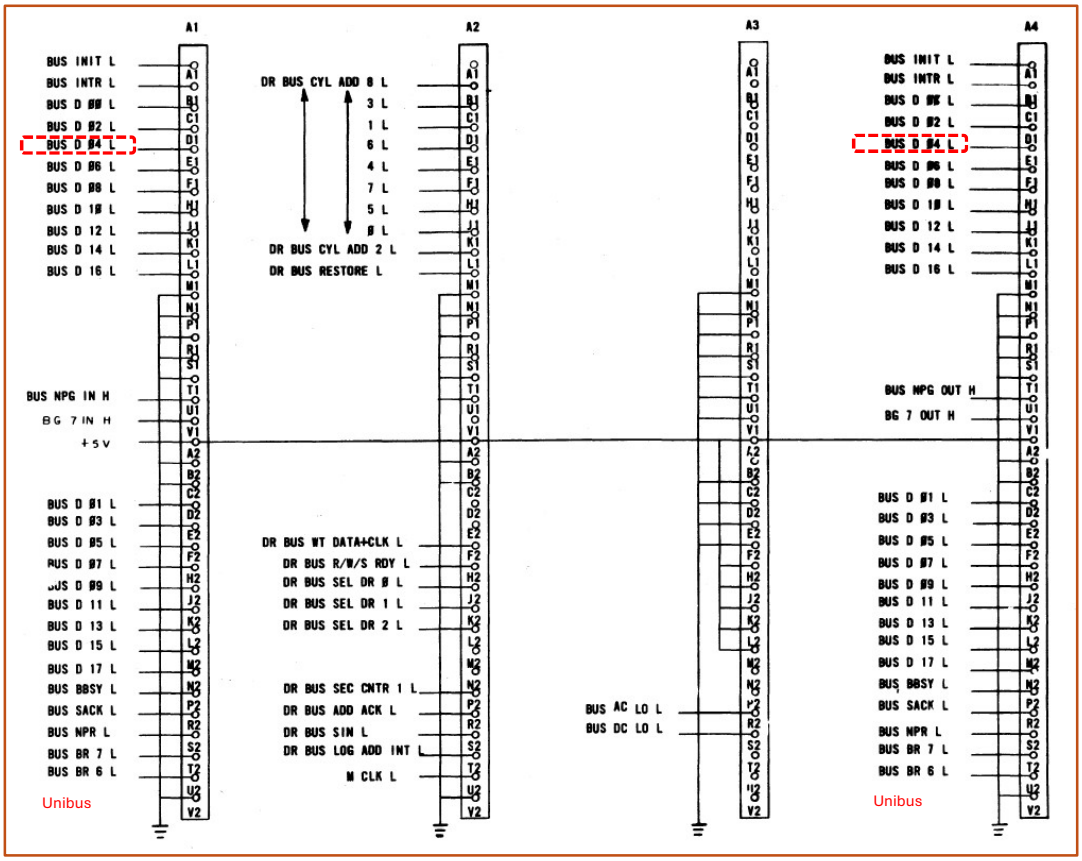
M7106, sheet 6

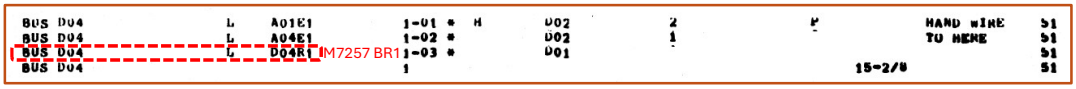


RK11-D Head Select Path: (backplane C, D, E, F is plug-in board A, B, C, D)

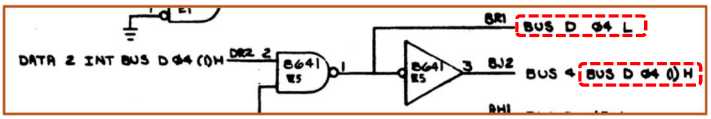
RK11-D Backplane connectors (top view)

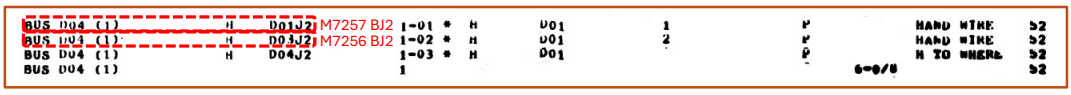




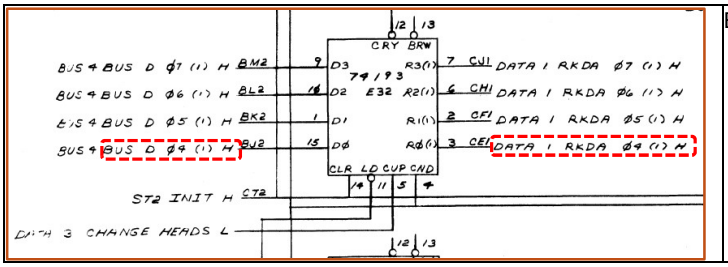


M7257 (Slot 4), sheet 6





M7256 (Slot 3), sheet 3



E32 pin 3:

- low selects upper head
- high selects lower head

M7255 (Slot 2), sheet 5

Backplane, Drive Bus BM2