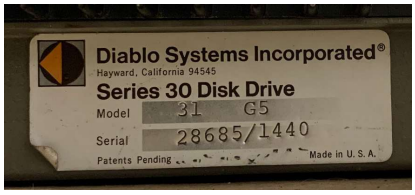
Diablo Model 31, G5, serial number 28685/1440, Restoration Notes



Restoration list:

1. ✓Check all polarized capacitors and replace bad ones
2. ✓Confirm how the drive is configured, which options
3. ✓Verify jumper options on backplane: Select Line Jumper and Attention Option Jumper, refer to section 2.2.3.5 in the manual
4. ✓Replace the air filter
5. ✓Current consumption with nothing running, just idle (smoke test)
6. ✓Clean the disk cartridge and spin up disk
7. ✓Verify index and sector pulses, verify sector address signals
8. ✓Read data from disk cartridge and check it using the emulator
9. ✓Write a bootable OS-8 image onto the disk cartridge and boot up OS-8 on the PDP-8/m
10. ✓Successfully run the RK05 Tester's "Write Loop Random" test
11. Pass the PDP-8 "maindec-08-dhrkc-h-pb" test

Confirm the Module Versions:

- J1 – PCB 11077 Rev J, SCH 11078 Rev 00M
- J2 – PCB 11110 Rev J, SCH 11111 Rev H, 11111-00 option
- J3 – PCB 11024 Rev N, SCH 11026 Rev L, 11026-02 (Attention Line Negative, has A10 & A15, no A13)
- J8 – PCB 11083 Rev J, SCH 11085 Rev P (no jumper E19; relay F43 is installed)
- J9 – PCB 11069 Rev K, SCH 11071 Rev ?
- J10 – PCB 11080 Rev J, SCH 11082-10 Rev AA,
  Resistors H28 11.5KΩ, H56 ?, *Jumpers* F9 10Ω, F39 n/c, K28 10Ω,
  Terminator Resistors F41 n/c, D39 n/c, D44 n/c, E42 n/c, H41 n/c,
  Input Clamp Diodes E39 n/c, F8 n/c, *Timing Resistors* F28 1 MegΩ, H53 75KΩ

Mistake, should be 003

			DESCRIPTION																		
			1440 BPS OPTION 005	1562K BPS OPTION 004	DAISY CHAIN OPTION 006	ERASE GATE OPTION 007	INTERRUPT OPTION 048	RESISTORS		JUMPERS			TERMINATOR RESISTORS					INPUT CLAMP DIODES		TIMING RESISTORS	
ASSY. NO.	REV	ECO NO.						H28	H56	F9	F39	K28	F41	D39	D44	E42	H41	E39	F8	F28	H53
11082-08	AA	8187	X					11.5K	11.5K	10Ω		10Ω		150Ω	150Ω	150Ω	150Ω			F28 SELECTED TO GIVE DATA	
11082-09	AA	8187	X			X		11.5K	11.5K			10Ω	150Ω	150Ω	150Ω	150Ω	150Ω	IN4454	IN4454	GATE TIMING OF 515 ± 10ns.	
11082-10	AA	8187	X		X			11.5K	11.5K	10Ω		10Ω								H53 SELECTED TO GIVE DATA	
11082-11	AA	8187	X		X	X		11.5K	11.5K			10Ω						IN4454	IN4454	GATE TIMING OF 485 ± 10ns.	
11082-12	AA	8187		X				10.5K	10.5K	10Ω		10Ω		150Ω	150Ω	150Ω	150Ω			F28 SELECTED TO GIVE DATA	
11082-13	AA	8187		X		X		10.5K	10.5K			10Ω	150Ω	150Ω	150Ω	150Ω	150Ω	IN4454	IN4454	GATE TIMING OF 470 ± 15ns.	
11082-14	AA	8187		X	X			10.5K	10.5K	10Ω		10Ω								H53 SELECTED TO GIVE DATA	
11082-15	AA	8187		X	X	X		10.5K	10.5K			10Ω						IN4454	IN4454	GATE TIMING OF 450 ±10ns.	
11082-16	AA	8187		X	X	X	X	10.5K	10.5K		10Ω							IN4454	IN4454		

Checking all polarized capacitors:

J	Loc.	Desc	good	bad
J1	A4	100 µF 20V, Ta, DxL = 8.8x19.5mm, C = 97 µF, ESR = 1.7 Ω, reformed @18V	✓	
J1	D7	100 µF 25V, Al, DxL = 9.6x20mm, C = 119 µF, ESR = 1.8 Ω, reformed @20V	✓	
J1	K3	100 µF 25V, Al, DxL = 9.6x20mm, C = 120 µF, ESR = 1.9 Ω, reformed @20V	✓	
J2	A7	100 µF 25V, Al, DxL = 9.6x20mm, C = 140 µF, ESR = 1.6 Ω, reformed @20V	✓	
J2	B27	2.2 µF 35V, Ta, DxL = 4.6x12mm, C = 2.6 µF, ESR = 2.4 Ω, reformed @30V	✓	
J3	B7	100 µF 25V, Al, DxL = 9.6x20mm, C = 138 µF, ESR = 1.7 Ω, reformed @20V	✓	
J3	F35	10 µF 25V, Al, DxL = 9.6x20mm, short at 7 Ω		✓
J8	A3	10 µF 25V, Al, DxL = 6.7x15mm, C = 5.4 µF, ESR = 36 Ω, reformed @20V		✓
J8	A6	10 µF 25V, Al, DxL = 6.7x15mm, C = 13 µF, ESR = 3.9 Ω, reformed @20V	✓	
J8	D6	22 µF 35V, Ta, DxL = 7.3x17mm, C = 25 µF, ESR = 1.5 Ω, reformed @30V	✓	
J8	H3	22 µF 35V, Ta, DxL = 7.3x17mm, C = 26 µF, ESR = 1.5 Ω, reformed @30V	✓	
J9	A4	10 µF 25V, Al, DxL = 6.7x15mm, C = 13.7 µF, ESR = 3.2Ω, reformed @20V Initially, this appeared to be shorted in the reforming test.	✓	
J9	A10	10 µF 25V, Al, DxL = 6.7x15mm, C = 14.9 µF, ESR = 4.4 Ω, reformed @20V	✓	
J9	E4	10 µF 25V, Al, DxL = 6.7x15mm, C = 14.4 µF, ESR = 4.2 Ω, reformed @20V	✓	
J9	H1	10 µF 25V, Al, DxL = 6.7x15mm, C = 16.8 µF, ESR = 4.2 Ω, reformed @20V	✓	
J9	K30	10 µF 25V, Al, DxL = 6.7x15mm, C = 13.6 µF, ESR = 4.2 Ω, reformed @20V	✓	
J9	K36	12 µF 20V, Ta, DxL = 4.7x12mm, C = 12.7 µF, ESR = 4.1 Ω, reformed @18V	✓	
J9	K48	39 µF 10V, Ta, DxL = 4.7x12mm, C = 43.7 µF, ESR = 1.3 Ω, reformed @9V	✓	
J10	B3	10 µF 25V, Al, DxL = 6.7x15mm, C = 11.0 µF, ESR = 48 Ω, reformed @20V		✓
J10	B7	10 µF 25V, Al, DxL = 6.7x15mm, C = 48 pF, ESR = Ω, reformed @20V		✓
J10	E9	10 µF 25V, Al, DxL = 6.7x15mm, C = 9.0 µF, ESR = 108 Ω, reformed @20V		✓
J10	K3	10 µF 25V, Al, DxL = 6.7x15mm, C = 11.3 µF, ESR = 117 Ω, reformed @20V		✓
J10	H30	10 µF 25V, Al, DxL = 6.7x15mm, C = 49 pF, ESR = Ω, reformed @20V		✓
J10	A71	12 µF 20V, Ta, DxL = 4.7x12mm, C = 14.5 µF, ESR = 2.2 Ω, reformed @18V	✓	
J10	A74	12 µF 20V, Ta, DxL = 4.7x12mm, C = 13.5 µF, ESR = 2.0 Ω, reformed @18V	✓	

All Capacitors (total of 25):

- Qty 4 – 100 µF 25V, Al, DxL = 9.6x20mm
- Qty 13 – 10 µF 25V, Al, DxL = 9.6x20mm
- Qty 1 – 100 µF 20V, Ta, DxL = 8.8x19.5mm
- Qty 1 – 2.2 µF 35V, Ta, DxL = 4.6x12mm
- Qty 2 – 22 µF 35V, Ta, DxL = 7.3x17mm
- Qty 3 – 12 µF 20V, Ta, DxL = 4.7x12mm
- Qty 1 – 39 µF 10V, Ta, DxL = 4.7x12mm

Bad Capacitors (total of 7):

- Qty 7 – 10 µF 25V, Al, DxL = 9.6x20mm

Replaced the 7 bad capacitors identified in the table above.

Jumper & Component Configuration Option Settings:

Select: “2” (which is drive 1 per DEC definitions)
Later note: I’ve been moving the Select jumper between “1” and “2”, which is RK8-E addresses 0 and 1, depending on the PDP-8 or Tester configuration at the moment.

Attention: “2” (jumper to pin M, which is “* High Density Indication”)
Other choices for the Attention jumper are:

- “1” (jumper to pin H, Write Protect Input)
- “3” (jumper to pin S, *Pseudo Sector Mark)
- “4” (jumper to pin XX, *Logical Address Interlock)

Removed the Attention jumper entirely.

Opt.	Description	Notes
060	Paint – Gray/Green without logo	Paint on cover
046	Attention Line Negative	J3 – jumpers A10 & A15 installed, jumper A13 open, 11026-02 Attention Line Negative
003	1440 kHz – 2040BPI – Option	J10 – component & jumper placement options
005	Write Protect – not included	J9 – components removed for Write Protect
006	Daisy Chain Option	J10 – component & jumper placement, terminator resistors removed
007	Erase Gate – not included	J10 – component & jumper placement, F9 installed
046	Attention Line Negative	J3 – jumpers A10 & A15 installed, jumper A13 open, 11026-02 Attention Line Negative
048	Interrupt Option – not included	J10 – component & jumper placement, F39 not installed

Have been looking for an MRAC15S connector for over a year and have not found one, and have not found a source of socket contacts that I could solder to a small PCB. I figured that if someday I find an MRAC14S it would be possible to clean the solder off of the tips of the pins and the real connector would make contact on the sides of the pins and not be affected by the residual solder. Connected the power cable through a spare Mate-N-Lok connector.

Connected the drive power to a pair of the Nice Power variable lab supplies each set to output 15 volts. I wanted to be able to monitor the current on both the +15V and -15V rails.

Turned on the power and no smoke!

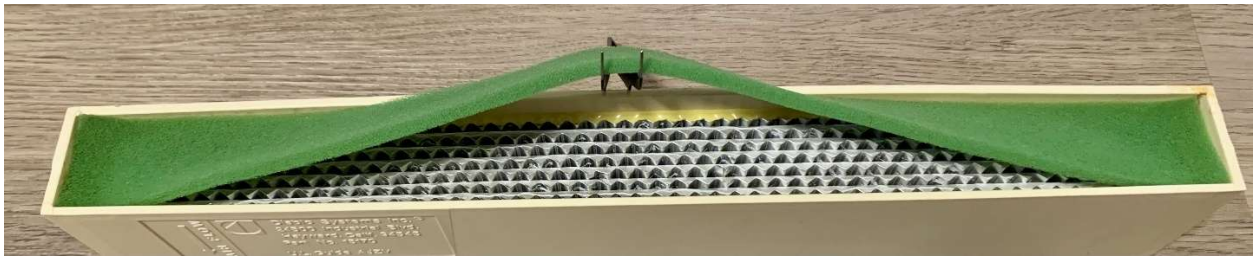
Table 6-1 Series 30 Options

Y	N	Option	Description
	✓	001	720 kHz – 1020BPI – IBM Compatible
	✓	002	781 kHz – 1100BPI – Diablo Standard
✓		003	1440 kHz – 2040BPI – Option
	✓	004	1562 kHz – 2200BPI – Option
	✓	005	Write Protect
	✓	008	Erase Gate (Not tied to Write Gate)
	✓	013	Paint – Orange with Diablo Logo
	✓	014	Paint – Orange without Logo
	✓	015	Unpainted without logo
	✓	017	Flangless Mount (table top trim)
	✓	018	Flush Mount
	✓	019	Extended Front
	✓	020	Upper and Lower Trim for Flush Mount
	✓	023	Drive Tester with Read/Write Data
		024	Extender Board Assembly
		025	Standard Density – 8 Sector
		026	High Density – 8 Sector
		027	Standard Density Alignment Pack
		029	Dual Unit Power Supply
		030	High Density Alignment Pack
		032	Power Supply Cable
		033-05’	Receptacle Connectors on 5’ flat cable (female)
		033-07’	Receptacle Connectors on 7’ flat cable (female)
		034-05’	Pin Connectors on 5’ flat cable (male)
		034-07’	Pin Connectors on 7’ flat cable (male)
		035	Receptacle terminator resistors (female)
		036	Pin terminator resistors (male)
		037	Receptacle terminator without resistors (female)
		038	Pin terminator without resistors (mail)
		039	Standard Density – 12 Sector
		040	Standard Density – 24 Sector
		041	High Density – 12 Sector
		042	High Density – 24 Sector
		043	Option 023 using external power
		044	Rack Mounting for Power Supply
	✓	045	Paint – Orange without Logo
		046	Attention Line Negative
		047	Attention Line Positive
	✓	048	Interrupt Option
		050	DTC Card FPC Interdata Controller
		051	Standard Density – 16 Sector
		052	High Density – 16 Sector
		053-05’	M/F Cable 5’
		053-07’	M/F Cable 7’
		054	32 Sector
		056	Cable Assembly (Interdata Controller)
		057	Terminator (no erase gate) Female with resistors
		058	Terminator (no erase gate) Male with resistors
✓		060	Paint – Gray/Green without logo
	✓	061	Paint – Blue without logo
	✓	062	Grained without logo
	✓	063	Paint – White White (Varian)
		064	Attention line with logical address interlock (Varian)
		065	Cartridge Closing Bail Assembly

Air Filter:

I was concerned about the air filtration to the spinning platter, and wanted this air channel to be as clean as possible. The old filter that came with the drive has a bunch of small white granules in the small channels in the filter.

The old filter:



Close-up photo of the old filter:

Purchased a new-old-stock air filter on eBay, https://www.ebay.com/itm/267148896688. Made him an offer. The new filter arrived and was enclosed in a plastic wrapper. The plastic was punctured and the entire thing smelled kind of "musty" but it appeared to be quite clean.

Removed the old filter, wiped out the area where the filter is located, and installed the new filter.

Disk Cartridge and Heads:

Cleaned the disk cartridge. The inspiration for the cleaning process was this:
https://users.glitchwrks.com/~glitch/2023/02/23/pack-cleaning
Wore nitrile gloves through all of the following. First wiped down the outside of the pack with a Kimwipe and 99% isopropyl alcohol. Took it apart to clean the inside of the case and the platter. Started by removing the 7 screws at the edges of the bottom side of the cartridge. Wiped down the inside of the case using a Kimwipe and 99% isopropyl alcohol. Then wiped the disk platter from the center outward only, never in the direction of rotation. Used a bright desk lamp to illuminate the surface of the platter at different angles to be able to see any tiny particles and kept wiping (from the center towards the outside only) to remove all of them. When it was clean than the pack was reassembled and the screws were reinstalled.

Cleaned the heads in the drive using a Kimwipe well moistened with 99% isopropyl alcohol.

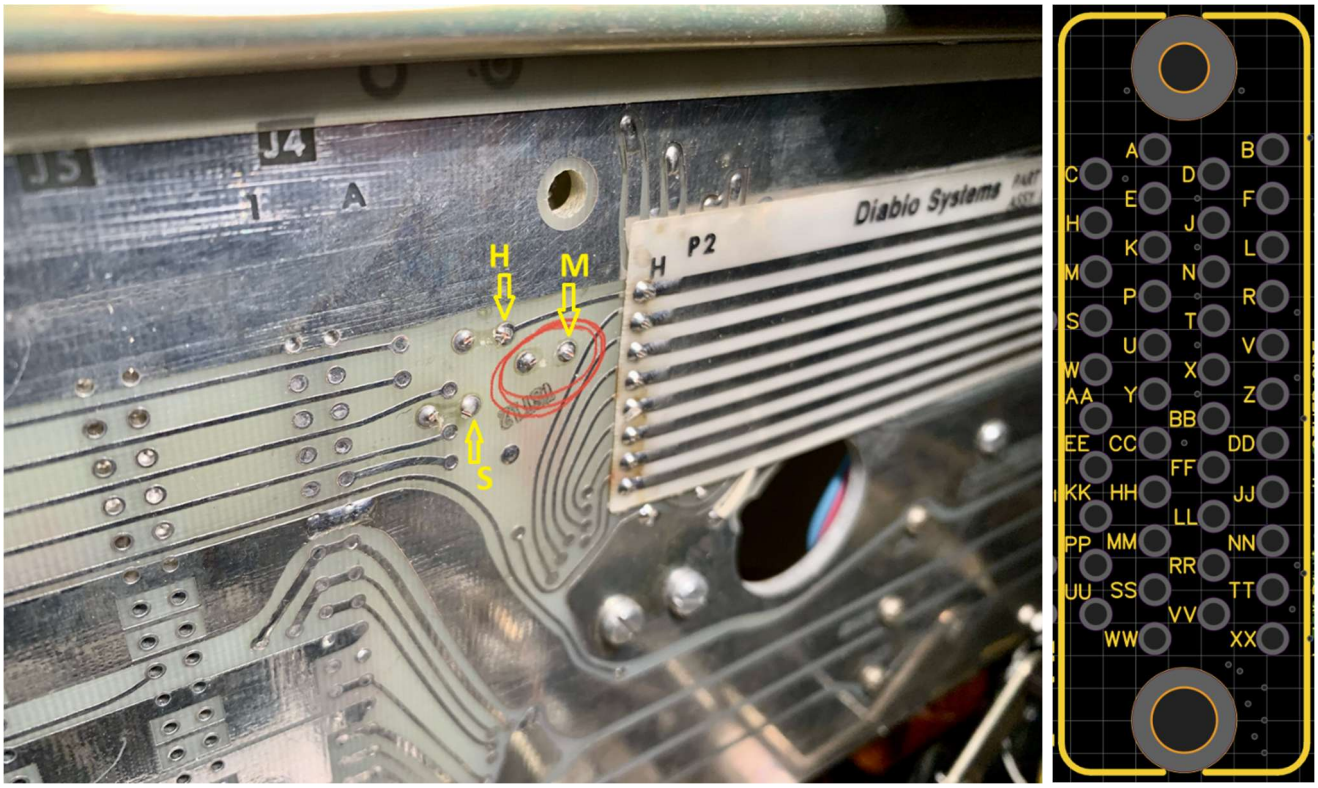
Next Smoke Test, Spinning Platter:

With the bad electrolytics replaced, drive cleaned up, air filter replaced, disk pack cleaned, I inserted the disk pack into the drive and flipped the switch from LOAD to RUN, and held my breath. The drive spins up fine, no scary noises coming from the drive.

The one problem remaining is the "High Density Indication" signal on pin M is inactive. I traced it back to the module in J10 where I can see that "High Density Indication" is active. The schematics show a jumper on the backplane that I haven't yet found that is in series with this signal getting to the MRAC42 connectors

There's a problem with the "High Density Indication" signal on pin M; it's inactive when the drive is spun up and drive is selected . Traced it back to the module in J10 where I can see that "High Density Indication" is active. The schematics show a jumper on the backplane that I haven't yet found that is in series with this signal getting to the MRAC42 connectors.

Now I found it by doing a contuctivity test with the beeper in the digital meter, testing conductivity between various backplane traces and the "High Density Indication" signal on the J10 board!

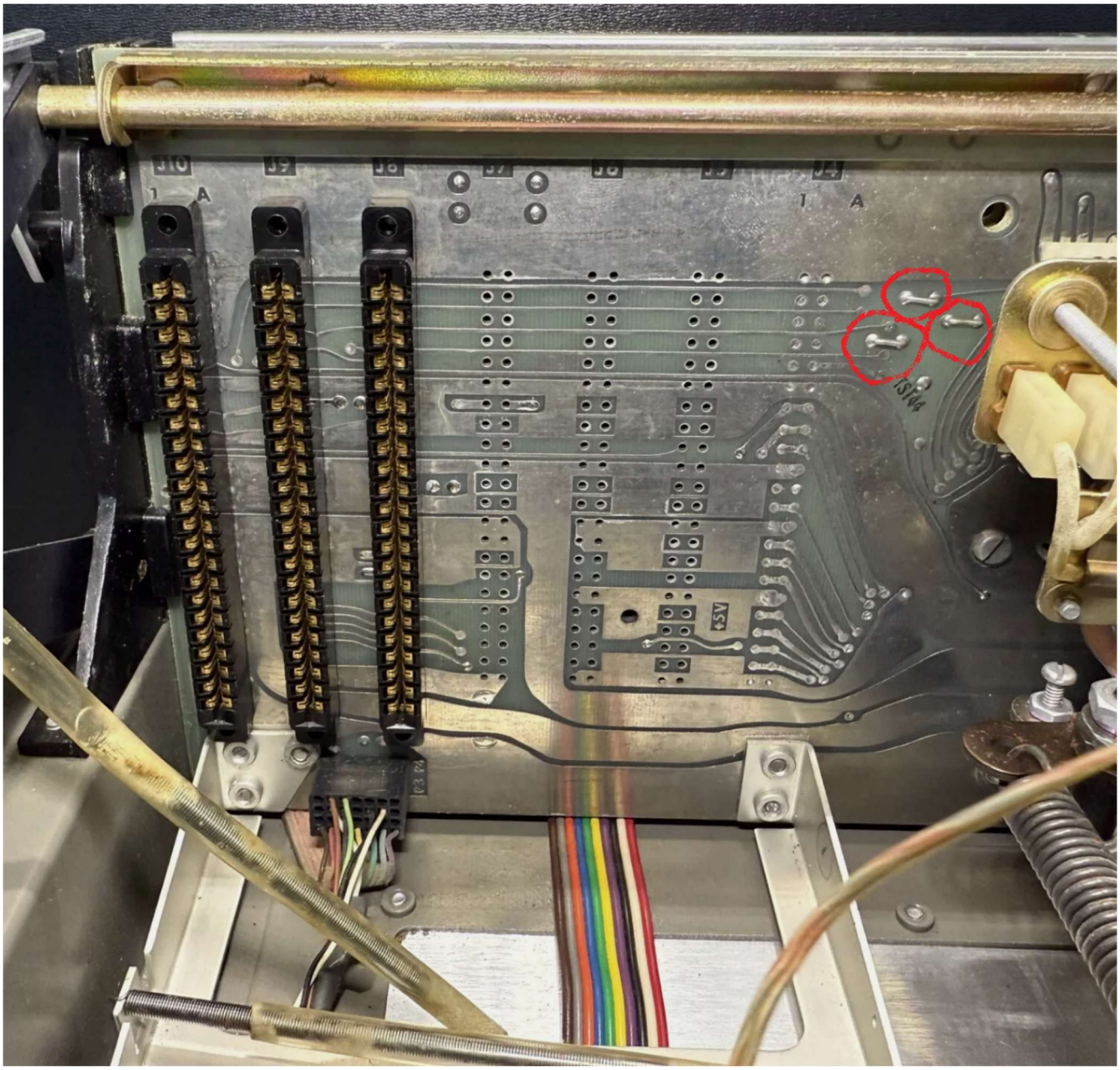


The jumpers for the signals on MRAC pins H, M, and S were apparently removed by the previous owner.

- H – "Write Protect Input"
- M – "High Density Indication"
- S – "Pseudo Sector Mark"

It's strange that the board in J10 is configured for high density but the backplane jumper for the "High Density Indication" signal is removed

For example, this is another drive, photo captured from an eBay listing, that has all three jumpers installed:



March 12, 2025

Added the “High Density Indication” jumper on the backplane.

Spun up the drive, “Display Status” shows the following response:

```
tester-0>disp status
  Drive Address =   0
  Addr Encoded (RK11D mode) = 0
  controller =      RK8-E
  bitRate =         1440000
  preamble1Length = 120
  preamble2Length = 82
     total bit_times_sector_to_start = 202
  bit_times_data_bits_after_start =    3104
  postambleLength = 36
  numberOfCylinders =        203
  numberOfSectorsPerTrack =  16
  numberOfHeads =            2
  microsecondsPerSector =    2500
  tester board version =     2
  emulator board version =   2

  Drive Status 1 = 0x18

  Drive Status 2 = 0x7
tester-0>
```

There were no exceptions flagged regarding Drive Status 1 & 2, so we can proceed.

Entered the disk read command and the following is the response:

```
tester-0>disk read first.rke
  External Disk Read Image.
  external drive is ready
  microSD card is present
  filesystem started
  microSD LED is on
  opening the disk image file
  file_open_write_disk_image_n 'FIRST.RKE'
sd_spi_go_low_frequency: Actual frequency: 398089
V2-Version Card
R3/R7: 0x1aa
R3/R7: 0xff8000
R3/R7: 0x80ff8000
Card Initialized: Standard Capacity Card: Version 2.x
SD card initialized
Standard Capacity: c_size: 239
Sectors: 0x3c000 : 245760
Capacity: 0x7800000 : 120 MB
sd_spi_go_high_frequency: Actual frequency: 12500000
filename = FIRST.RKE
  writing the file header
  Writing header to file 'FIRST.RKE'
  Reading external disk data
    cylinder = 0
### ERROR, read command time exceeded in disk_read_image reading data,
    Check the controller mode setting, DISP STATUS, then MODE CONT <setting>
tester-0>
```

It seems possible that bad index or sector pulses or sector address signals might cause this.

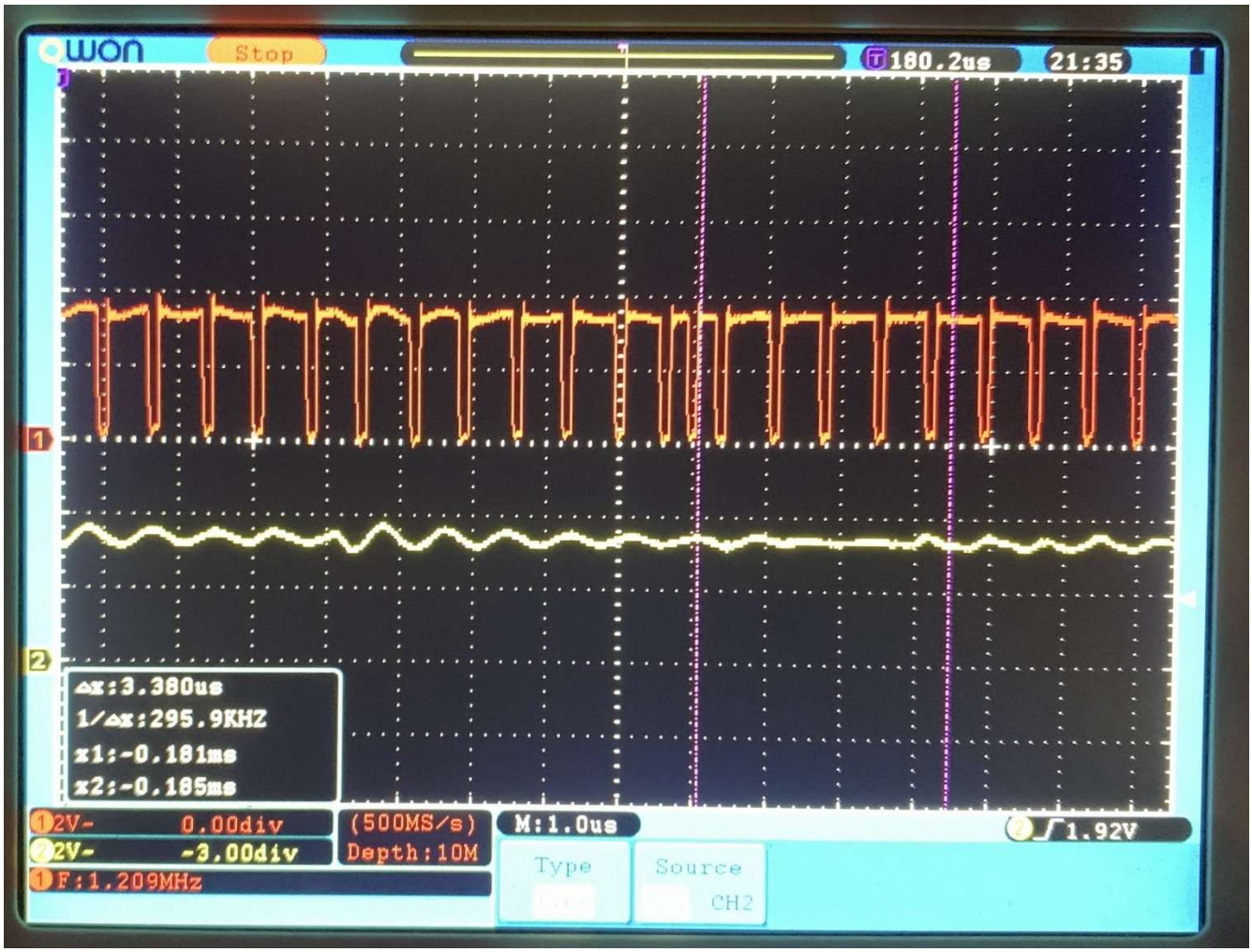
Confirmed that index and sector pulses and sector address signals are valid, so that's not the problem.

Set up a simple read loop:

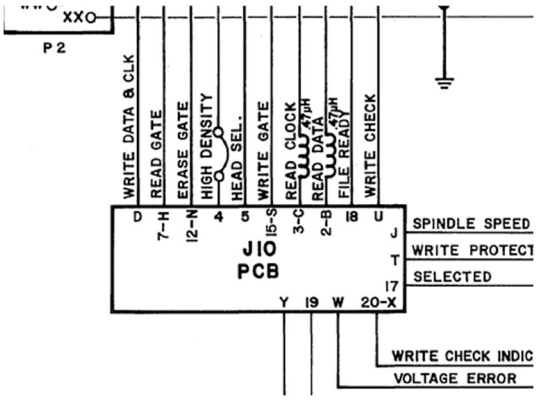
```
tester-0>m chs
  Make Cylinder Head Sector list. Enter Cylinder Head Sector parameters
  chs_list>0 0 0
  chs_list>x
List End, 1 items
tester-0>disp chs
  Cylinder Head Sector List
   #  cyl  h  sect
   0,   0, 0,  0
tester-0>read loop
  Read Loop test. Hit any key to stop the loop.
    list_item = 0
    list_item = 0
### ERROR, read command time exceeded in write_loop_zero reading data, testing
tester-0>
```

But even with the read command time exceeded error, the read gate is still active so the read data and clock signals can be probed.

Read Clock is CH1 and Read Data is CH2. It appears that the data pulses are still present in the read clock, and data isn't being separated onto Read Data as it should be. The bit rate appears to be about 1.44 Mbps.

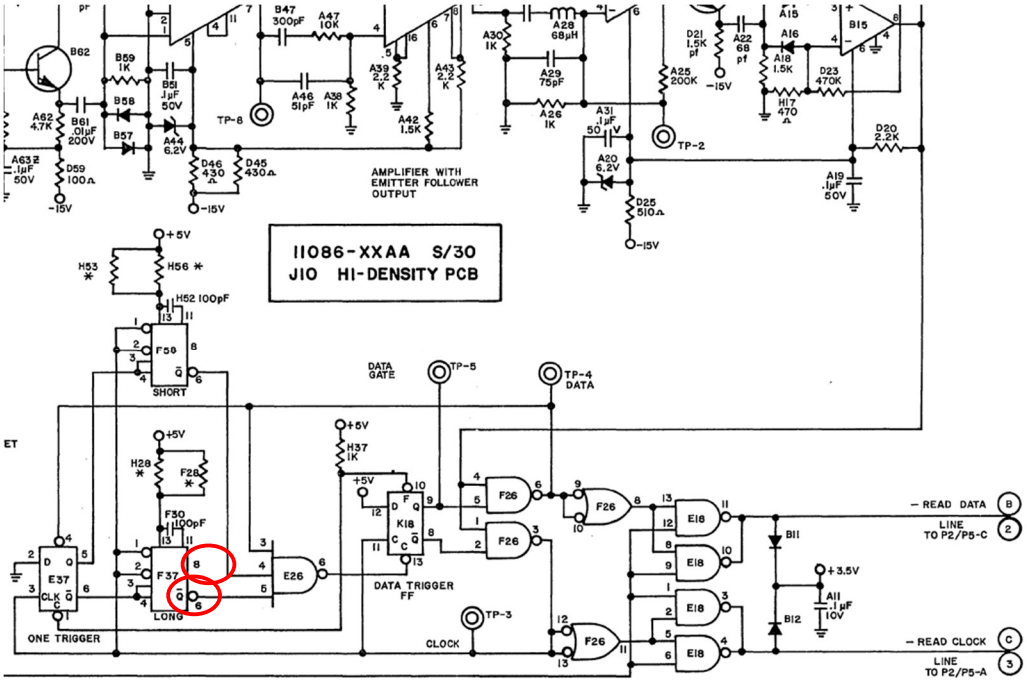


Trace Read Clock back from J10-3-C and Read Data back from J10-2-B.



On J10, TP3 looks like red trace above; TP4 always high; TP5 always low

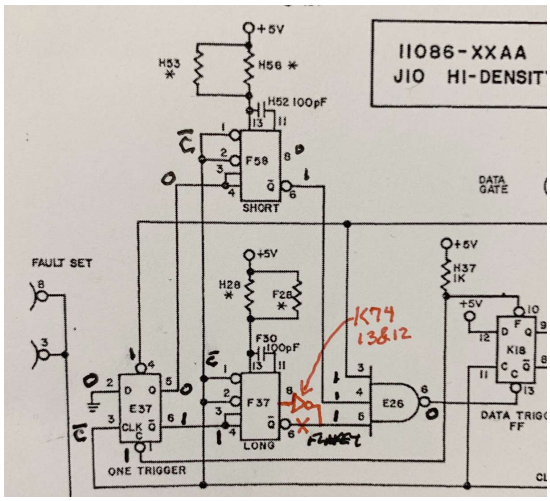
The schematic of the data recovery circuit on J10:



The Q output (pin 8) of F37 has pulses, but the Q-bar output (pin 6) appears to be stuck high.

F37 pin 8, Q output	F37 pin 6, Q-bar output
	

Since the Q-bar output seems defective, a temporary fix is to connect an unused inverter to the Q output of F37 (pin 8), and connect the output of that inverter to E26 pin 5:



March 13, 2025

Cut the leg of F37 pin 6, the Q-bar output of the DM8601 retriggerable one-shot. Connected a jumper from F37 pin 8 (the Q output of the one-shot) to K74 pin 13 (input of the spare inverter). Connected a second jumper from K74 pin 12 (output of the spare inverter) to the pad beneath F37 pin 6 (where the Q-bar output of the one-shot was connected before the pin was cut. This is a temporary work-around until the replacment DM8601 arrives.

After this temporary fix, clock and data appear to be correct, with a stream of periodic clock pulses and data pulses that appear in the center between the clock pulses:

...and the data rate appears to be about 1.4 Mbps

Next step: attempt to read the disk cartridge using the Tester. Entered the Disk Read command

```
tester-0>disk read d2315.rke
  External Disk Read Image.
  external drive is ready
  microSD card is present
  filesystem started
  microSD LED is on
  opening the disk image file
  file_open_write_disk_image_n 'D2315.RKE'
sd_spi_go_low_frequency: Actual frequency: 398089
V2-Version Card
R3/R7: 0x1aa
R3/R7: 0xff8000
R3/R7: 0x80ff8000
Card Initialized: Standard Capacity Card: Version 2.x
SD card initialized
Standard Capacity: c_size: 239
Sectors: 0x3c000 : 245760
Capacity: 0x7800000 : 120 MB
sd_spi_go_high_frequency: Actual frequency: 12500000
filename = D2315.RKE
  writing the file header
  Writing header to file 'D2315.RKE'
  Reading external disk data
    cylinder = 0
    cylinder = 20
    cylinder = 40
    cylinder = 60
    cylinder = 80
    cylinder = 100
    cylinder = 120
    cylinder = 140
    cylinder = 160
    cylinder = 180
    cylinder = 200
  Reading data from disk is complete.
  Writing external disk data to microSD.
  Writing disk image data to file 'D2315.RKE':
  cylinders=203, heads=2, sectors=16
    cylinder = 0
    cylinder = 20
    cylinder = 40
    cylinder = 60
    cylinder = 80
    cylinder = 100
    cylinder = 120
    cylinder = 140
    cylinder = 160
    cylinder = 180
    cylinder = 200
  writing image to microSD is complete
  Closing the microSD file.
  Closing the microSD file is complete
  The entire operation is complete
tester-0>
```

Made a backup of D2315.rke and copied it to another microSD card that was inserted into an emulator attached to the PDP-8/m. PDP-8/m has two emulators connected to its RK8-E. Drive 0 has a known good OS-8 image and drive 1 has the newly created D2315.RKE file.

RKB0: has a valid PDP-8 OS-8 directory and 71 files. However a entering DIR RKB1: produces:

```
.DIR RKB1:
BAD INPUT DIRECTORY
```

Wrote the OS8 image onto the 2315 disk cartridge using the Tester disk write command:

```
tester-0>disk write os8.rke
```

Then connected the Diablo drive to the PDP-8. Connected through the emulator on the right which is not loaded and set to drive 1. This emulator is only a pass-through for the disk signals. The Diablo drive is configured as drive 0. So, the Diablo is the only drive connected to the RK8-E controller in the PDP-8.

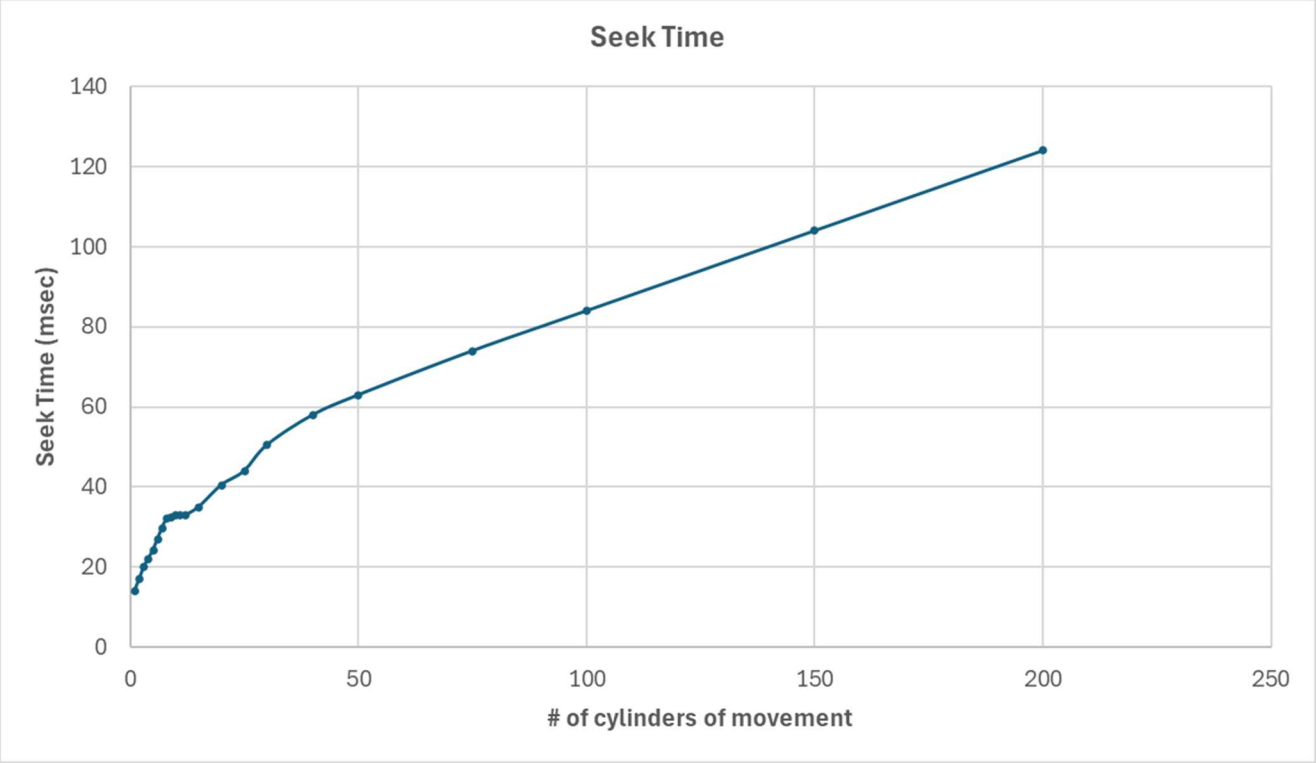
Was able to boot OS8 from the Diablo drive!

Still need to properly repair the board in J10. A pair of DM8601 one-shot ICs are on order. Need to replace the one at location F37 on the J10 board and remove the temporary jumpers.

March 14, 2025

There's still a problem with the drive. When running the `write loop random` test, there are occasional errors. Discovered that when seeking more than about 20 sectors (it seems to vary) then there are intermittent errors in the `write loop verify` test. The CHS list contained: 0 0 0, 20 0 0.

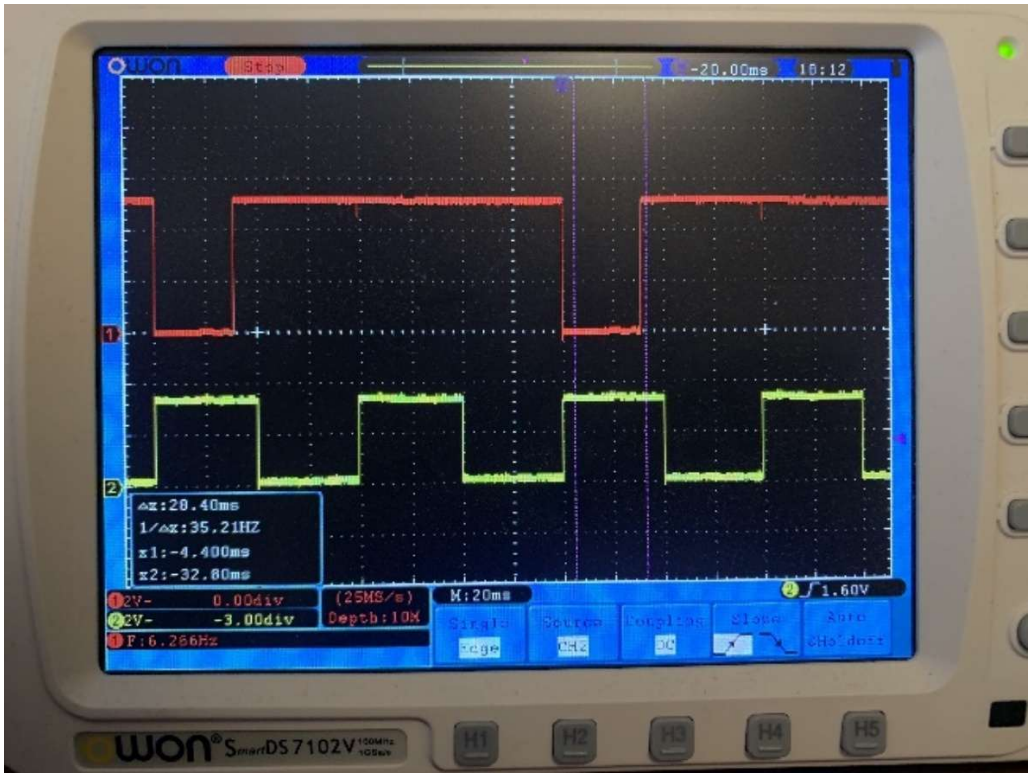
Collected data on the time when RWS ready is inactive after a seek operation, `w l n` command:



March 15, 2025

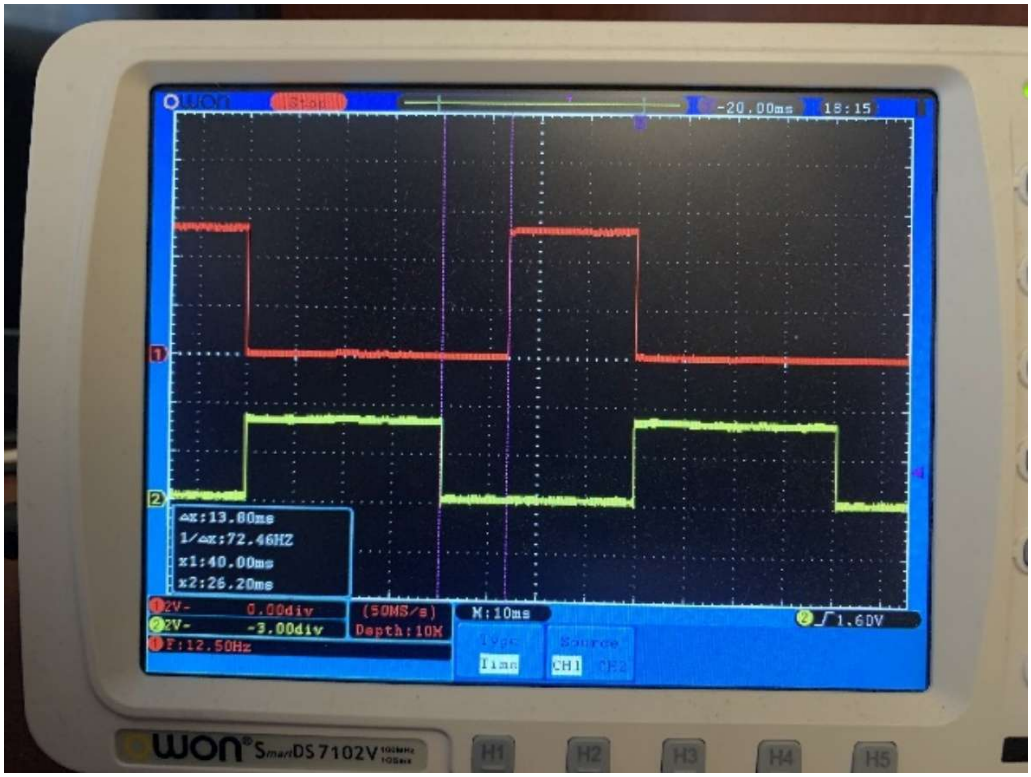
Observe the test points on module J2 in the digital circuit related to head movement. Entered a CHS list containing: 0 0 0, 20 0 0. CH1 (red) is TPx, CH2 (yellow) is BUS_RWS_RDY_L (pin F on the MRAC42):

- TP1 – always high, low sets the “SEEK INCOMPLETE FF”
- TP2 – always high, “RESTORE FF1-Q-bar”
- TP3 – same as RWS Ready, “-R/S/R/W”
- TP4 – “-REV & 1st SPEED”

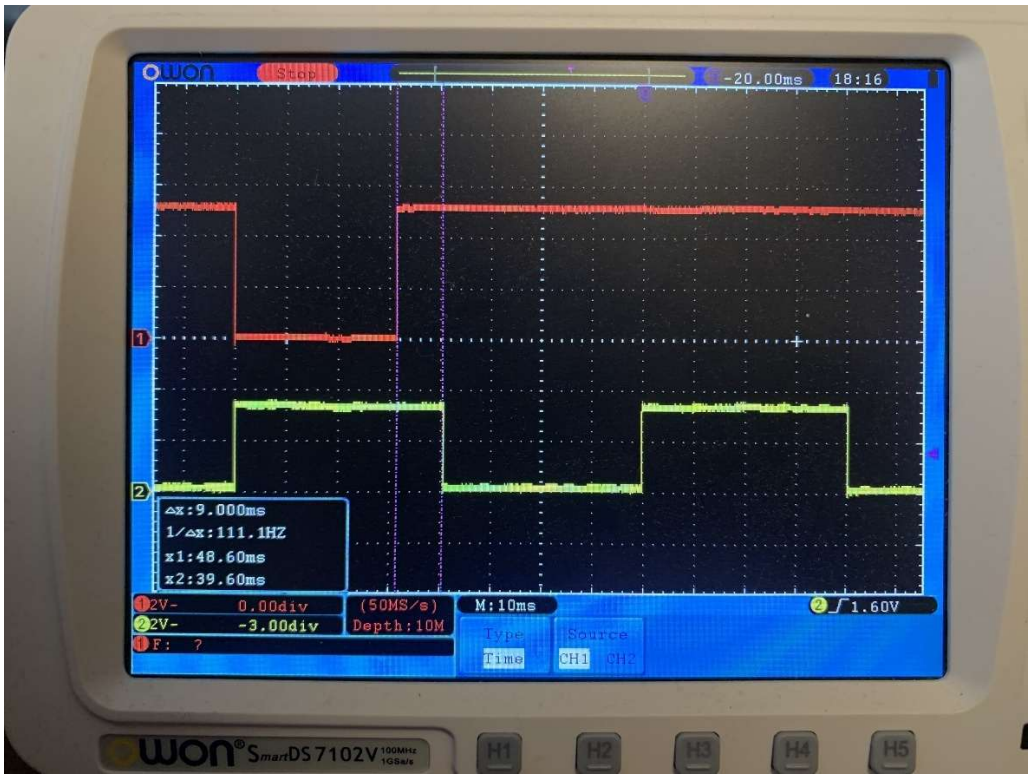


- TP5 – always high, “INITIAL RESET”

- TP6 – active-low “Motion Indicator Level”



- TP7 –



March 16, 2025

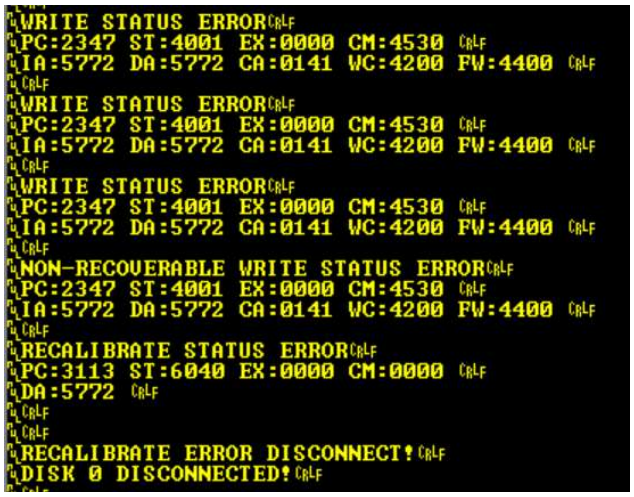
Motion Indicator Level signal, module J2 TP6:

In the last paragraph in section 4.6: “The remaining circuit on the J1 PCB is the Motion Indicator Level, which gives a low output at pins 14 and R only when the positioner has been stationary for the preceding 30 milliseconds. This signal is used to detect motion or the lack of motion during a Seek or Restore Operation.”

The signal shown in CH1 (red) above is the inverted Motion Indicator Level signal.

March 17, 2025

Connected the Diablo Model 31 to the RK8-E in the PDP-8/m, and ran “maindec-08-dhrkc-h-pb”. The following group of 3 Write Status Errors and one Non-recoverable Write Status Error repeated 6 times, followed by the Recalibrate Status Error at the end:



Before running this test with the Diablo I confirmed that the same maindec ran fine when the RK05 Emulator was attached to the 8/m.

March 19, 2025

Connected the Diablo Model 31 to the Tester. The read/write errors in the Tester appear to be related to a race condition in the Tester. The Tester asserts BUS_STROBE_L and shortly after checks BUS_RWS_RDY_L to determine if the seek operation has completed. With the Tester attached to the Diablo drive there's a 20µs delay from BUS_STROBE_L until the Diablo drive de-asserts BUS_RWS_RDY_L, so the Tester is checking too soon. Currently the Tester asserts BUS_STROBE_L and immediately checks BUS_RWS_RDY_L, which has not yet transitioned to the inactive state. Because of this, the Tester observes that the drive is ready before the drive is able to assert that the drive is not ready.

A debug pulse generating function (that generates a pulse on GP6) was inserted into the Tester software to observe the time where the Tester begins to sample the state of the BUS_RWS_RDY_L signal.

Photo #1,
CH1 – GP6 software debug pulse, CH2 – BUS_RWS_RDY_L
Shows that the sofware starts polling BUS_RWS_RDY_L before it goes to the not-ready state (high)

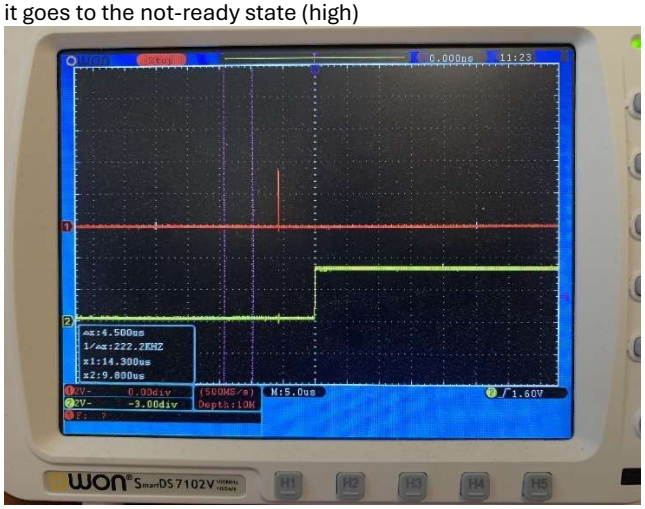


Photo #2,
CH1 – GP6 software debug pulse, CH2 – BUS_RWS_RDY_L
A high-level view of photo #1, shows that the sofware starts polling BUS_RWS_RDY_L at every seek operation

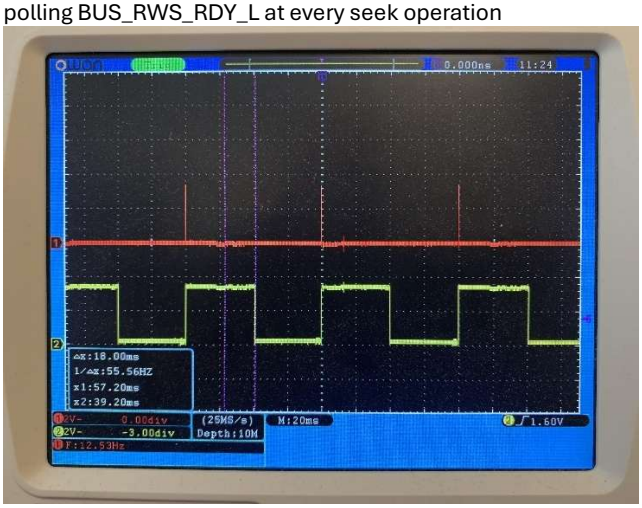


Photo #3,
CH1 – BUS_STROBE_L, CH2 – BUS_RWS_RDY_L
Shows when BUS_STROBE_L goes active and inactive. Same time base as photo #3 (20µs/division)

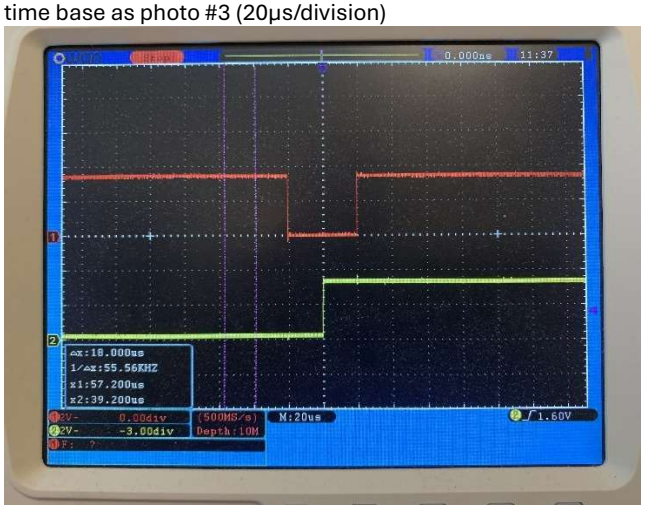
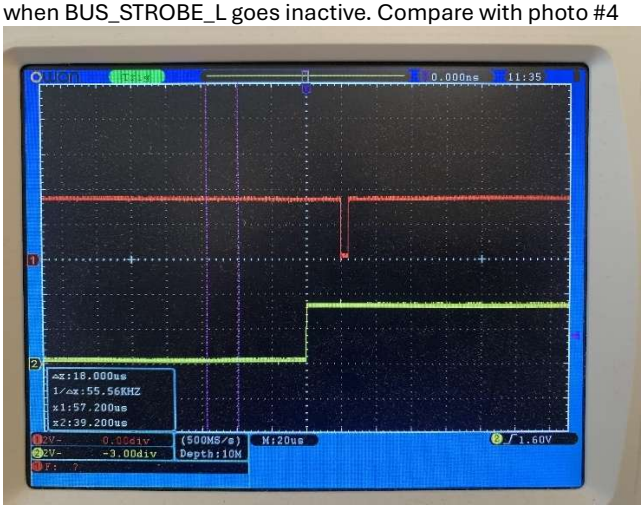


Photo #4,
CH1 – BUS_ADDR_ACCEPTED_L, CH2 – BUS_RWS_RDY_L
Shows BUS_ADDR_ACCEPTED_L is asserted at the same time when BUS_STROBE_L goes inactive. Compare with photo #4



Compared to the RK05 Emulator, the Diablo drive seems to have rather high latency to assert BUS_RWS_RDY_L after BUS_STROBE_L is asserted. The Diablo drive also seems to have a high latency to assert BUS_ADDR_ACCEPTED_L after BUS_STROBE_L is asserted.

These problems can fixed by having the Tester first observe that the command has been accepted by monitoring a latched version of the address accepted signal (BUS_ADDR_ACCEPTED_L) from the drive. The Tester receives BUS_ADDR_ACCEPTED_L from the drive and latches an FPGA internal signal called "address_accepted" which can be monitored in bit 6 of the Drive Status 1 register. The Tester should detect address_accepted prior to monitoring BUS_RWS_RDY_L to determine when the seek operation is complete.

This fix was implemented in all of the Tester functions that perform a disk seek operation. The Tester "write loop random" test now functions properly without reporting read/write data errors.

March 20, 2025

With the RK05 Emulator connected to the Tester, compare BUS_RWS_RDY_L, BUS_STROBE_L, and BUS_ADDR_ACCEPTED_L. Events happen much faster compared to the Diablo Drive.

Photo #1,
CH1 – BUS_STROBE_L, CH2 – BUS_RWS_RDY_L
Shows when BUS_STROBE_L goes active and inactive. Same time base as photo #2 (500ns/division)

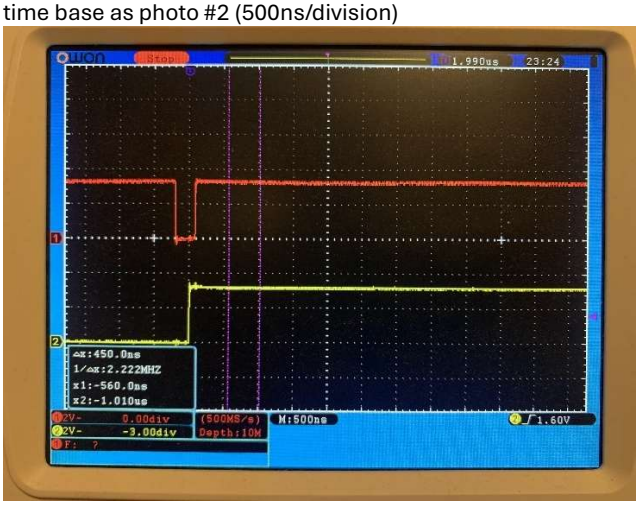
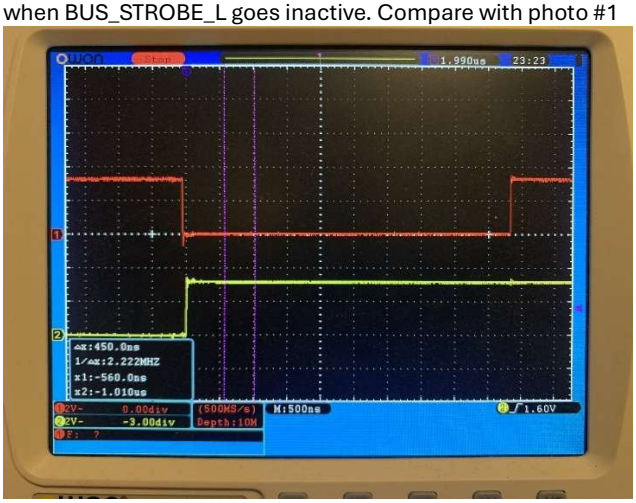


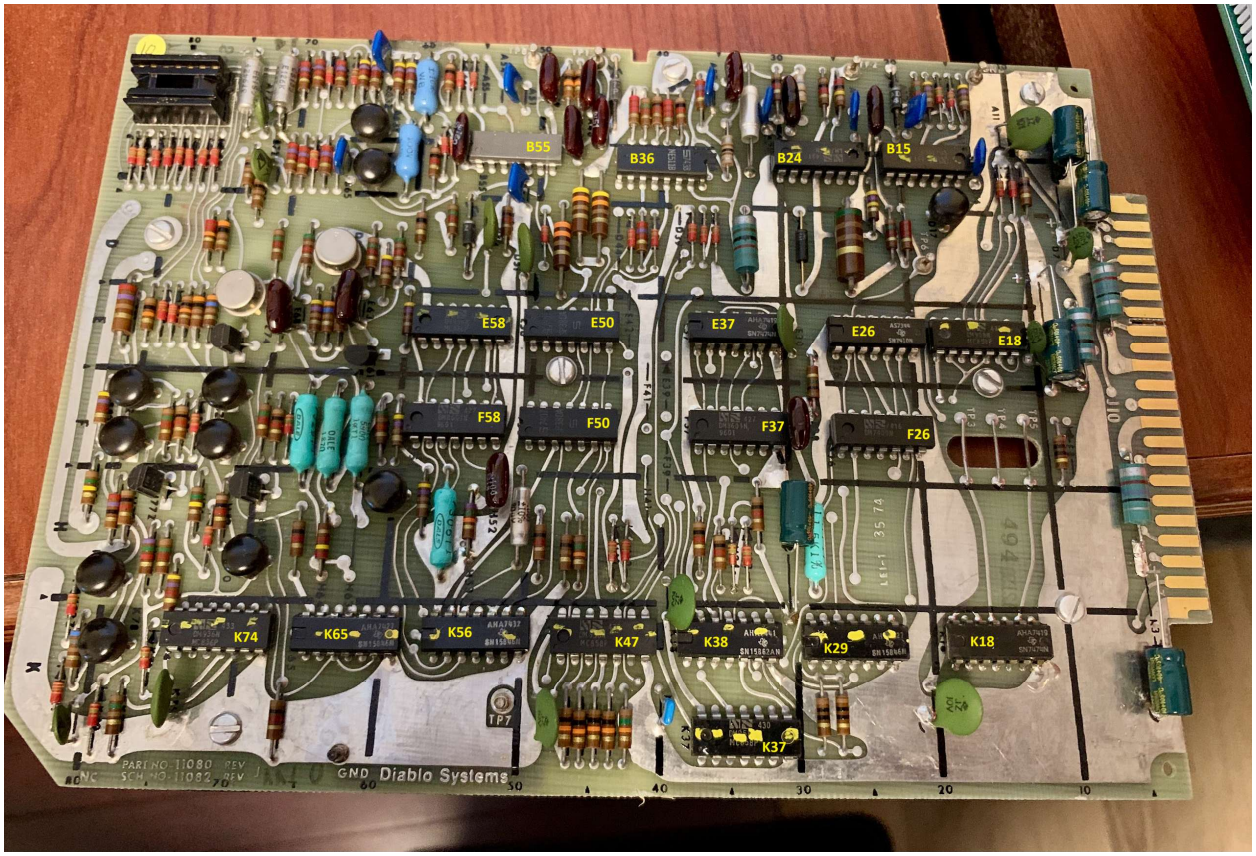
Photo #2,
CH1 – BUS_ADDR_ACCEPTED_L, CH2 – BUS_RWS_RDY_L
Shows BUS_ADDR_ACCEPTED_L is asserted at the same time when BUS_STROBE_L goes inactive. Compare with photo #1



I'm wondering whether the Diablo drive responding slowly to the BUS_STROBE_L might be the cause of the "maindec-08-dhrkc-h-pb" test failures.

Afterthoughts:

- I thought about designing an extender board to be able to more easily probe circuits on the six plug-in cards. The extender would need to offset in one direction to have mechanical clearance from the frame of the disk drive. Fortunately, most of the probing was on J10, which is on the end of the backplane, on the left side of the drive. It was possible to remove the metal shield from the J10 board to be able to probe circuitry from the back.



- The Tester command `read loop` was very convenient for debugging the fault in the data separator circuit.

```
tester-0>m chs
  Make Cylinder Head Sector list. Enter Cylinder Head Sector parameters
  chs_list>0 0 0
  chs_list>x
List End, 1 items
tester-0>disp chs
  Cylinder Head Sector List
   #  cyl  h  sect
   0,   0, 0,  0
tester-0>read loop
```

- x