


## 6-axis inertial measurement unit (IMU) for automotive applications



LGA-14L  
Typ: 2.5 x 3.0 x 0.83 mm<sup>3</sup>

## Features

- AEC-Q100 qualified 
- Extended temperature range from -40 to +105°C
- Embedded compensation for high stability over temperature
- Accelerometer user-selectable full scale up to  $\pm 16\text{ g}$
- Extended gyroscope range from  $\pm 125$  to  $\pm 2000\text{ dps}$
- SPI and I<sup>2</sup>C host serial interface
- Six-channel synchronized output to enhance accuracy of dead-reckoning algorithms
- Smart programmable interrupts
- Embedded 3 KB FIFO available to underload host processor
- ECOPACK and RoHS compliant

## Applications

- Dead reckoning (DR)
- Vehicle-to-everything (V2X)
- Telematics, eTolling
- Anti theft systems
- Impact detection and crash reconstruction
- Motion-activated functions
- Vibration monitoring and compensation, driving comfort

## Description

The ASM330LHM is an IMU sensor featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope with an extended temperature range up to +105°C and designed to address automotive nonsafety applications.

ST's family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve both the automotive and consumer market. The ASM330LHM is AEC-Q100 compliant and industrialized through a dedicated MEMS production flow to meet automotive reliability standards. All the parts are fully tested with respect to temperature to ensure the highest quality level.

The sensing elements are manufactured using ST's proprietary micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHM has a full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16\text{ g}$  and a wide angular rate range of  $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000\text{ dps}$  that enables its usage in a broad range of automotive applications.

All the design aspects of the ASM330LHM have been optimized to reach superior output stability, extremely low noise, and full data synchronization to the benefit of sensor-assisted applications like dead reckoning and sensor fusion.

The ASM330LHM is available in a 14-lead plastic, land grid array (LGA) package.

## Product status

Custom data

## Product summary

Order code	ASM330LHMTR
Temp. range [°C]	-40 to +105
Package	LGA-14L (2.5 x 3.0 x 0.83 mm <sup>3</sup> )
Packing	Tape and reel

## Product resources

[TN0018](#) (design and soldering)

## Product labels





## 1 Overview

The ASM330LHM is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

This device is suitable for telematics and dead-reckoning applications as well as vehicle-to-vehicle (V2X) and impact detection as a result of its high stability over temperature and time, combined with superior sensing precision.

The event-detection interrupts enable efficient and reliable motion-activated functions, implementing hardware recognition of free-fall events, 6D orientation, activity or inactivity, and wake-up events.

Up to 3 KB of FIFO allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the ASM330LHM leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHM is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultracompact solutions.



## 2 Embedded low-power features

The ASM330LHM has been designed to feature the following on-chip functions:

- 3 KB data buffering
  - 100% efficiency with flexible configurations and partitioning
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Activity / inactivity recognition



### 3 Pin description

Figure 1. Pin connections

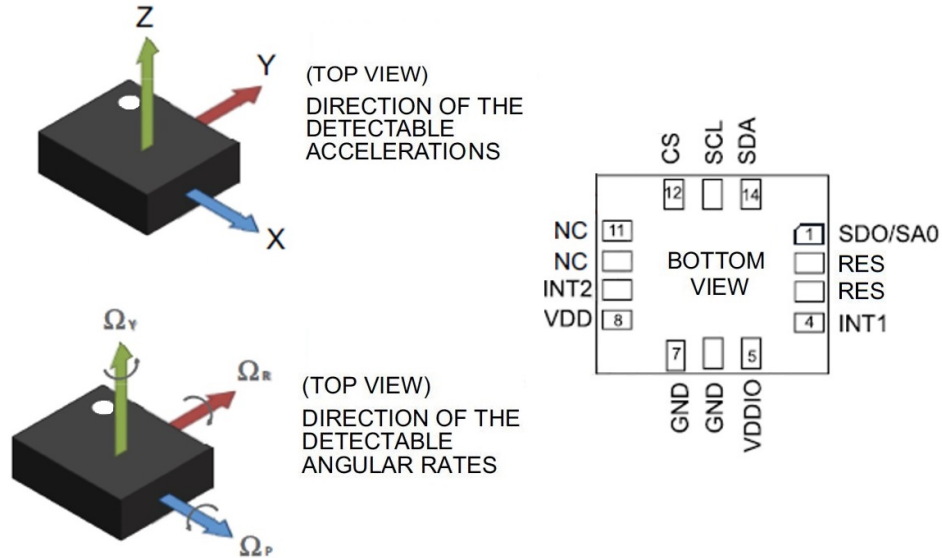


Table 1. Pin description

Pin#	Name	Function
1	SDO SA0	SPI 4-wire serial data output (SDO) I <sup>2</sup> C least significant bit of the device address (SA0)
2	RES	Connect to VDDIO or GND
3	RES	Connect to VDDIO or GND
4	INT1 <sup>(1)</sup>	Programmable interrupt #1
5	VDDIO <sup>(2)</sup>	Power supply for I/O pin
6	GNSD	Connect to GND
7	GND	Connect to GND
8	VDD <sup>(3)</sup>	Power supply
9	INT2	Programmable interrupt #2 (INT2) / Data enabled (DEN)
10	NC	Leave unconnected
11	NC	Leave unconnected
12	CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled and reset)
13	SCL	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. INT1 must be set to 0 or left unconnected during power-on.

2. Recommended 100 nF filter capacitor.

3. Recommended 100 nF plus 10  $\mu$ F capacitors.



## 4 Module specifications

### 4.1 Mechanical characteristics

@VDD = 3.0 V, T = -40°C to +105°C, up to gyroscope FS = ±2000 dps unless otherwise noted. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.0 V to 3.6 V.

**Table 2. Mechanical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		g
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
LA_So	Linear acceleration sensitivity <sup>(2)</sup>	@LA_FS = ±2 g		0.061		mg/LSB
		@LA_FS = ±4 g		0.122		
		@LA_FS = ±8 g		0.244		
		@LA_FS = ±16 g		0.488		
G_So	Angular rate sensitivity <sup>(2)</sup>	@G_FS = ±125 dps		4.37		mdps/LSB
		@G_FS = ±250 dps		8.75		
		@G_FS = ±500 dps		17.5		
		@G_FS = ±1000 dps		35.0		
		@G_FS = ±2000 dps		70.0		
LA_So%	Sensitivity tolerance <sup>(3)</sup>	at component level @25°C	-5		+5	%
G_So%	Sensitivity tolerance <sup>(3)</sup>	at component level @25°C	-5		+5	%
LA_SoDr	Linear acceleration sensitivity change vs. temperature <sup>(4)</sup>			±100		ppm/°C
G_SoDr	Angular rate sensitivity change vs. temperature <sup>(4)</sup>			±100		ppm/°C
LA_TyOff	Linear acceleration zero-g level offset accuracy <sup>(5)</sup>		-100		+100	mg
G_TyOff	Angular rate zero-rate level <sup>(5)</sup>		-12		+12	dps
LA_TCOff	Linear acceleration zero-g level change vs. temperature <sup>(4)</sup>			±0.20		mg/°C
G_TCOff	Angular rate typical zero-rate level change vs. temperature <sup>(4)</sup>			±0.01		dps/°C
LA_Cx	Linear acceleration cross-axis sensitivity	T = 25°C		±1		%
G_Cx	Angular rate cross-axis sensitivity	T = 25°C		±1		%
Rn	Rate noise density <sup>(6)</sup>			5	12	mdps/√Hz
NL	Nonlinearity <sup>(7)</sup>	Best-fit straight line		0.01		% FS
ARW	Angular random walk <sup>(7)</sup>	T = 25°C		0.21		deg/√h
BI	Bias instability <sup>(7)</sup>	T = 25°C		3		deg/h
An	Acceleration noise density <sup>(8)</sup>	@LA_FS = ±2 g		80	270	μg/√Hz



Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_ODR	Linear acceleration output data rate			12.5 26 52 104 208 416 833 1667 3333 6667		Hz
G_ODR	Angular rate output data rate			12.5 26 52 104 208 416 833 1667 3333 6667		
Vst	Linear acceleration self-test output change <sup>(9)(10)(11)(12)</sup>		40		1700	mg
	Angular rate self-test output change <sup>(13)(14)</sup>	FS = $\pm 250$ dps	20		80	dps
		FS = $\pm 2000$ dps	150		700	dps
Top	Operating temperature range		-40		+105	°C

1. Typical specifications are not guaranteed.
2. Sensitivity values after factory calibration test and trimming.
3. Subject to change.
4. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.
5. Across temperature and life. Assuming post-solder effect compensated at the end of production line.
6. Gyroscope rate noise density is independent of the ODR for FS up to  $\pm 2000$  dps, max value specified at ambient temperature.
7. Based on characterization data on a limited number of samples. Not measured during final test for production.
8. Accelerometer noise density is independent of the ODR, max value specified at ambient temperature.
9. The sign of the linear acceleration self-test output change is defined by the STx\_XL bits in a dedicated register for all axes.
10. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at  $\pm 2$  g full scale.
11. Accelerometer self-test limits are full-scale independent.
12. The self-test output change limits include full VDD range and impact of soldering.
13. The sign of the angular rate self-test output change is defined by the STx\_G bits in a dedicated register for all axes.
14. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at  $\pm 2000$  dps full scale.



## 4.2 Electrical characteristics

@VDD = 3.0 V, T = -40°C to +105°C, up to gyroscope FS = ±2000 dps unless otherwise noted

**Table 3. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
VDD	Supply voltage		2.0		3.6	V
VDDIO	Power supply for I/O		1.62		3.6	V
GA_Idd	Gyroscope and accelerometer current consumption	ODR = 1.6 kHz		2.0	2.5	mA
A_Idd	Accelerometer current consumption	ODR < 1.6 kHz		360	530	µA
IddPD	Gyroscope and accelerometer current consumption during power-down	@25°C		3	13	µA
Ton	Turn-on time <sup>(2)</sup>			35		ms
V <sub>IH</sub> <sup>(3)</sup>	Digital high-level input voltage		0.7 * VDDIO			V
V <sub>IL</sub> <sup>(3)</sup>	Digital low-level input voltage				0.3 * VDDIO	V
V <sub>OH</sub> <sup>(3)</sup>	High-level output voltage	I <sub>OH</sub> = 4 mA <sup>(4)</sup>	VDDIO - 0.2			V
V <sub>OL</sub> <sup>(3)</sup>	Low-level output voltage	I <sub>OL</sub> = 4 mA <sup>(4)</sup>			0.2	V
Top	Operating temperature range		-40		+105	°C

1. Typical specifications are not guaranteed.
2. Time to obtain stable sensitivity (within ±5% of final value) switching from power-down to normal operation
3. Specified by design characterization and not tested in production
4. 4 mA is the minimum driving capability, that is, the minimum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

## 4.3 Temperature sensor characteristics

@VDD = 3.0 V, T = 25°C unless otherwise noted. The product is factory calibrated at 3.0 V.

**Table 4. Temperature sensor characteristics**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
TODR	Temperature refresh rate			52		Hz
Toff	Temperature offset <sup>(2)</sup>		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time <sup>(3)</sup>				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+105	°C

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25°C.
3. Time from power ON bit to valid output data. Based on characterization.



## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

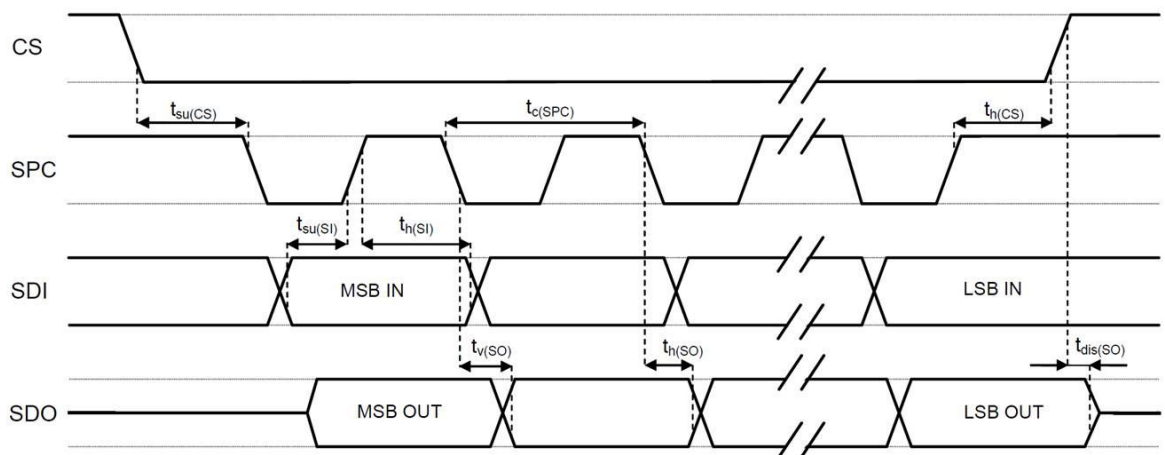
Subject to general operating conditions for VDD and Top.

**Table 5. SPI slave timing values (in mode 3)**

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are specified at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

**Figure 2. SPI slave timing diagram (in mode 3)**



**Note:** Measurement points are done at  $0.3 \cdot VDDIO$  and  $0.7 \cdot VDDIO$  for both input and output ports.





#### 4.4.2 I<sup>2</sup>C - inter-IC control interface

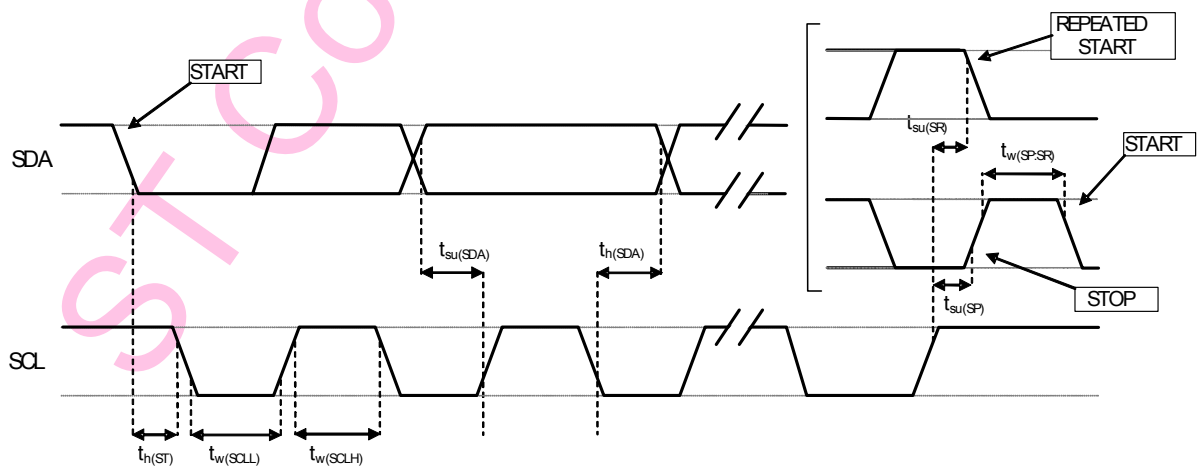
Subject to general operating conditions for VDD and Top.

**Table 6. I<sup>2</sup>C slave timing values**

Symbol	Parameter	I <sup>2</sup> C standard mode <sup>(1)</sup>		I <sup>2</sup> C fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		$\mu$ s
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_h(SDA)$	SDA data hold time	0	3.45	0	0.9	$\mu$ s
$t_h(ST)$	START condition hold time	4		0.6		
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

**Figure 3. I<sup>2</sup>C slave timing diagram**



**Note:** Measurement points are done at  $0.3 \cdot VDDIO$  and  $0.7 \cdot VDDIO$  for both ports.



## 4.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
Sg	Acceleration <i>g</i> for 0.3 ms	3000	<i>g</i>
ESD	Electrostatic discharge protection (HBM)	2	kV
V <sub>in</sub>	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to VDDIO +0.3	V

**Note:** Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.



## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 g acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky), and noting the output value again. By doing so,  $\pm 1$  g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see [Table 2](#)).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see [Table 2](#)).

### 4.6.2 Zero-g and zero-rate level

Linear acceleration zero-g level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 g on both the X-axis and Y-axis, whereas the Z-axis measures 1 g. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-g offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-g level change vs. temperature" in [Table 2](#). The zero-g level tolerance (TyOff) describes the standard deviation of the range of zero-g levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see [Table 2](#)).



## 5 Digital interfaces

### 5.1 I<sup>2</sup>C/SPI interface

The registers embedded inside the ASM330LHM may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (that is, connected to VDDIO).

**Table 8. Serial interface pin description**

Pin name	Pin description
CS	Enables SPI I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
SCL/SPC	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I <sup>2</sup> C less significant bit of the device address

#### 5.1.1 I<sup>2</sup>C serial interface

The ASM330LHM I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 9. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to VDDIO through external pull-up resistors. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the standard mode.

In order to disable the I<sup>2</sup>C block, (I2C\_disable) = 1 must be written in CTRL4\_C (13h).



## I<sup>2</sup>C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the ASM330LHM is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by the CTRL3\_C (12h) (IF\_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 10 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 10. SAD+read/write patterns**

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

**Table 11. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 12. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 13. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+ W		SUB		SR	SAD+ R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		



Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

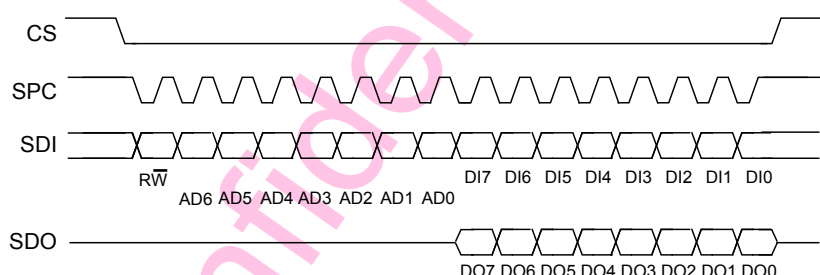
### 5.1.2

#### SPI bus interface

The ASM330LHM SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

**Figure 4. Read and write protocol (in mode 3)**



**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

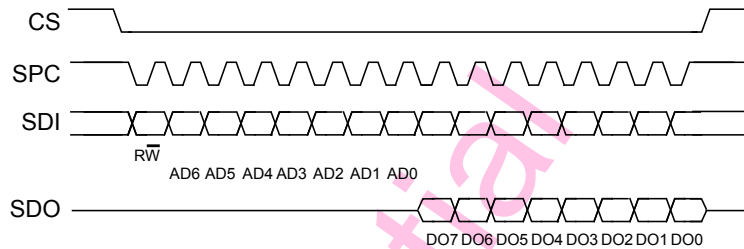
In multiple read/write commands, further blocks of 8 clock periods are added. When the CTRL3\_C (12h) (IF\_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3\_C (12h) (IF\_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.



### 5.1.2.1 SPI read

**Figure 5. SPI read protocol (in mode 3)**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

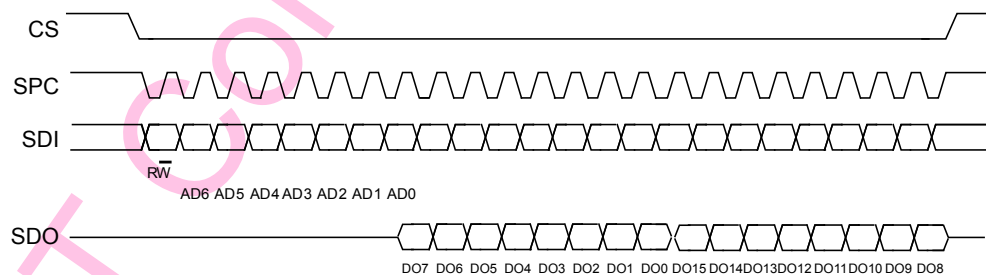
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

**bit 16-...:** data DO(...-8). Further data in multiple byte reads.

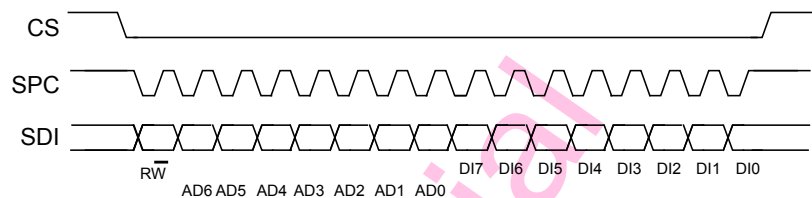
**Figure 6. Multiple byte SPI read protocol (2-byte example) (in mode 3)**





### 5.1.2.2 SPI write

**Figure 7. SPI write protocol (in mode 3)**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

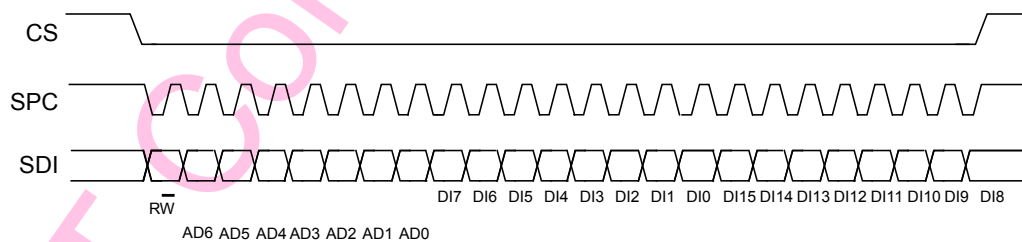
**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

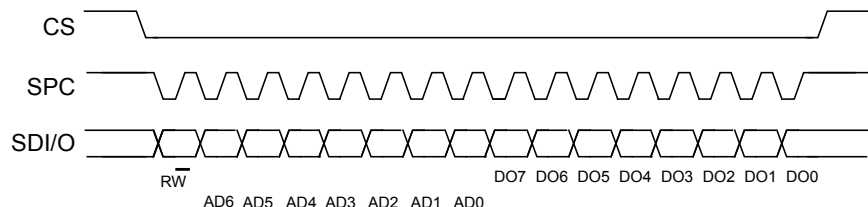
**Figure 8. Multiple byte SPI write protocol (2-byte example) (in mode 3)**



### 5.1.2.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the CTRL3\_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

**Figure 9. SPI read protocol in 3-wire mode (in mode 3)**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.





## 6 Functionality

### 6.1 Operating modes

In the ASM330LHM, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The ASM330LHM has three operating modes available:

- Only accelerometer active and gyroscope in power-down or sleep mode
- Only gyroscope active and accelerometer in power-down
- Both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR\_XL[3:0] in CTRL1\_XL (10h) while the gyroscope is activated from power-down by writing ODR\_G[3:0] in CTRL2\_G (11h). For combo mode, the ODRs are totally independent.

### 6.2 Gyroscope power modes

In the ASM330LHM, the gyroscope can be configured in two different operating modes: power-down and high-performance mode. High-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

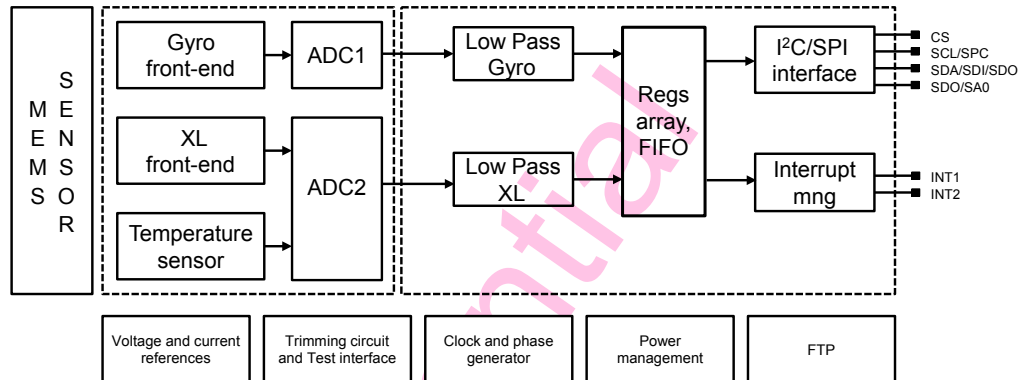
### 6.3 Accelerometer power modes

In the ASM330LHM, the accelerometer can be configured in two different operating modes: power-down and high-performance mode. High-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).



## 6.4 Block diagram of filters

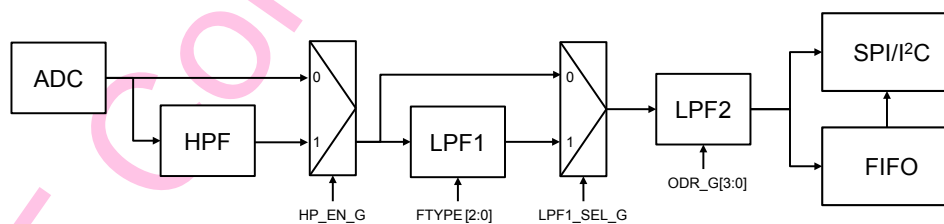
Figure 10. Block diagram of filters



### 6.4.1 Block diagram of the gyroscope filter

The gyroscope filtering chain appears below.

Figure 11. Gyroscope filtering chain



The gyroscope ODR is selectable from 12.5 Hz up to 6.66 kHz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see [Table 52. Gyroscope LPF1 bandwidth selection](#). The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

**Note:** Data can be acquired from the output registers and FIFO.

Table 15. Gyroscope LPF2 bandwidth selection

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
12.5	4.3
26	8.3
52	16.7
104	33
208	67
417	133
833	267
1667	539
3333	1137
6667	3333



### 6.4.2 Block diagrams of the accelerometer filters

In the ASM330LHM, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 12. Accelerometer chain

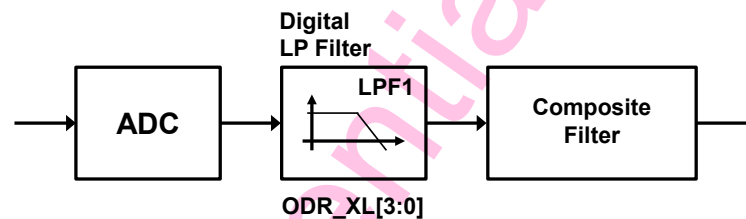
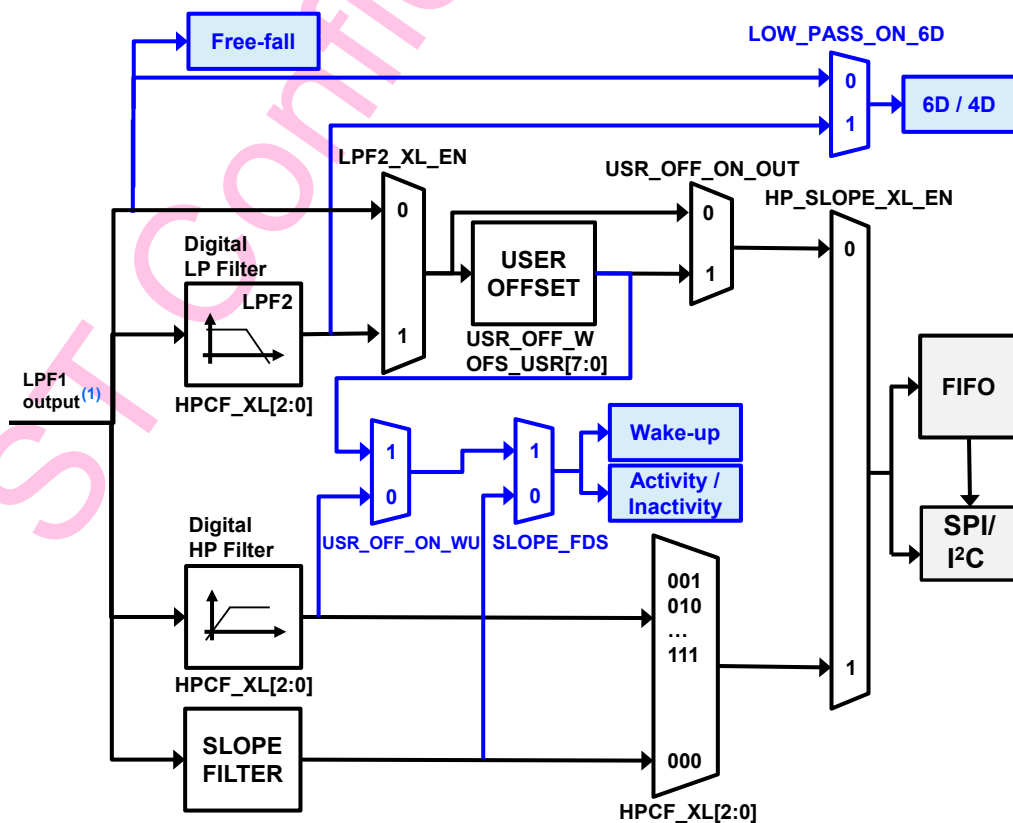


Figure 13. Accelerometer composite filter



1. The cutoff value of the LPF1 output is  $ODR/2$ .



## 6.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The ASM330LHM embeds 3 KB of data in FIFO to store the following data:

- Gyroscope
- Accelerometer
- Timestamp
- Temperature

Writing data in the FIFO is triggered by the accelerometer / gyroscope data-ready signal.

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO\_DATA\_OUT\_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

The programmable FIFO watermark threshold can be set in FIFO\_CTRL1 (07h) and FIFO\_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO\_STATUS1 (3Ah), FIFO\_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1\_CTRL (0Dh) and INT2\_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- Bypass mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 (0Ah) register.

### 6.5.1 Bypass mode

In bypass mode (FIFO\_CTRL4 (0Ah)(FIFO\_MODE\_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

### 6.5.2 FIFO mode

In FIFO mode (FIFO\_CTRL4 (0Ah)(FIFO\_MODE\_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO\_CTRL4 (0Ah)(FIFO\_MODE\_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO\_CTRL4 (0Ah)(FIFO\_MODE\_[2:0]) to 001.

The FIFO buffer memorizes up to 3 KB of data but the depth of the FIFO can be resized by setting the WTM[8:0] bits in FIFO\_CTRL1 (07h) and FIFO\_CTRL2 (08h). If the STOP\_ON\_WTM bit in FIFO\_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[8:0] bits in FIFO\_CTRL1 (07h) and FIFO\_CTRL2 (08h).



### 6.5.3 Continuous mode

Continuous mode **FIFO\_CTRL4 (0Ah)**(FIFO\_MODE\_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag **FIFO\_STATUS2 (3Bh)**(FIFO\_WTM\_IA) is asserted when the number of unread samples in FIFO is greater than or equal to **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**(WTM[8:0]).

It is possible to route the FIFO\_WTM\_IA flag to the INT1 pin by writing in register **INT1\_CTRL (0Dh)** (INT1\_FIFO\_TH) = 1 or to the INT2 pin by writing in register **INT2\_CTRL (0Eh)**(INT2\_FIFO\_TH) = 1.

A full-flag interrupt can be enabled, **INT1\_CTRL (0Dh)**(INT1\_FIFO\_FULL) = 1 or **INT2\_CTRL (0Eh)** (INT2\_FIFO\_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO\_OVR\_IA flag in **FIFO\_STATUS2 (3Bh)** is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in **FIFO\_STATUS1 (3Ah)** and **FIFO\_STATUS2 (3Bh)**(DIFF\_FIFO\_[9:0]).

### 6.5.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (**FIFO\_CTRL4 (0Ah)**(FIFO\_MODE\_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

### 6.5.5 Bypass-to-continuous mode

In bypass-to-continuous mode (**FIFO\_CTRL4 (0Ah)**(FIFO\_MODE\_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

### 6.5.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode (**FIFO\_CTRL4 (0Ah)**(FIFO\_MODE\_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D



### 6.5.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (**FIFO\_DATA\_OUT\_TAG** (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO\_DATA\_OUT registers from (79h) to (7Eh)).

The DIFF\_FIFO\_[9:0] field in the **FIFO\_STATUS1** (3Ah) and **FIFO\_STATUS2** (3Bh) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of the accelerometer or gyroscope sensors. The flag COUNTER\_BDR\_IA in **FIFO\_STATUS2** (3Bh) alerts that the counter has reached a selectable threshold (CNT\_BDR\_TH\_[9:0] field in **COUNTER\_BDR\_REG1** (0Bh) and **COUNTER\_BDR\_REG2** (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG\_COUNTER\_BDR bit in **COUNTER\_BDR\_REG1** (0Bh). As for the other FIFO status events, the flag COUNTER\_BDR\_IA can be routed to the INT1 or INT2 pins by asserting the corresponding bits (INT1\_CNT\_BDR of **INT1\_CTRL** (0Dh) and INT2\_CNT\_BDR of **INT2\_CTRL** (0Eh)).

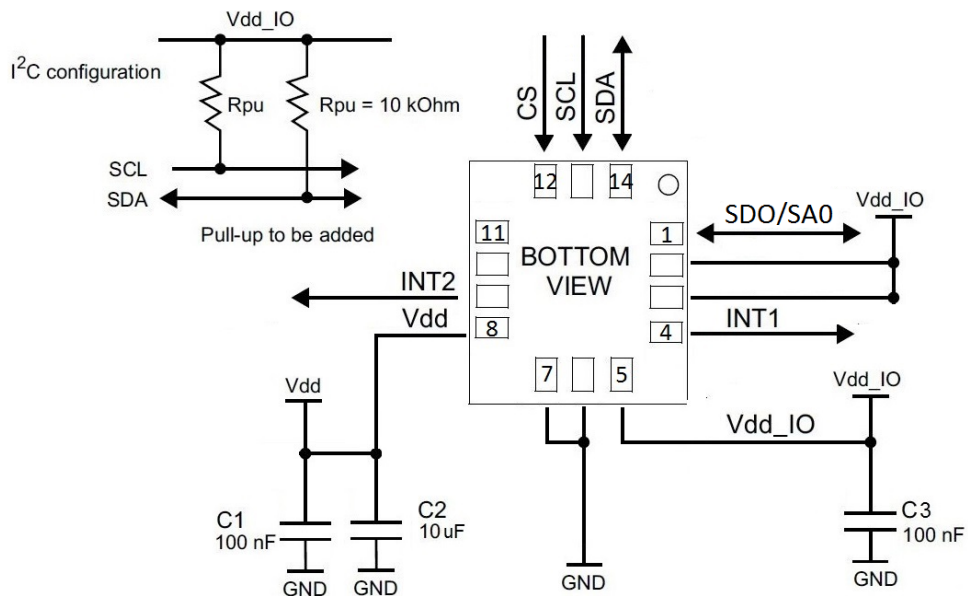
Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR\_CHG\_EN bit in **FIFO\_CTRL2** (08h).



## 7 Application hints

### 7.1 ASM330LHM electrical connections

Figure 14. ASM330LHM electrical connections



The device core is supplied through the VDD line while the I/O pads are supplied through the VDDIO line. As a common design practice, the power supply decoupling capacitors C1 = 100 nF ceramic and C2 = 10 µF aluminum should be placed as near as possible to pin 8, while C3 = 100 nF ceramic should be positioned as close as possible to pin 5.

All the voltage and ground supplies must be present at the same time to have proper IC behavior.

The functionality of the device and the measured acceleration/angular rate data are selectable and accessible through the I<sup>2</sup>C or SPI interfaces. When using the I<sup>2</sup>C protocol, CS must be tied high. Every time the CS line is set to low level, the I<sup>2</sup>C bus is internally reset.

All the functions, the threshold and the timing of the two interrupt pins can be completely programmed by the user through the I<sup>2</sup>C/SPI interface.



The procedure to correctly initialize the device is as follows:

1. INT1: Leave unconnected or connect with external pull-down during power-on. Pull-up must be avoided on this pin.
2. INT2: Recommended to not connect with external pull-up.
3. Properly configure the device:
  - a. SPI case: I2C\_disable = 1 in CTRL4\_C (13h) and DEVICE\_CONF = 1 in CTRL9\_XL (18h).
  - b. I<sup>2</sup>C case: I2C\_disable = 0 (default) in CTRL4\_C (13h) and DEVICE\_CONF = 1 in CTRL9\_XL (18h).

**Table 16. Internal pin status**

Pin#	Name	Function	Pin status
1	SDO	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).
	SA0	I <sup>2</sup> C least significant bit of the device address (SA0)	
2	RES	Connect to VDDIO or GND	Default: input without pull-up
3	RES	Connect to VDDIO or GND	Default: input without pull-up
4	INT1	Programmable interrupt 1	Default: input with pull-down <sup>(1)</sup>
5	VDDIO	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	VDD	Power supply	
9	INT2	Programmable interrupt 2 (INT2) / Data enabled (DEN)	Default: output forced to ground
10	NC	Leave unconnected	Default: input with pull-up
11	NC	Leave unconnected	Default: input with pull-up
12	CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)	Default: input with pull-up Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and DEVICE_CONF = 1 in register CTRL9_XL (18h).
13	SCL	I <sup>2</sup> C serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up
14	SDA	I <sup>2</sup> C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up

1. INT1 must be set to 0 or left unconnected during power-on.





## 8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

**Table 17. Registers address map**

Name	Type	Register address		Default	Comment
		Hex	Binary		
PIN_CTRL	R/W	02	00000010	00111111	
RESERVED	-	04-06			Reserved
FIFO_CTRL1	R/W	07	00000111	00000000	
FIFO_CTRL2	R/W	08	00001000	00000000	
FIFO_CTRL3	R/W	09	00001001	00000000	
FIFO_CTRL4	R/W	0A	00001010	00000000	
COUNTER_BDR_REG1	R/W	0B	00001011	00000000	
COUNTER_BDR_REG2	R/W	0C	00001100	00000000	
INT1_CTRL	R/W	0D	00001101	00000000	
INT2_CTRL	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01101011	
CTRL1_XL	R/W	10	00010000	00000000	
CTRL2_G	R/W	11	00010001	00000000	
CTRL3_C	R/W	12	00010010	00000100	
CTRL4_C	R/W	13	00010011	00000000	
CTRL5_C	R/W	14	00010100	00000000	
CTRL6_C	R/W	15	00010101	00000000	
CTRL7_G	R/W	16	00010110	00000000	
CTRL8_XL	R/W	17	0001 0111	00000000	
CTRL9_XL	R/W	18	00011000	11100000	
CTRL10_C	R/W	19	00011001	00000000	
ALL_INT_SRC	R	1A	00011010	output	
WAKE_UP_SRC	R	1B	00011011	output	
RESERVED		1C	00011100	output	
D6D_SRC	R	1D	00011101	output	
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F	00011111		
OUT_TEMP_L	R	20	00100000	output	
OUT_TEMP_H	R	21	00100001	output	
OUTX_L_G	R	22	00100010	output	
OUTX_H_G	R	23	00100011	output	
OUTY_L_G	R	24	00100100	output	
OUTY_H_G	R	25	00100101	output	
OUTZ_L_G	R	26	00100110	output	
OUTZ_H_G	R	27	00100111	output	



Name	Type	Register address		Default	Comment
		Hex	Binary		
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-39			Reserved
FIFO_STATUS1	R	3A	00111010	output	
FIFO_STATUS2	R	3B	00111011	output	
RESERVED	-	3C-3F			
TIMESTAMP0_REG	R	40	01000000	output	
TIMESTAMP1_REG	R	41	01000001	output	
TIMESTAMP2_REG	R	42	01000010	output	
TIMESTAMP3_REG	R	43	01000011	output	
RESERVED	-	44-55			
INT_CFG0	R/W	56	01010110	00000000	
RESERVED	-	57	01010111		Reserved
INT_CFG1	R/W	58	01011000	00000000	
THS_6D	R/W	59	01011001	00000000	
RESERVED	-	5A	01011010		Reserved
WAKE_UP_THS	R/W	5B	01011011	00000000	
WAKE_UP_DUR	R/W	5C	01011100	00000000	
FREE_FALL	R/W	5D	01011101	00000000	
MD1_CFG	R/W	5E	01011110	00000000	
MD2_CFG	R/W	5F	01011111	00000000	
RESERVED	-	60-62		00000000	Reserved
INTERNAL_FREQ_FINE	R	63	01100011	output	
RESERVED	-	64-72		00000000	Reserved
X_OFS_USR	R/W	73	01110011	00000000	
Y_OFS_USR	R/W	74	01110100	00000000	
Z_OFS_USR	R/W	75	01110101	00000000	
RESERVED	-	76-77			Reserved
FIFO_DATA_OUT_TAG	R	78	01111000	output	
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	
RESERVED	-	7F			Reserved



Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

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## 9 Register description

The device contains a set of registers that are used to control its behavior and to retrieve linear acceleration, angular rate, and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data over the serial interface.

### 9.1 PIN\_CTRL (02h)

Enable pull-up on SDO pin (R/W)

**Table 18. PIN\_CTRL register**

0	SDO_PU_EN	1 <sup>(1)</sup>	1 <sup>(1)</sup>	1 <sup>(1)</sup>	1 <sup>(1)</sup>	1 <sup>(1)</sup>	1 <sup>(1)</sup>
---	-----------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 1 for the correct operation of the device.

**Table 19. PIN\_CTRL register description**

SDO_PU_EN	Enables pull-up on SDO pin. Default value: 0 (0: SDO pin pull-up disconnected; 1: SDO pin with pull-up)
-----------	------------------------------------------------------------------------------------------------------------

### 9.2 FIFO\_CTRL1 (07h)

FIFO control register 1 (R/W)

**Table 20. FIFO\_CTRL1 register**

WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0
------	------	------	------	------	------	------	------

**Table 21. FIFO\_CTRL1 register description**

WTM[7:0]	FIFO watermark threshold, in conjunction with WTM8 in <a href="#">FIFO_CTRL2 (08h)</a> 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.
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### 9.3

#### FIFO\_CTRL2 (08h)

FIFO control register 2 (R/W)

**Table 22. FIFO\_CTRL2 register**

STOP_ON_WTM	0 <sup>(1)</sup>	0 <sup>(1)</sup>	ODRCHG_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	WTM8
-------------	------------------	------------------	-----------	------------------	------------------	------------------	------

1. This bit must be set to 0 for the correct operation of the device.

**Table 23. FIFO\_CTRL2 register description**

STOP_ON_WTM	<p>Sensing chain FIFO stop values memorization at threshold level</p> <p>(0: FIFO depth is not limited (default);</p> <p>1: FIFO depth is limited to threshold level, defined in <a href="#">FIFO_CTRL1 (07h)</a> and <a href="#">FIFO_CTRL2 (08h)</a>)</p>
ODRCHG_EN	<p>Enables ODR CHANGE virtual sensor to be batched in FIFO</p>
WTM8	<p>FIFO watermark threshold, in conjunction with WTM[7:0] in <a href="#">FIFO_CTRL1 (07h)</a></p> <p>1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO</p> <p>Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.</p>



## 9.4

### FIFO\_CTRL3 (09h)

FIFO control register 3 (R/W)

**Table 24. FIFO\_CTRL3 register**

BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0
----------	----------	----------	----------	----------	----------	----------	----------

**Table 25. FIFO\_CTRL3 register description**

BDR_GY_[3:0]	<p>Selects batch data rate (write frequency in FIFO) for gyroscope data. (0000: gyroscope not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: 6.5 Hz; 1100-1111: reserved)</p>
BDR_XL_[3:0]	<p>Selects batch data rate (write frequency in FIFO) for accelerometer data. (0000: accelerometer not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011-1111: reserved)</p>



## 9.5

### FIFO\_CTRL4 (0Ah)

FIFO control register 4 (R/W)

**Table 26. FIFO\_CTRL4 register**

DEC_TS_BATCH_1	DEC_TS_BATCH_0	ODR_T_BATCH_1	ODR_T_BATCH_0	0 <sup>(1)</sup>	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0
----------------	----------------	---------------	---------------	------------------	------------	------------	------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 27. FIFO\_CTRL4 register description**

DEC_TS_BATCH[1:0]	<p>Selects decimation for timestamp batching in FIFO. The write rate is the maximum rate between the accelerometer and gyroscope BDR divided by the decimation decoder.</p> <p>(00: timestamp not batched in FIFO (default);</p> <p>01: decimation 1: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])</math> [Hz];</p> <p>10: decimation 8: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/8</math> [Hz];</p> <p>11: decimation 32: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/32</math> [Hz])</p>
ODR_T_BATCH[1:0]	<p>Selects batch data rate (write frequency in FIFO) for temperature data</p> <p>(00: temperature not batched in FIFO (default);</p> <p>01: 1.6 Hz;</p> <p>10: 12.5 Hz;</p> <p>11: 52 Hz)</p>
FIFO_MODE[2:0]	<p>FIFO mode selection</p> <p>(000: bypass mode: FIFO disabled;</p> <p>001: FIFO mode: stops collecting data when FIFO is full;</p> <p>010: reserved;</p> <p>011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode;</p> <p>100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode;</p> <p>101: reserved;</p> <p>110: continuous mode: if the FIFO is full, the new sample overwrites the older one;</p> <p>111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.)</p>



## 9.6 COUNTER\_BDR\_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

**Table 28. COUNTER\_BDR\_REG1 register**

dataready_ pulsed	RST_ COUNTER_BDR	TRIG_ COUNTER_BDR	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	CNT_BDR_ TH_9	CNT_BDR_ TH_8
----------------------	---------------------	----------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 29. COUNTER\_BDR\_REG1 register description**

dataready_pulsed	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after an interface reading) (default); 1: data-ready pulsed mode (the data ready pulses are 75 µs long)
RST_COUNTER_BDR	Resets the internal counter of batch events for a single sensor. This bit is automatically reset to 0 if it was set to 1.
TRIG_COUNTER_BDR	Selects the trigger for the internal counter of batch events between the accelerometer and the gyroscope. (0: accelerometer batch event; 1: gyroscope batch event)
CNT_BDR_TH[9:8]	In conjunction with CNT_BDR_TH[7:0] in <a href="#">COUNTER_BDR_REG2 (0Ch)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to 1.

## 9.7 COUNTER\_BDR\_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

**Table 30. COUNTER\_BDR\_REG2 register**

CNT_BDR_ TH_7	CNT_BDR_ TH_6	CNT_BDR_ TH_5	CNT_BDR_ TH_4	CNT_BDR_ TH_3	CNT_BDR_ TH_2	CNT_BDR_ TH_1	CNT_BDR_ TH_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 31. COUNTER\_BDR\_REG2 register description**

CNT_BDR_TH[7:0]	In conjunction with CNT_BDR_TH[9:8] in <a href="#">COUNTER_BDR_REG1 (0Bh)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to 1.
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## 9.8 INT1\_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The output of the pin is the OR combination of the signals selected here and in register MD1\_CFG (5Eh).

**Table 32. INT1\_CTRL register**

DEN_DRDY_flag	INT1_CNT_BDR	INT1_FIFO_FULL	INT1_FIFO_OVR	INT1_FIFO_TH	INT1_BOOT	INT1_DRDY_G	INT1_DRDY_XL
---------------	--------------	----------------	---------------	--------------	-----------	-------------	--------------

**Table 33. INT1\_CTRL register description**

DEN_DRDY_flag	Sends DEN_DRDY (DEN stamped on sensor data flag) to the INT1 pin
INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on the INT1 pin
INT1_FIFO_FULL	Enables FIFO full flag interrupt on the INT1 pin
INT1_FIFO_OVR	Enables FIFO overrun interrupt on the INT1 pin
INT1_FIFO_TH	Enables FIFO threshold interrupt on the INT1 pin
INT1_BOOT	Enables boot status on the INT1 pin
INT1_DRDY_G	Gyroscope data-ready interrupt on the INT1 pin.
INT1_DRDY_XL	Accelerometer data-ready interrupt on the INT1 pin

## 9.9 INT2\_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The output of the pin is the OR combination of the signals selected here and in register MD2\_CFG (5Fh).

**Table 34. INT2\_CTRL register**

0 <sup>(1)</sup>	INT2_CNT_BDR	INT2_FIFO_FULL	INT2_FIFO_OVR	INT2_FIFO_TH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL
------------------	--------------	----------------	---------------	--------------	----------------	-------------	--------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 35. INT2\_CTRL register description**

INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on the INT2 pin
INT2_FIFO_FULL	Enables FIFO full flag interrupt on the INT2 pin
INT2_FIFO_OVR	Enables FIFO overrun interrupt on the INT2 pin
INT2_FIFO_TH	Enables FIFO threshold interrupt on the INT2 pin
INT2_DRDY_TEMP	Temperature sensor data-ready interrupt on the INT2 pin
INT2_DRDY_G	Gyroscope data-ready interrupt on the INT2 pin
INT2_DRDY_XL	Accelerometer data-ready interrupt on the INT2 pin

## 9.10 WHO\_AM\_I (0Fh)

WHO\_AM\_I register (R). This is a read-only register. Its value is fixed at 6Bh.

**Table 36. WhoAml register**

0	1	1	0	1	0	1	1
---	---	---	---	---	---	---	---



## 9.11

### CTRL1\_XL (10h)

Accelerometer control register 1 (R/W)

**Table 37. CTRL1\_XL register**

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	LPF2_XL_EN	0
---------	---------	---------	---------	--------	--------	------------	---

1. This bit must be set to 0 for the correct operation of the device.

**Table 38. CTRL1\_XL register description**

ODR_XL[3:0]	<p>Accelerometer ODR selection (0000: power-down (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: reserved; 11xx: reserved)</p>
FS[1:0]_XL	<p>Accelerometer full-scale selection (00: <math>\pm 2</math> g (default); 01: <math>\pm 16</math> g; 10: <math>\pm 4</math> g; 11: <math>\pm 8</math> g)</p>
LPF2_XL_EN	<p>Accelerometer high-resolution selection: (0: output from first stage digital stage filtering selected (default); 1: output from LPF2 second filtering stage selected)</p>



## 9.12

### CTRL2\_G (11h)

Gyroscope control register 2 (R/W)

**Table 39. CTRL2\_G register**

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	0 <sup>(1)</sup>
--------	--------	--------	--------	-------	-------	--------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 40. CTRL2\_G register description**

ODR_G[3:0]	Gyroscope ODR selection (0000: power-down; 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: reserved; 11xx: reserved)
FS[1:0]_G	Gyroscope chain full-scale selection (00: $\pm 250$ dps; 01: $\pm 500$ dps; 10: $\pm 1000$ dps; 11: $\pm 2000$ dps)
FS_125	Selects gyroscope chain full-scale $\pm 125$ dps (0: FS selected through bits FS[1:0]_G; 1: FS set to $\pm 125$ dps)



### 9.13 CTRL3\_C (12h)

Control register 3 (R/W)

**Table 41. CTRL3\_C register**

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0 <sup>(1)</sup>	SW_RESET
------	-----	-----------	-------	-----	--------	------------------	----------

1. This bit must be set to 0 for the correct operation of the device.

**Table 42. CTRL3\_C register description**

BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) Note: The accelerometer must be ON. This bit is automatically cleared.
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to 0 when H_LACTIVE is set to 1. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.



## 9.14

### CTRL4\_C (13h)

Control register 4 (R/W)

**Table 43. CTRL4\_C register**

0 <sup>(1)</sup>	SLEEP_G	INT2_on_INT1	0 <sup>(1)</sup>	DRDY_MASK	I2C_disable	LPF1_SEL_G	0 <sup>(1)</sup>
------------------	---------	--------------	------------------	-----------	-------------	------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 44. CTRL4\_C register description**

SLEEP_G	Enables gyroscope sleep mode. Default value: 0 (0: disabled; 1: enabled)
INT2_on_INT1	All interrupt signals available on INT1 pin enable. Default value: 0 (0: interrupt signals divided between INT1 and INT2 pins; 1: all interrupt signals in logic or on INT1 pin)
DRDY_MASK	Enables data available (0: disabled; 1: mask DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked).
I2C_disable	Disables I <sup>2</sup> C interface. Default value: 0 (0: SPI and I <sup>2</sup> C interfaces enabled (default); 1: I <sup>2</sup> C interface disabled)
LPF1_SEL_G	Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE[2:0] in CTRL6_C (15h). (0: disabled; 1: enabled)


**9.15**
**CTRL5\_C (14h)**

Control register 5 (R/W)

**Table 45. CTRL5\_C register**

0 <sup>(1)</sup>	ROUNDING1	ROUNDING0	0 <sup>(1)</sup>	ST1_G	ST0_G	ST1_XL	ST0_XL
------------------	-----------	-----------	------------------	-------	-------	--------	--------

1. This bit must be set to 0 for the correct operation of the device.

**Table 46. CTRL5\_C register description**

ROUNDING[1:0]	Circular burst mode (wraparound) read of the output registers. Default value: 00 (00: no wraparound; 01: accelerometer only; 10: gyroscope only; 11: gyroscope + accelerometer)
ST[1:0]_G	Enables angular rate sensor self-test. Default value: 00 (00: self-test disabled; Other: refer to <a href="#">Table 47</a> )
ST[1:0]_XL	Enables linear acceleration sensor self-test. Default value: 00 (00: self-test disabled; Other: refer to <a href="#">Table 48</a> )

**Table 47. Angular rate sensor self-test mode selection**

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Reserved
1	1	Negative sign self-test

**Table 48. Linear acceleration sensor self-test mode selection**

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Reserved


**9.16**
**CTRL6\_C (15h)**

Control register 6 (R/W)

**Table 49. CTRL6\_C register**

TRIG_EN	LVL1_EN	LVL2_EN	0 <sup>(1)</sup>	USR_OFF_W	FTYPE_2	FTYPE_1	FTYPE_0
---------	---------	---------	------------------	-----------	---------	---------	---------

1. This bit must be set to 0 for the correct operation of the device.

**Table 50. CTRL6\_C register description**

TRIG_EN	Enables DEN data edge-sensitive trigger. Refer to Table 51.
LVL1_EN	Enables DEN data level-sensitive trigger. Refer to Table 51.
LVL2_EN	Enables DEN level-sensitive latched. Refer to Table 51.
USR_OFF_W	Weight of accelerometer user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), and Z_OFS_USR (75h) (0 = 2 <sup>-10</sup> g/LSB; 1 = 2 <sup>-6</sup> g/LSB)
FTYPE[2:0]	Gyroscope low-pass filter (LPF1) bandwidth selection. Table 52 shows the selectable bandwidth values.

**Table 51. Trigger mode selection**

TRIG_EN, LVL1_EN, LVL2_EN	Trigger mode
100	Edge-sensitive trigger mode is selected.
010	Level-sensitive trigger mode is selected.
011	Level-sensitive latched mode is selected.
110	Level-sensitive FIFO enable mode is selected.

**Table 52. Gyroscope LPF1 bandwidth selection**

FTYPE[2:0]	12.5 Hz	26 Hz	52 Hz	104 Hz	208 Hz	416 Hz	833 Hz	1.67 kHz	3.33 kHz	6.67 kHz
000	4.3	8.3	16.7	33	67	133	222	274	292	297
001	4.3	8.3	16.7	33	67	128	186	212	220	223
010	4.3	8.3	16.7	33	67	112	140	150	153	154
011	4.3	8.3	16.7	33	67	134	260	390	451	470
100	4.3	8.3	16.7	34	62	86	96	99	NA	
101	4.3	8.3	16.9	31	43	48	49	50	NA	
110	4.3	8.3	13.4	19	23	24.6	25	25	NA	
111	4.3	8.3	9.8	11.6	12.2	12.4	12.6	12.6	NA	



## 9.17 CTRL7\_G (16h)

Control register 7 (R/W)

**Table 53. CTRL7\_G register**

0 <sup>(1)</sup>	HP_EN_G	HPM1_G	HPM0_G	0 <sup>(1)</sup>	0 <sup>(1)</sup>	USR_OFF_ON_OUT	0 <sup>(1)</sup>
------------------	---------	--------	--------	------------------	------------------	----------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 54. CTRL7\_G register description**

HP_EN_G	Enables gyroscope digital high-pass filter. The filter is enabled only if the gyroscope is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HPM_G[1:0]	Gyroscope digital HP filter cutoff selection. Default: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11: 1.04 Hz)
USR_OFF_ON_OUT	Enables accelerometer user offset correction block; it is valid for the low-pass path - see Figure 13. Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

## 9.18 CTRL8\_XL (17h)

Control register 8 (R/W)

**Table 55. CTRL8\_XL register**

HPCF_XL_2	HPCF_XL_1	HPCF_XL_0	HP_REF_MODE_XL	FASTSETTL_MODE_XL	HP_SLOPE_XL_EN	0 <sup>(1)</sup>	LOW_PASS_ON_6D
-----------	-----------	-----------	----------------	-------------------	----------------	------------------	----------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 56. CTRL8\_XL register description**

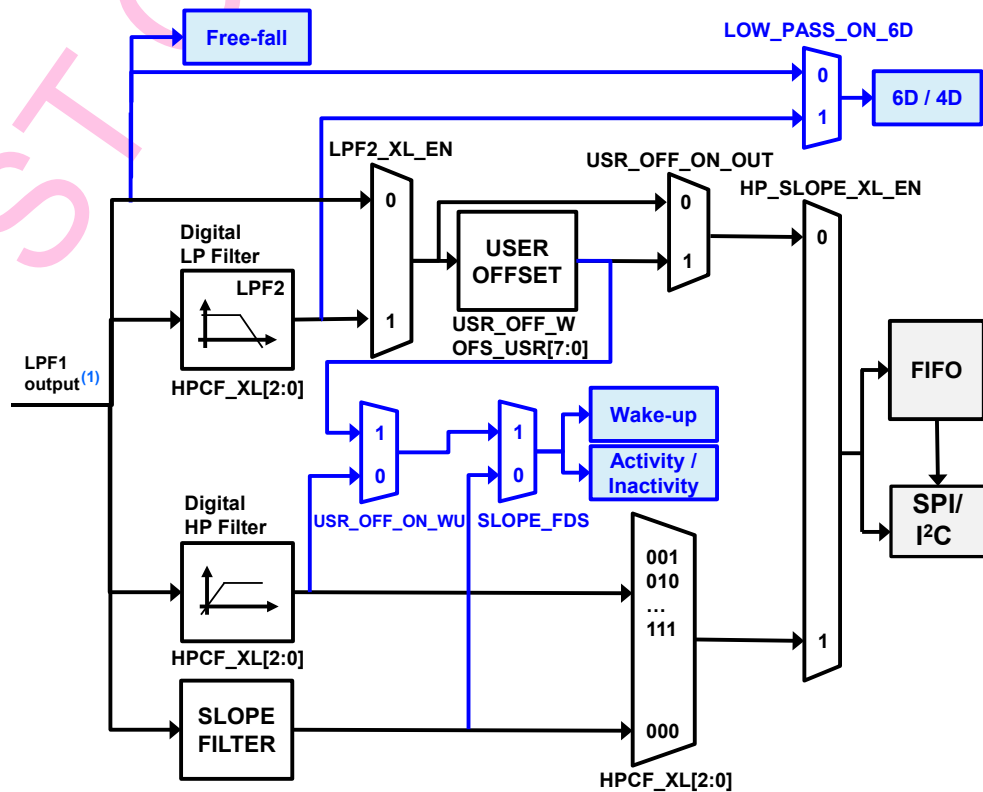
HPCF_XL[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 57.
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0 <sup>(1)</sup> (0: disabled, 1: enabled)
FASTSETTL_MODE_XL	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power-down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to Figure 15.
LOW_PASS_ON_6D	LPF2 on 6D function selection. Refer to Figure 15. Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)

1. When enabled, the first output data have to be discarded.




**Table 57. Accelerometer bandwidth configurations**

Filter type	HP_SLOPE_XL_EN	LPF2_XL_EN	HPCF_XL_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	-	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

**Figure 15. Accelerometer block diagram**


1. The cutoff value of the LPF1 output is ODR/2.



## 9.19 CTRL9\_XL (18h)

Control register 9 (R/W)

**Table 58. CTRL9\_XL register**

DEN_X	DEN_Y	DEN_Z	DEN_XL_G	DEN_XL_EN	DEN_LH	DEVICE_CONF	0 <sup>(1)</sup>
-------	-------	-------	----------	-----------	--------	-------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 59. CTRL9\_XL register description**

DEN_X	DEN value stored in LSB of X-axis. Default value: 1 (0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB)
DEN_Y	DEN value stored in LSB of Y-axis. Default value: 1 (0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB)
DEN_Z	DEN value stored in LSB of Z-axis. Default value: 1 (0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB)
DEN_XL_G	DEN stamping sensor selection. Default value: 0 (0: DEN pin info stamped in the gyroscope axis selected by bits [7:5]; 1: DEN pin info stamped in the accelerometer axis selected by bits [7:5])
DEN_XL_EN	Extends DEN functionality to accelerometer sensor. Default value: 0 (0: disabled; 1: enabled)
DEN_LH	DEN active level configuration. Default value: 0 (0: active low; 1: active high)
DEVICE_CONF	Enables the proper device configuration. Default value: 0 It is recommended to always set this bit to 1 during device configuration. (0: default; 1: enabled)

## 9.20 CTRL10\_C (19h)

Control register 10 (R/W)

**Table 60. CTRL10\_C register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	TIMESTAMP_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
------------------	------------------	--------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 61. CTRL10\_C register description**

TIMESTAMP_EN	Enables timestamp counter. Default value: 0 (0: disabled; 1: enabled)  The counter is readable in <a href="#">TIMESTAMP0 (40h)</a> , <a href="#">TIMESTAMP1 (41h)</a> , <a href="#">TIMESTAMP2 (42h)</a> , and <a href="#">TIMESTAMP3 (43h)</a> .
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## 9.21 ALL\_INT\_SRC (1Ah)

Source register for all interrupts (R)

**Table 62. ALL\_INT\_SRC register**

TIMESTAMP_ENDCOUNT	0	SLEEP_CHANGE_IA	D6D_IA	0	0	WU_IA	FF_IA
--------------------	---	-----------------	--------	---	---	-------	-------

**Table 63. ALL\_INT\_SRC register description**

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

## 9.22 WAKE\_UP\_SRC (1Bh)

Wake-up interrupt source register (R)

**Table 64. WAKE\_UP\_SRC register**

0	SLEEP_CHANGE_IA	FF_IA	SLEEP_STATE	WU_IA	X_WU	Y_WU	Z_WU
---	-----------------	-------	-------------	-------	------	------	------

**Table 65. WAKE\_UP\_SRC register description**

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep status bit. Default value: 0 (0: activity status; 1: inactivity status)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)



## 9.23

### D6D\_SRC (1Dh)

Portrait, landscape, face-up, and face-down source register (R)

**Table 66. D6D\_SRC register**

DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL
----------	--------	----	----	----	----	----	----

**Table 67. D6D\_SRC register description**

DEN_DRDY	DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. <sup>(1)</sup>
D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

1. The DEN data-ready signal can be latched or pulsed depending on the value of the `dataready_pulsed` bit of the `COUNTER_BDR_REG1 (0Bh)` register.



## 9.24 STATUS\_REG (1Eh)

Status register (R)

**Table 68. STATUS\_REG register**

0	0	0	0	0	TDA	GDA	XLDA
---	---	---	---	---	-----	-----	------

**Table 69. STATUS\_REG register description**

TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

## 9.25 OUT\_TEMP\_L (20h), OUT\_TEMP\_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

**Table 70. OUT\_TEMP\_L register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 71. OUT\_TEMP\_H register**

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 72. OUT\_TEMP register description**

Temp[15:0]	Temperature sensor output data The value is expressed as two's complement sign extended on the MSB.
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## 9.26 OUTX\_H\_G (23h), OUTX\_L\_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 73. OUTX\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 74. OUTX\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 75. OUTX\_H\_G, OUTX\_L\_G register description**

D[15:0]	Gyroscope pitch axis output expressed in two's complement
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## 9.27 OUTY\_H\_G (25h), OUTY\_L\_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 76. OUTY\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 77. OUTY\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 78. OUTY\_H\_G, OUTY\_L\_G register description**

D[15:0]	Gyroscope roll axis output expressed in two's complement
---------	----------------------------------------------------------

## 9.28 OUTZ\_H\_G (27h), OUTZ\_L\_G (26h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 79. OUTZ\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 80. OUTZ\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 81. OUTZ\_H\_G, OUTZ\_L\_G register description**

D[15:0]	Gyroscope yaw axis output expressed in two's complement
---------	---------------------------------------------------------



### 9.29 OUTX\_H\_A (29h), OUTX\_L\_A (28h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 82. OUTX\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 83. OUTX\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 84. OUTX\_H\_A, OUTX\_L\_A register description**

D[15:0]	Accelerometer X-axis output expressed as two's complement
---------	-----------------------------------------------------------

### 9.30 OUTY\_H\_A (2Bh), OUTY\_L\_A (2Ah)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 85. OUTY\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 86. OUTY\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 87. OUTY\_H\_A, OUTY\_L\_A register description**

D[15:0]	Accelerometer Y-axis output expressed as two's complement
---------	-----------------------------------------------------------

### 9.31 OUTZ\_H\_A (2Dh), OUTZ\_L\_A (2Ch)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 88. OUTZ\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 89. OUTZ\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 90. OUTZ\_H\_A, OUTZ\_L\_A register description**

D[15:0]	Accelerometer Z-axis output expressed as two's complement
---------	-----------------------------------------------------------



### 9.32 FIFO\_STATUS1 (3Ah)

FIFO status register 1 (R)

**Table 91. FIFO\_STATUS1 register**

DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 92. FIFO\_STATUS1 register description**

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO (in conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh)).
-----------------	-------------------------------------------------------------------------------------------------------------------------

### 9.33 FIFO\_STATUS2 (3Bh)

FIFO status register 2 (R)

**Table 93. FIFO\_STATUS2 register**

FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	COUNTER_BDR_IA	FIFO_OVR_LATCHED	0	DIFF_FIFO_9	DIFF_FIFO_8
-------------	-------------	--------------	----------------	------------------	---	-------------	-------------

**Table 94. FIFO\_STATUS2 register description**

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[8:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[9:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_[9:8]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO (in conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah)). Default value: 00





## 9.34

**TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)**

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 25 µs.

**Table 95. TIMESTAMP3 register**

D31	D30	D29	D28	D27	D26	D25	D24
-----	-----	-----	-----	-----	-----	-----	-----

**Table 96. TIMESTAMP2 register**

D23	D22	D21	D20	D19	D18	D17	D16
-----	-----	-----	-----	-----	-----	-----	-----

**Table 97. TIMESTAMP1 register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 98. TIMESTAMP0 register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D[31:0]	Timestamp output registers: 1LSB = 25 µs
---------	------------------------------------------

The formula below can be used to calculate a better estimation of the actual timestamp resolution:

$$TS\_Res = 1 / (40000 + (0.0015 * INTERNAL\_FREQ\_FINE * 40000))$$

where INTERNAL\_FREQ\_FINE is the content of [INTERNAL\\_FREQ\\_FINE \(63h\)](#).



### 9.35 INT\_CFG0 (56h)

Activity/inactivity functions, configuration of filtering, and interrupt latch mode configuration (R/W)

**Table 99. INT\_CFG0 register**

0 <sup>(1)</sup>	INT_CLR_ON_READ	SLEEP_STATUS_ON_INT	SLOPE_FDS	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	LIR
------------------	-----------------	---------------------	-----------	------------------	------------------	------------------	-----

1. This bit must be set to 0 for the correct operation of the device.

**Table 100. INT\_CFG0 register description**

INT_CLR_ON_READ	This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0 (0: latched interrupt signal cleared at the end of the ODR period; 1: latched interrupt signal immediately cleared)
SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If the INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on the INT pins. Default value: 0 (0: sleep change notification on the INT pins; 1: sleep status reported on the INT pins)
SLOPE_FDS	HPF or SLOPE filter selection on wake-up and activity/inactivity functions. Default value: 0 (0: SLOPE filter applied; 1: HPF applied)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

### 9.36 INT\_CFG1 (58h)

Enables interrupt function register (R/W)

**Table 101. INT\_CFG1 register**

INTERRUPTS_ENABLE	INACT_EN1	INACT_EN0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------------	-----------	-----------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 102. INT\_CFG1 register description**

INTERRUPTS_ENABLE	Enables hardcoded functions
INACT_EN[1:0]	Enables activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, accelerometer and gyroscope do not change; 01: sets accelerometer ODR to 12.5 Hz, gyroscope does not change; 10: sets accelerometer ODR to 12.5 Hz, gyroscope to sleep mode; 11: sets accelerometer ODR to 12.5 Hz, gyroscope to power-down mode)



### 9.37

## THS\_6D (59h)

Portrait/landscape position register (R/W)

**Table 103. THS\_6D register**

D4D_EN	SIXD_THS1	SIXD_THS0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
--------	-----------	-----------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 104. THS\_6D register description**

D4D_EN	Enables detection of 4D orientation. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
SIXD_THS[1:0]	Threshold for 4D/6D function (00: 80 degrees (default); 01: 70 degrees; 10: 60 degrees; 11: 50 degrees)

### 9.38

## WAKE\_UP\_THS (5Bh)

Wake-up configuration register (R/W)

**Table 105. WAKE\_UP\_THS register**

0 <sup>(1)</sup>	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0
------------------	---------------	---------	---------	---------	---------	---------	---------

1. This bit must be set to 0 for the correct operation of the device.

**Table 106. WAKE\_UP\_THS register description**

USR_OFF_ON_WU	Sends the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up function.
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000



### 9.39 WAKE\_UP\_DUR (5Ch)

Free-fall, wake-up and sleep mode functions duration setting register (R/W)

**Table 107. WAKE\_UP\_DUR register**

FF_DUR5	WAKE_DUR1	WAKE_DUR0	WAKE_THS_W	SLEEP_DUR3	SLEEP_DUR2	SLEEP_DUR1	SLEEP_DUR0
---------	-----------	-----------	------------	------------	------------	------------	------------

**Table 108. WAKE\_UP\_DUR register description**

FF_DUR5	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in <a href="#">FREE_FALL (5Dh)</a> configuration. 1 LSB = 1 ODR_time
WAKE_DUR[1:0]	Wake-up duration event. Default: 00 1LSB = 1 ODR_time
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default:0 (0: 1 LSB =FS_XL / (2 <sup>6</sup> ); 1: 1 LSB = FS_XL / (2 <sup>8</sup> ))
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

### 9.40 FREE\_FALL (5Dh)

Free-fall function duration setting register (R/W)

**Table 109. FREE\_FALL register**

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0
---------	---------	---------	---------	---------	---------	---------	---------

**Table 110. FREE\_FALL register description**

FF_DUR[4:0]	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR5 in <a href="#">WAKE_UP_DUR (5Ch)</a> configuration
FF_THS[2:0]	Free-fall threshold setting (000: 156 mg (default); 001: 219 mg; 010: 250 mg; 011: 312 mg; 100: 344 mg; 101: 406 mg; 110: 469 mg; 111: 500 mg)



## 9.41

### MD1\_CFG (5Eh)

Routing functions to INT1 (R/W)

**Table 111. MD1\_CFG register**

INT1_SLEEP_CHANGE	0 <sup>(1)</sup>	INT1_WU	INT1_FF	0 <sup>(1)</sup>	INT1_6D	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------------	------------------	---------	---------	------------------	---------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 112. MD1\_CFG register description**

INT1_SLEEP_CHANGE <sup>(1)</sup>	Routes activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_WU	Routes wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)
INT1_FF	Routes free-fall event to INT1. Default value: 0 (0: routing free-fall event to INT1 disabled; 1: routing free-fall event to INT1 enabled)
INT1_6D	Routes 6D event to INT1. Default value: 0 (0: routing 6D event to INT1 disabled; 1: routing 6D event to INT1 enabled)

1. Activity/inactivity interrupt mode (sleep change or sleep status) depends on SLEEP\_STATUS\_ON\_INT bit in the INT\_CFG0 (56h) register.



## 9.42

### MD2\_CFG (5Fh)

Routing functions to INT2 (R/W)

**Table 113. MD2\_CFG register**

INT2_ _CHANGE	0 <sup>(1)</sup>	INT2_WU	INT2_FF	0 <sup>(1)</sup>	INT2_6D	0 <sup>(1)</sup>	INT2_ TIMESTAMP
------------------	------------------	---------	---------	------------------	---------	------------------	--------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 114. MD2\_CFG register description**

INT2_SLEEP_CHANGE	Routes activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_WU	Routes wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_FF	Routes free-fall event to INT2. Default value: 0 (0: routing free-fall event on INT2 disabled; 1: routing free-fall event on INT2 enabled)
INT2_6D	Routes 6D event to INT2. Default value: 0 (0: routing 6D event to INT2 disabled; 1: routing 6D event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin

1. Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP\_STATUS\_ON\_INT bit in the INT\_CFG0 (56h) register.



## 9.43 INTERNAL\_FREQ\_FINE (63h)

Internal frequency register (R)

**Table 115. INTERNAL\_FREQ\_FINE register**

FREQ_FINE7	FREQ_FINE6	FREQ_FINE5	FREQ_FINE4	FREQ_FINE3	FREQ_FINE2	FREQ_FINE1	FREQ_FINE0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 116. INTERNAL\_FREQ\_FINE register description**

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement.
----------------	----------------------------------------------------------------------------------------------------------------------------------------------

The formula below can be used to calculate a better estimation of the actual ODR:

$$\text{ODR\_Actual} = (6667 + ((0.0015 * \text{INTERNAL\_FREQ\_FINE}) * 6667)) / \text{ODR\_Coeff}$$

Selected_ODR	ODR_Coeff
12.5	512
26	256
52	128
104	64
208	32
416	16
833	8
1667	4
3333	2
6667	1

The Selected\_ODR parameter has to be derived from the ODR\_XL selection ([Table 38. CTRL1\\_XL register description](#)) in order to estimate the accelerometer ODR and from the ODR\_G selection ([Table 40. CTRL2\\_G register description](#)) in order to estimate the gyroscope ODR.



#### 9.44 X\_OFS\_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the X-axis

**Table 117. X\_OFS\_USR register**

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 118. X\_OFS\_USR register description**

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127].
-----------------	---------------------------------------------------------------------------------------------------------------------------------------------------------------------

#### 9.45 Y\_OFS\_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

**Table 119. Y\_OFS\_USR register**

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 120. Y\_OFS\_USR register description**

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].
-----------------	------------------------------------------------------------------------------------------------------------------------------------------------------------------------

#### 9.46 Z\_OFS\_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

**Table 121. Z\_OFS\_USR register**

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 122. Z\_OFS\_USR register description**

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].
-----------------	------------------------------------------------------------------------------------------------------------------------------------------------------------------------





## 9.47 FIFO\_DATA\_OUT\_TAG (78h)

FIFO tag register (R)

**Table 123. FIFO\_DATA\_OUT\_TAG register**

TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY
--------------	--------------	--------------	--------------	--------------	-----------	-----------	------------

**Table 124. FIFO\_DATA\_OUT\_TAG register description**

TAG_SENSOR_[4:0]	Identifies the sensor in: FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h), FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh), and FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh)
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot
TAG_PARITY	Parity check of TAG content

**Table 125. FIFO tag**

TAG_SENSOR_[4:0]	Sensor name
0x01	Gyroscope
0x02	Accelerometer
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change



## 9.48 FIFO\_DATA\_OUT\_X\_H (7Ah) and FIFO\_DATA\_OUT\_X\_L (79h)

FIFO data output X (R)

**Table 126.** FIFO\_DATA\_OUT\_X\_H register

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 127.** FIFO\_DATA\_OUT\_X\_L register

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 128.** FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_X\_L register description

D[15:0]	FIFO X-axis output
---------	--------------------

## 9.49 FIFO\_DATA\_OUT\_Y\_H (7Ch) and FIFO\_DATA\_OUT\_Y\_L (7Bh)

FIFO data output Y (R)

**Table 129.** FIFO\_DATA\_OUT\_Y\_H register

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 130.** FIFO\_DATA\_OUT\_Y\_L register

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 131.** FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Y\_L register description

D[15:0]	FIFO Y-axis output
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## 9.50 FIFO\_DATA\_OUT\_Z\_H (7Eh) and FIFO\_DATA\_OUT\_Z\_L (7Dh)

FIFO data output Z (R)

**Table 132.** FIFO\_DATA\_OUT\_Z\_H register

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 133.** FIFO\_DATA\_OUT\_Z\_L register

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 134.** FIFO\_DATA\_OUT\_Z\_H, FIFO\_DATA\_OUT\_Z\_L register description

D[15:0]	FIFO Z-axis output
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## 10 Soldering information

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The LGA package is compliant with the [ECOPACK](#) and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note [TN0018](#) available on [www.st.com](http://www.st.com).

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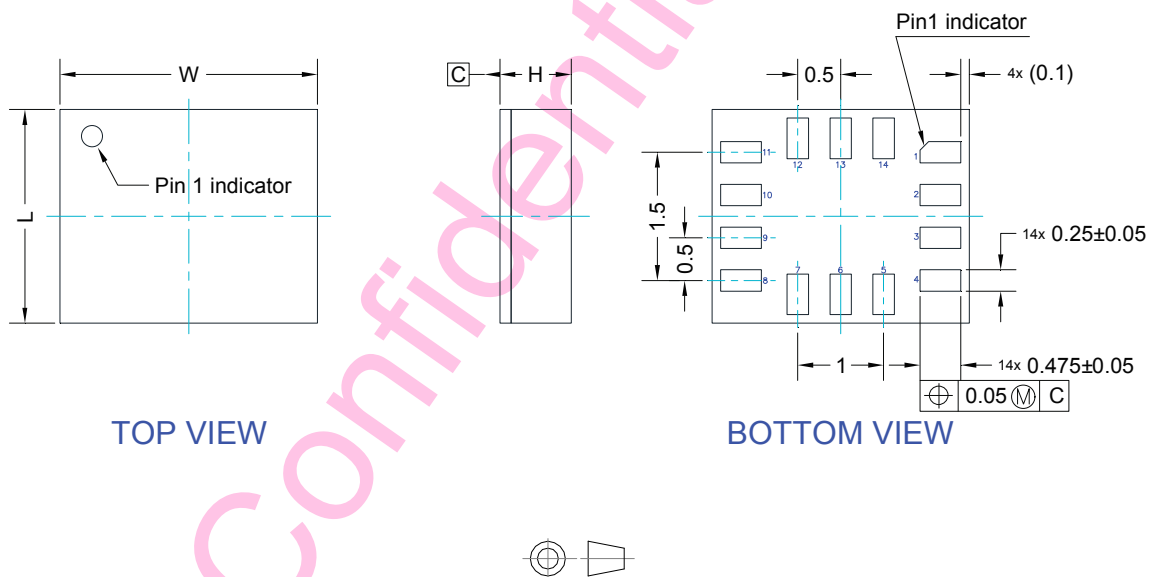


## 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 11.1 LGA-14L package information

**Figure 16. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data**



Dimensions are in millimeter unless otherwise specified  
 General tolerance is +/- 0.1 mm unless otherwise specified

#### OUTER DIMENSIONS

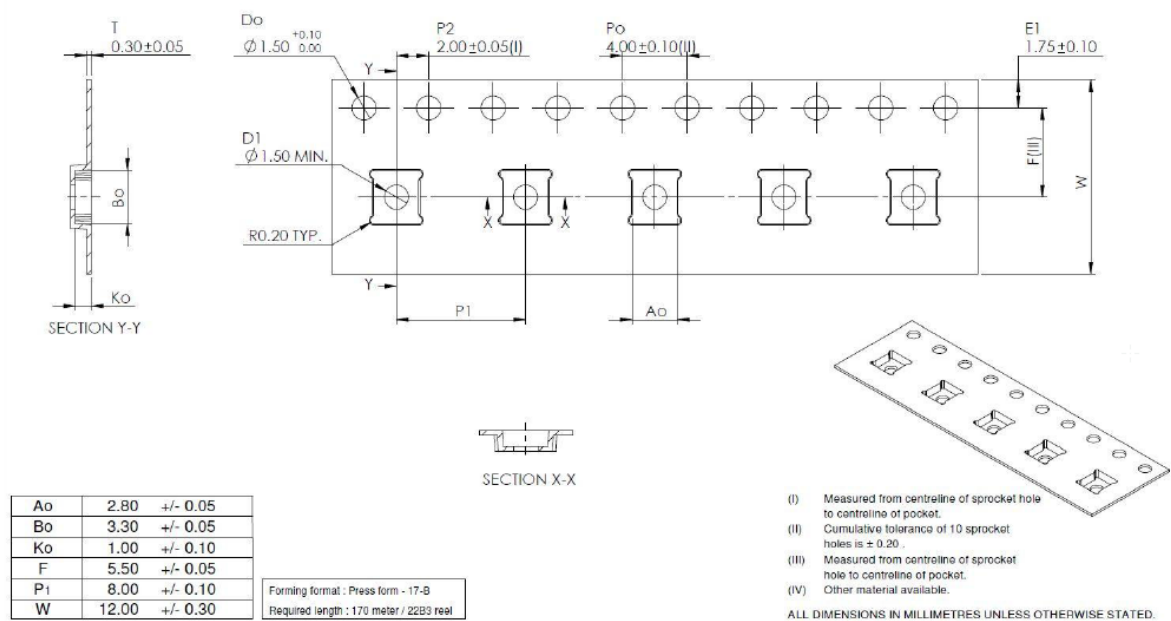
ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496\_5

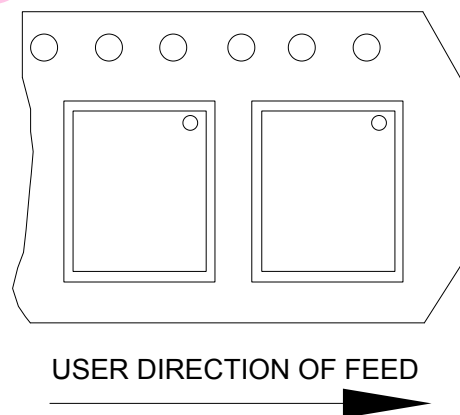


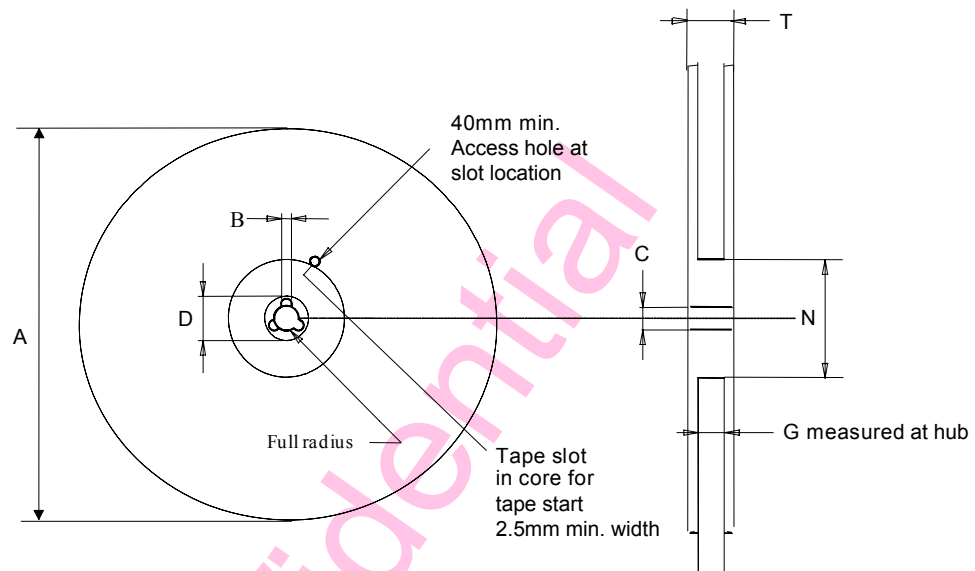
## 11.2 LGA-14 packing information

**Figure 17. Carrier tape information for LGA-14 package**



**Figure 18. LGA-14 package orientation in carrier tape**




**Figure 19. Reel information for carrier tape of LGA-14 package**

**Table 135. Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4



## Revision history

Table 136. Document revision history

Date	Version	Changes
20-Sep-2023	1	Initial release



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