

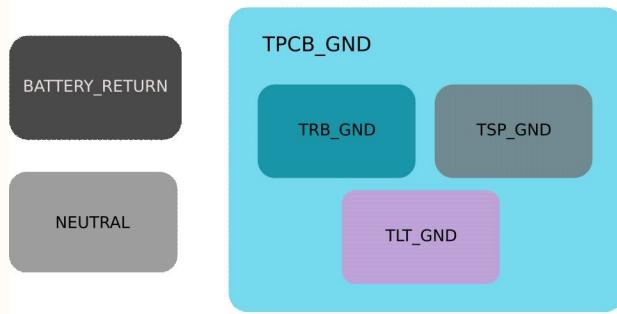
# TOF Read Out Board

- |   |  |                                  |
|---|--|----------------------------------|
| A | Sheet 0: Cover Sheet                     | Sheet 21: Analog Front End       |
| B | Sheet 1: TOF Ground Scheme               | Sheet 22: DRS4 Channel 9         |
| C | Sheet 2: UCLA Readout Top                | Sheet 23: FTDI UART              |
| D | Sheet 3: 4V Distribution                 | Sheet 24: Sensors                |
|   | Sheet 4: 3V3 FPGA Distribution           | Sheet 25: MarsZX2 SD Card        |
|   | Sheet 5: 3V3 Distribution                | Sheet 26: TCA Top Module         |
|   | Sheet 6: 2V5 DRS4 Distribution           | Sheet 27: TCA CLK                |
|   | Sheet 7: 3V/2V5 ADC Distribution         | Sheet 28: TCA LP Filter          |
|   | Sheet 8: 1V8 Supply                      | Sheet 29: MarsZX2 LVDS GPIO      |
|   | Sheet 9: -1V Distribution                | Sheet 30: Analog Calibration DAC |
|   | Sheet 10: Clock Synthesizer Distribution | Sheet 31: Galvanic I2C Interface |
|   | Sheet 11: Mars SOM Power                 | Sheet 32: I2C Multiplexer        |
|   | Sheet 12: MarsZX2 Carrier                | Sheet 33: Mars Power On Reset    |
|   | Sheet 13: Clock Synthesizer              |                                  |
|   | Sheet 14: Ethernet                       |                                  |
|   | Sheet 15: GPIO External Top Module       |                                  |
|   | Sheet 16: GPIO LED                       |                                  |
|   | Sheet 17: GPIO Expander                  |                                  |
|   | Sheet 18: DRS4 Top Module                |                                  |
|   | Sheet 19: DRS4                           |                                  |
|   | Sheet 20: DRS4 ADC                       |                                  |

Title <b>Cover</b>			GAPS TOF 475 Portola Plaza Los Angeles, CA 310-825-0344
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	igarcia91@g.ucla.edu		
	andrew.peck@cern.ch		
	spq@ucla.edu		

# Time Of Flight Ground Scheme

Euler diagram for grounds

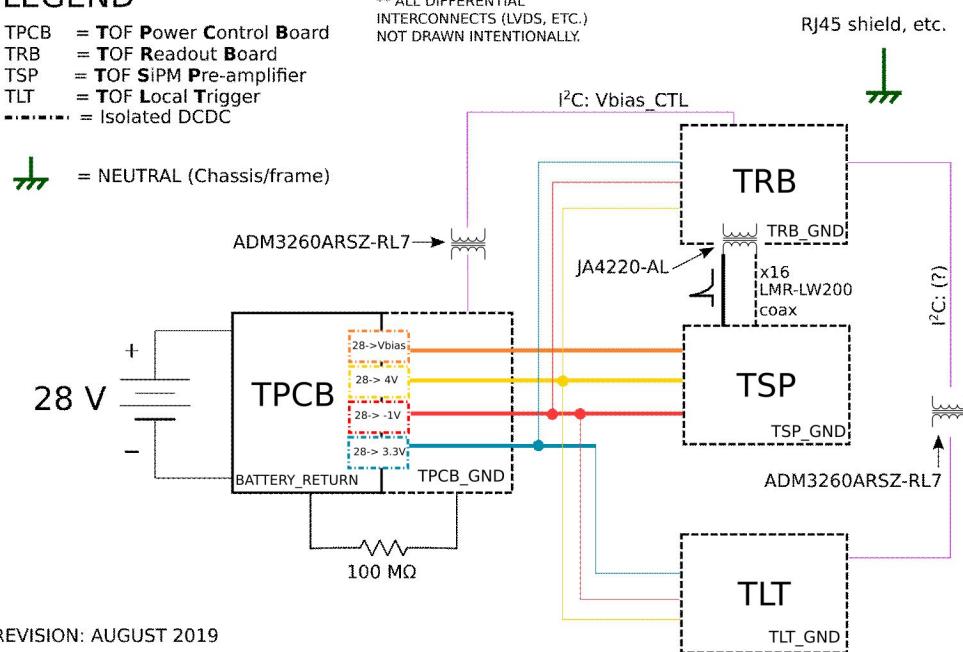


Since TRB, TSP and TLT are contained in TPCB ground, they are all common. Different labels are used for more clarity in the schematics.

## LEGEND

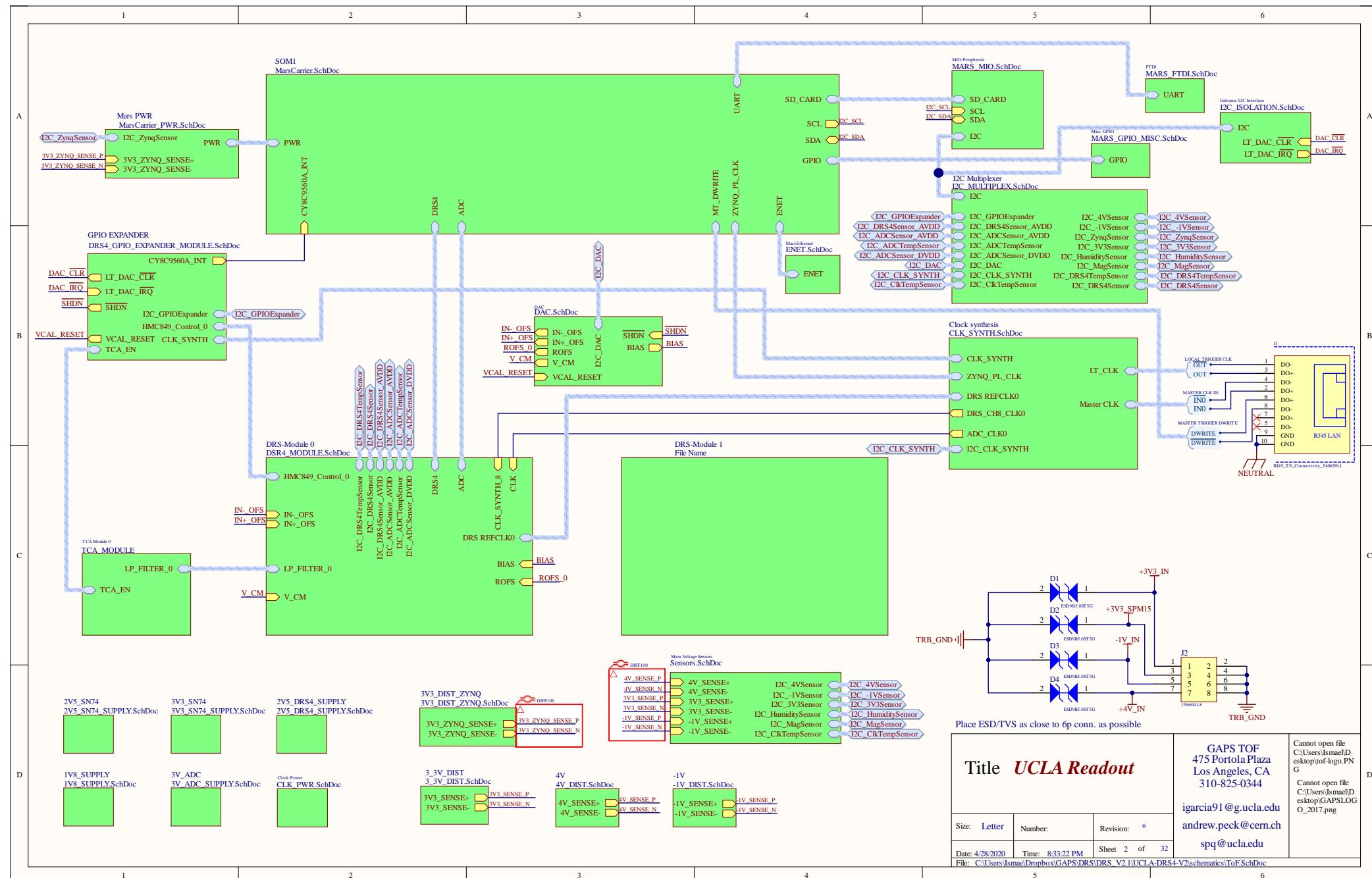
**TPCB** = TOF Power Control Board  
**TRB** = TOF Readout Board  
**TSP** = TOF SiPM Pre-amplifier  
**TLT** = TOF Local Trigger  
 ----- = Isolated DCDC

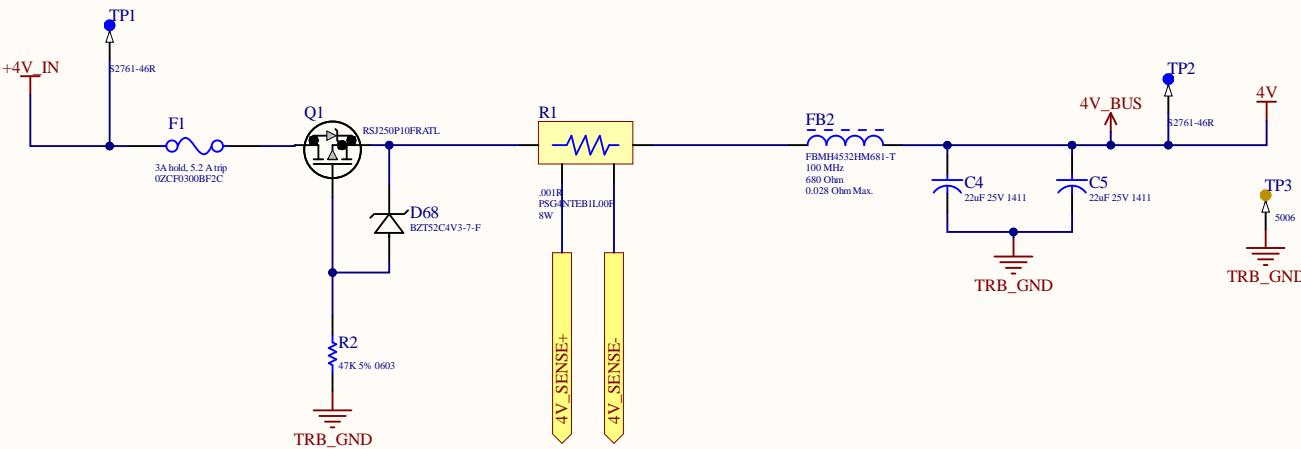
\*\* ALL DIFFERENTIAL  
INTERCONNECTS (LVDS, ETC.)  
NOT DRAWN INTENTIONALLY.



REVISION: AUGUST 2019

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## Title *4V Distribution*

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A

A

B

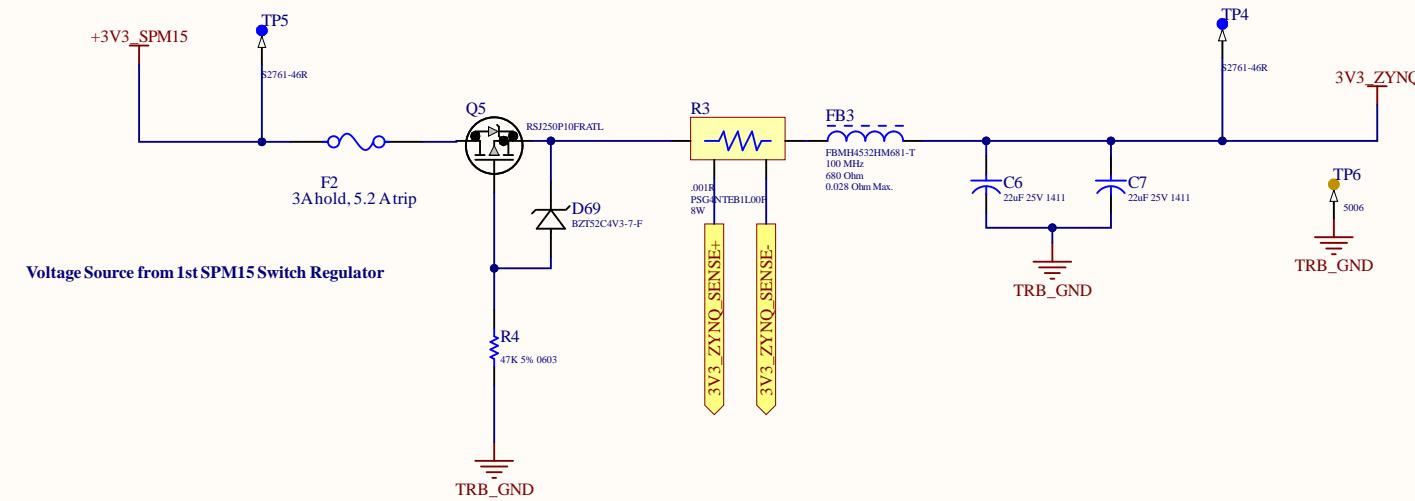
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C

C

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D



## Title **3V3 FPGA**

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A

A

B

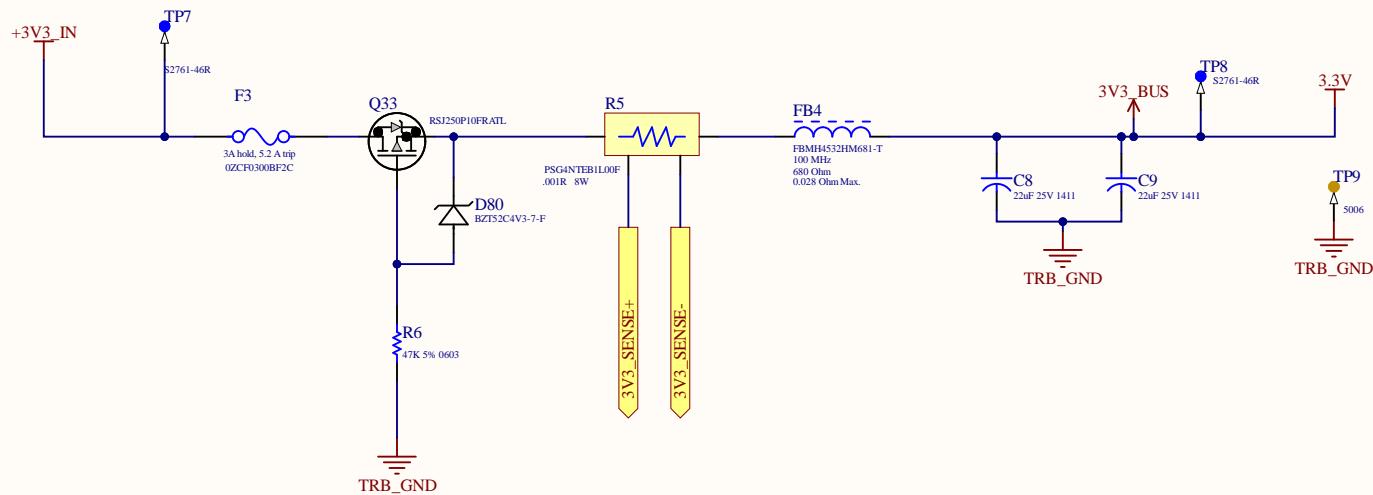
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C

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D

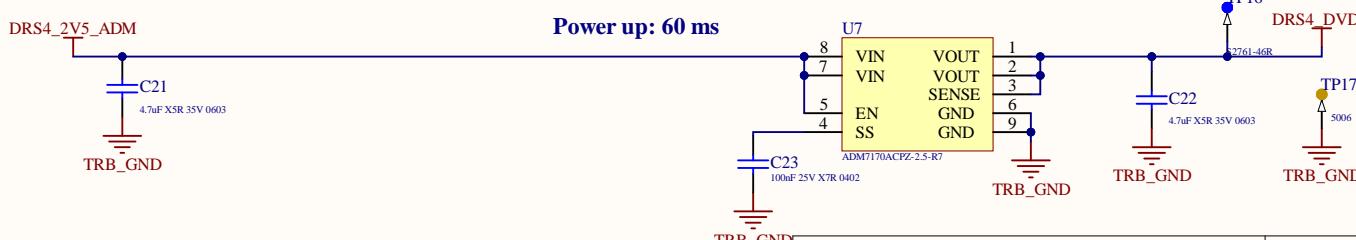
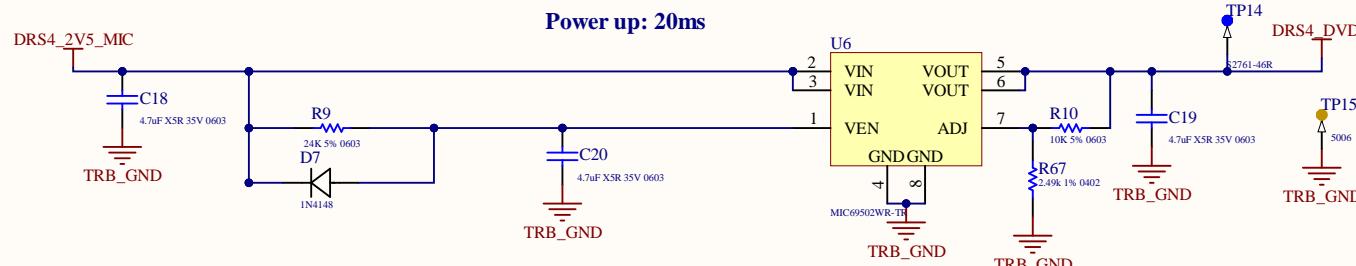
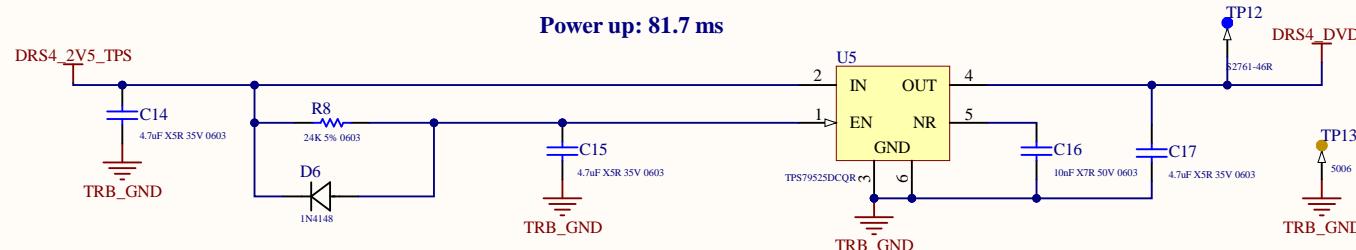
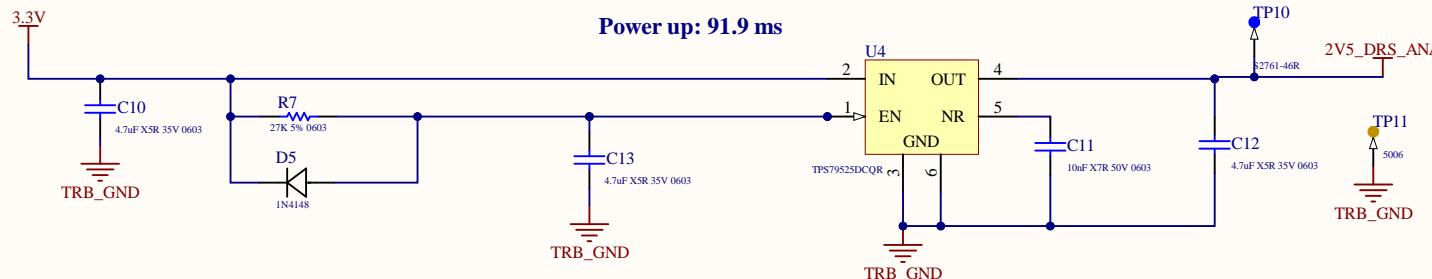


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## Title 2.5V DRS4 supply

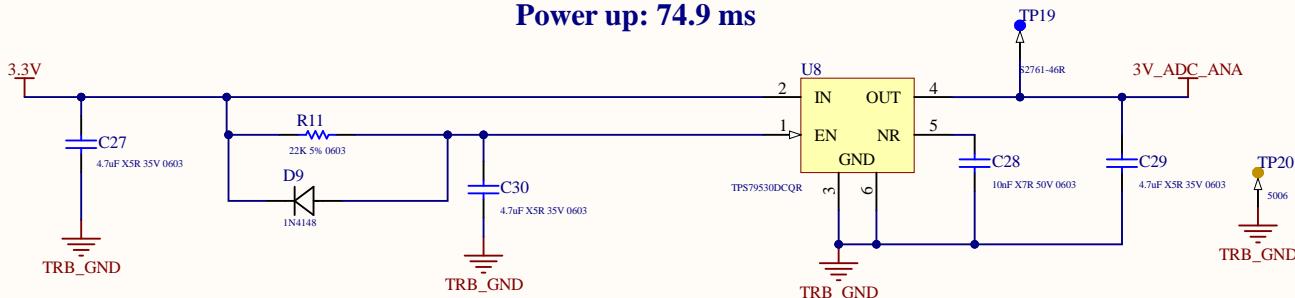
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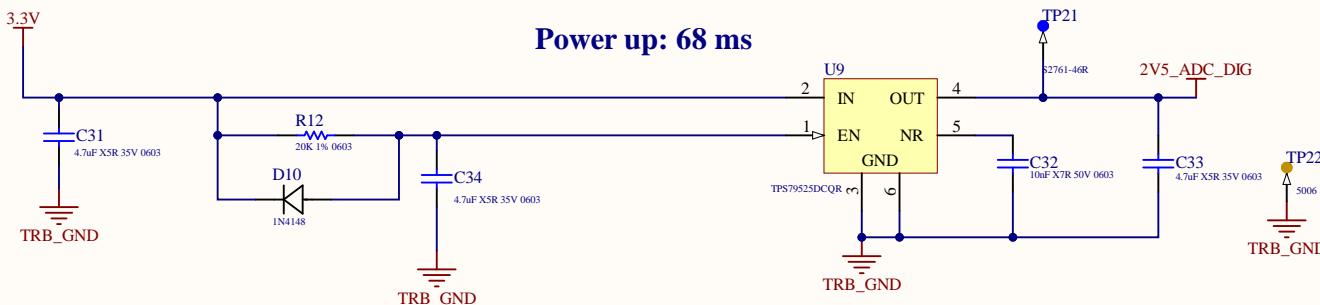
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A

**Power up: 74.9 ms**

B

**Power up: 68 ms**

C

**Title 3V ADC**

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A

A

B

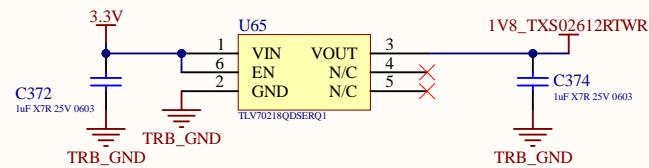
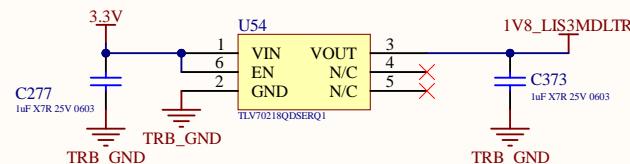
B

C

C

D

D



## Title *IV8 Supply*

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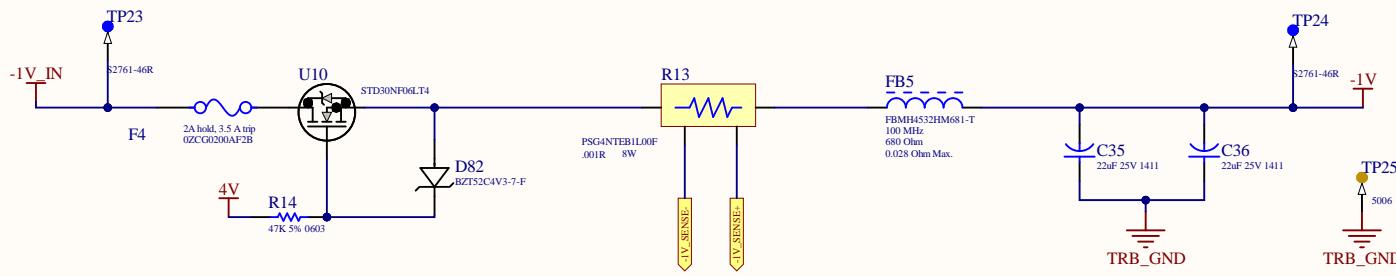
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A

A

B

B



C

C

D

D

## Title ***-1V Distribution***

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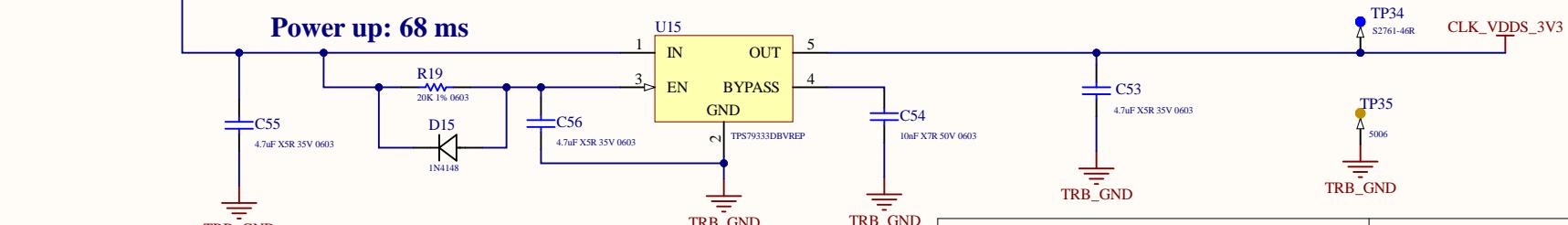
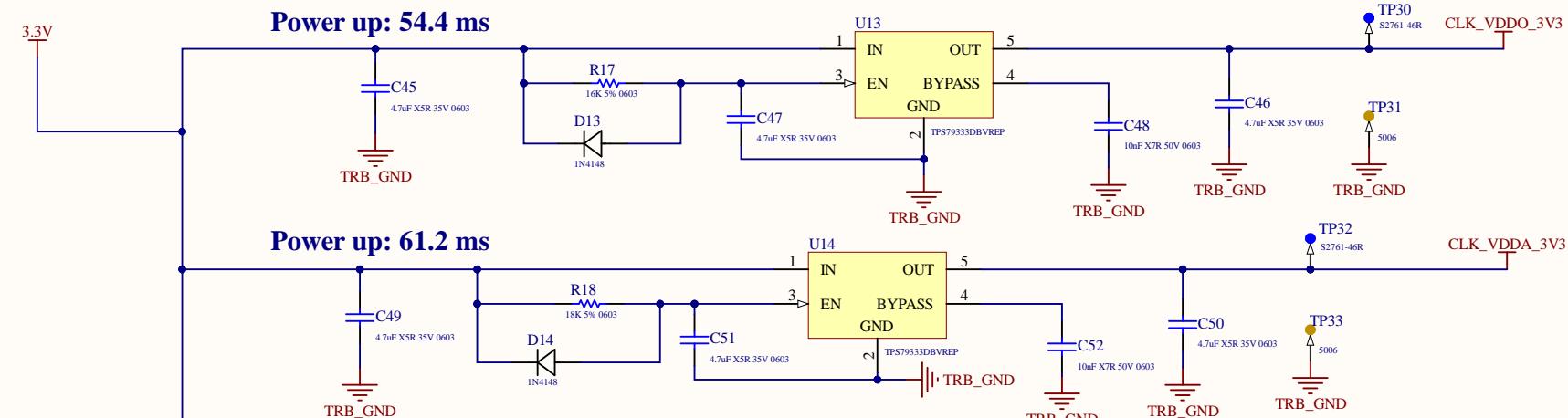
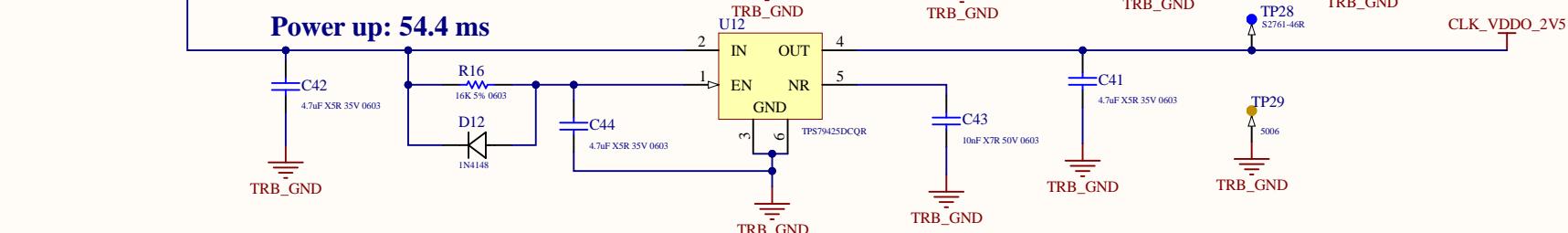
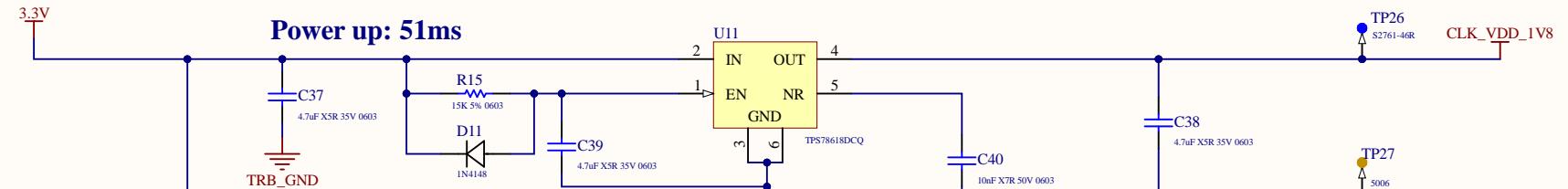
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## Title *Clock power*

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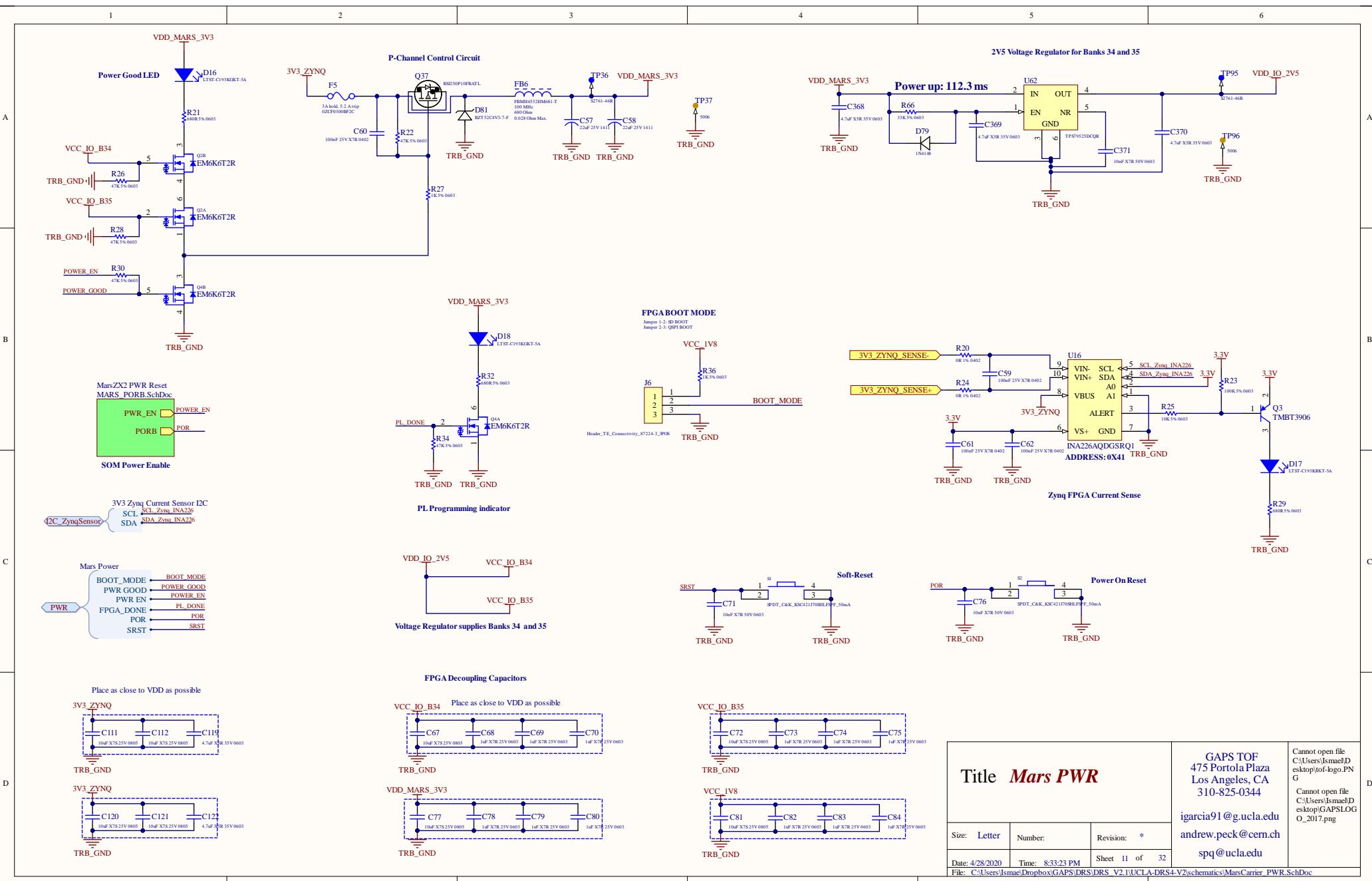
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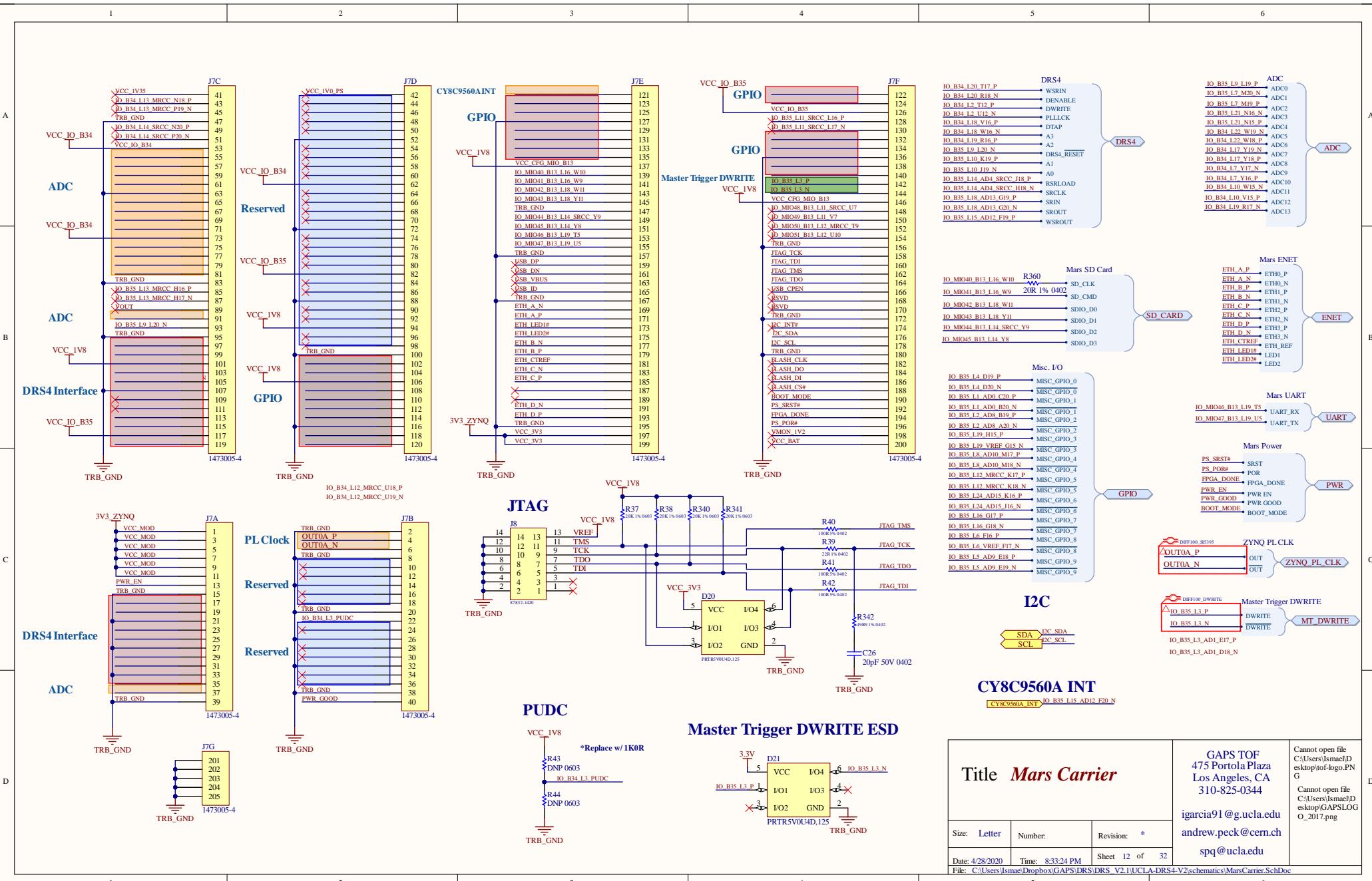
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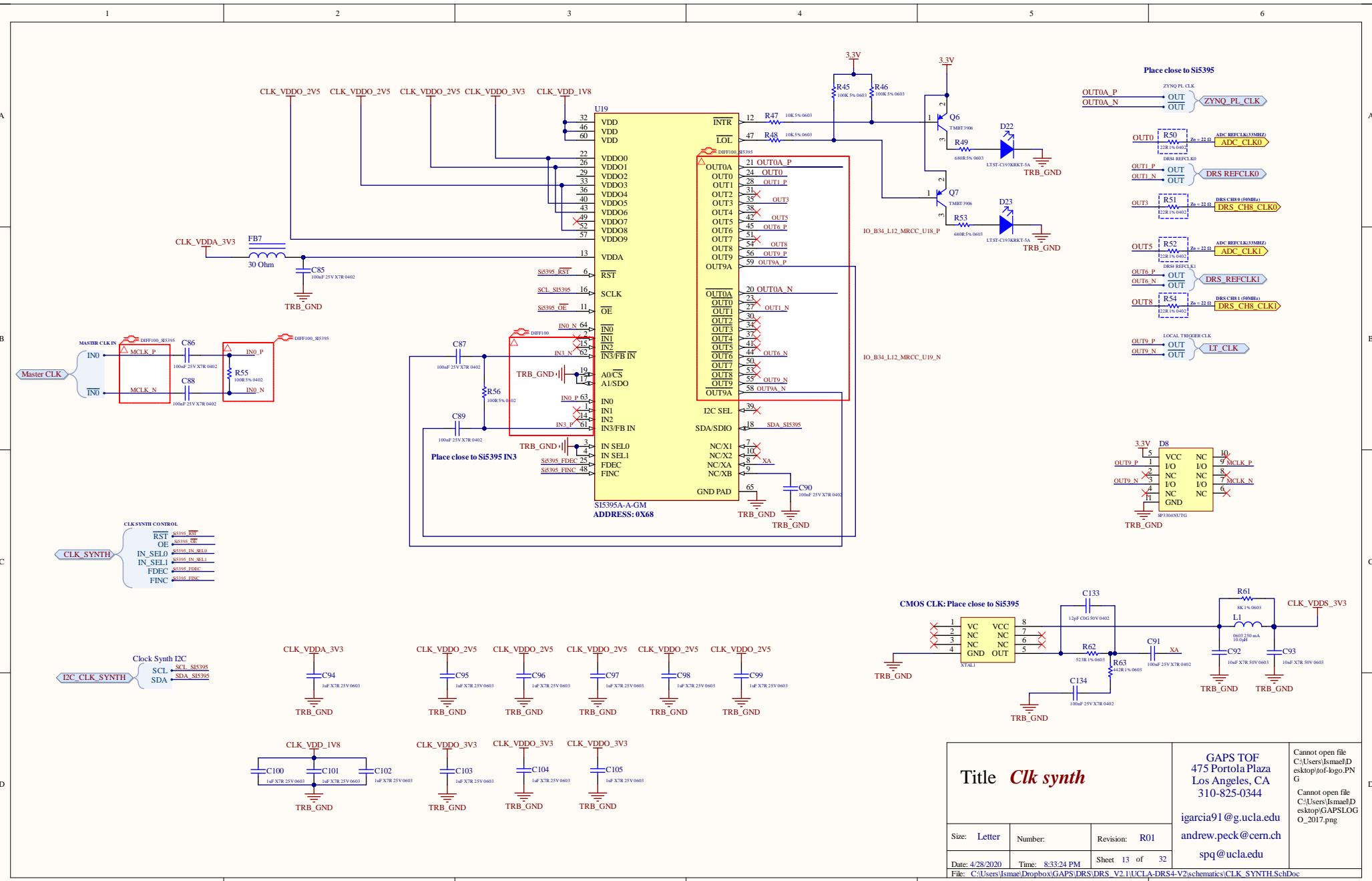
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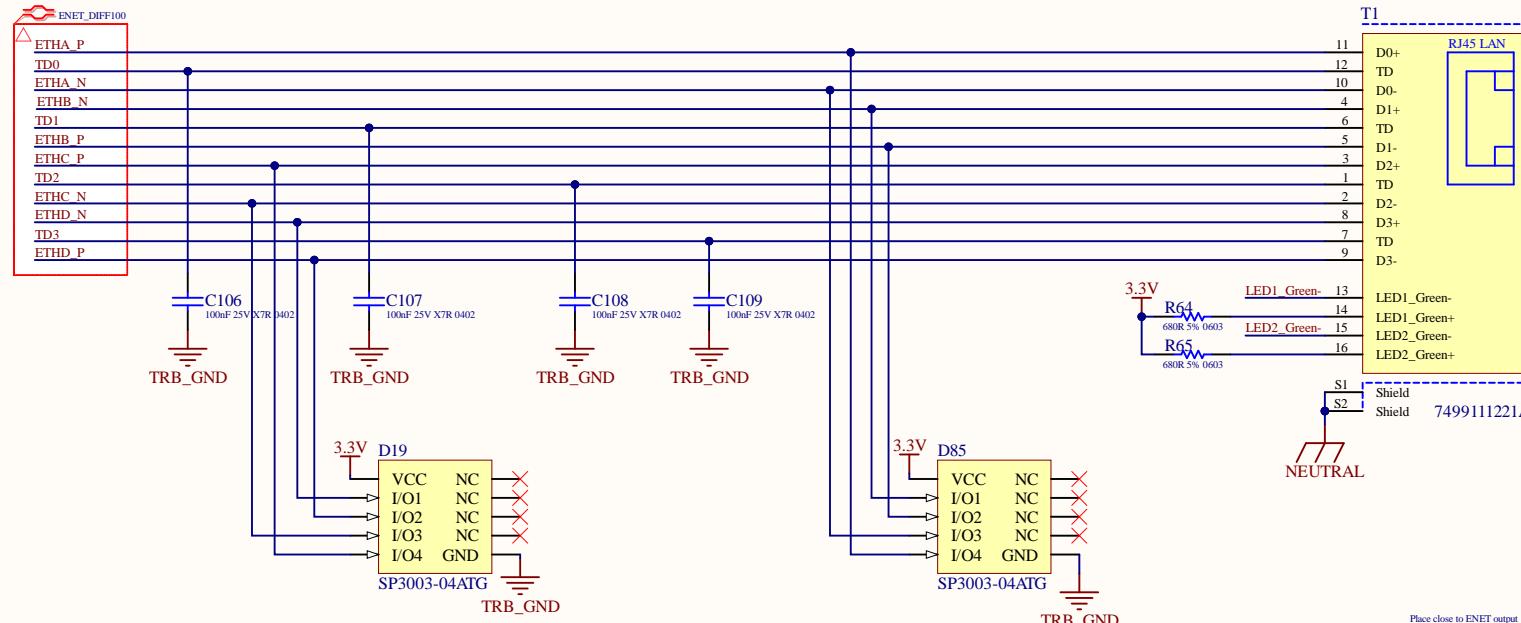
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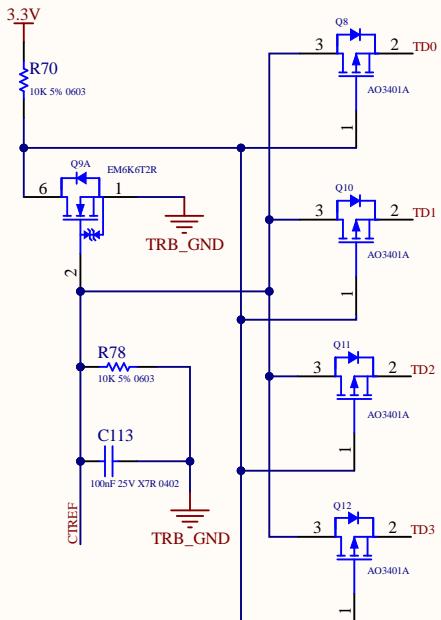




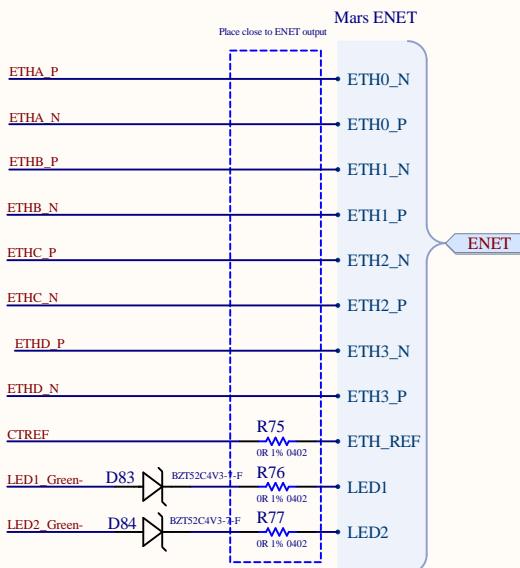
A



B



C



D

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A

A

B

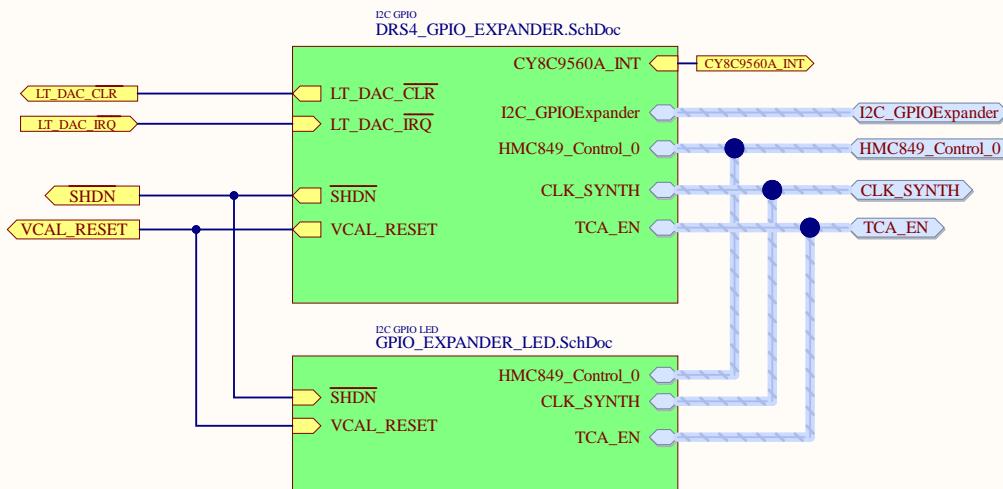
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D



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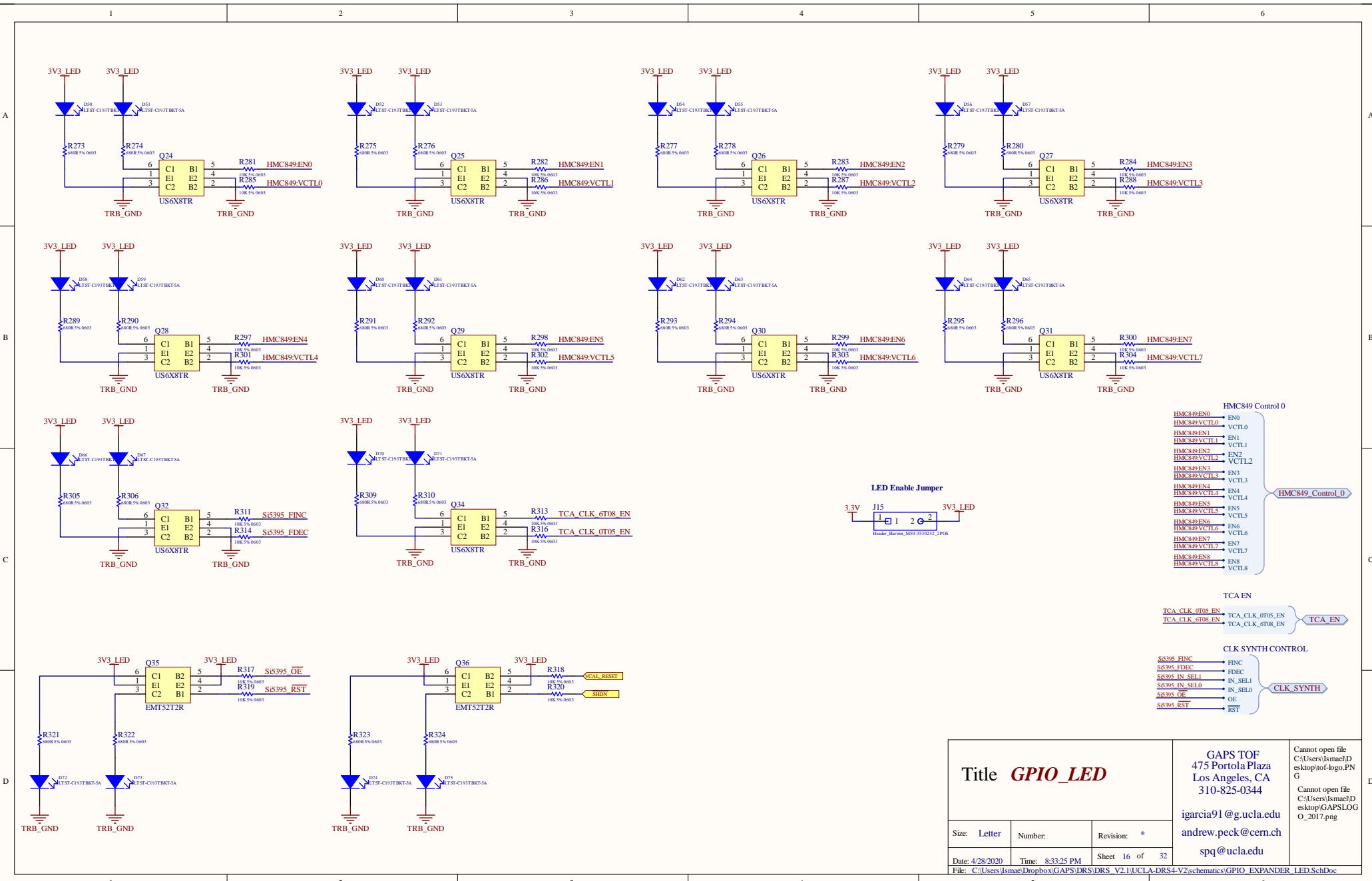
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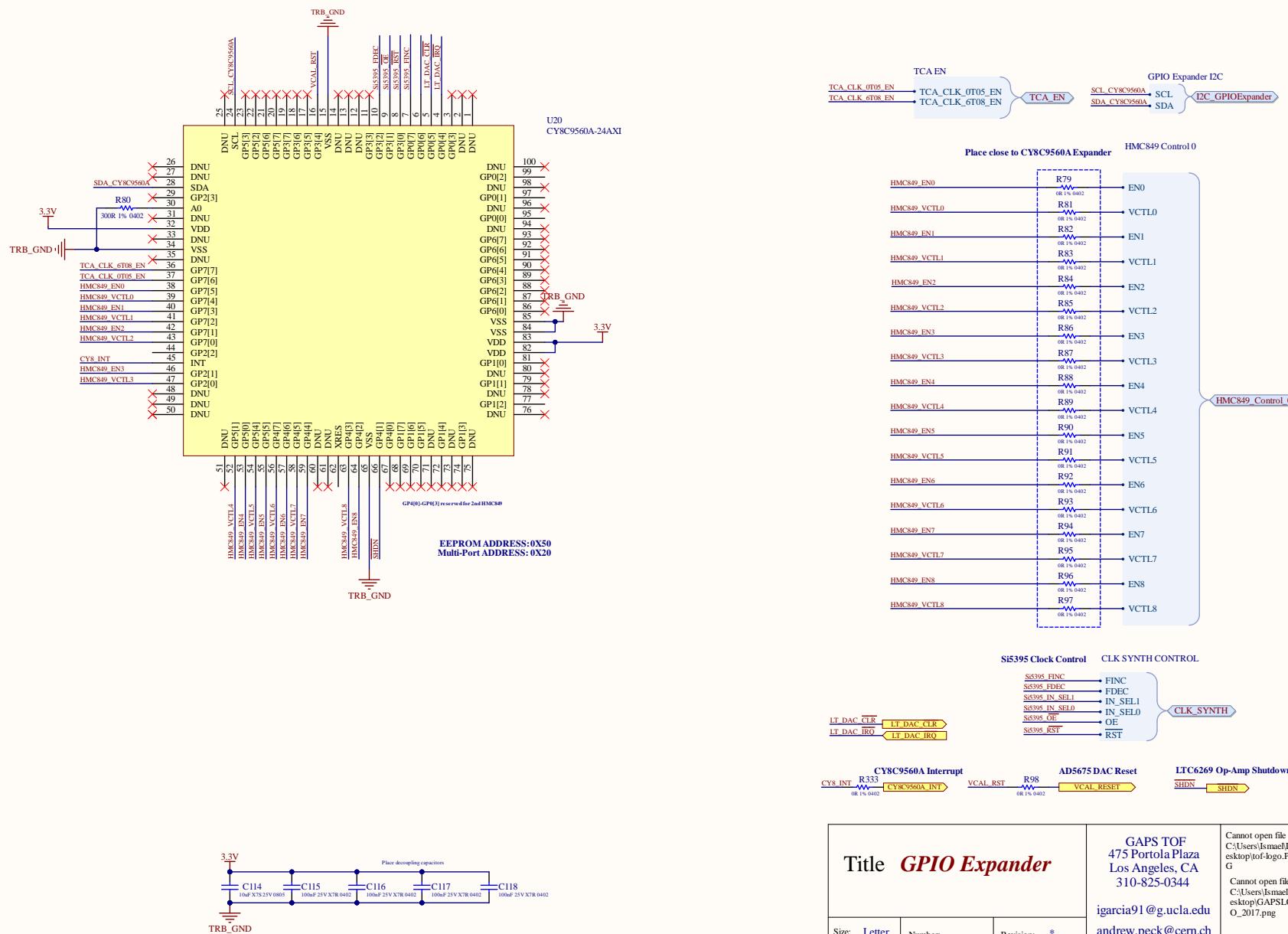
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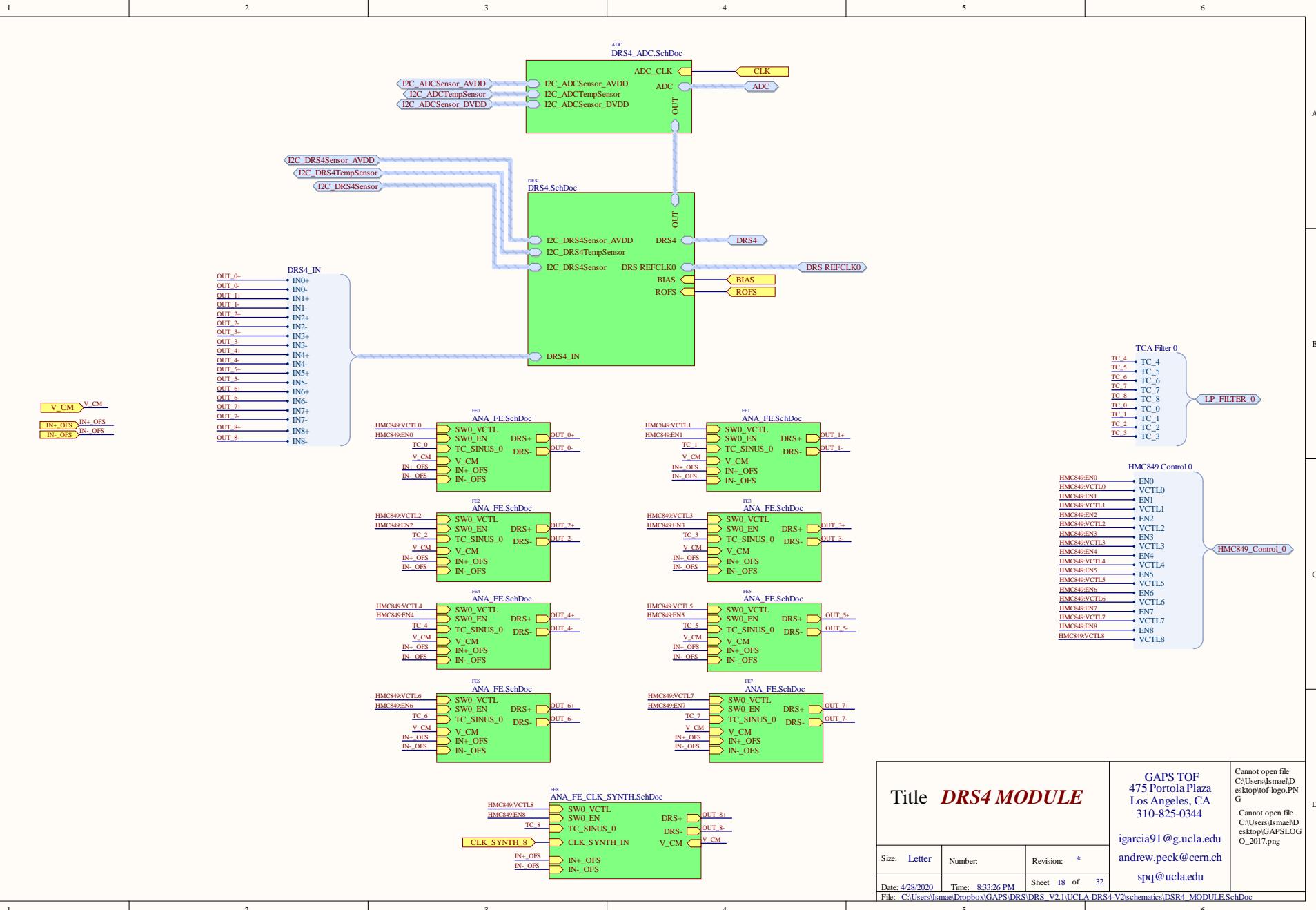
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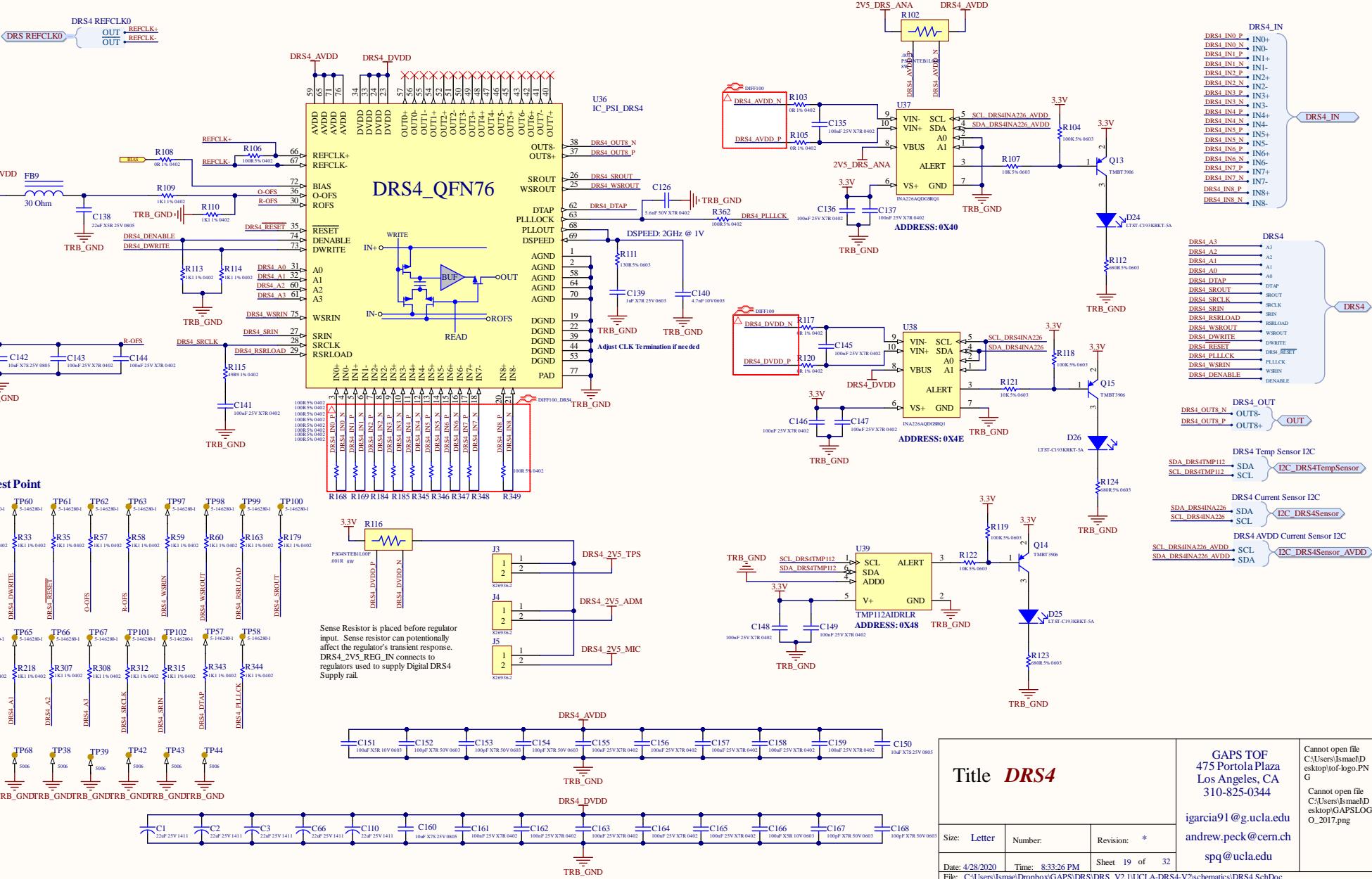
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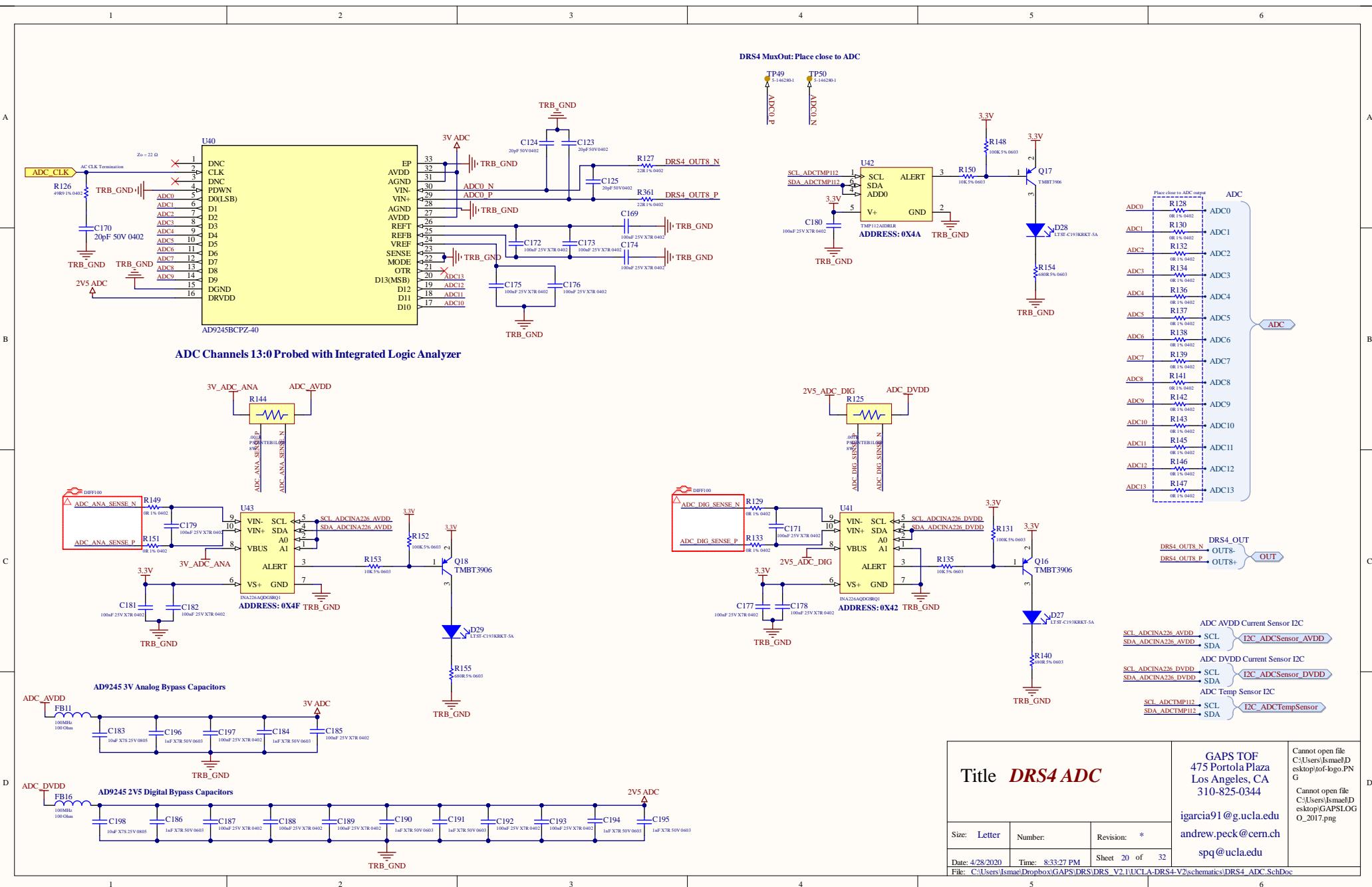
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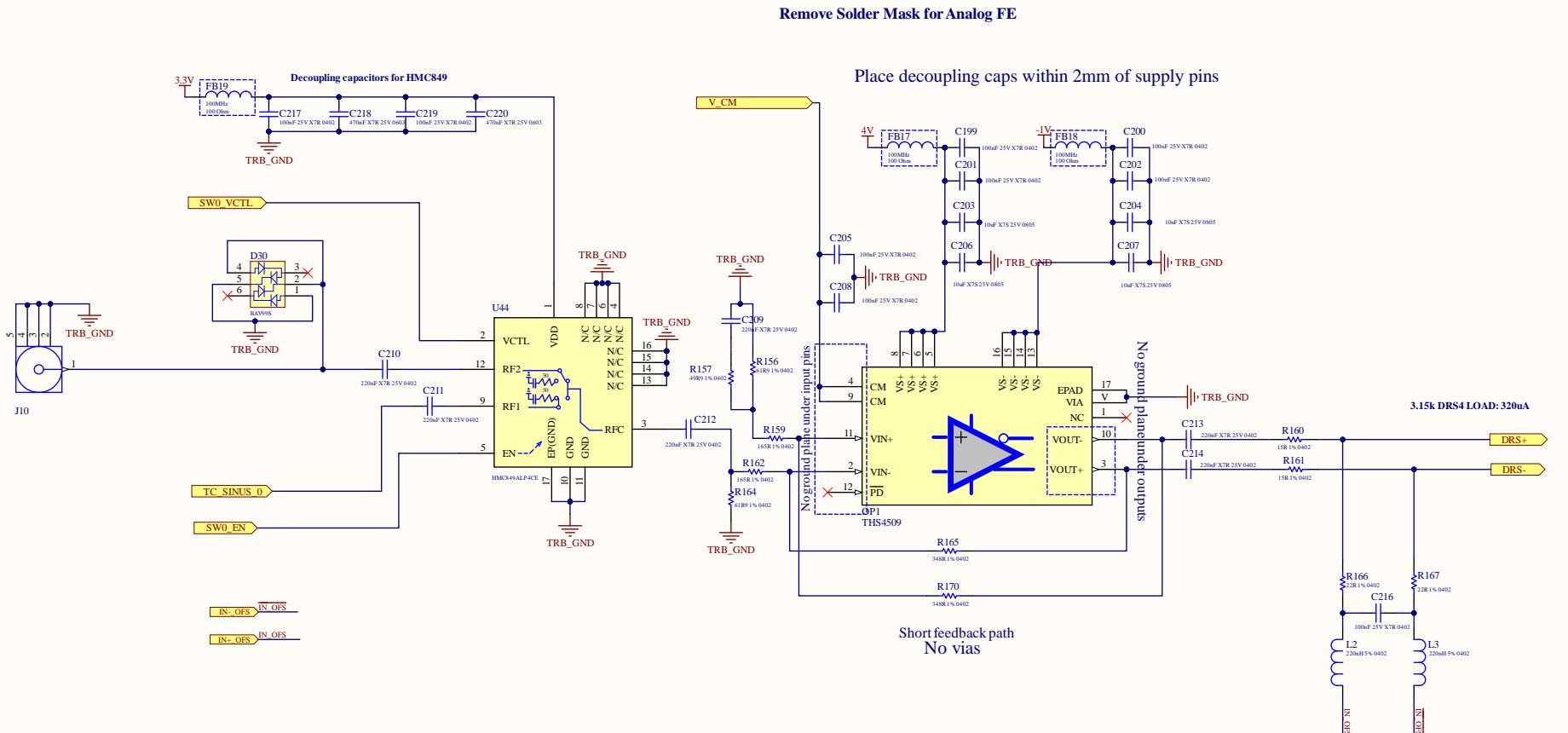




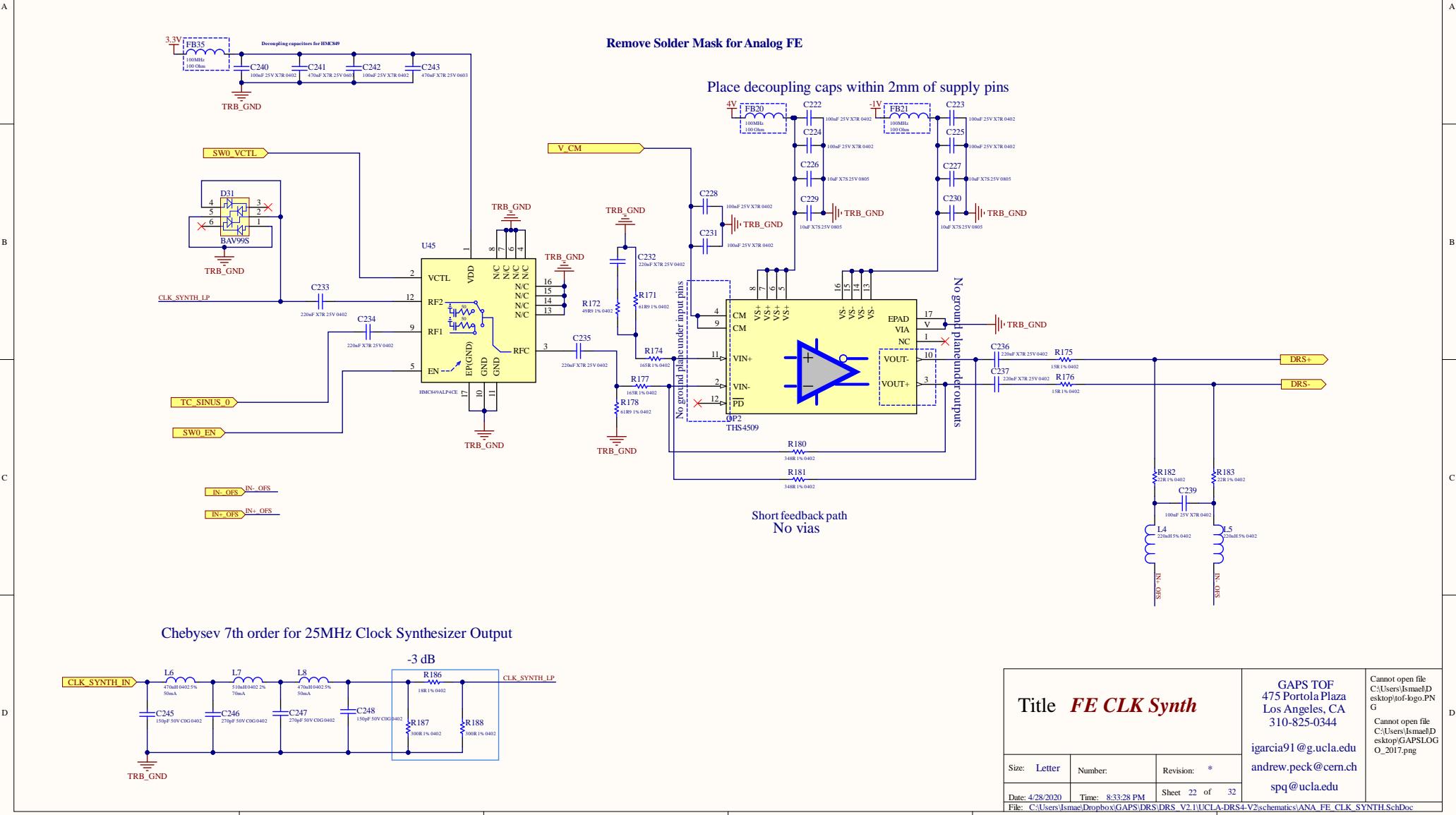






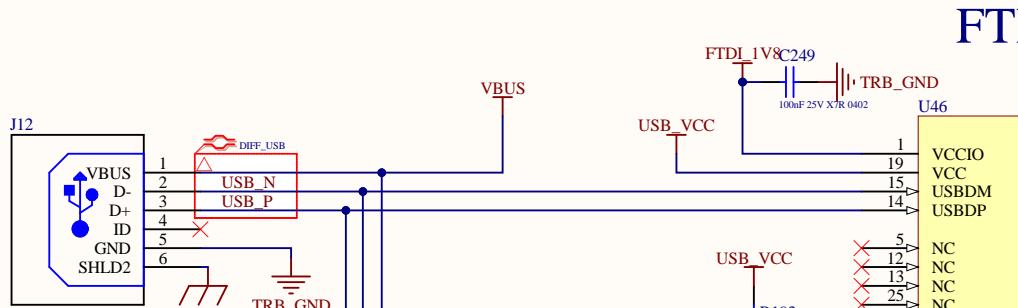


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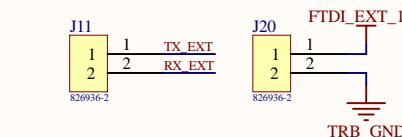


A

A



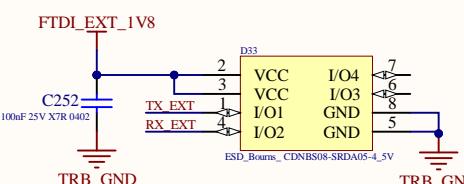
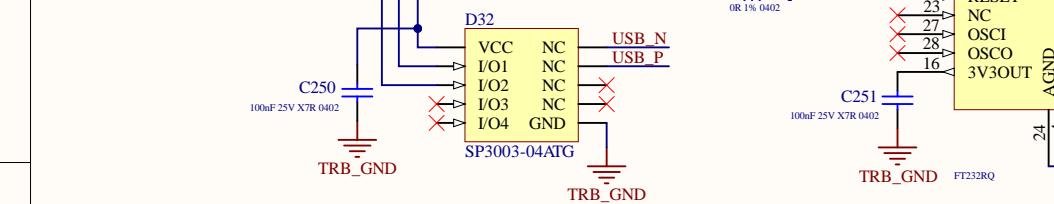
## FTDI



FTDI's TX needs to connect to SOM's RX  
FTDI's RX needs to connect to SOM's TX

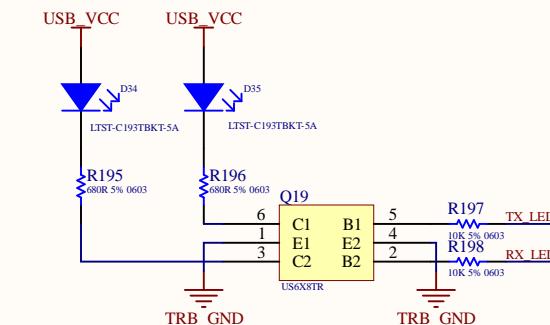
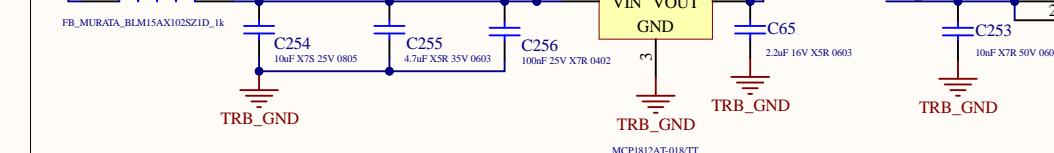
B

B



C

C



D

D

Title **FTDI**

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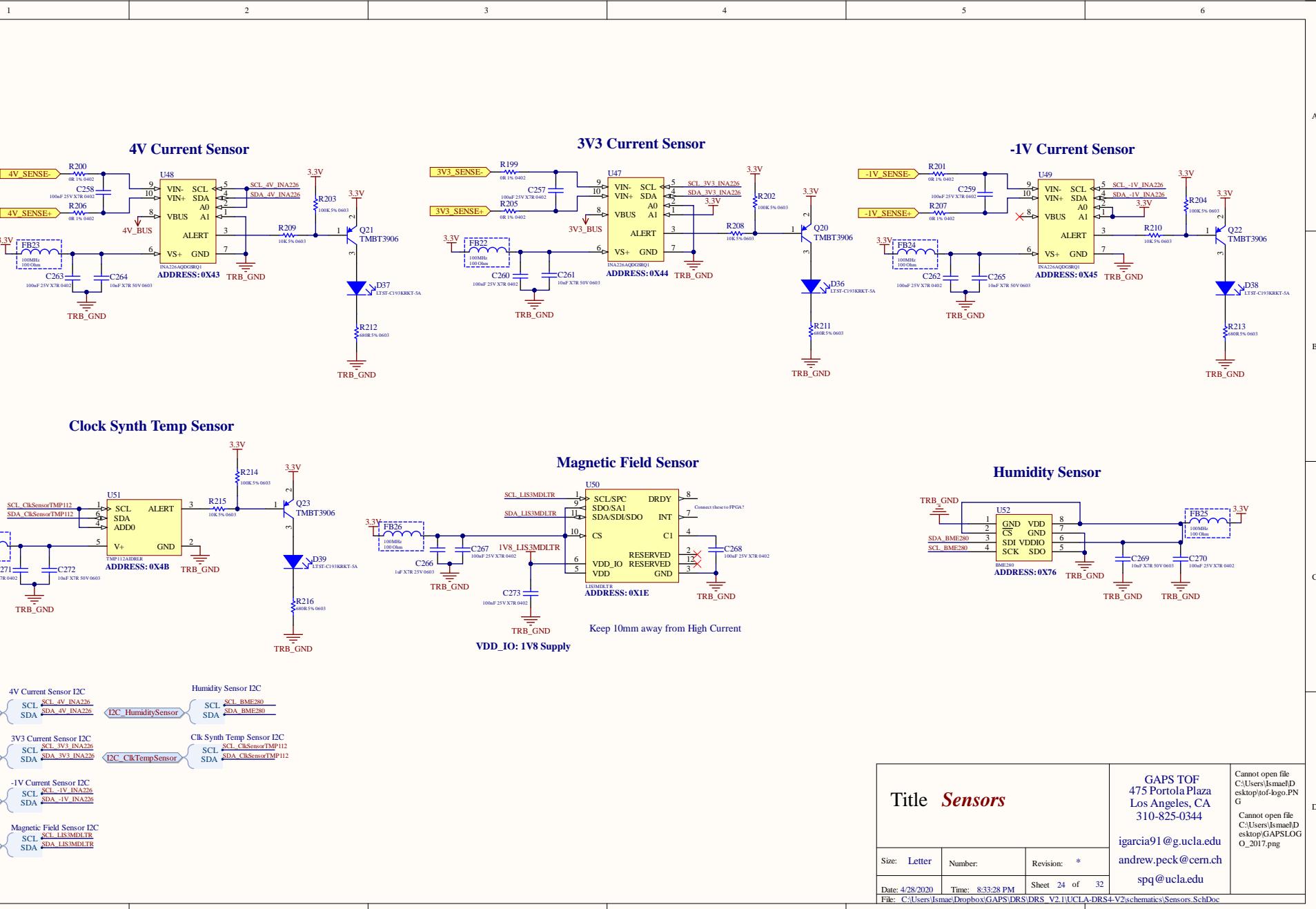
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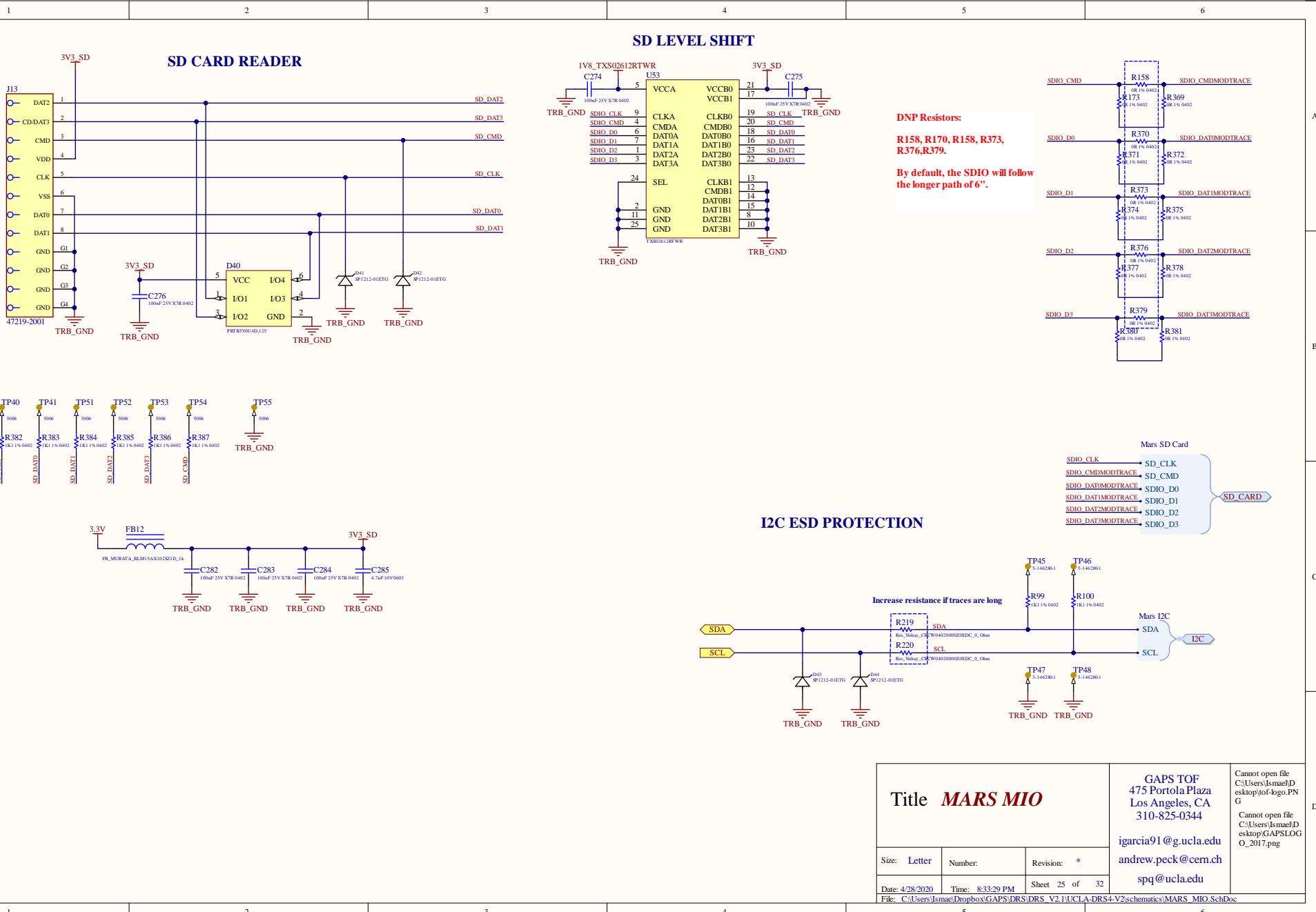
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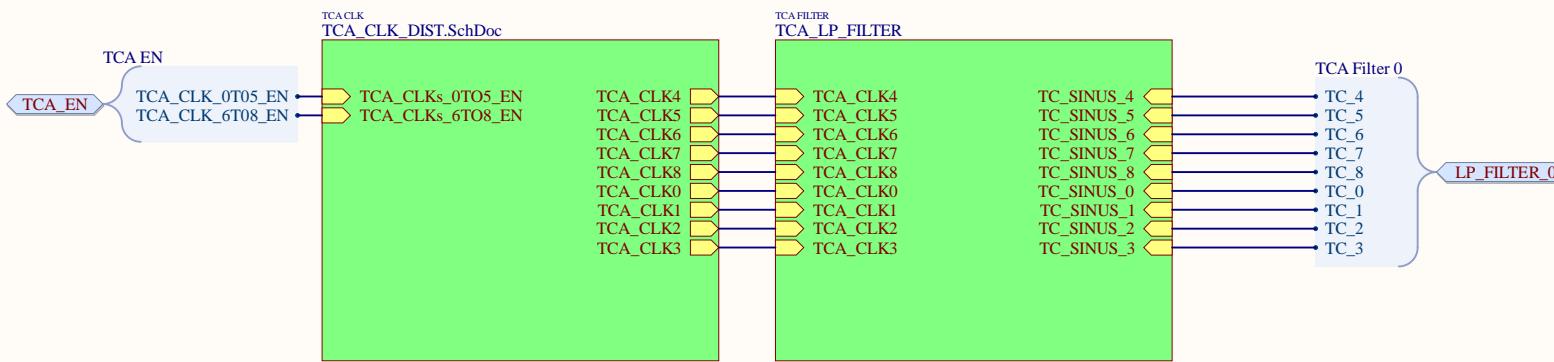
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## Title *TCA Module*

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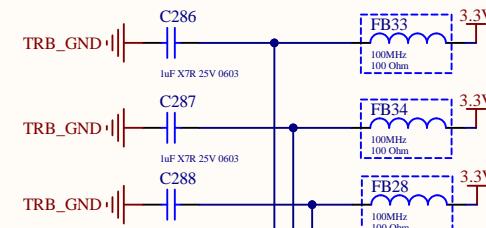
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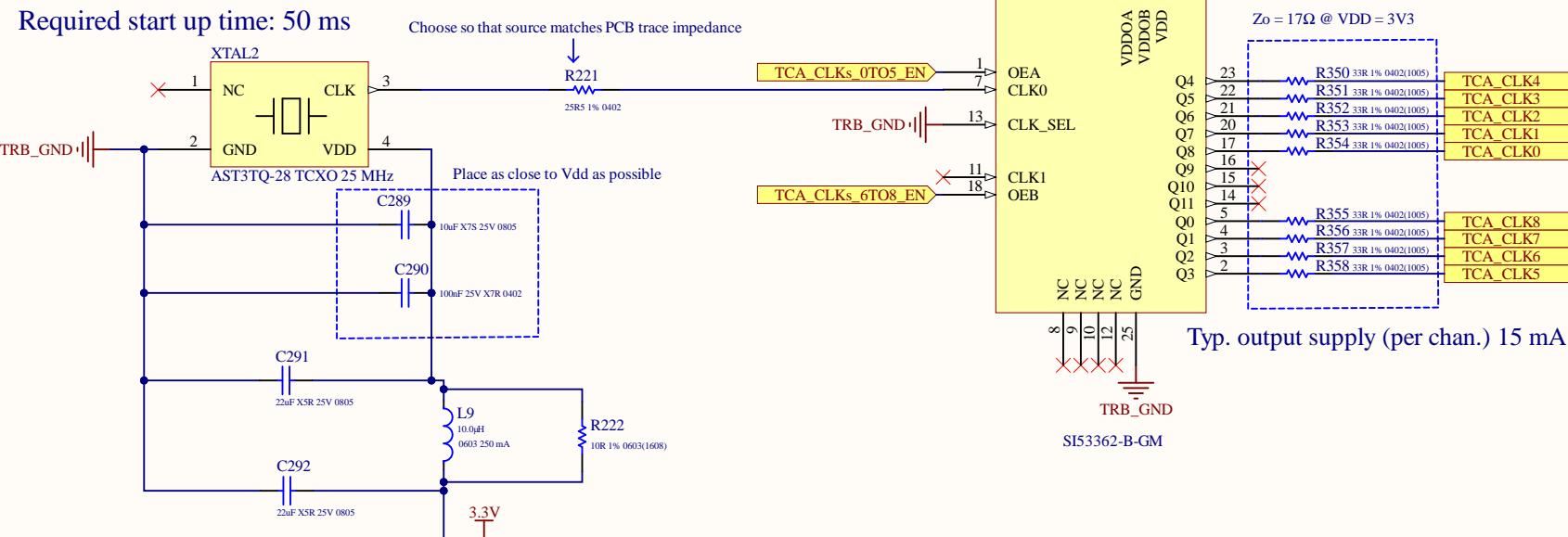
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## Title **TCA CLK**

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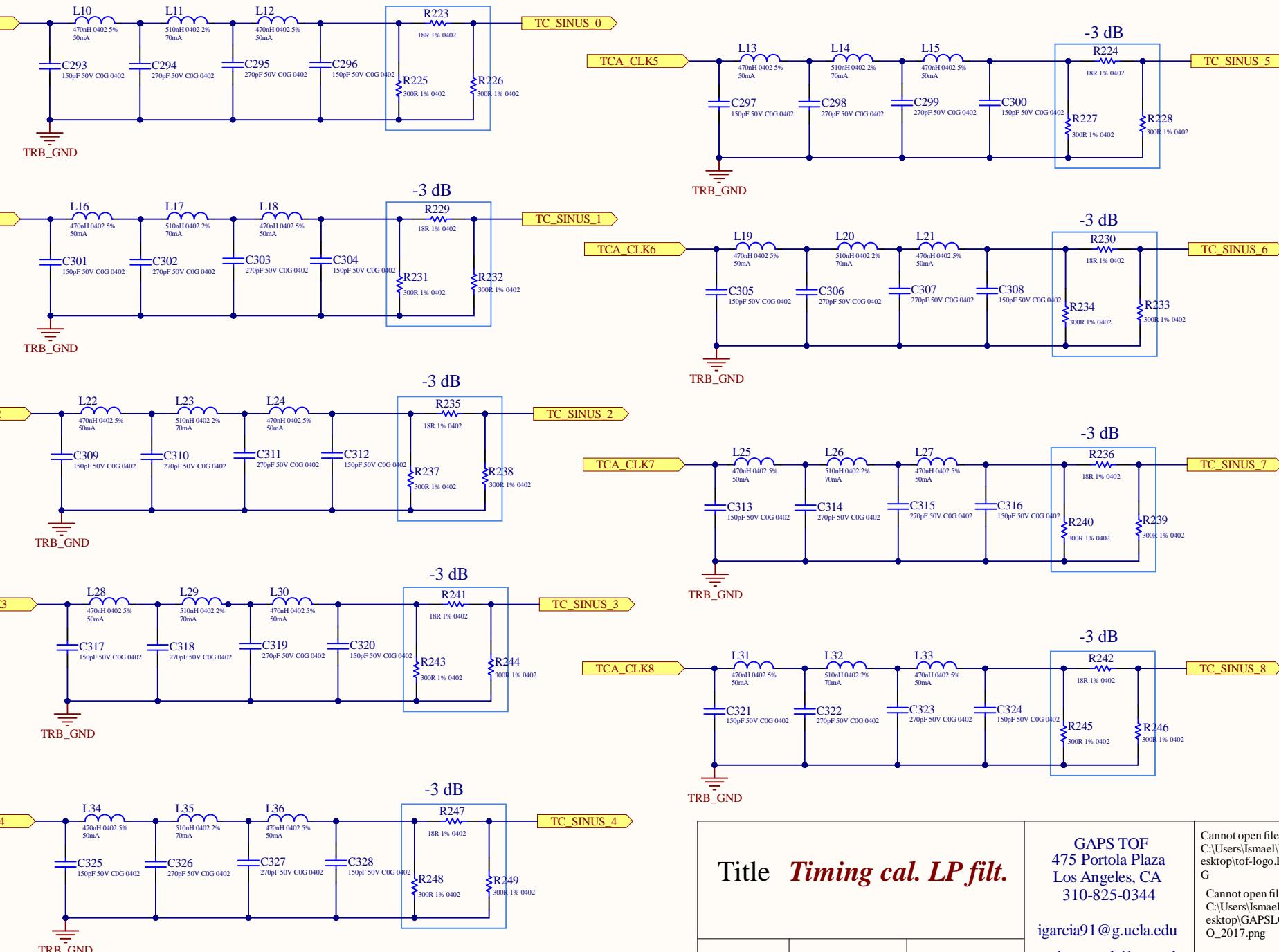
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**7th order Chebyshev: ~500 mVpp, 25 MHz sinusoid  
-3 dB**

**Remove Solder Mask**



**Title *Timing cal. LP filt.***

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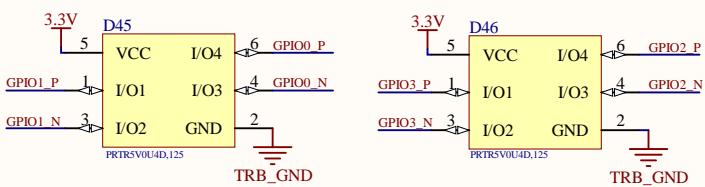
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310-825-0344

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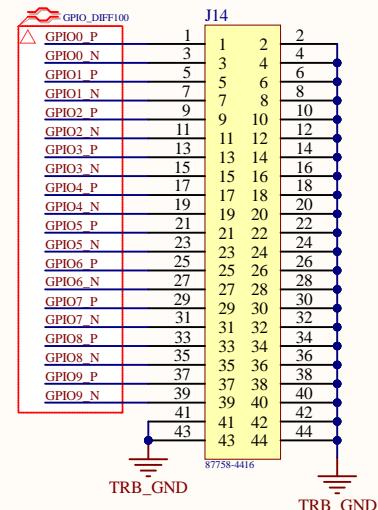
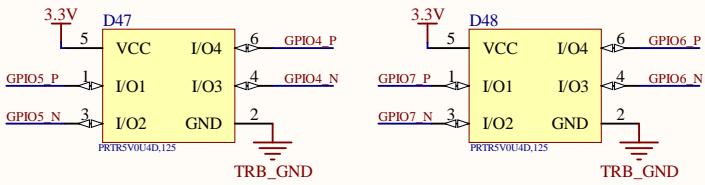
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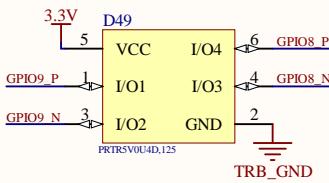
B

Misc. I/O

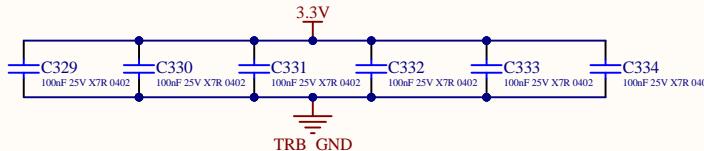
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MISC_GPIO_0	GPIO0_N
MISC_GPIO_1	GPIO1_P
MISC_GPIO_1	GPIO1_N
MISC_GPIO_2	GPIO2_P
MISC_GPIO_2	GPIO2_N
MISC_GPIO_3	GPIO3_P
MISC_GPIO_3	GPIO3_N
MISC_GPIO_4	GPIO4_P
MISC_GPIO_4	GPIO4_N
MISC_GPIO_5	GPIO5_P
MISC_GPIO_5	GPIO5_N
MISC_GPIO_6	GPIO6_P
MISC_GPIO_6	GPIO6_N
MISC_GPIO_7	GPIO7_P
MISC_GPIO_7	GPIO7_N
MISC_GPIO_8	GPIO8_P
MISC_GPIO_8	GPIO8_N
MISC_GPIO_9	GPIO9_P
MISC_GPIO_9	GPIO9_N



C



D



## Title *MARS GPIO*

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Date: 4/28/2020	Time: 8:33:30 PM	Sheet 29 of 32
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File: C:\Users\Ismael\Dropbox\GAPS\DRS\DRS_V2.1\UCLA-DRS4-V2\schematics\MARS_GPIO_MISC.SchDoc
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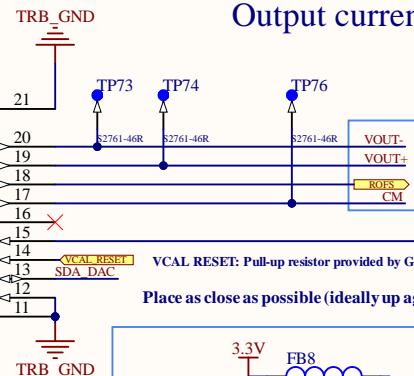
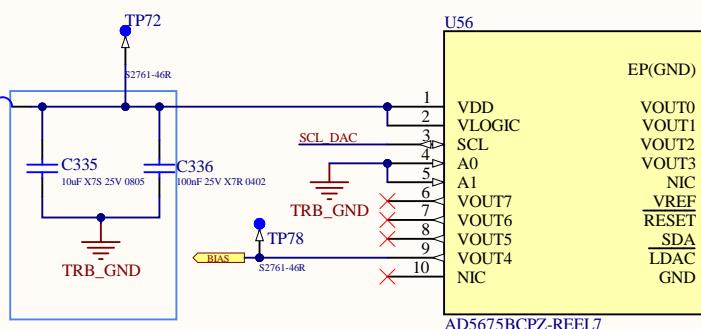
igarcia91@g.ucla.edu  
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A

Place as close as possible (ideally up against device)

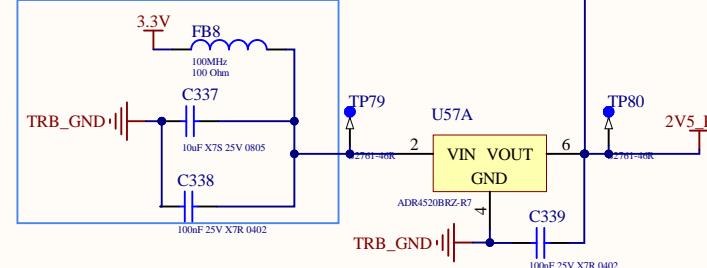


Output current drive: 15 mA

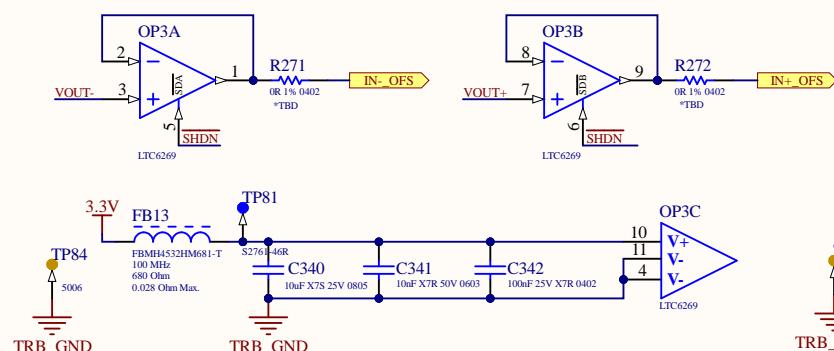


B

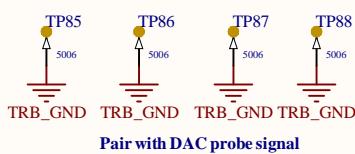
Mount on analog plane



C



D

Title *ANA calibration*

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Date: 4/28/2020 Time: 8:33:30 PM Sheet 30 of 32

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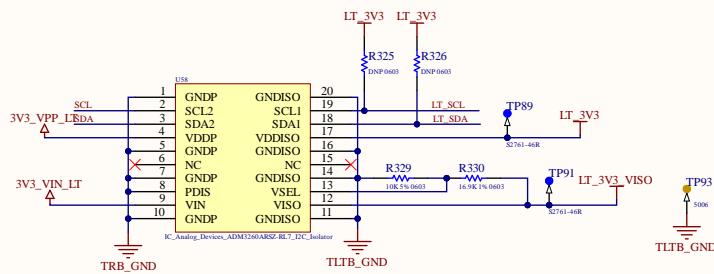
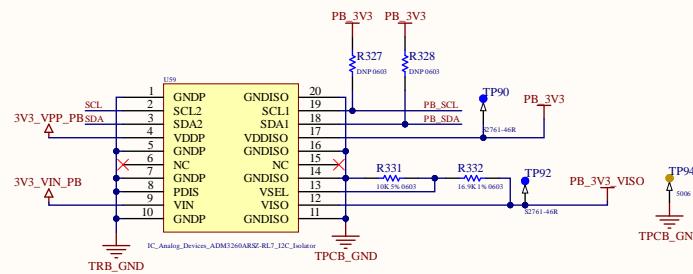
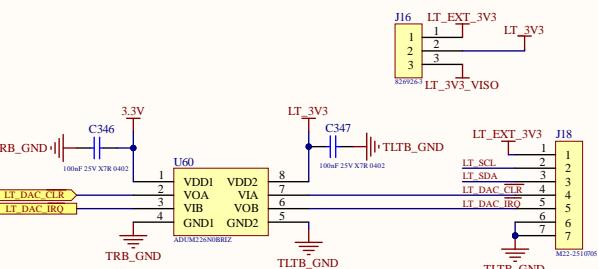
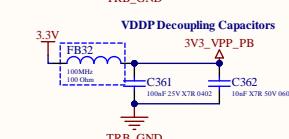
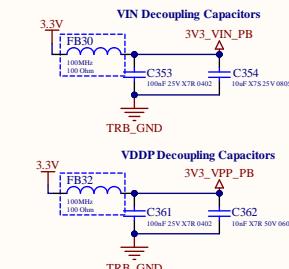
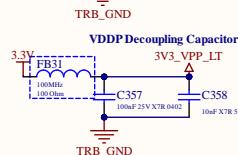
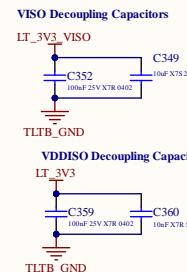
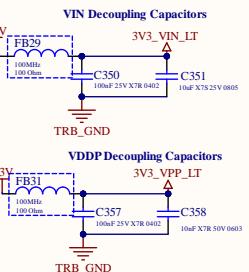
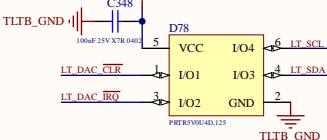
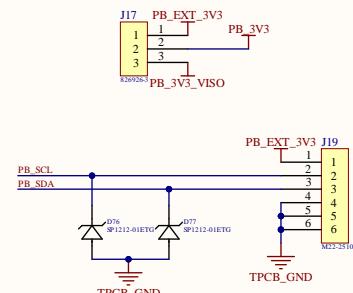
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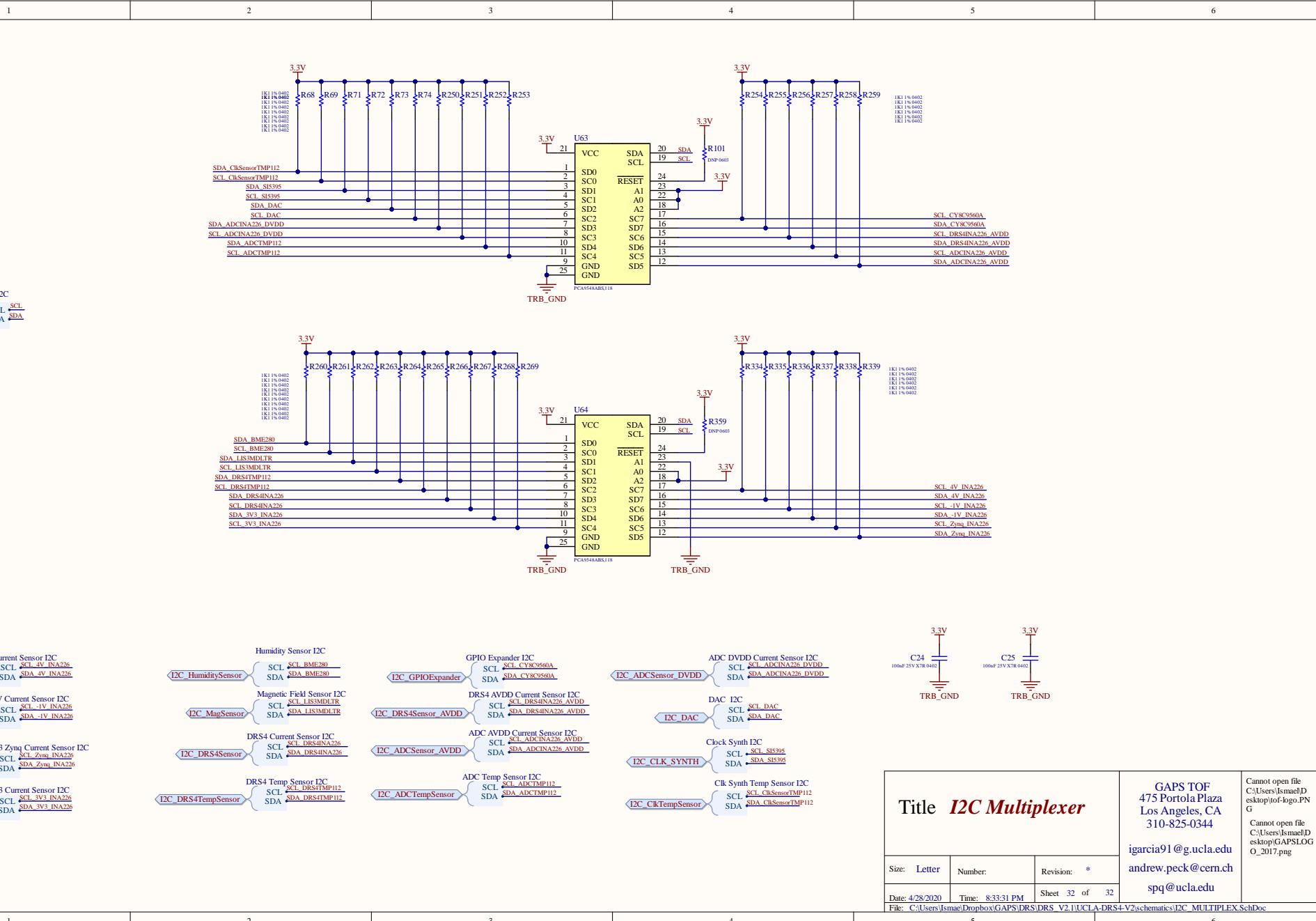
**Local Trigger I2C Isolation****Power Board I2C Isolation****Select between Isolated DC/DC or External VDD****Select between Isolated DC/DC or External VDD****Title *I2C ISOLATION***

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Sheet 31 of 32			*

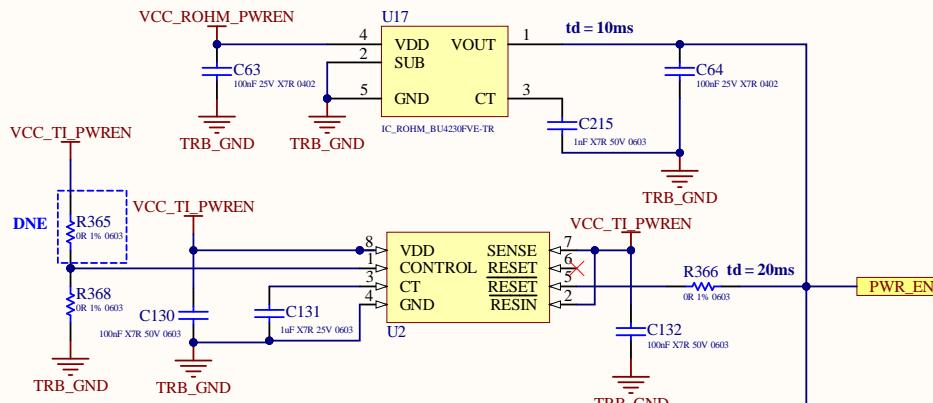


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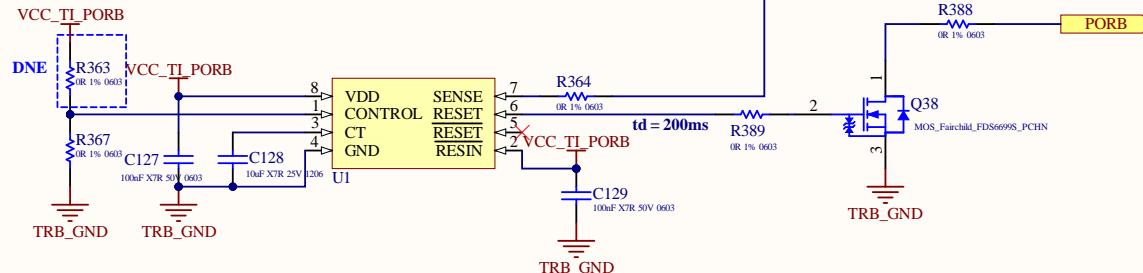
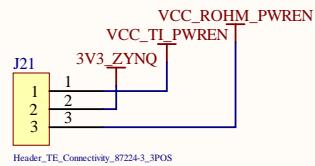


B

(J21) Select between ROHM reset circuit or Texas Instrument reset circuit for Power Enable



C



Title

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