1.1 Solution

Row	SOUT	CIN	S = CIN ⊕ SOUT	COUT = CIN · SOUT
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

1.2 Solution

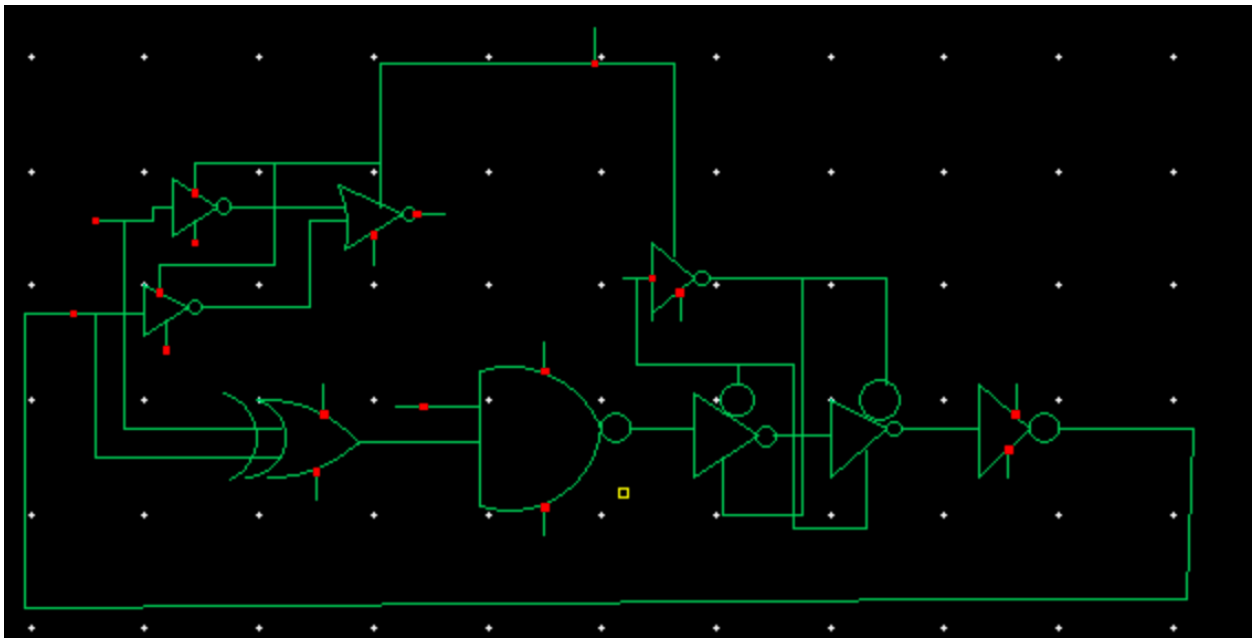
Cycle	RST	CIN	SOUT (at start of cycle)	S = CIN ⊕ SOUT	COUT = CIN · SOUT	D = NAND(S,RST)	Notes / Truth-table row hit
0	0	0	X (unknown)	–	–	1	**Init**: force next SOUT=0
1	1	0	0	0	0	1	**Row 0**: (SOUT=0, CIN=0)
2	1	1	0	1	0	0	**Row 1**: (SOUT=0, CIN=1) → next SOUT=1
3	1	0	1	1	0	0	**Row 2**: (SOUT=1, CIN=0) → next SOUT=1
4	1	1	1	0	1	1	**Row 3**: (SOUT=1, CIN=1) → next SOUT=0

1.3 Solution

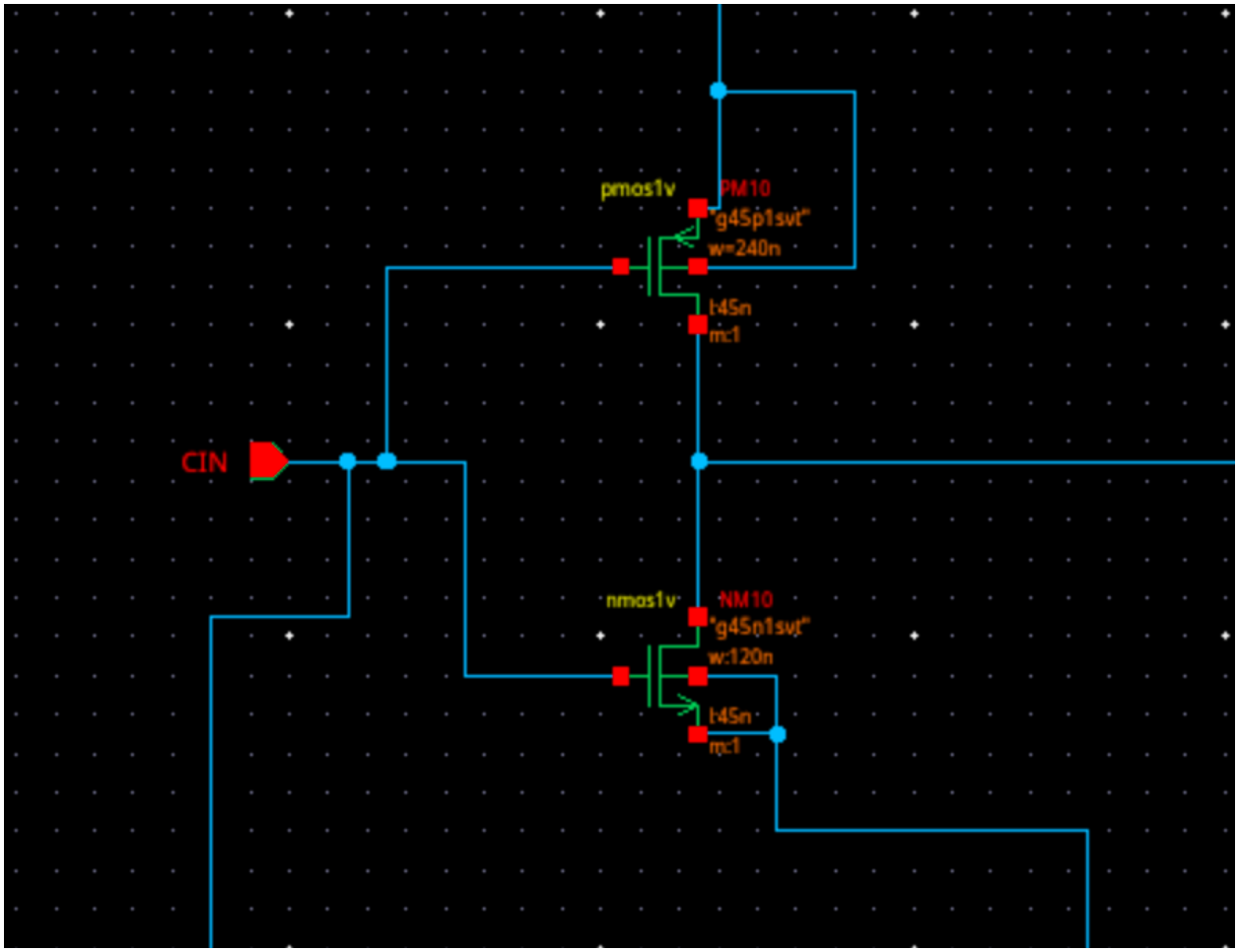
Per instructions, **annotate the first cycle** that exercises each truth-table row:

- Row 0 → **Cycle 1**
- Row 1 → **Cycle 2**
- Row 2 → **Cycle 3**
- Row 3 → **Cycle 4**

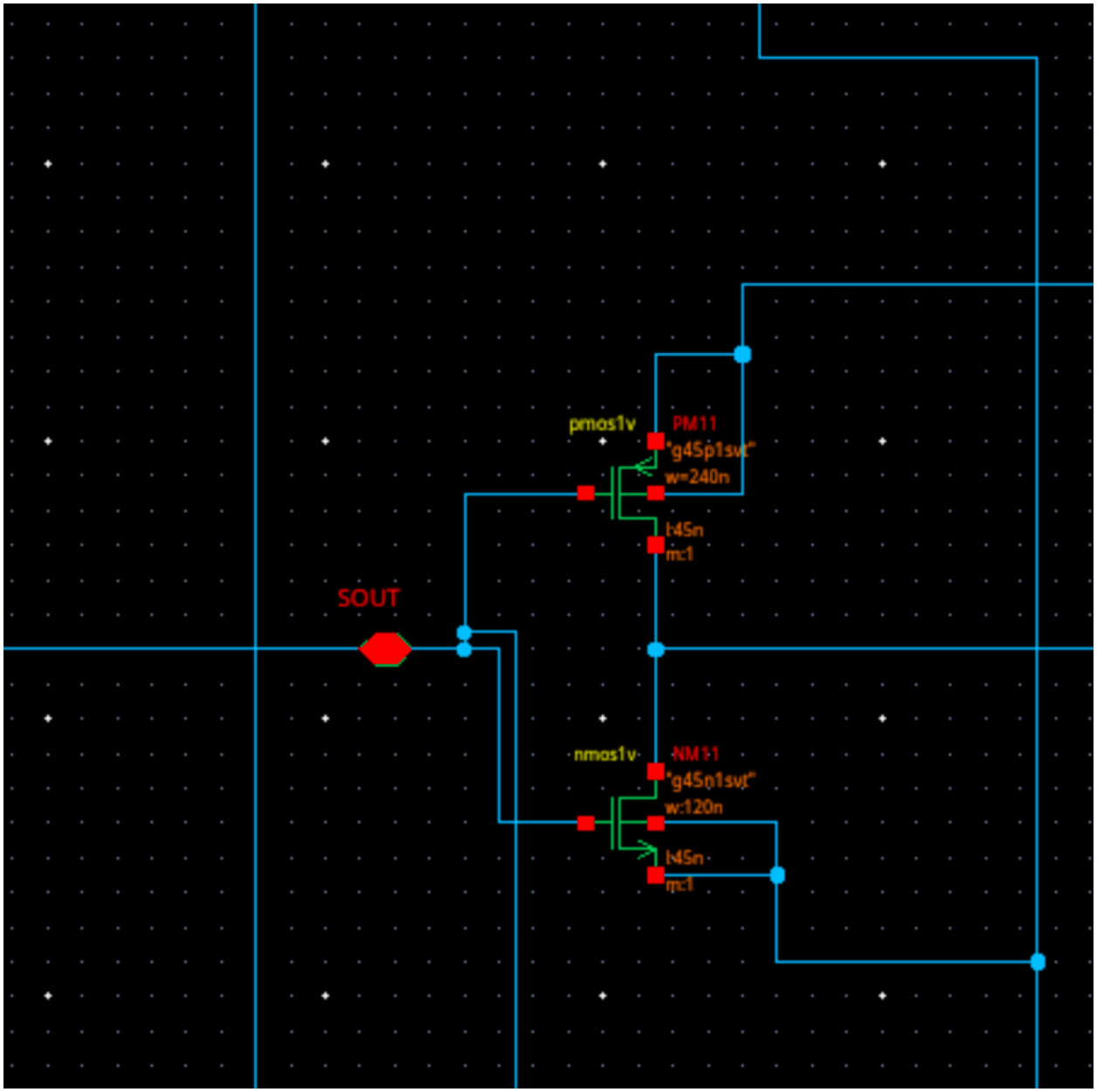
2.1 Solution



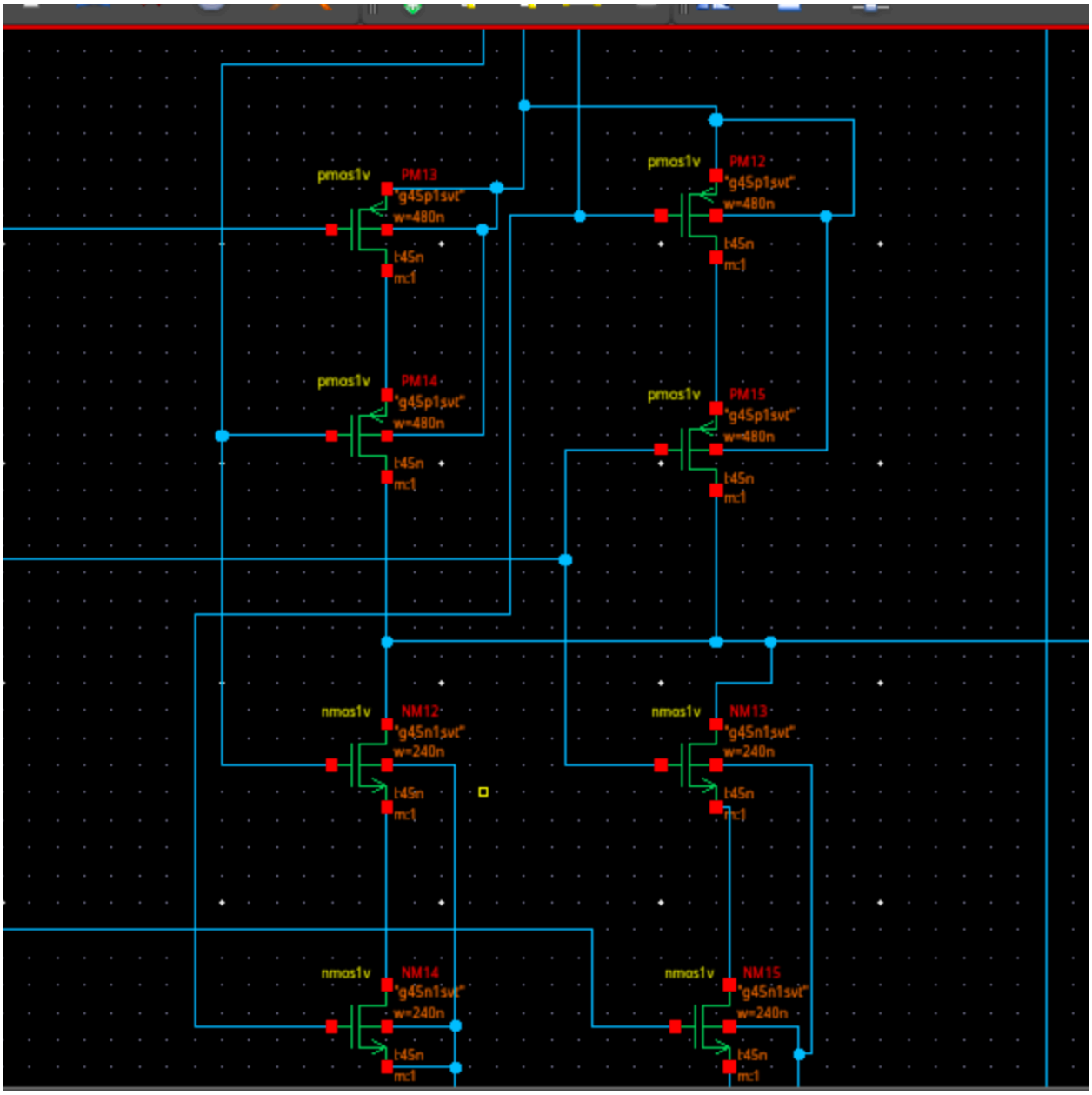
2.2 Solution


pmos1v
PM10
"g45p1svt"
w=240n
l=45n
m=1
CIN
nmos1v
NM10
"g45n1svt"
w=120n
l=45n
m=1

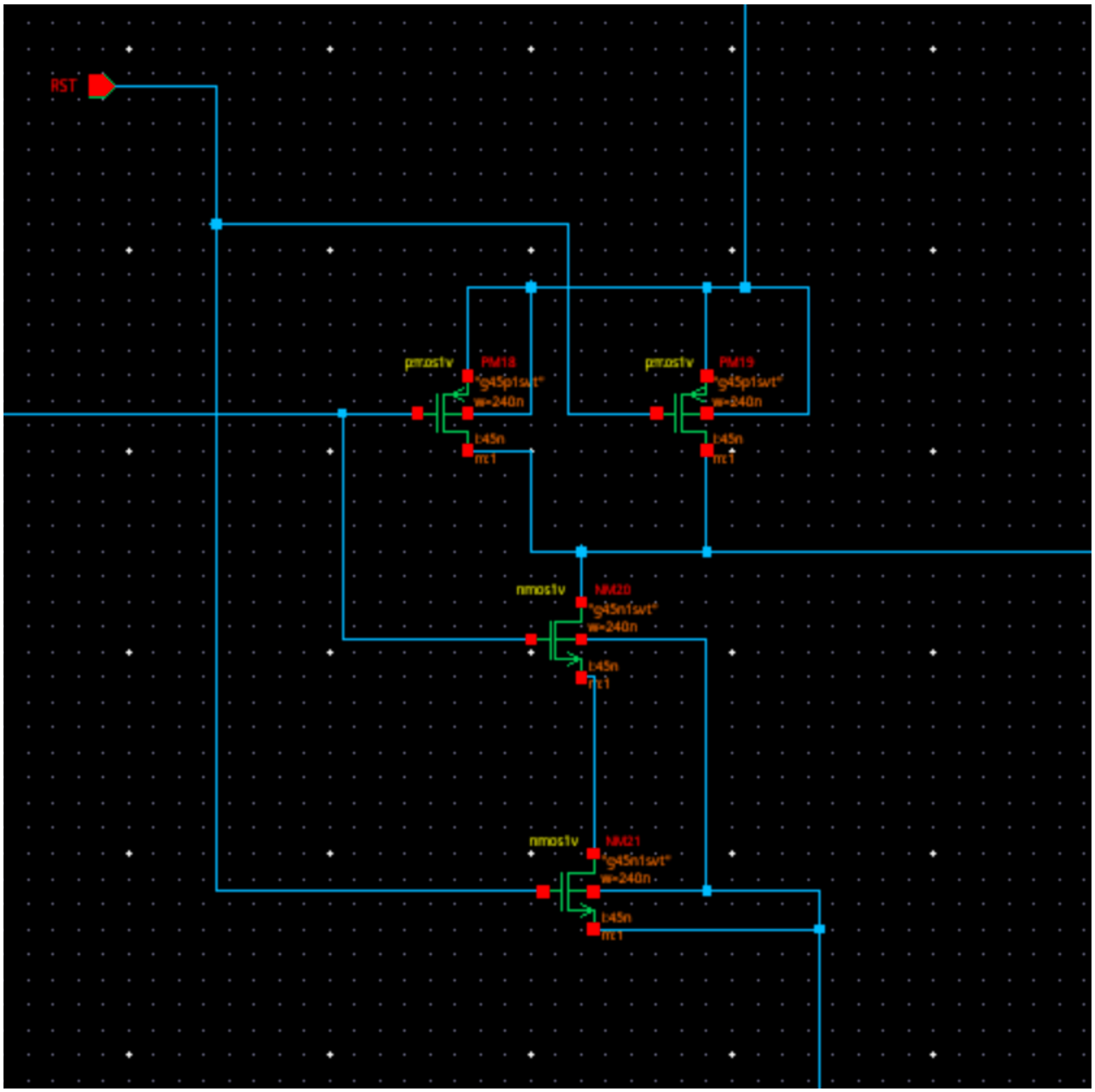
NOT GATE


pmos1v
PM11
"g45p1svt"
w=240n
l=45n
m=1
SOUT
nmos1v
NM11
"g45n1svt"
w=120n
l=45n
m=1

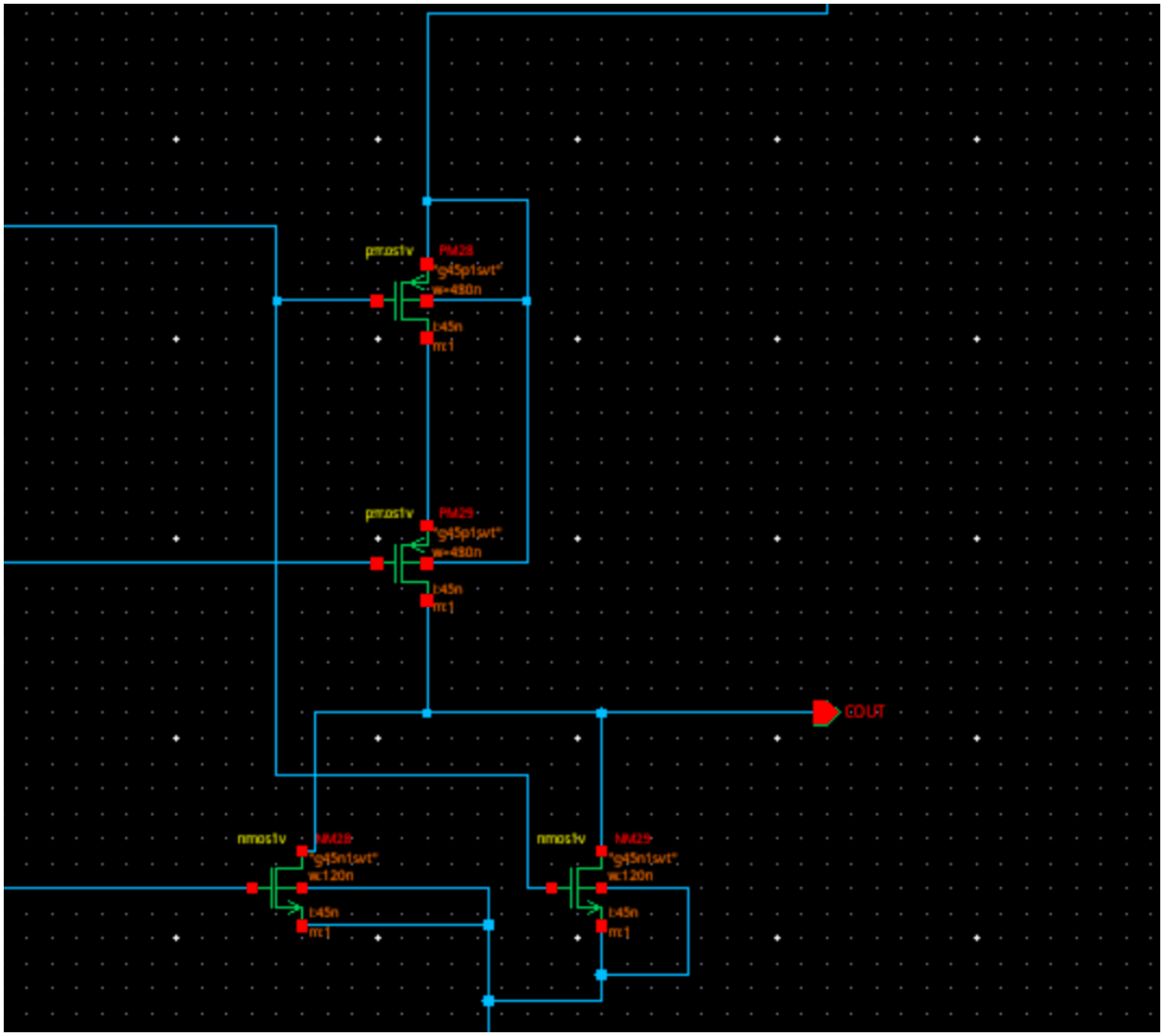
NOT GATE


pmos1v
PM13
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM12
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM14
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM15
"g45p1svt"
w=480n
l=45n
m=1
nmos1v
NM12
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM13
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM14
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM15
"g45n1svt"
w=240n
l=45n
m=1

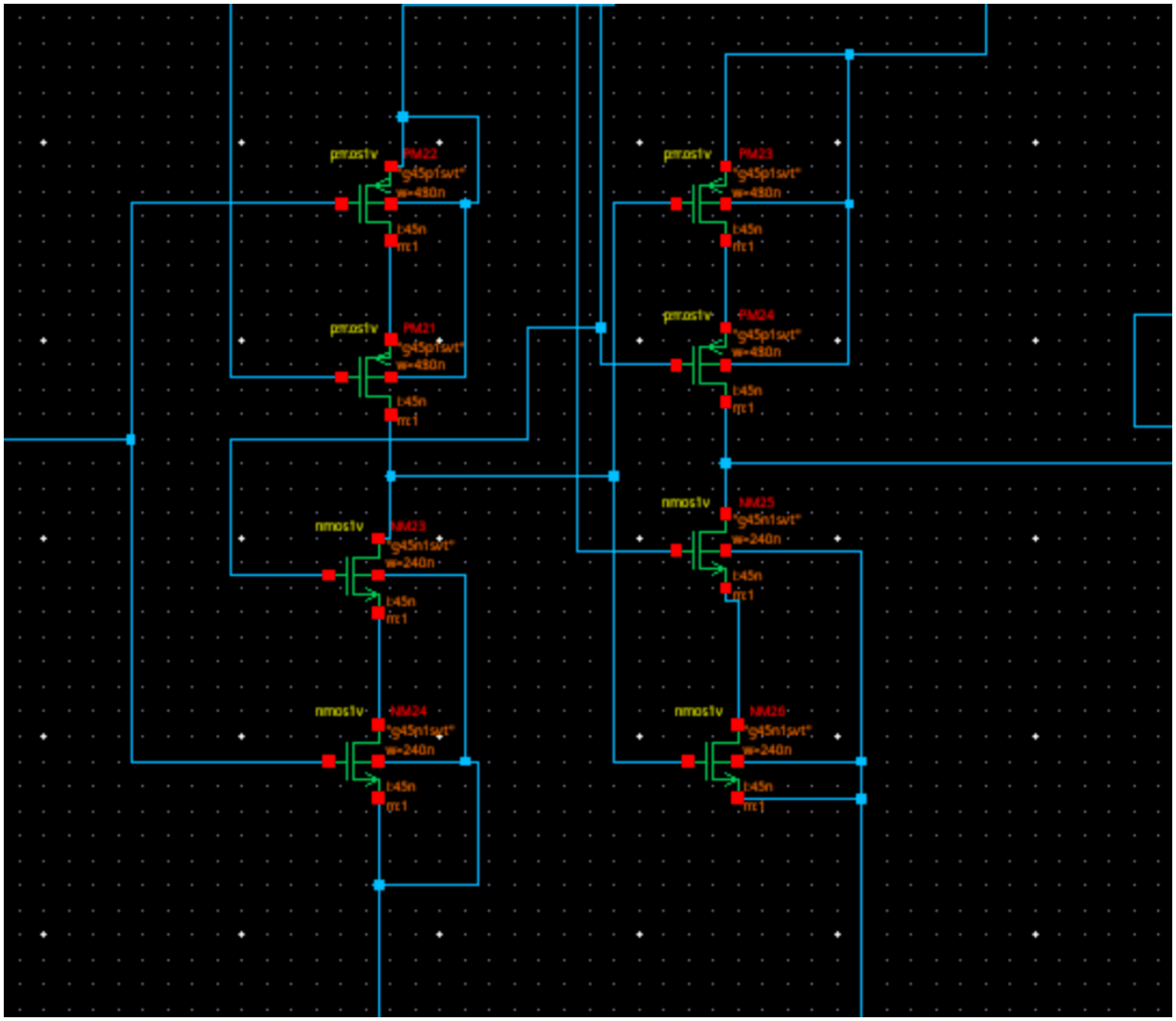
XOR gate


RST
pmos1v
PM18
"g45p1svt"
w=240n
l=45n
m=1
pmos1v
PM19
"g45p1svt"
w=240n
l=45n
m=1
nmos1v
NM20
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM21
"g45n1svt"
w=240n
l=45n
m=1

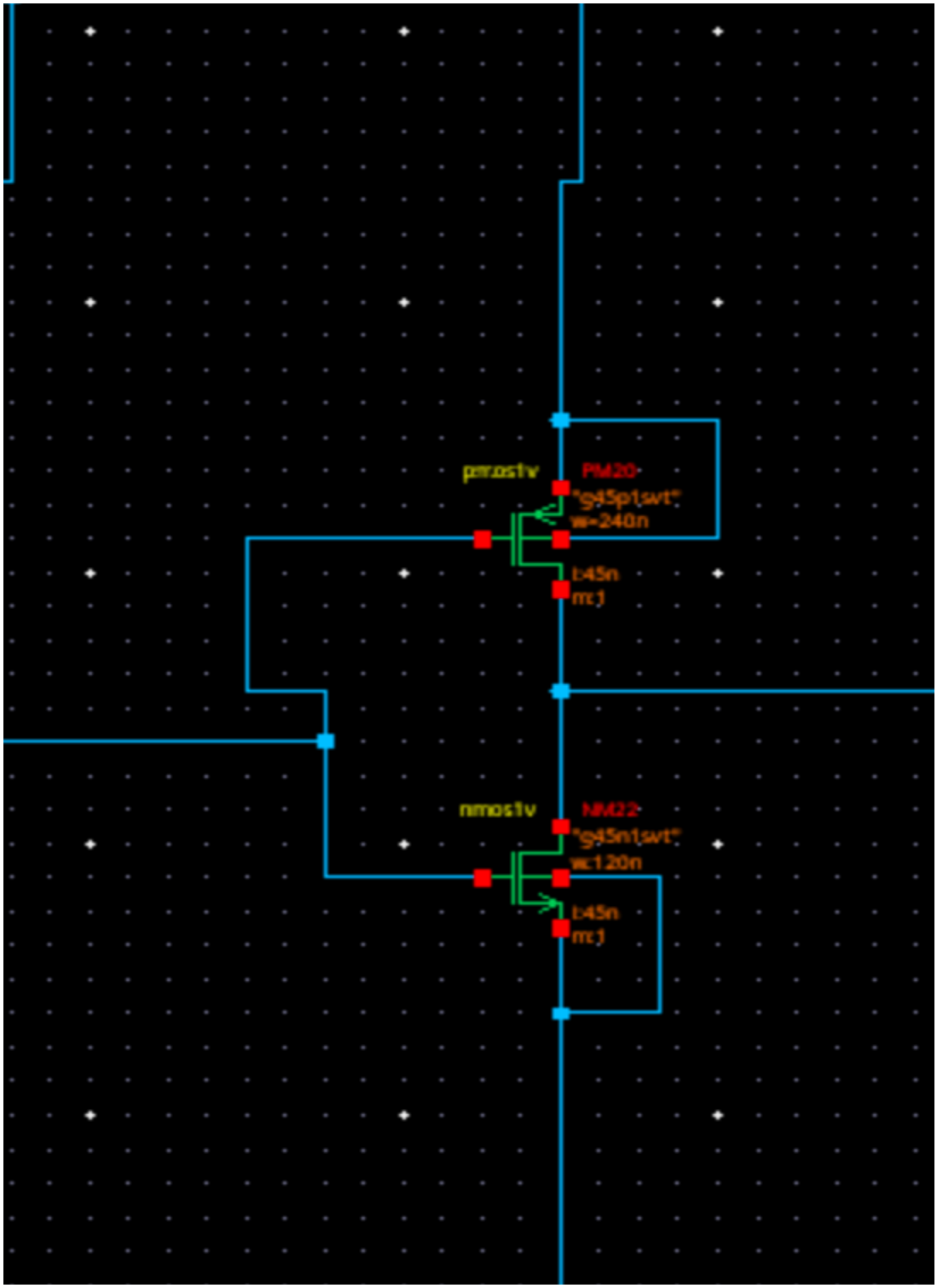
NAND gate


pmos1v
PM28
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM29
"g45p1svt"
w=480n
l=45n
m=1
OUT
nmos1v
NM28
"g45n1svt"
w=120n
l=45n
m=1
nmos1v
NM29
"g45n1svt"
w=120n
l=45n
m=1

NOR GATE

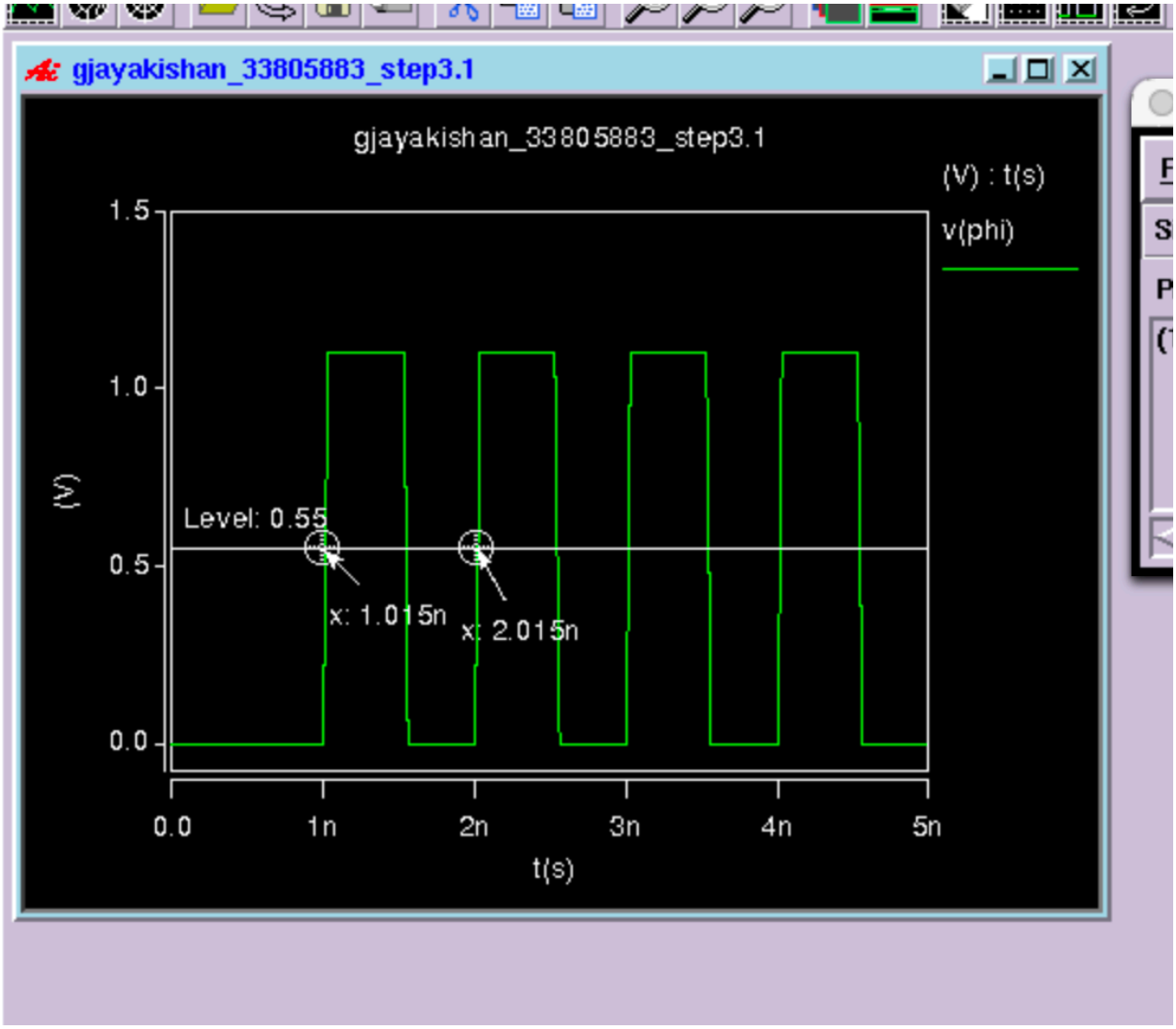

pmos1v
PM22
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM23
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM21
"g45p1svt"
w=480n
l=45n
m=1
pmos1v
PM24
"g45p1svt"
w=480n
l=45n
m=1
nmos1v
NM23
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM25
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM24
"g45n1svt"
w=240n
l=45n
m=1
nmos1v
NM26
"g45n1svt"
w=240n
l=45n
m=1

Latches



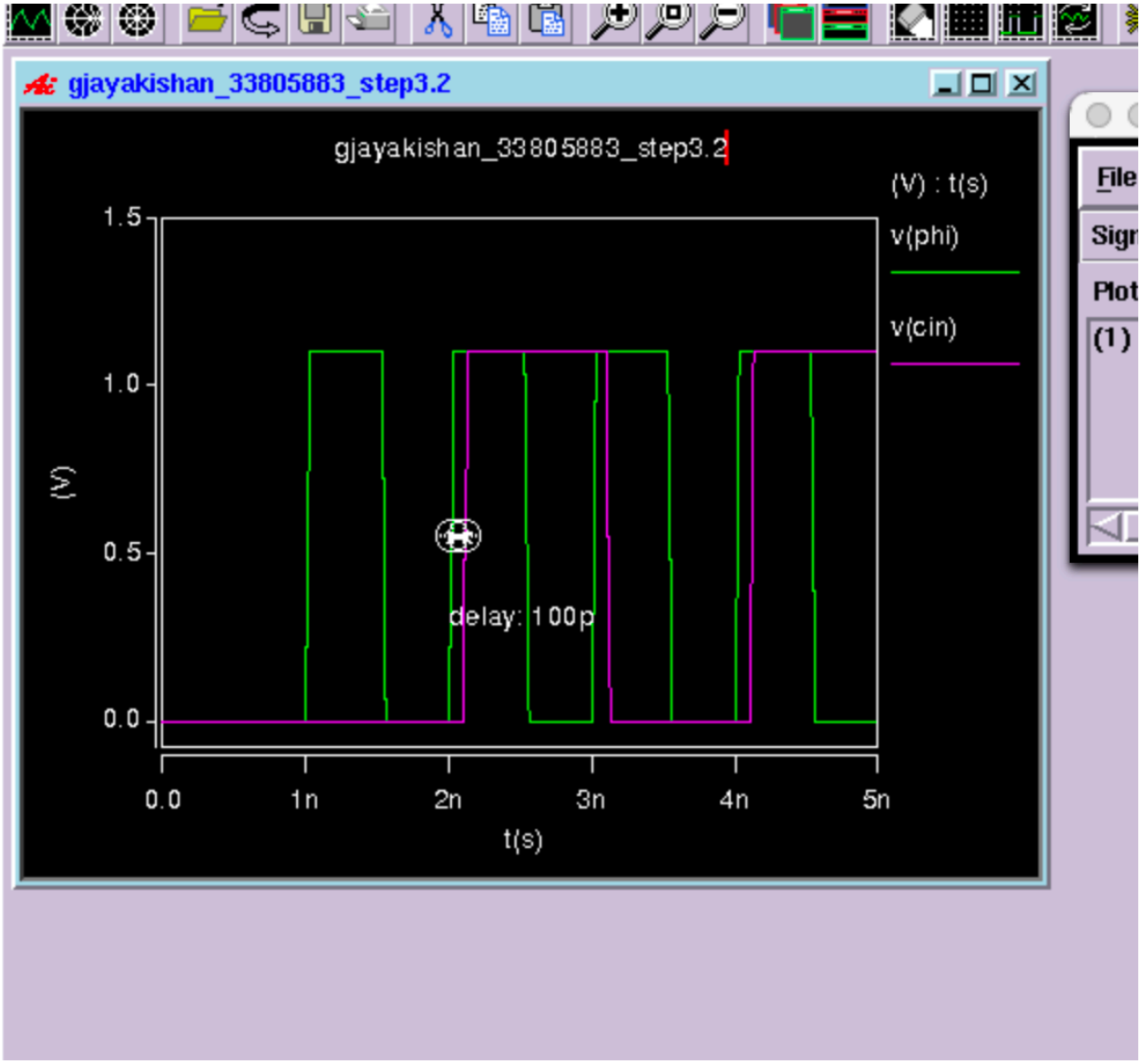
LAST inverter

3.1 Solution

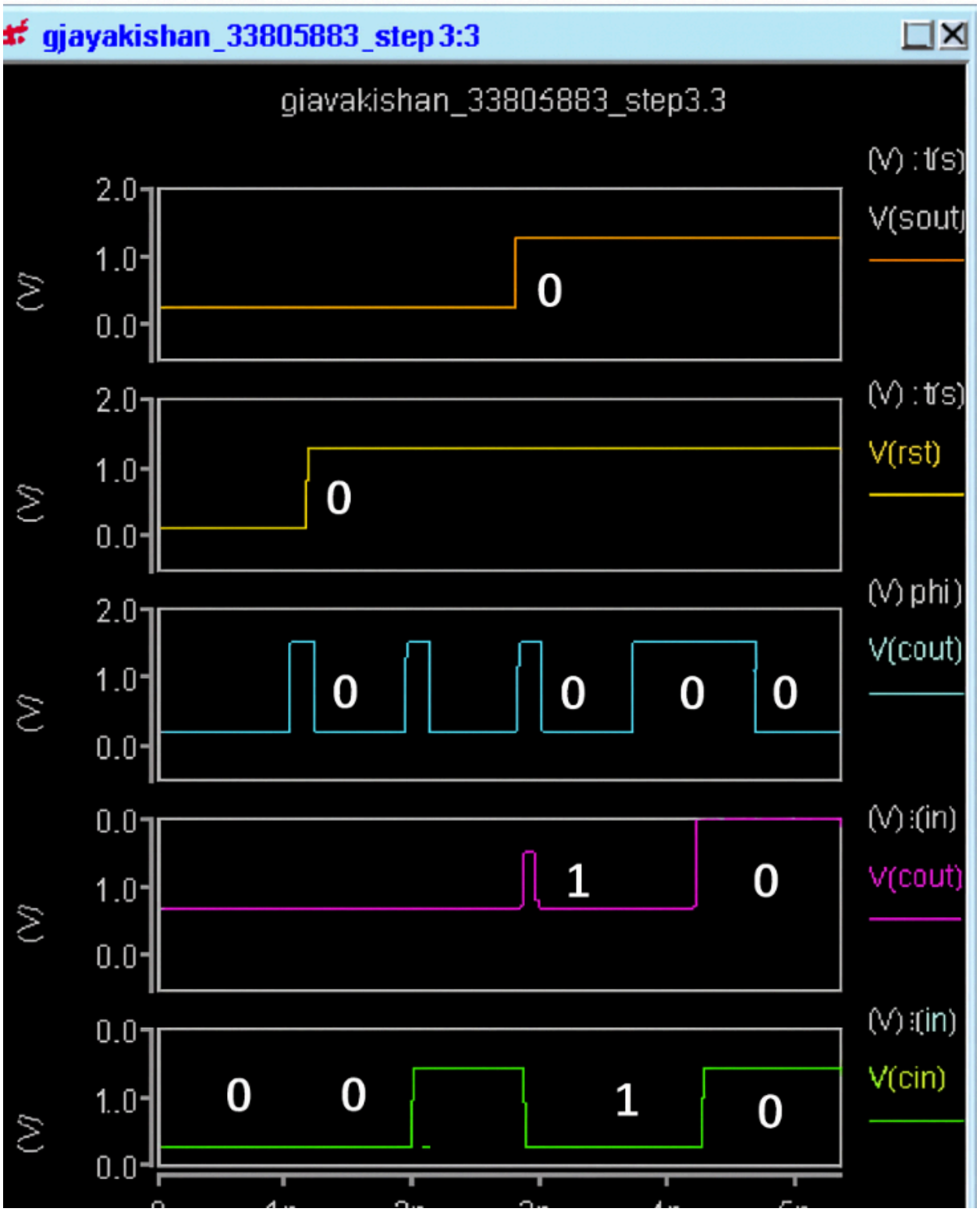


Measured 50% crossing of PHI at 1.015 ns (first rising edge) and 2.015 ns (second rising edge), matching theoretical values for tclk = 1 ns, tr = 30 ps

3.2 Solution

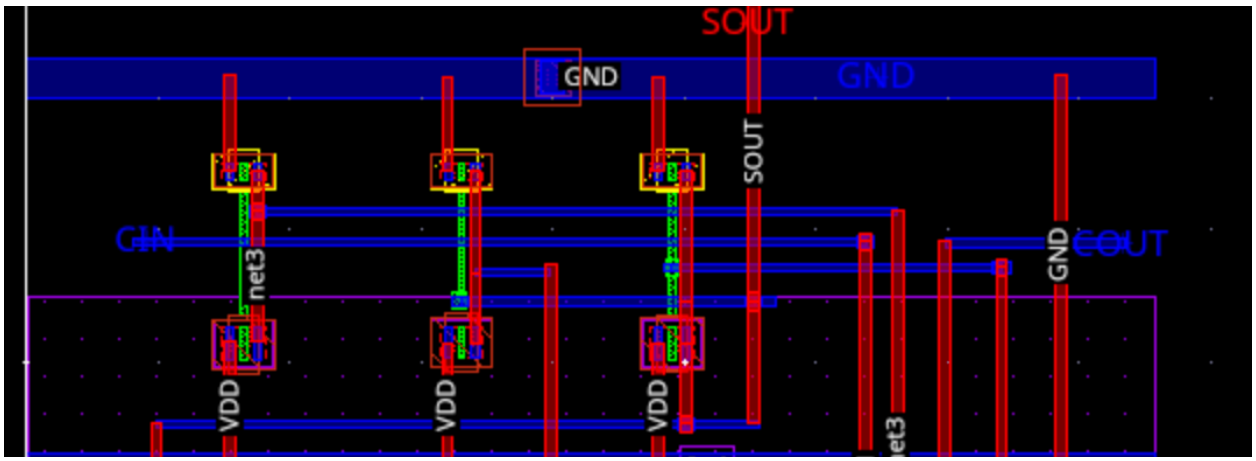

gjayakishan_33805883_step3.2
gjayakishan_33805883_step3.2
(V) : t(s)
v(phi)
v(cin)
1.5
1.0
0.5
0.0
(V)
delay: 100p
0.0
1n
2n
3n
4n
5n
t(s)
File
Sign
Plot
(1)

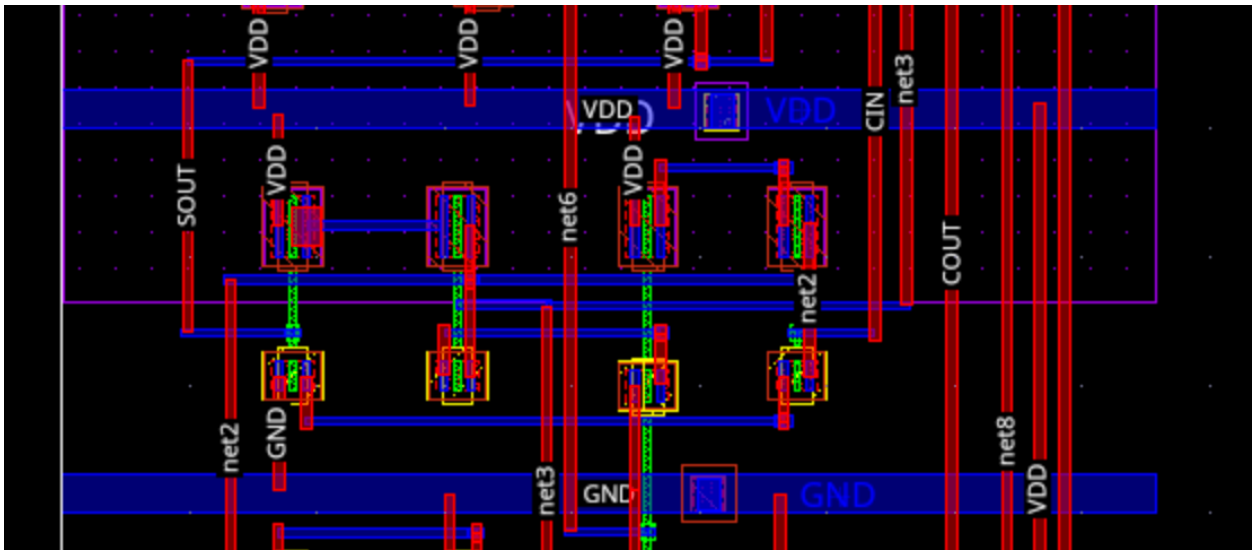
3.3 Solution

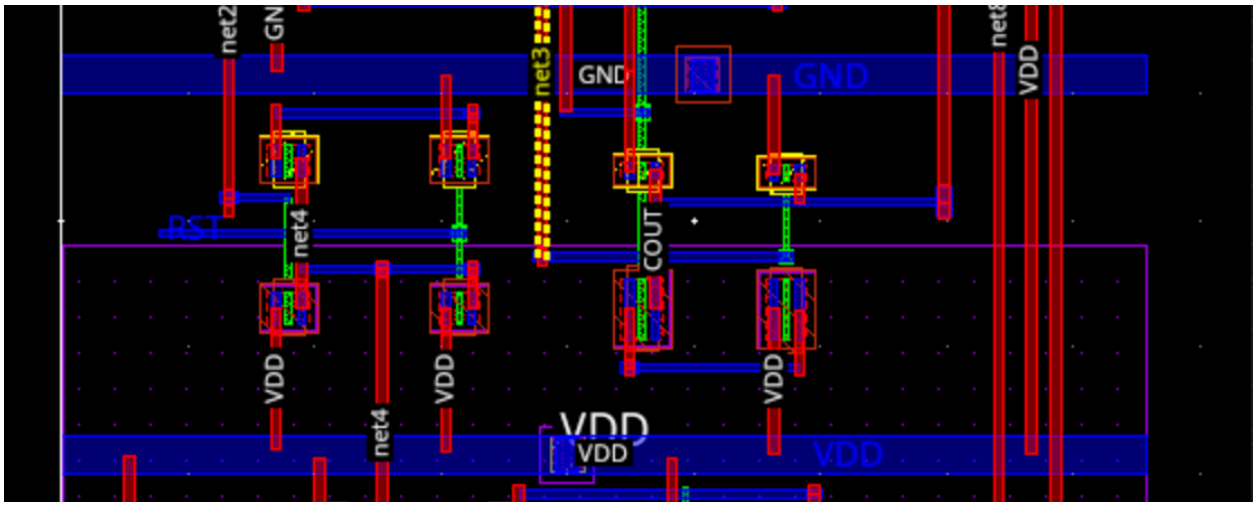

gjayakishan_33805883_step 3:3
giavakishan_33805883_step3.3
(V) : t(s)
V(sout)
2.0
1.0
0.0
(V)
0
(V) : t(s)
V(rst)
2.0
1.0
0.0
(V)
0
(V) phi)
V(cout)
2.0
1.0
0.0
(V)
0
0
0
0
(V) :(in)
V(cout)
0.0
1.0
0.0
(V)
1
0
(V) :(in)
V(cin)
0.0
1.0
0.0
(V)
0
0
1
0

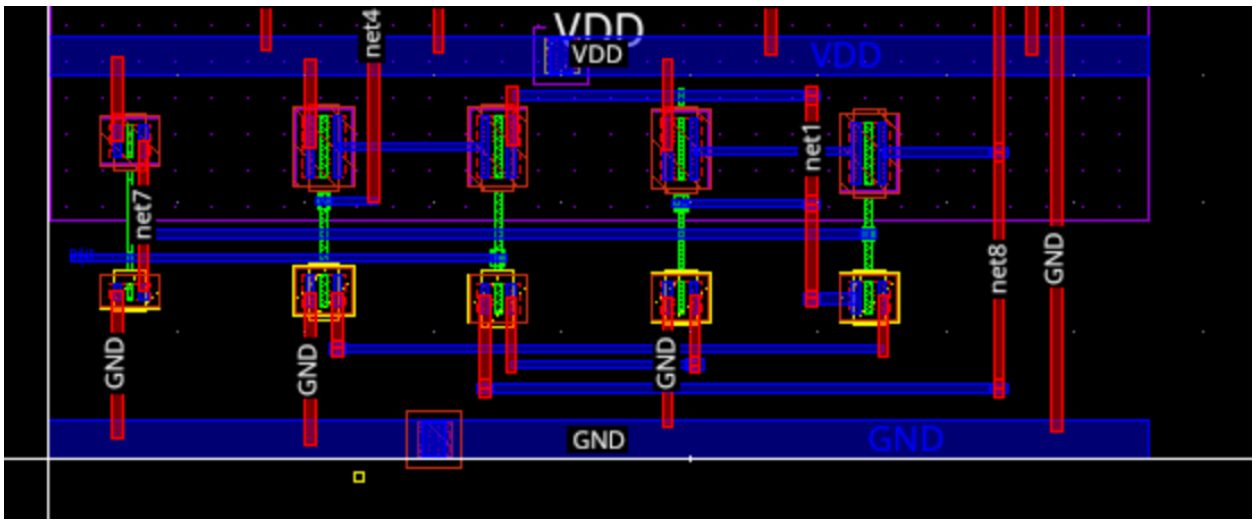
The annotated waveform shows correct operation of the half-adder accumulator bitslice. Each cycle matches the expected truth-table outputs for SOUT and COUT given the applied CIN and RST inputs. Inputs were delayed 100 ps after PHI's rising edge, and PHI has a 1 ns period.

Step 4.1 solution

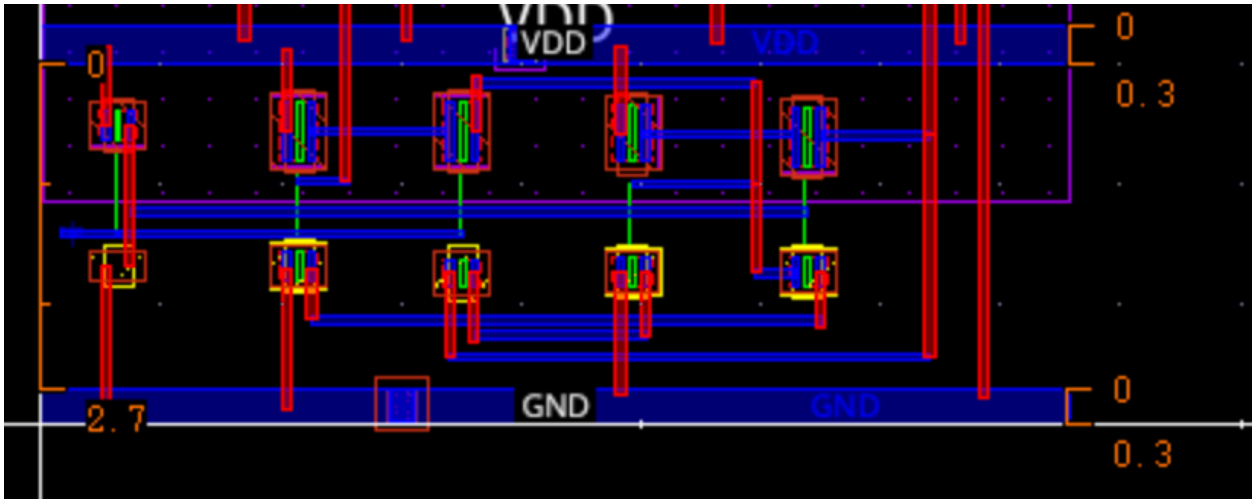



VDD
VDD
VDD
VDD
VDD
VDD
CIN
net3
SOUT
VDD
net6
VDD
net2
COUT
net2
GND
net3
GND
GND
net8
VDD

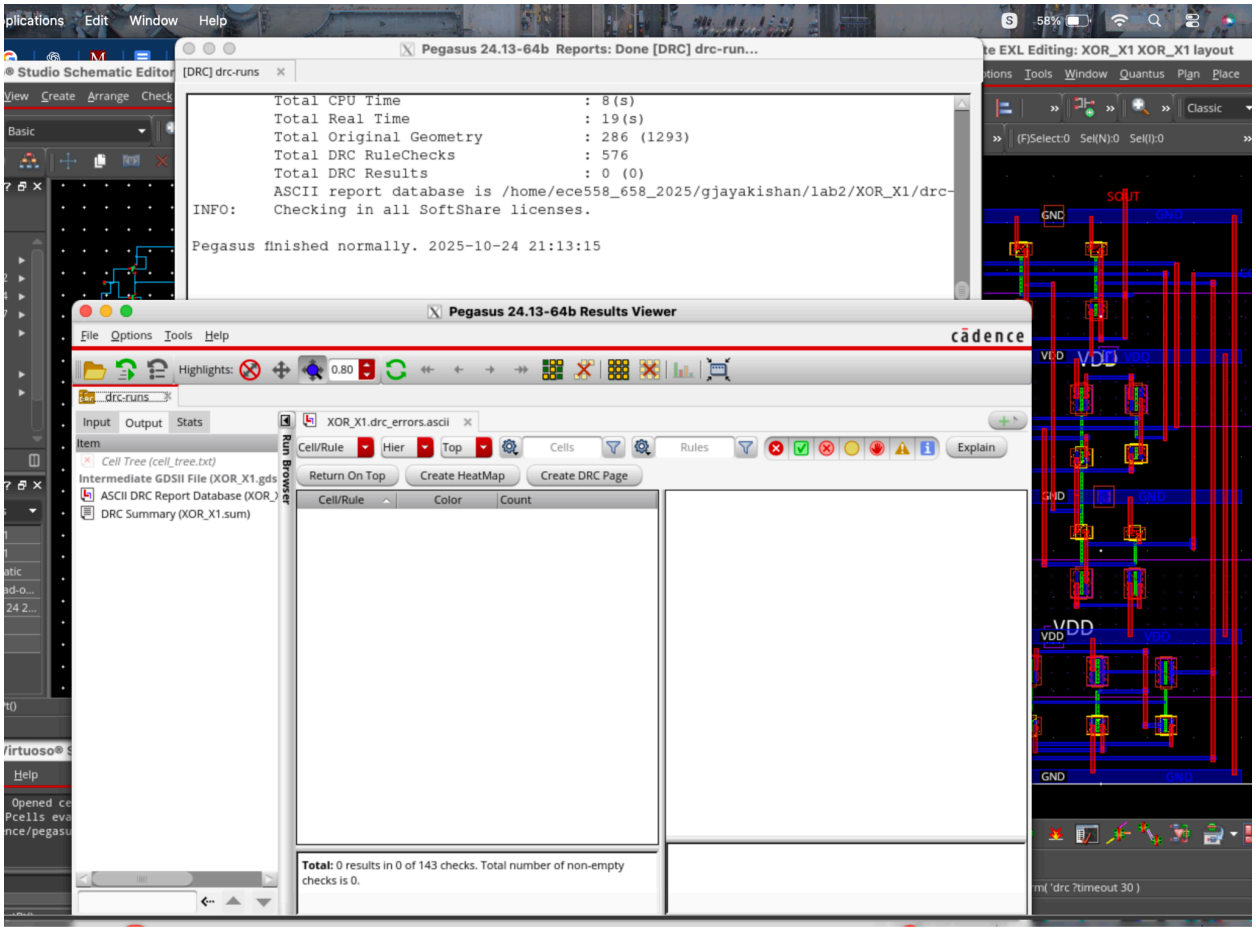

net2
GND
net3
GND
GND
net8
VDD
RST
net4
COUT
VDD
VDD
VDD
net4
VDD
VDD
VDD


net4
VDD
VDD
VDD
net1
net7
net8
GND
GND
GND
GND
GND
GND

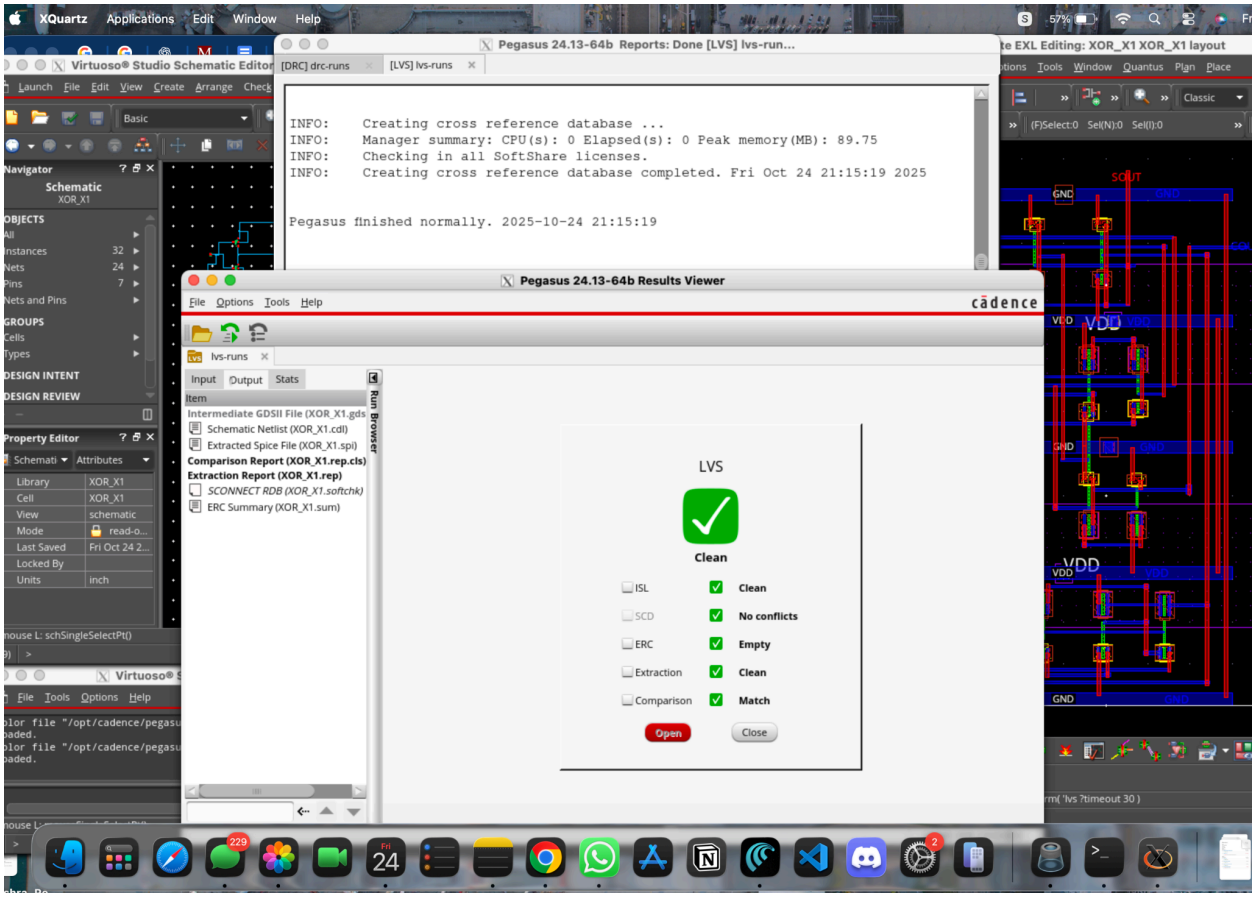
4.2 solution



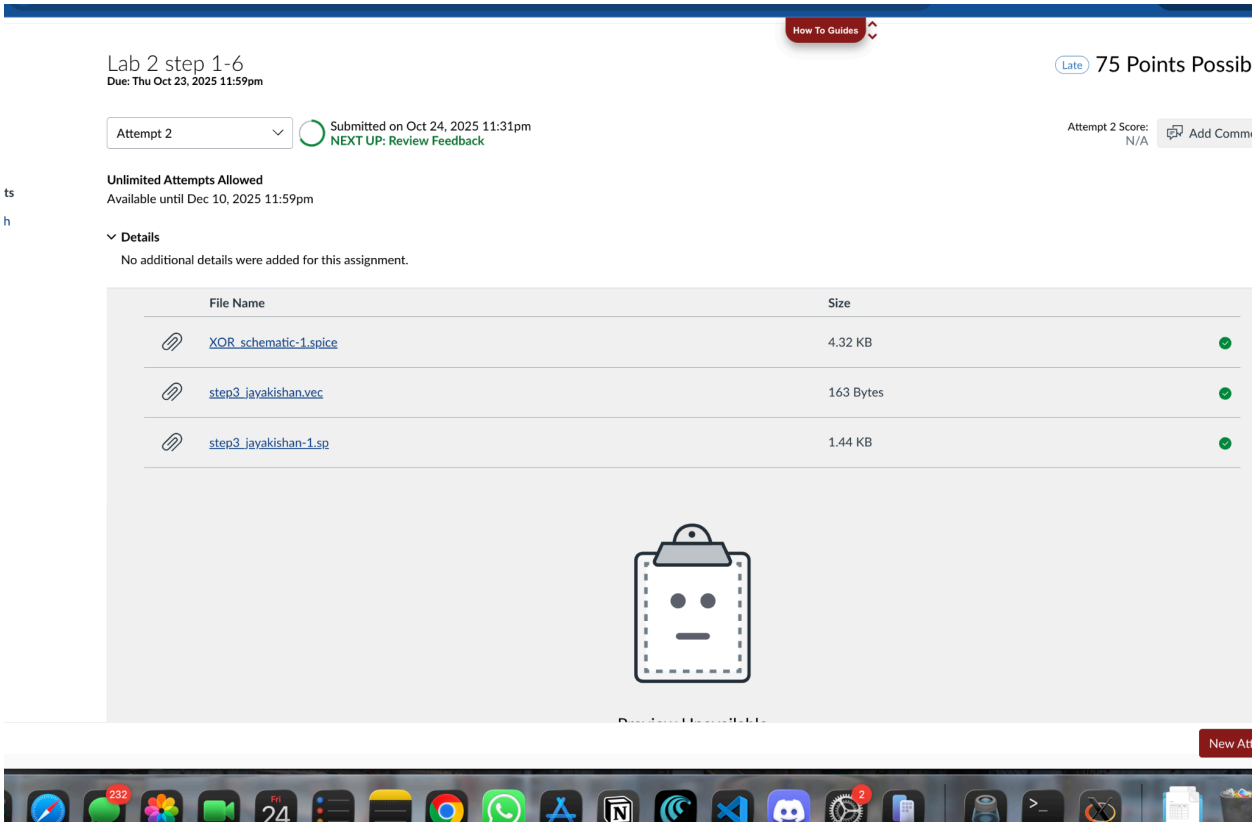
Step 4.3



4.4 solution



4.5 solution



5.1 solution

The purpose of this step was to measure the post-layout average power of the extracted XOR_X1 cell at different clock frequencies and analyze how the power scales with frequency. The extracted netlist used was named XOR_X1-post-layout.sp, whose subcircuit declaration is
“.SUBCKT XOR_X1 CIN COUT GND PHI RST SOUT VDD.”

The transistor models from the gpdk045 process library were included using
“.include '/opt/cadence/gpdk045/gpdk045_v_6_0/models/hspice/g45n1svt.inc'”
and
“.include '/opt/cadence/gpdk045/gpdk045_v_6_0/models/hspice/g45p1svt.inc'.”

All simulations were performed at a supply voltage of 1.1 V and a temperature of 25 °C. The rise and fall times of the input signals were set to 30 ps, with a 100 ps offset between the clock (PHI) and the input transitions. Four transient simulations were carried out for clock frequencies of 500 MHz, 667 MHz, 1 GHz, and 2 GHz.

The measured average powers were 1.064×10^{-5} W at 500 MHz, 1.419×10^{-5} W at 667 MHz, 2.112×10^{-5} W at 1 GHz, and 4.187×10^{-5} W at 2 GHz. The results show a nearly linear increase in power with frequency, indicating that dynamic switching power dominates total consumption in this CMOS design.

5.2 solution

The total power of the circuit can be modeled as a linear function of frequency:

$P(f) = P_{static} + k f$

where P_{static} represents the leakage (static) power and k is the dynamic power coefficient. Using the 500 MHz and 2 GHz results,

$k = (P_2 - P_1) / (f_2 - f_1) = (4.187\times10^{-5} - 1.064\times10^{-5}) / (2.0\times10^{9} - 5.0\times10^{8}) = 2.08\times10^{-14}$ W/Hz.

The static power was then obtained as

$P_{static} = P_1 - k f_1 = 1.064\times10^{-5} - (2.08\times10^{-14})(5.0\times10^{8}) = 2.3\times10^{-7}$ W.

Thus, the fitted power-frequency equation becomes

$P(f) = 2.3\times10^{-7} + (2.08\times10^{-14}) f$.

The slope k represents the dynamic switching component of power, while the intercept corresponds to static leakage power of about 0.23 μW. The model fits the measured data almost perfectly, confirming the expected linear relationship between power and frequency in CMOS logic.

5.3 solution

The frequency at which static power equals ten percent of the total power can be found from the relationship

$P_{static} = 0.1 (P_{static} + k f)$,

which simplifies to $f = 9 P_{static} / k$. Substituting the calculated values gives

$f = 9 (2.3\times10^{-7}) / (2.08\times10^{-14}) = 9.9\times10^{7}$ Hz ≈ 100 MHz.

At approximately 100 MHz, static leakage power contributes about ten percent of the total power. Beyond this frequency, dynamic switching power overwhelmingly

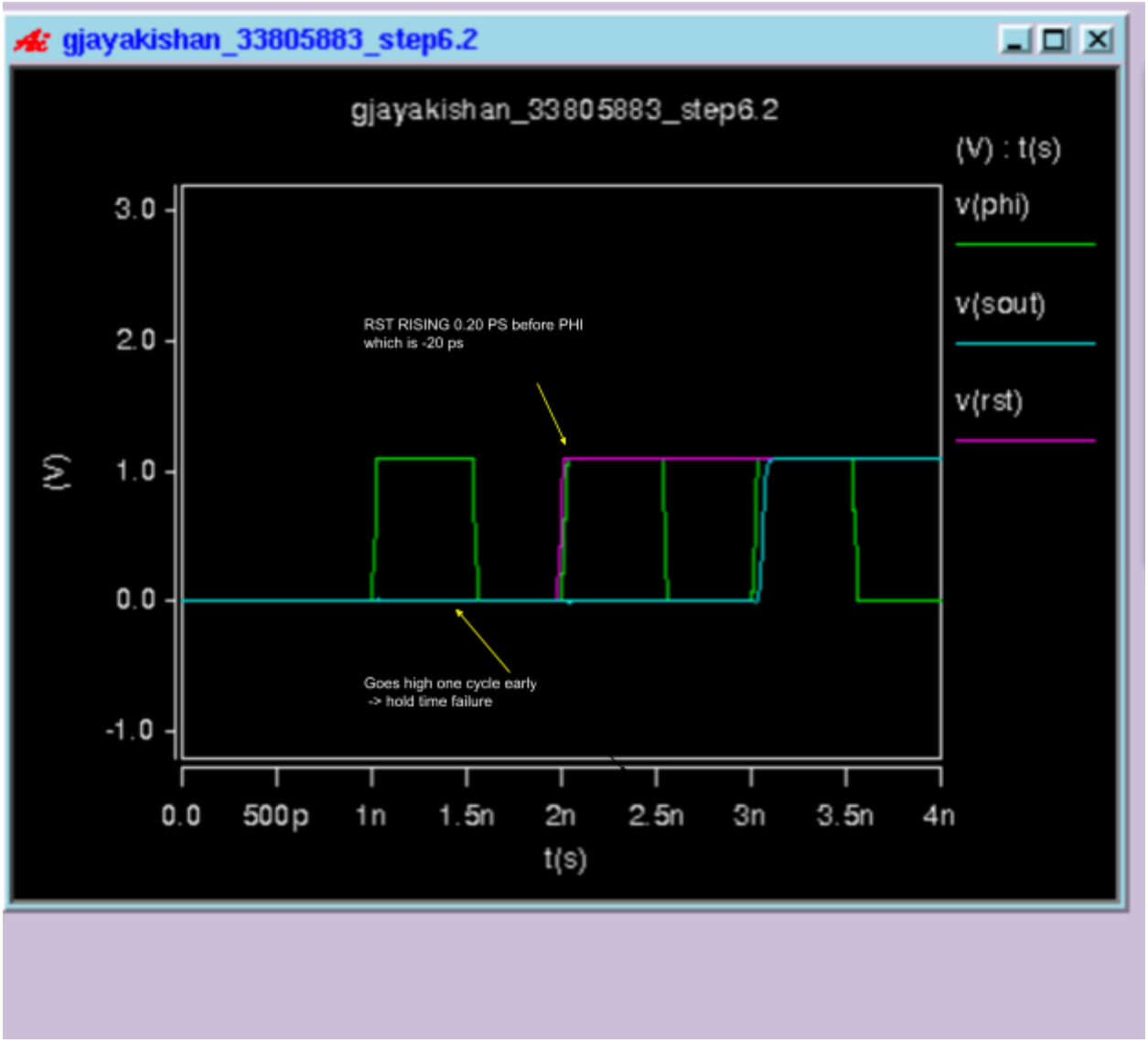
dominates, which is consistent with the expected behavior of a 45 nm CMOS circuit operating at nominal voltage.

In summary, the post-layout power analysis of the XOR_X1 cell demonstrates a clear linear scaling of average power with clock frequency. The static power is about 2.3×10^{-7} W, the dynamic coefficient k is 2.08×10^{-14} W/Hz, and the crossover frequency where static power contributes ten percent of total power is around 100 MHz. At higher frequencies, total power is almost entirely dynamic, confirming typical CMOS operation.

6.1 solution

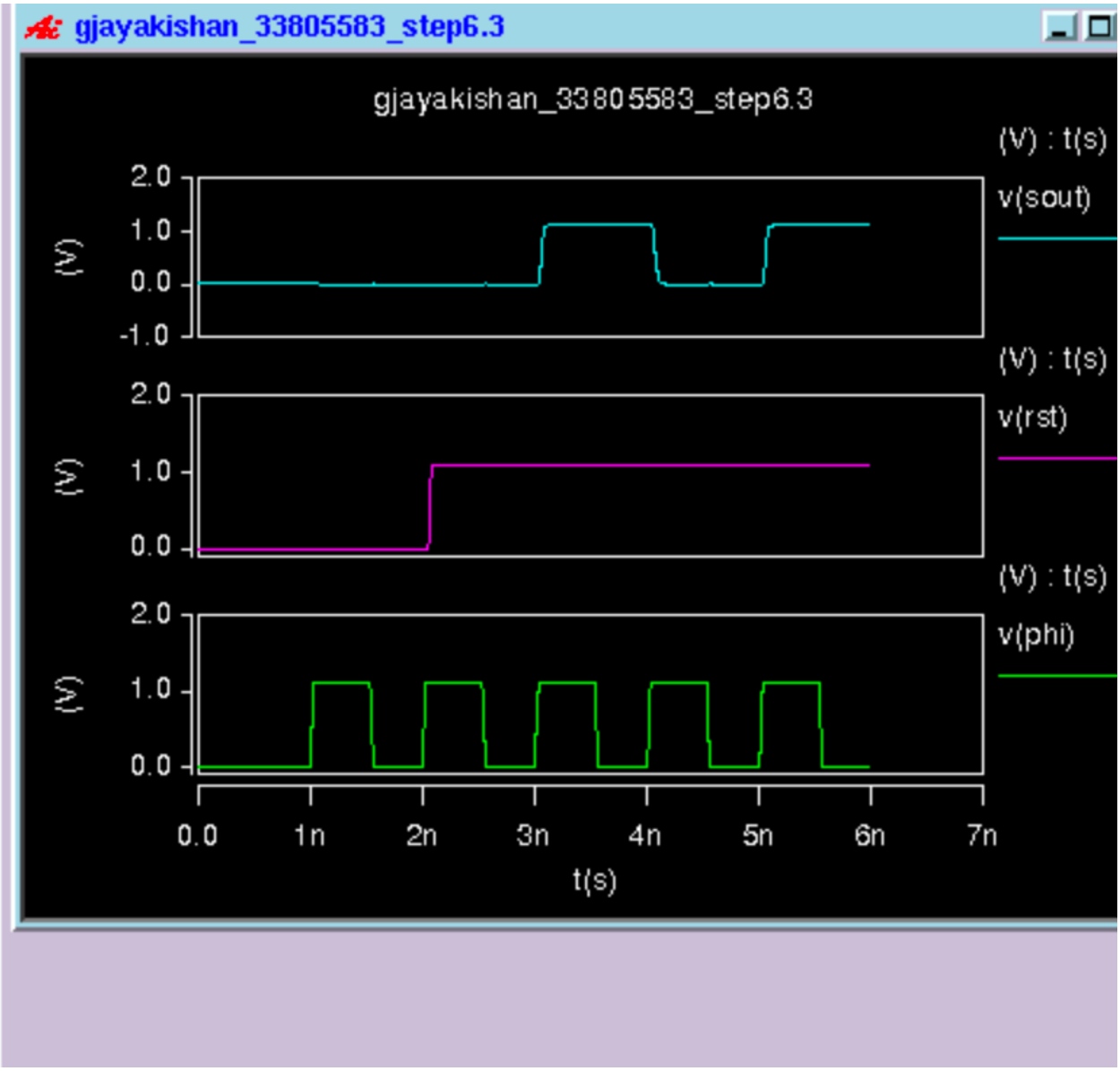
To check for hold-time failures, I varied the timing of the RST signal relative to the rising edge of the clock (PHI). Using the extracted netlist, RST was defined as a PWL source so its rising edge could be shifted earlier or later. When RST rose too soon, the stored output (SOUT) changed one cycle early, indicating a hold-time violation. I measured the timing offset between RST and PHI (50 % point) using an HSPICE `.meas` command

6.2 solution



When RST rose 20 ps before PHI (Δt = –20 ps), SOUT went high one cycle too early, showing a clear hold-time failure. The waveform confirms this: the RST (purple) edge precedes PHI (green), and SOUT (cyan) switches prematurely. The measured offset of –20 ps marks the violation.

Solution 6.3



Delaying RST by +10 ps relative to PHI removes the failure. RST now rises slightly after PHI, and SOUT stays stable until the next valid cycle. The waveform shows normal behavior: no premature switching and correct data storage.