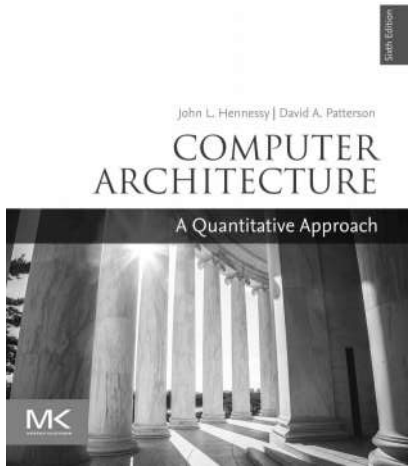
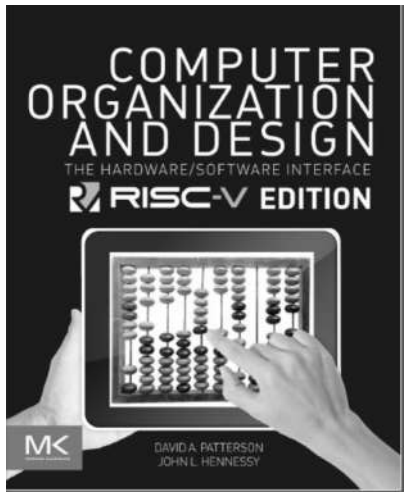
Textbook/reference books



John L. Hennessy, David A. Patternson; Computer Architecture: A Quantitative Approach; sixth Edition.



David A. Patternson, John L. Hennessy ; Computer Organization and Design- The Hardware/Software Interface; RISC-V Edition.

Computer Architecture

Textbook/reference books

John L. Hennessy, David A. Patternson; Computer Architecture: A Quantitative Approach. Fifth Edition. 机械工业出版社，2012

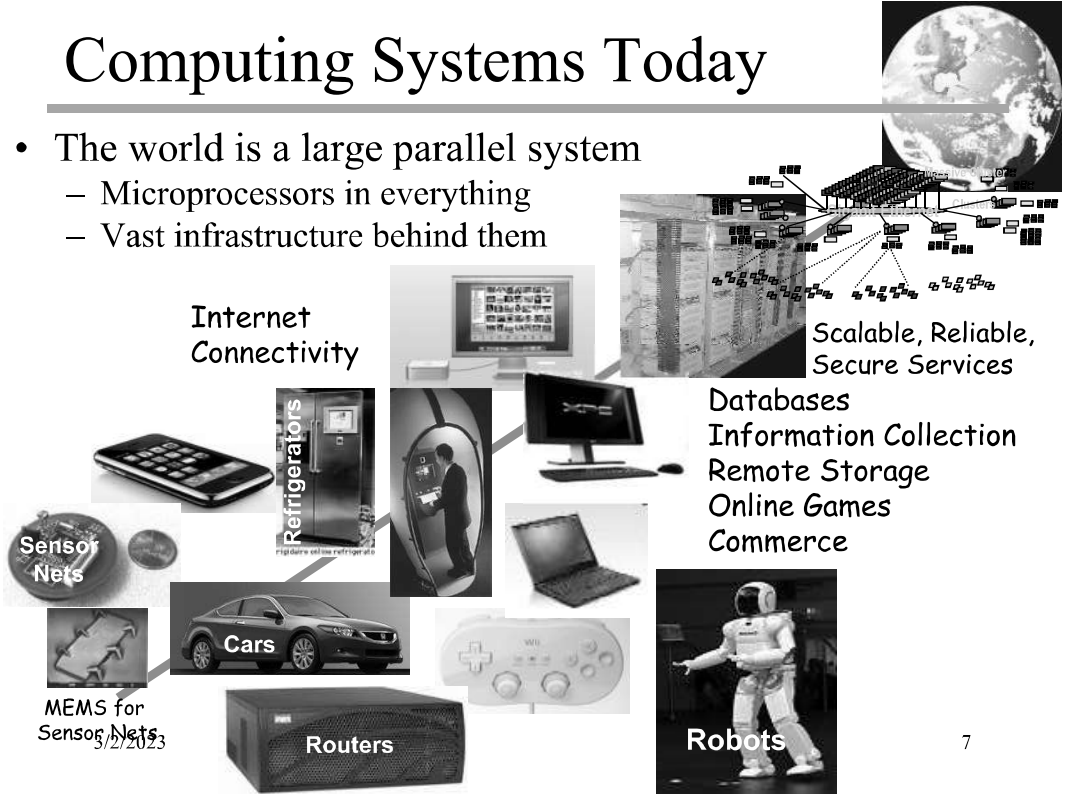
David A. Patternson, John L. Hennessy, Computer Organization & Design : The Hardware/Software Interface, Third Edition. San Francisco: Morgan Kaufmann Publishers, Inc. 2005

Computer Architecture: Course introduction

- Course code:TMP2771
- Credit hours: 32
- Credit: 2.0
- Assessment and evaluation methods:
  - –classroom performance 30%， exam 70%
- Background: Computer Organization or equivalent, based on Hennessy and Patterson's Computer Organization and Design
- Textbook/reference books: Hennessy and Patterson's Computer Architecture, A Quantitative Approach, 5th or 6th Edition

Computing Systems Today

- The world is a large parallel system
  - Microprocessors in everything
  - Vast infrastructure behind them

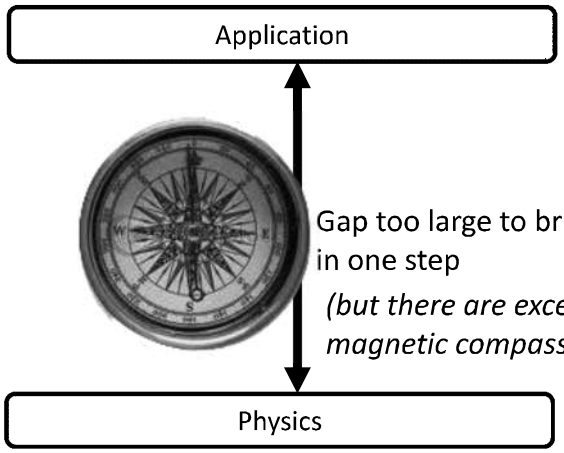


Syllabus

- Computer architecture is an aspect of computer systems from outside

- Objectives:
  - –Build a complete concept of computer systems (from outside/users)
  - –Learn analysis and design methods of the computer system
  - –Master basic structure and principle of new computer systems

What is Computer Architecture?

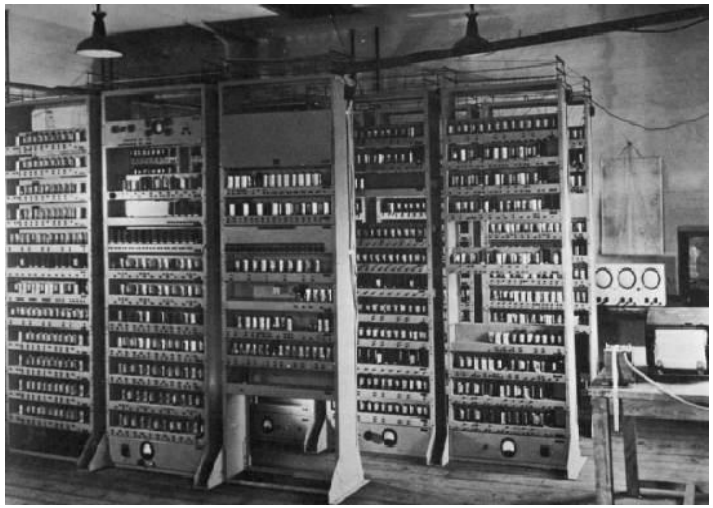


Gap too large to bridge in one step

(but there are exceptions, e.g. magnetic compass)

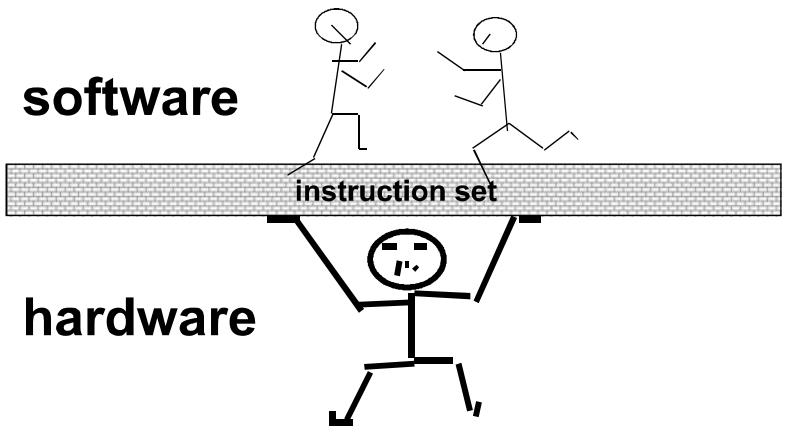
广义的定义：计算机体系结构是抽象层的设计，这些抽象层使得我们可以使用可用的制造技术高效地实现信息处理应用系统

Computing Devices Then…

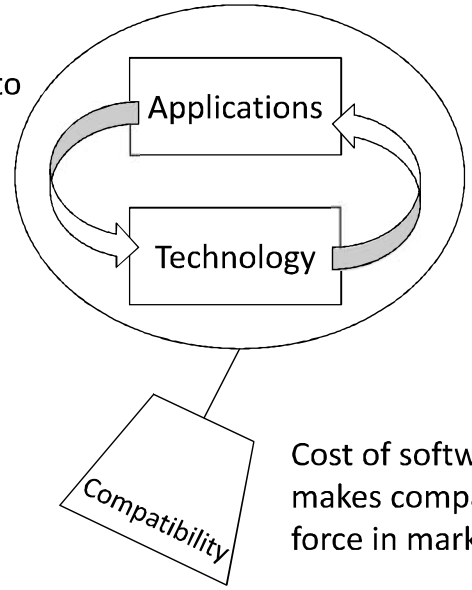


EDSAC, University of Cambridge, UK, 1949

ISA: a Critical Interface



Applications suggest how to improve technology, provide revenue to fund development



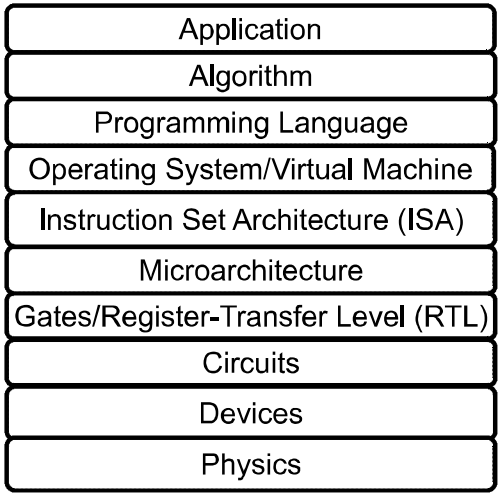
Improved technologies make new applications possible

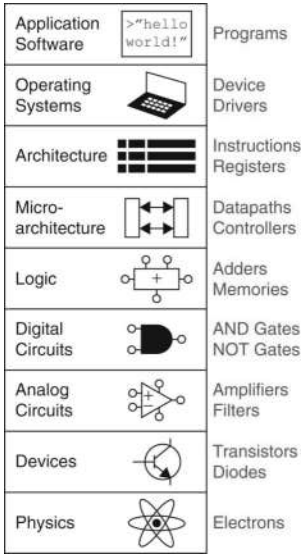
Cost of software development makes compatibility a major force in market

ISA

- Memory addressing
- Addressing modes
- Types and sizes of operands
- Operations
- Control flow instructions
- Encoding an ISA
- ……

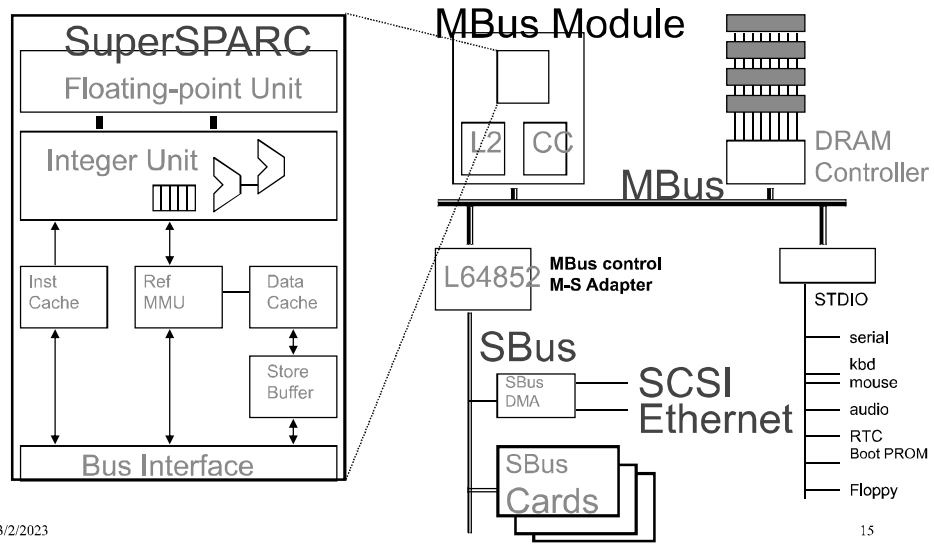
What is Computer Architecture?





Example Organization

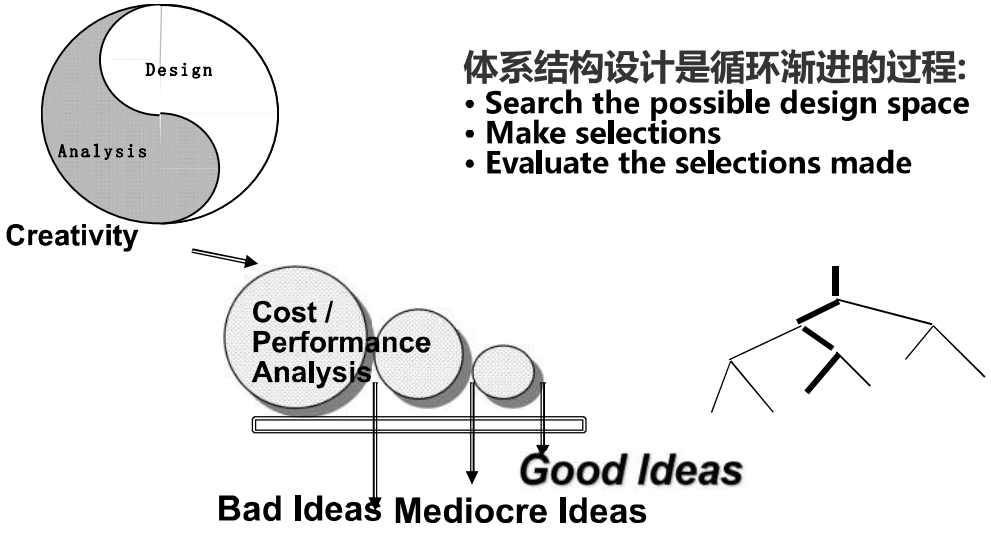
- TI SuperSPARC^{tm} TMS390Z50 in Sun SPARCstation20



ISA examples

- Digital Alpha(v1, v3) 1992-97
- HP PA-RISC (v1.1, v2.0) 1986-96
- Sun Sparc(v8, v9) 1987-95
- SGI MIPS (MIPS I, II, III, IV, V) 1986-96
- Intel(8086,80286,80386, 1978-96
  80486,Pentium, MMX, ...)

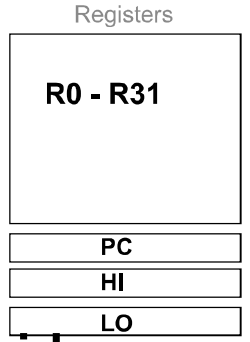
Design flow



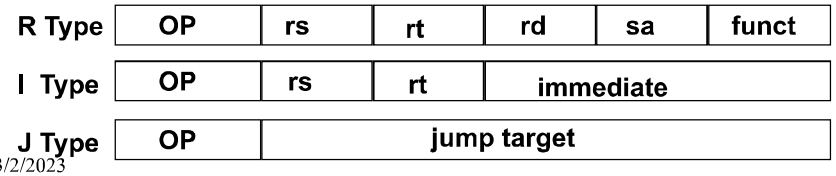
Good measurement tools are required to accurately evaluate the selection.

MIPS R3000 Instruction Set Architecture

- Instruction types
  - Load/Store
  - Computational
  - Jump and Branch
  - Floating Point
    - coprocessor
  - Memory Management
  - Special



All instructions 32 bits wide

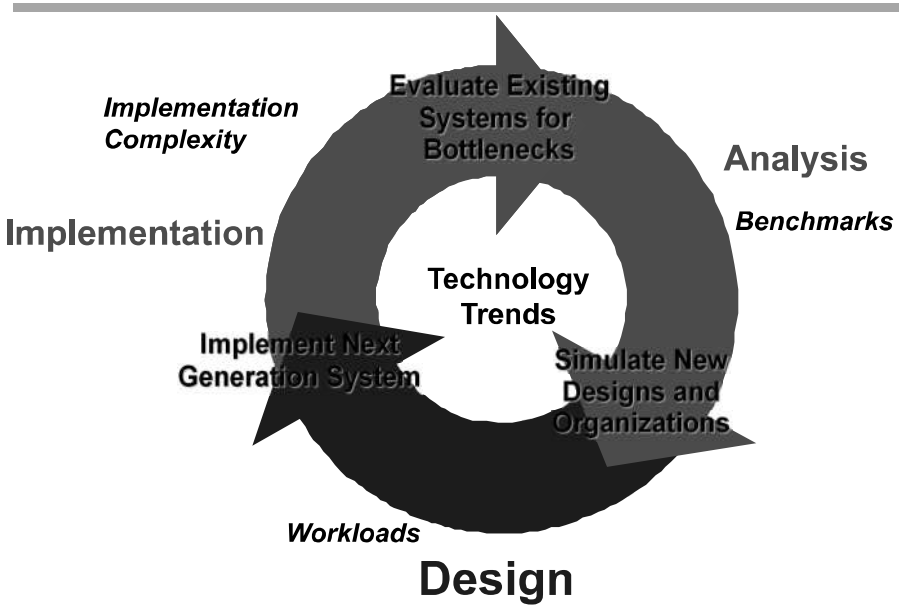


IBM 360 series machines

Model	M30	M40	M50	M65
Datapath width	8 bits	16 bits	32 bits	64 bits
Microcode size	4k x 50	4k x 52	2.75k x 85	2.75k x 87
Clock cycle time (ROM)	750 ns	625 ns	500 ns	200 ns
Main memory cycle time	1500 ns	2500 ns	2000 ns	750 ns
Price (1964 $)	$192,000	$216,000	$460,000	$1,080,000
Price (2018 $)	$1,560,000	$1,760,000	$3,720,000	$8,720,000

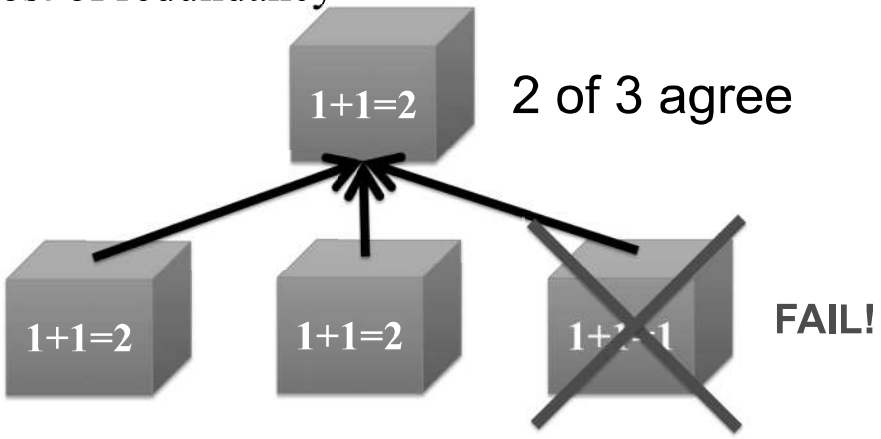
Fred Brooks, Jr.

Design Methodologie



Dependability via Redundancy

- Increasing transistor density reduces the cost of redundancy



Technology trends

- History
  - Mainframes,
  - Minicomputers,
  - Microprocessors
  - RISC vs CISC，VLIW
- Challenges
  - Denard Scaling, Moore's Law
  - Security
- Opportunity
  - Open Architectures
  - Domain Specific Languages and Architecture
  - Agile Hardware Development

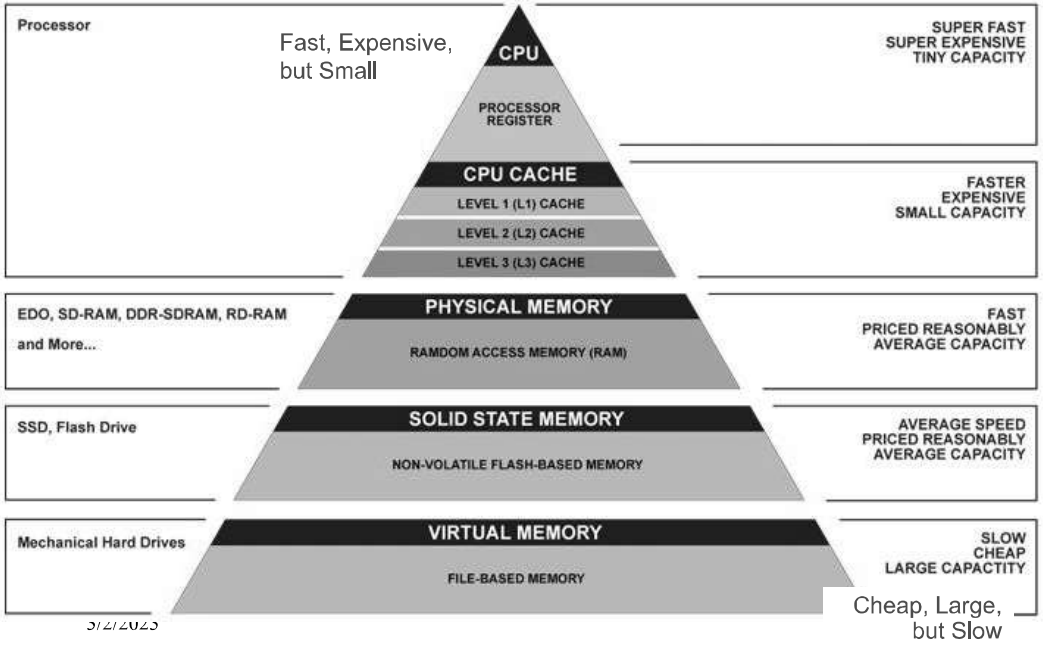
*A New Golden Age for Computer Architecture: Domain-Specific Hardware/Software Co-Design, Enhanced Security, Open Instruction Sets, and Agile Chip Development

John Hennessy and David Patterson
June 4, 2018

New "Great Ideas"

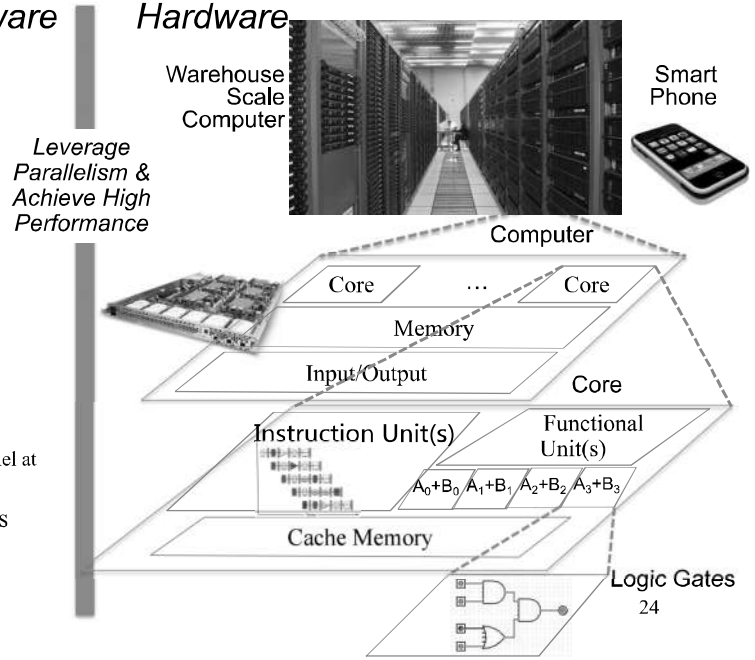
Personal Mobile Devices

Memory Hierarchy

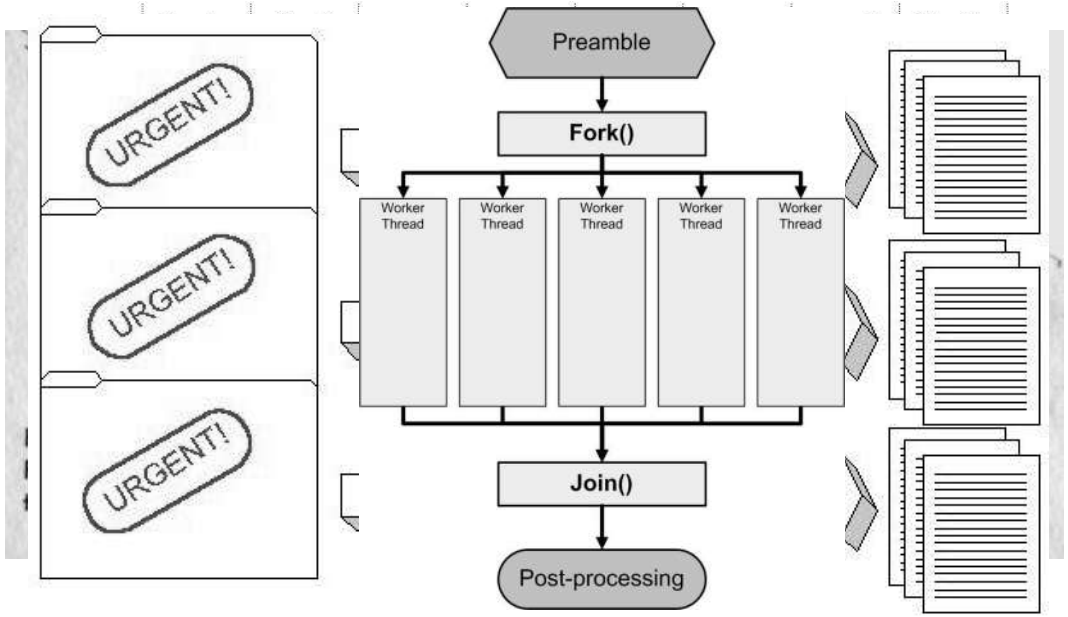


New "Great Ideas"

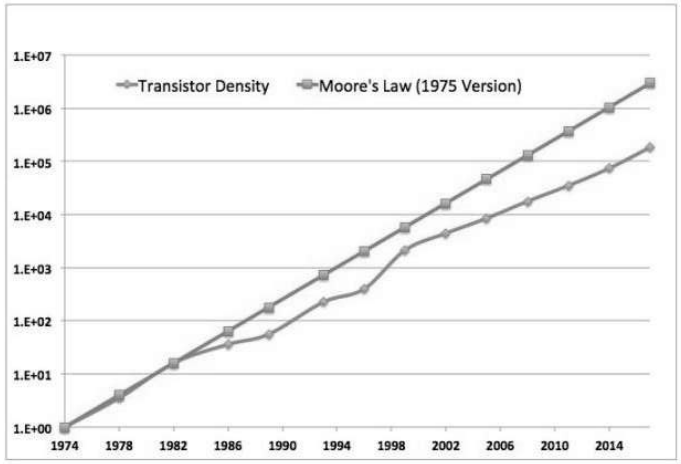
- Parallel Requests
  Assigned to computer
  e.g., Search "PingPang"
- Parallel Threads
  Assigned to core
  e.g., Lookup, Ads
- Parallel Instructions
  >1 instruction @ one time
  e.g., 5 pipelined instructions
- Parallel Data
  >1 data item @ one time
  e.g., Add of 4 pairs of words
- Hardware Descriptions
  All gates functioning in parallel at same time
- Programming Languages



Parallelism/Pipelining/Prediction



Moore's Law Slowdown in Intel Processors

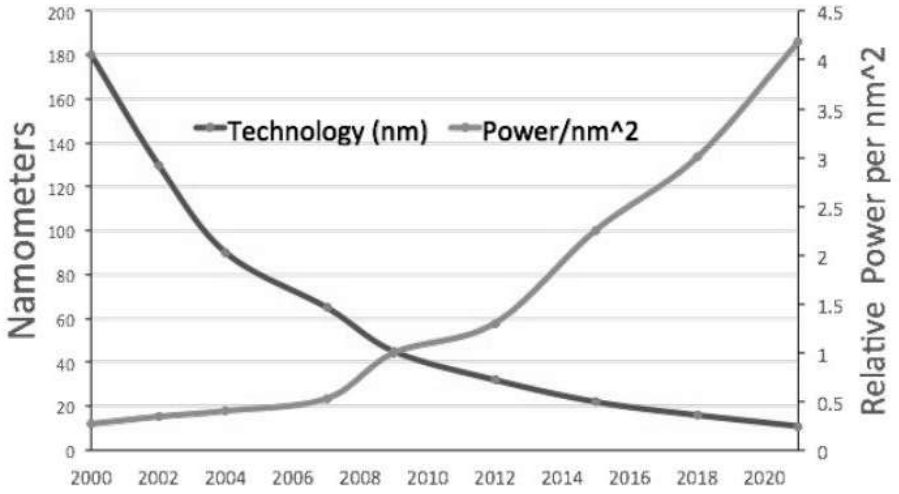


Cost of downtime

Application	Cost of downtime per hour	Annual losses with downtime of 1% (87.6 h/year)	0.5% (43.8 h/year)	0.1% (8.8 h/year)
Brokerage service	$4,000,000	$350,400,000	$175,200,000	$35,000,000
Energy	$1,750,000	$153,300,000	$76,700,000	$15,300,000
Telecom	$1,250,000	$109,500,000	$54,800,000	$11,000,000
Manufacturing	$1,000,000	$87,600,000	$43,800,000	$8,800,000
Retail	$650,000	$56,900,000	$28,500,000	$5,700,000
Health care	$400,000	$35,000,000	$17,500,000	$3,500,000
Media	$50,000	$4,400,000	$2,200,000	$400,000

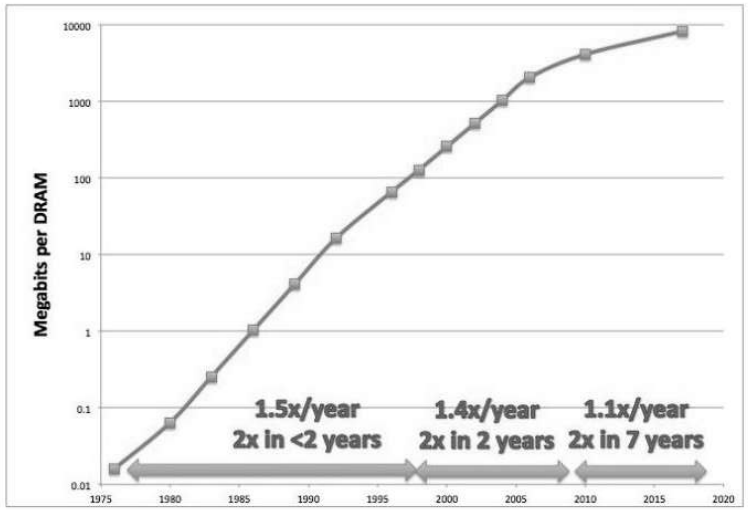
Figure 1.3 Costs rounded to nearest $100,000 of an unavailable system are shown by analyzing the cost of downtime (in terms of immediately lost revenue), assuming three different levels of availability, and that downtime is distributed uniformly. These data are from Landstrom (2014) and were collected and analyzed by Contingency Planning Research.

Technology & Power: Dennard Scaling

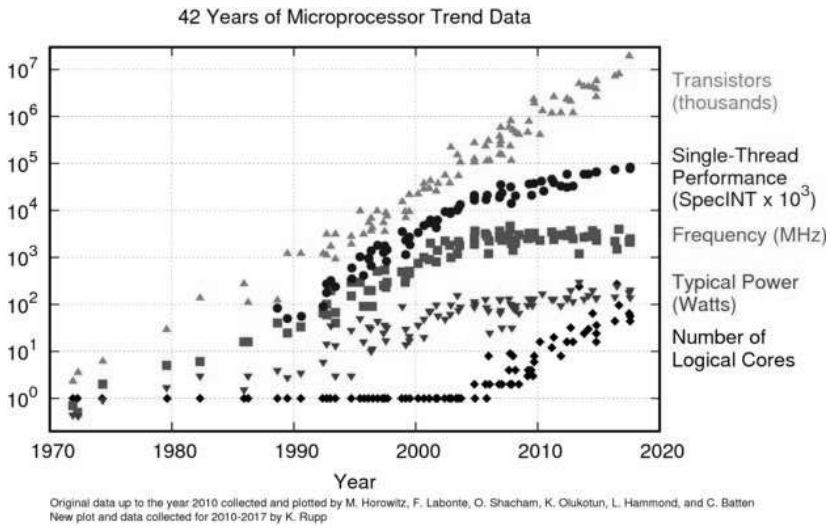


Energy scaling for fixed task is better, since more and faster transistors

Moore's Law in DRAMs



Microprocessor Performance



Source: karlrupp.net

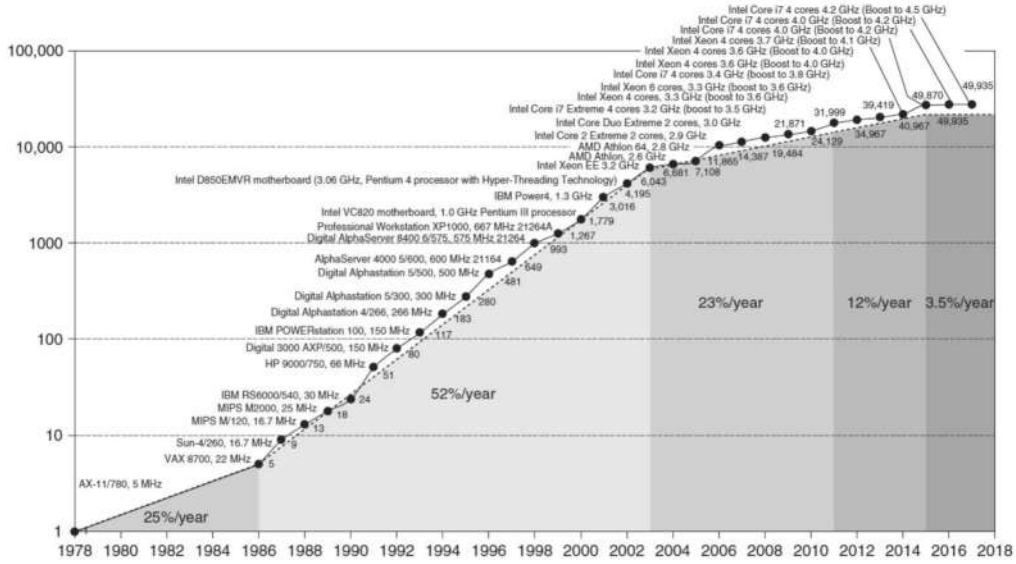
Performance improvements

- Improvements in semiconductor technology
- Feature size, clock speed
- Improvements in computer architectures
- Enabled by High Level Language compilers, UNIX
- Lead to RISC architectures

Processor Technology Trends

- Transistor density increases by 35% per year and die size increases by 10-20% per year… more functionality
- Transistor speed improves linearly with size (complex equation involving voltages, resistances, capacitances)
- Wire delays do not scale down at the same rate as logic delays
- The power wall: it is not possible(not impossible?) to consistently run at higher frequencies without hitting power/thermal limits; fancy cooling required beyond ~150W

Single Processor Performance



Source: H&P textbook

Power Impact

- Dynamic Power proportional to activity x C x V^2 x f
- Power wall: fancy cooling required beyond ~150W
- Increasing frequency led to power wall in early 2000s
- Frequency has stagnated since then
- End of voltage (Dennard) scaling in early 2010s
- Has led to dark silicon and dim silicon (occasional turbo)

What Helps Performance?

- In a clock cycle, can do more work -- since transistors are faster, transistors are more energy-efficient, and there's more of them
- Better architectures: finding more parallelism in one thread, better branch prediction, better cache policies, better memory organizations, more thread-level parallelism, moving computations to memory, accelerating some kernels, …

Performance Stagnation(停滞)

- Running out of ideas to improve single thread performance
- Power wall makes it harder to add complex features
- Power wall makes it harder to increase frequency
- Transistor count will stagnate shortly
- Additional performance provided by: more cores, occasional spikes in frequency, accelerators

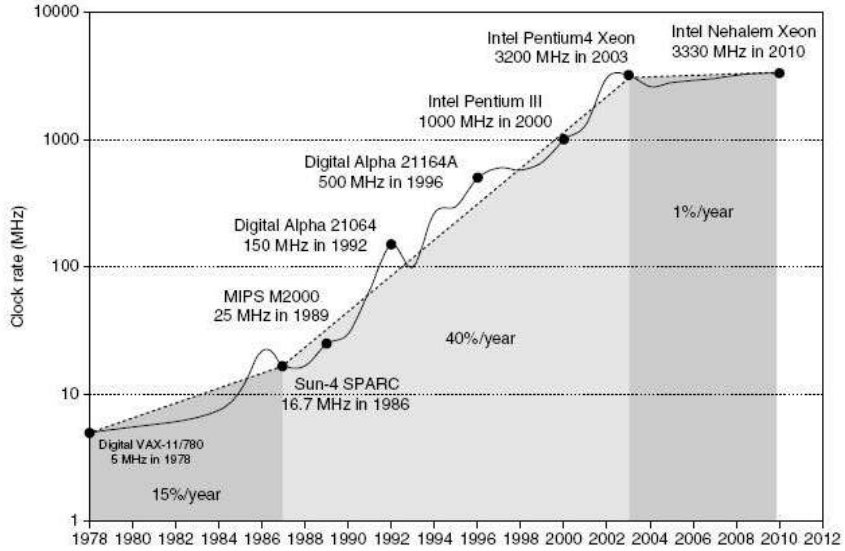
Points to Note

- The 52% growth per year is because of faster clock speeds and architectural innovations (led to 25x higher speed)
- Clock speed increases have dropped to 1% per year in recent years
- The 22% growth includes the parallelization from multiple cores
- Moore's Law: transistors on a chip double every 18-24 months

More Diverse Platforms

Image credits: uber, extremetech, anandtech

Clock Speed Increases



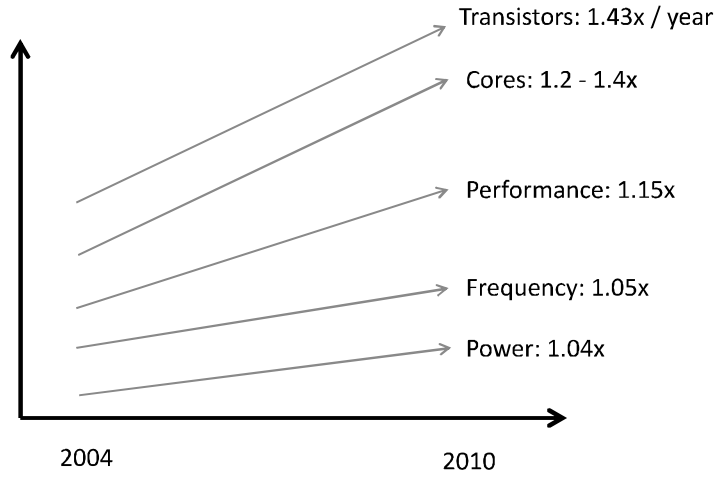
Source: H&P textbook

Where Are We Headed?

Modern trends:

- Clock speed improvements are slowing (power constraints)
- Difficult to further optimize a single core for performance
- Multi-cores: each new processor generation will accommodate more cores
- Need better programming models and efficient execution for multi-threaded applications
- Need better memory hierarchies
- Need greater energy efficiency
- Dark silicon, accelerators
- Reduced data movement
- Emergence of new metrics: security, reliability
- Emergence of new workloads: ML, graphs, genomics

Recent Microprocessor Trends



Source: Micron University Symp.

作业-1

- Top500超级计算机的体系结构调研报告
- 神威太湖之光(Sunway TaihuLight)、“天河2号-2A”及2022年其他TOP500超级计算机
- 超级计算机体系结构特点及主要关注的问题
- 一共十组，*根据学号最低有效位（X: 0-9）进行分组（组号Y=X+1）*，分别调研top10中的一款机器
- 以小组为单位提交报告和PPT(10slides)，3月15日前将doc+ppt发至指定邮箱
- 邮件标题格式：2023春国际架构作业1-第Y小组
- 各组选出一名代表做课堂报告

Rank	System	Cores	Rmax (PFlop/s)	Rpeak (PFlop/s)	Power (kW)
1	**Frontier** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE DOE/SC/Oak Ridge National Laboratory United States	8,730,112	1,102.00	1,685.65	21,100
2	**Supercomputer Fugaku** - Supercomputer Fugaku, A64FX 48C 2.2GHz, Tofu interconnect D, Fujitsu RIKEN Center for Computational Science Japan	7,630,848	442.01	537.21	29,899
3	**LUMI** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE EuroHPC/CSC Finland	1,110,144	151.90	214.35	2,942

Exercise-1

Which of the following descriptions about “Computer architecture” is true?

A. Computer architecture refers only to instruction set design.
B. Computer architecture means the implementation of a machine, which has two components: organization and hardware.
C. Computer architecture design doesn’t need to provide support to compilers.
D. Computer architecture is intended to cover all three aspects of computer design ---- instruction set architecture, organization and hardware.

Questions?

Summary of the systems in the Top10

- Frontier is the new No. 1 system in the TOP500. This HPE Cray EX system is the first US system with a peak performance exceeding one ExaFlop/s. It is currently being integrated and tested at the ORNL in Tennessee, USA, where it will be operated by the Department of Energy (DOE). It currently has achieved 1.102 Exaflop/s using 8,730,112 cores. The new HPE Cray EX architecture combines 3rd Gen AMD EPYC™ CPUs optimized for HPC and AI with AMD Instinct™ 250X accelerators and Slingshot-11 interconnect.
- Fugaku, now the No. 2 system, is installed at the RIKEN Center for Computational Science (R-CCS) in Kobe, Japan. It has 7,630,848 cores which allowed it to achieve an HPL benchmark score of 442 Pflop/s. This puts it 3x ahead of the No. 3 system in the list.
- The new LUMI system, another HPE Cray EX system installed at EuroHPC center at CSC in Finland, is the new No. 3 with a performance of 151.9 Pflop/s just ahead of No 4. The European High-Performance Computing Joint Undertaking (EuroHPC JU) is pooling European resources to develop top-of-the-range Exascale supercomputers for processing big data. One of the pan-European pre-Exascale supercomputers, LUMI, is in CSC's data center in Kajaani, Finland.
- Summit, an IBM-built system at ORNL in Tennessee, USA, is now listed at the No. 4 spot worldwide with a performance of 148.8 Pflop/s on the HPL benchmark which is used to rank the TOP500 list. Summit has 4,356 nodes, each housing two Power9 CPUs with 22 cores and six NVIDIA Tesla V100 GPUs, each with 80 streaming multiprocessors (SM). The nodes are linked together with a Mellanox dual-rail EDR InfiniBand network.
- -

4	**Summit** - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148.60	200.79	10,096
5	**Sierra** - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM / NVIDIA / Mellanox DOE/NNSA/LLNL United States	1,572,480	94.64	125.71	7,438
6	**Sunway TaihuLight** - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway, NRCPC National Supercomputing Center in Wuxi China	10,649,600	93.01	125.44	15,371
7	**Perlmutter** - HPE Cray EX235n, AMD EPYC 7763 64C 2.45GHz, NVIDIA A100 SXM4 40 GB, Slingshot-10, HPE DOE/SC/LBNL/NERSC United States	761,856	70.87	93.75	2,589

Summary of the systems in the Top10

- Sierra, a system at the Lawrence Livermore National Laboratory, CA, USA, is at No. 5. Its architecture is very similar to the #4 systems Summit. It is built with 4,320 nodes with two Power9 CPUs and four NVIDIA Tesla V100 GPUs. Sierra achieved 94.6 Pflop/s.
- Sunway TaihuLight is a system developed by China's National Research Center of Parallel Computer Engineering & Technology (NRCPC) and installed at the National Supercomputing Center in Wuxi, China's Jiangsu province, is listed at the No. 6 position with 93 Pflop/s.
- Perlmutter at No. 7 is based on the HPE Cray "Shasta" platform, and a heterogeneous system with AMD EPYC based nodes and 1536 NVIDIA A100 accelerated nodes. Perlmutter achieved 64.6 Pflop/s
- Now at No. 8, Selene is an NVIDIA DGX A100 SuperPOD installed inhouse at NVIDIA in the USA. The system is based on an AMD EPYC processor with NVIDIA A100 for acceleration and a Mellanox HDR InfiniBand as network and achieved 63.4 Pflop/s.
- Tianhe-2A (Milky Way-2A), a system developed by China's National University of Defense Technology (NUDT) and deployed at the National Supercomputer Center in Guangzhou, China is now listed as the No. 9 system with 61.4 Pflop/s.
- The Adastra system installed at GENCI-CINES is new to the list at No. 10. It is the third new HPE Cray EX system and the second fastest system in Europe. It achieved 46.1 Pflop/s.

8	**Selene** - NVIDIA DGX A100, AMD EPYC 7742 64C 2.25GHz, NVIDIA A100, Mellanox HDR Infiniband, Nvidia NVIDIA Corporation United States	555,520	63.46	79.22	2,646
9	**Tianhe-2A** - TH-IVB-FEP Cluster, Intel Xeon E5-2692v2 12C 2.2GHz, TH Express-2, Matrix-2000, NUDT National Super Computer Center in Guangzhou China	4,981,760	61.44	100.68	18,482
10	**Adastra** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE Grand Equipement National de Calcul Intensif - Centre Informatique National de l'Enseignement Suprieur (GENCI-CINES) France	319,072	46.10	61.61	921

TOP500 DESCRIPTION

- Nworld - Position within the TOP500 ranking
- Manufacturer - Manufacturer or vendor
- Computer - Type indicated by manufacturer or vendor
- Installation Site - Customer
- Location - Location and country
- Year - Year of installation/last major update
- Field of Application
- #Proc. - Number of processors (Cores)
- Rmax - Maximal LINPACK performance achieved
- Rpeak - Theoretical peak performance
- Nmax - Problem size for achieving Rmax
- N1/2 - Problem size for achieving half of Rmax