KEY POINTS OF THE FINAL EXAMINATION

1st Semester, 2022-2023

- Knowledge Shares of the exam points:
  - Classic digital logic (Chp1-3): 50~60%
  - Modern EDA (Chp4-7): 40~50%
- Question Types
  - Short answers
  - Circuit analysis and design
  - Verilog programming

- ☐ Chp 1
  - ☐ Number systems and code systems, including 1's and 2's complements (Sect. 1.2)
    - ◆ Conversions of a number among different number systems
  - ☐ Digital logic fundamentals, simplification of logic functions using formulas, and K-maps with constraints (5 points at least). (Sect. 1.3)
  - ☐ Logic symbols of commonly used logic gates (Sect.1.4)
- ☐ Chp 2
  - ☐ The steps to analyze a combinational circuit.
  - ☐ Sect 2.3, commonly used comb. circuits, including encoders, decoder, MUX, comparators, and adders, about their principles, logic functions, and symbols.
    - ◆ You may SKIP their respective design processes.
  - ☐ Carry-Lookahead Adders' principles, and merits/demerits over Serial Carry Adders.
  - ☐ Signed binary number adders
    - ◆ How to calculate the OF flag?
    - ◆ 3 treatments of the extra bit, including their principles.
  - ☐ Sect 2.4, design process steps. Given a truth table, derive functions, and device the logic diagram.
  - ☐ Sect 2.5, basic concepts, like propagation delays, wave forms, etc.
    - ◆ Methods to handle hazards.
- ☐ Chp 3
  - ☐ Sect 3.1 basic concepts, categories, and fig. 3-1 of sequential circuits, STGs (State-Transition Graphs) as well.
  - ☐ Sect 3.2, symbols, characteristic tables and functions of all FLIP-FLOPS.
    - ◆ Know the ways to construct a required type of flip-flop using other types of flip-flops, like to build a JK using a D flip-flop.
  - ☐ Sect 3.3, The steps to analyze a sequential circuit. Understand what exactly each step is accomplishing.
  - ☐ Sect 3.4

- ◆ Registers: the principles of all types of registers: parallel/serial input/output registers.
- ◆ Counters: the following knowledge and skills are REQUIRED:
  - ● Suppose you are required to design a 12-carry counter with a 74HC161 giving its function table and pin assignments, using the specified method of asynchronous clearing, synchronous clearing, or presetting. You need to
    - ■ draw the STG including invalid states,
    - ■ and draw the logic diagram by connecting wires, basic gates to a 74HC161 IC, like fig.3-64, fig.3-65, and fig.3-67.
  - ● Know how to design a 200-carry counter using two 74HC161s similarly.

☐ Sect 3.6, basic concepts, like clock cycle, aperture time, max propagation delay time, etc.

☐ Chp 4 to 5

☐ Verilog fundamentals

- ◆ grammar, common system tasks and system functions.
- ◆ Values, constants, wires and variables, vectors and arrays.
- ◆ Operators.

☐ Three styles of programming: gate-level, data-flow, and behavioral styles.

☐ Comprehend the typical EDA design process (fig. 5-2).

☐ Chp 6-7: modules and their corresponding test benches.

☐ 6.1, Basic gates

☐ 6.2, Encoders (the first two methods), HC148 as well.

☐ 6.3 Decoders, HC4511 as well.

☐ 6.4-6.6, MUX, comparators, and 4-bit serial carry adders.

☐ 7.2, D, JK, and T flip-flops

☐ 7.3.1 and 7.3.2, registers.

☐ 7.5, counters, and HC161.

☐ 7.6, understand the “Triple-always” module (p.7-30) and its test bench (p. 7-32)

The final examination may include the above key points, as well as other knowledge and skills introduced in our classes.

STUDY HARD, AND BEST WISHES TO YOU ALL!