计算机组成原理-复习
Principle of Computer Organization

示例

- The delays of circuit elements are given as follows:

Stage	IF	ID	EX	MEM	WB
Delay	200ps	200ps	400ps	200ps	100ps

<1>Mark the stages the following instructions use and calculate the time to execute

Instruction	IF	ID	EX	MEM	WB	Total
ADD						
LDUR						
STUR						
XOR						
CBZ						

<2> Which instruction(s) exercises the critical path?

<3> What is the fastest you could clock this single-cycle datapath? (1 ps = 10^{-12} s)

示例

<1>Mark the stages the following instructions use and calculate the time to execute

Instruction	IF	ID	EX	MEM	WB	Total
ADD	X	X	X		X	900ps
LDUR	X	X	X	X	X	1100ps
STUR	X	X	X	X		1000ps
XOR	X	X	X		X	900ps
CBZ	X	X	X			800ps

<2> Which instruction(s) exercises the critical path?

Load word (lw), as it both reads from memory and writes to register, which most instructions don't use both memory and writing to register.

<3> What is the fastest you could clock this single-cycle datapath? (1 ps = 10-12 s)

1/(1100 ps) = 1/(800 * 10-12s) = 1012 / 1100 = 909090909 = 909MHz

- Put the corresponding letters for each 32-bit value in order from least to greatest. (Hint: the question isn't asking you to write down what each one is, it only asks for the relative order!)
  - A: 0xFF000000 (IEEE754 single precision)
  - B: 0xFF000000 (2's complement)
  - C: 0xFF000000 (sign-magnitude)
  - D: 0xFF000000 (biased notation移码)
  - E: 0xF0000000 (2's complement)
  - F: 0xF0000000 (1's complement)

Least							Greatest

- Convert $-ABCD_{hex}$ into :
  - Sign and magnitude
  - 2’complement
  - Biased notation
  - IEEE754 Single Precision(Hex)
  - IEEE754 Double Precision(Hex)

- 1G main memory, byte-addressing, 128KB Cache. Now a data locate at 0x123456(byte-addressing), will mapping towhich cache unit in different situation below, and how about its TAG and Total cache size?

0x123456	The data will Mapping to (*block(s)*)	TAG		Tatal Size
		TAG for the data(Hex)	bits	
Direct-mapped, 16 bytes/block				
Direct-mapped, 64 bytes/block				
2-Way set associative 16 bytes/block				
4-Way set associative 32 bytes/block				

示例

0x123456	The data will Mapping to (*block(s)*)	TAG		Tatal Size
		TAG for the data(Hex)	bits	
Direct-mapped, 16 bytes/block	**0x345**	**0x9**	**15**	**(15+1)*8K/8+128K=144KB**
Direct-mapped, 64 bytes/block	**0xD1**	**0x9**	**15**	**(15+1)*2K/8+128K=132**
2-Way set associative 16 bytes/block	**0x345 *2+0,+1**	**0x12**	**16**	**(16+1)*8K/8+128K=145KB**
4-Way set associative 32 bytes/block	**0x1A2 *4+0,+1,+2,+3**	**0x24**	**17**	**(17+1)*4K/8+128K=137K**