



Government Engineering College, Gandhinagar

**Computer Engineering
B.E. Semester III
(AY 2021-22)**

SUBJECT: Digital Fundamental (3130704)



Government Engineering College

Sec-28 Gandhinagar

Certificate

This is to certify that

Mr./Ms. Aparna Ch. Shrivastava Of class

..... Division B, Enrollment No. N2D37 Has

Satisfactorily completed his/her term work

Subject for the term ending in

DF

2022.

Date: -

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department

Vision/Mission

Vision:

To be a premier engineering institution imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communications skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	Solve the given problem using fundamentals of number systems and Boolean algebra
CO-2	Analyze working of logic families and logic gates and design simple circuits using gates.
CO-3	Design and implement combinational and sequential logic circuit and verify it's working
CO-4	Examine the process of Analog to digital conversion PLO's too given to Analog conversion
CO-5	Implement PLO's for given logical Problem

7. Assignment Index

Sr. No	Assignment	Date	Page No.	Sign
1	Assignment 1	30/09/2022	1	✓
2	Assignment 2	17/10/2022	9	✓
3	Assignment 3	30/11/2022	19	✓
4	Assignment 4	14/12/2022	27	✓
5	Assignment 5	30/12/2022	33	✓

8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1	17/09/2022	14	
2	Practical 2	17/09/2022	16	
3	Practical 3	01/10/2022	18	
4	Practical 4	01/10/2022	20	
5	Practical 5	15/10/2022	21	
6	Practical 6	15/10/2022	24	
7	Practical 7	19/10/2022	27	
8	Practical 8	19/10/2022	29	
9	Practical 9	03/12/2022	33	
10	Practical 10	03/12/2022	34	
11	Practical 11	17/12/2022	36	

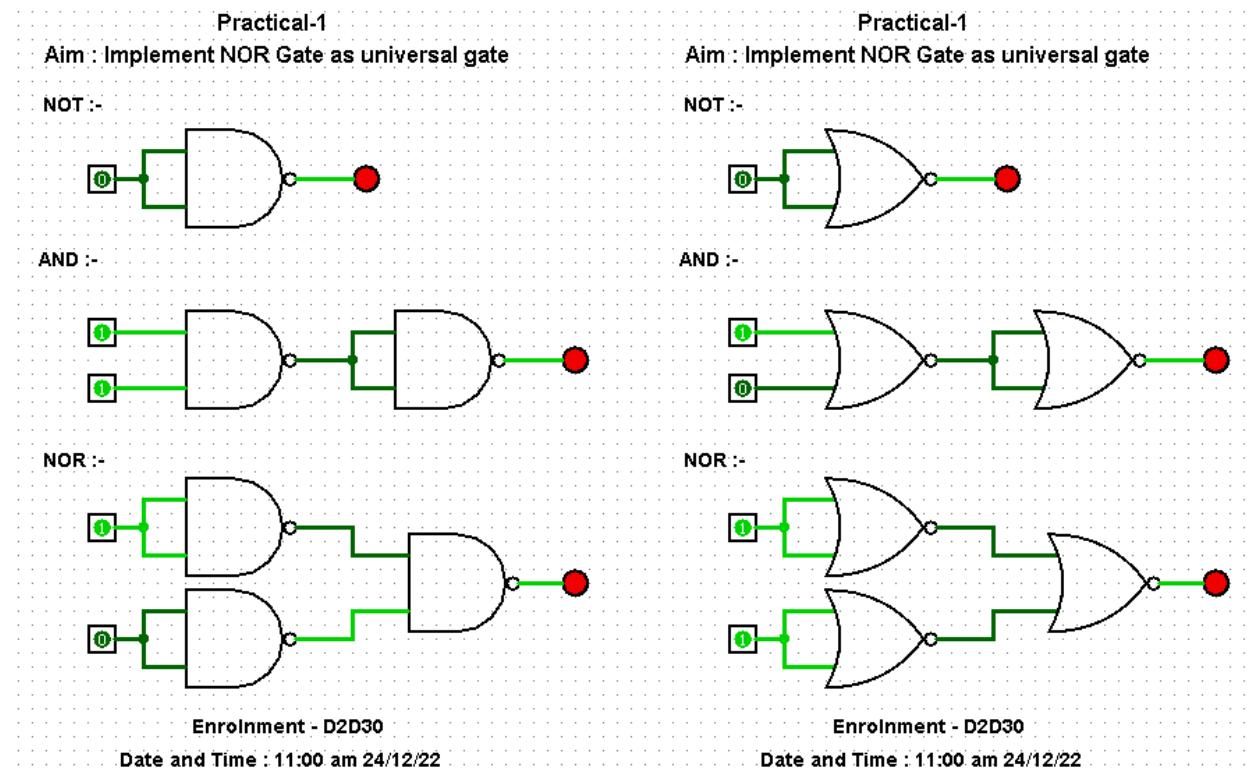
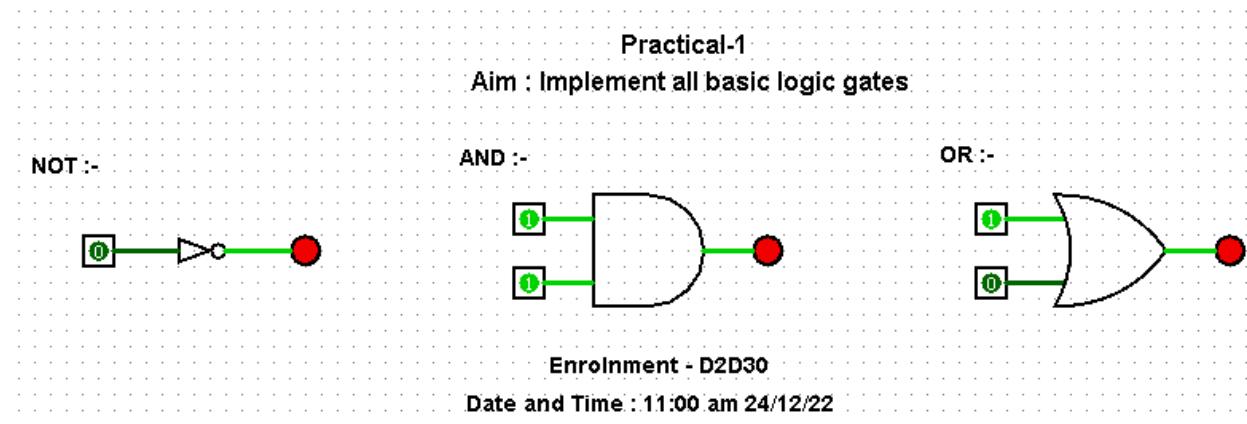
14.Practical 1

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

Module 1

Aim: Getting familiar with Logisim, Study and implement all basic logic gates.
Implement NAND and NOR logic gates as universal gates.

Code:

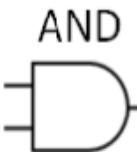


Brief Explanation & Truth Tables:

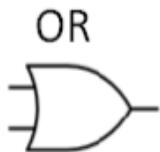
In an OR gate, the output of an OR gate attains state 1 if one or more inputs attain state 1.

In the AND gate, the output of an AND gate attains state 1 if and only if all the inputs are in state 1.

In a NOT gate, the output of a NOT gate attains state 1 if and only if the input does not attain state 1.



INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1



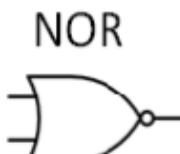
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1



INPUT		OUTPUT
A		
0		1
1		0



INPUT		OUTPUT
A	B	
0	0	1
1	0	1
0	1	1
1	1	0



INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

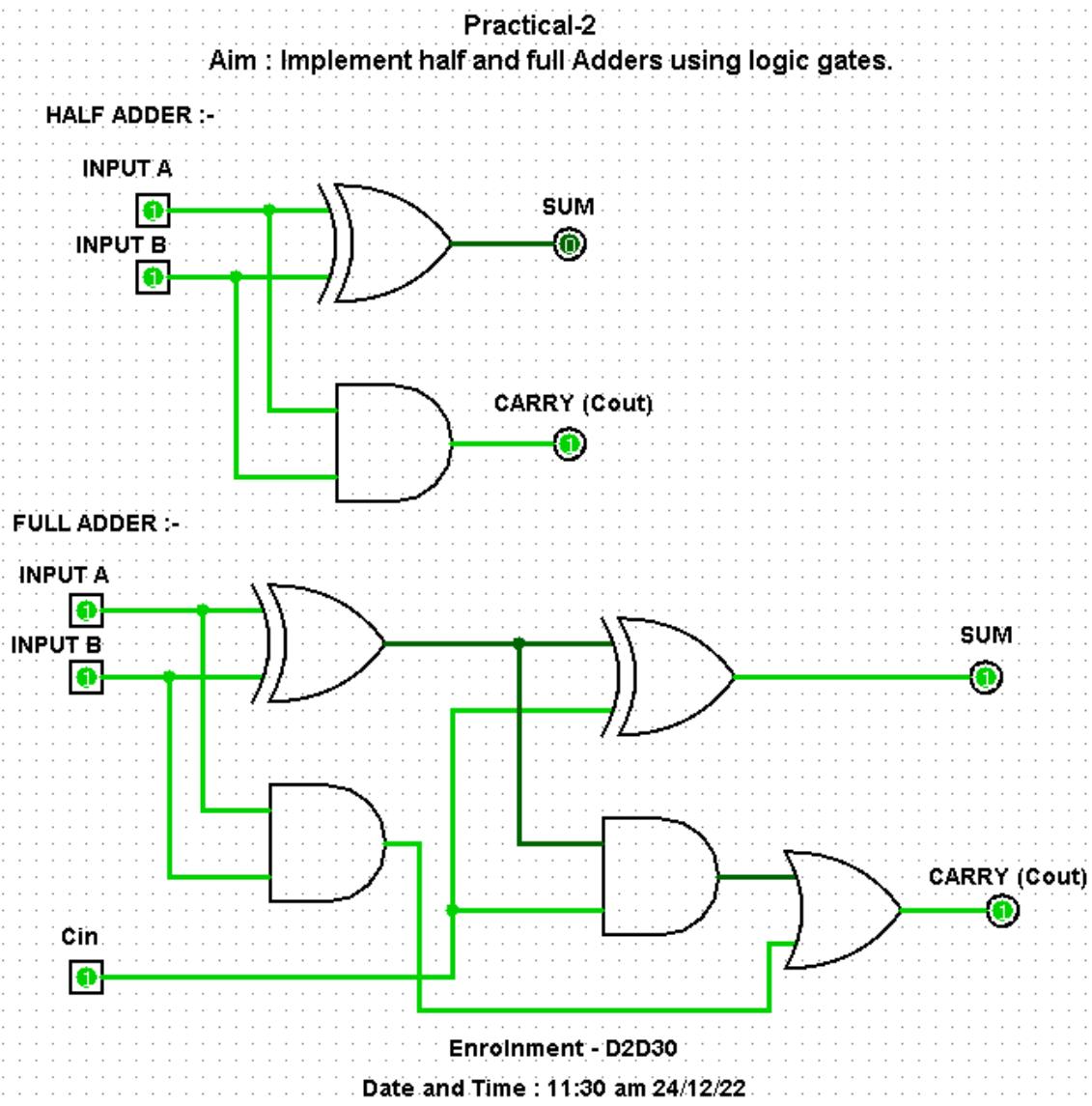
15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Adders using logic gates.

Code:



Brief Explanation & Truth Tables:

A half-adder circuit consists of two input terminals- namely A and B. Both of these add two input digits (one-bit numbers) and generate the output in the form of a carry and a sum.

Input		Output	
A	B	CARRY	SUM
0	0	0	0
1	1	1	0
0	1	0	1
1	0	0	1

The full adder adds three binary digits. Among all the three, one is the carry that we obtain from the previous addition as C-IN, and the two are inputs A and B. It designates the input carry as the C-OUT and the normal output as S

Input			Output	
A	B	C	SUM	CARRY OUT
0	0	0	0	0
1	1	1	1	1
0	1	1	0	1
1	0	1	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

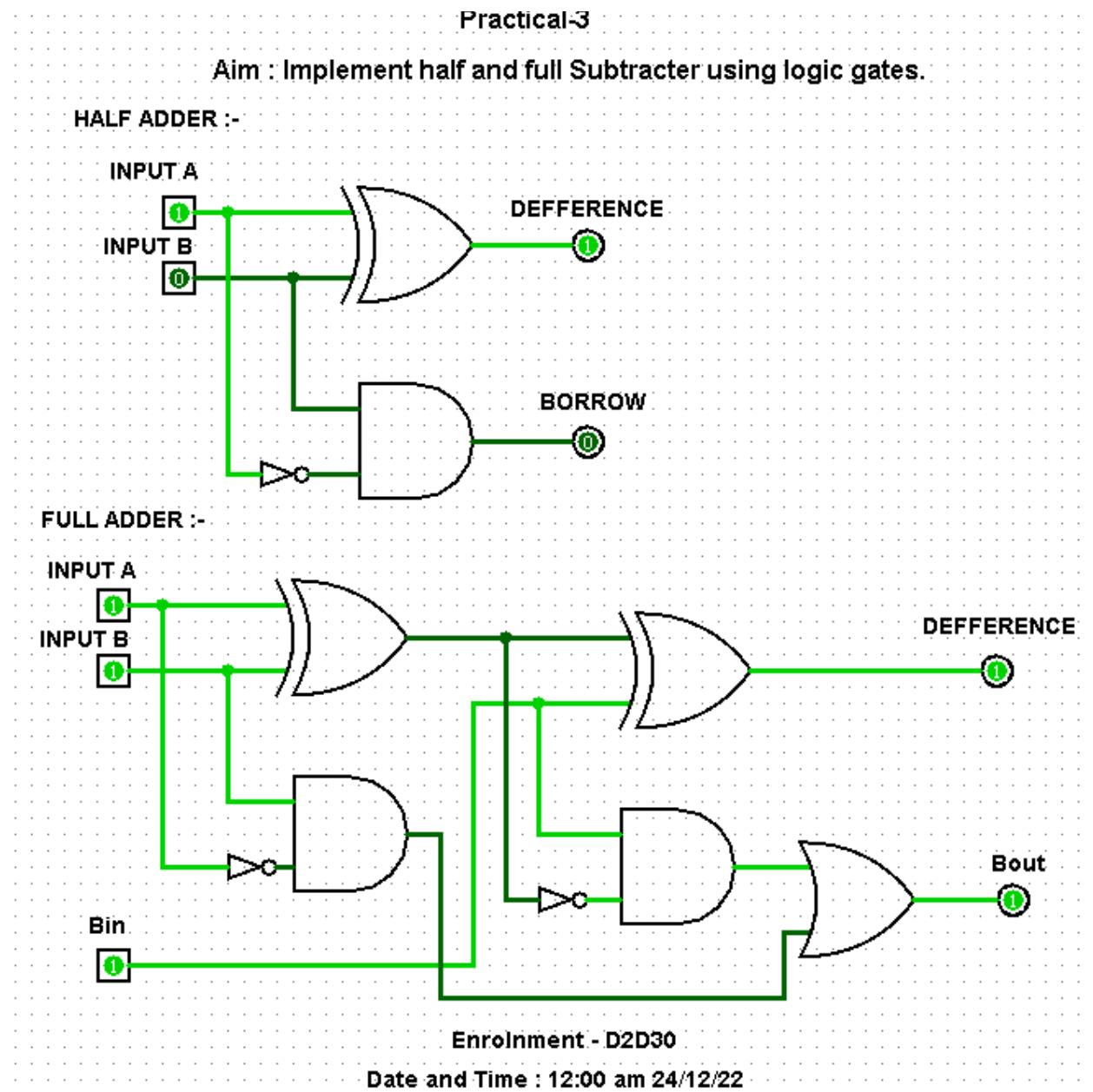
16. Practical 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Subtractors using logic gates.

Code:



Brief Explanation & Truth Tables:

The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively.

Half Subtractor Truth Tables:

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor Truth Table:

Inputs			Outputs	
A	B	Borrow _{in}	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

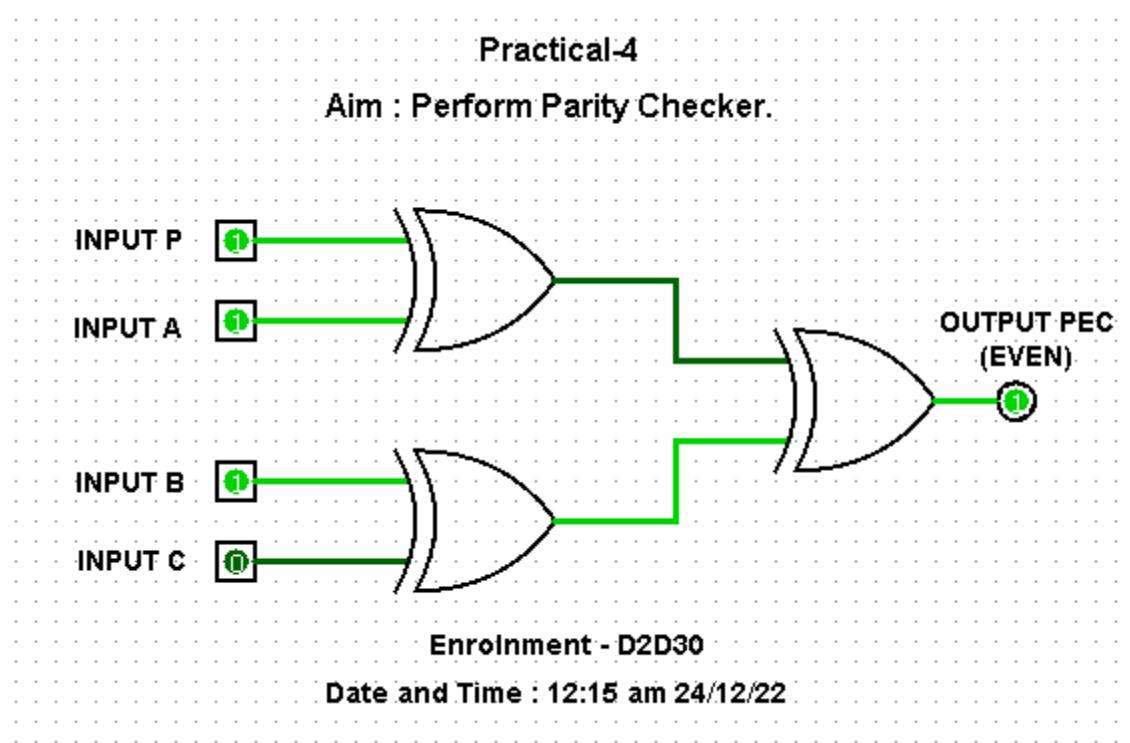
17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Perform Parity Checker

Code:



D_3	D_2	D_1	D_0	Even-parity P	Odd-parity P
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

18. Practical 5

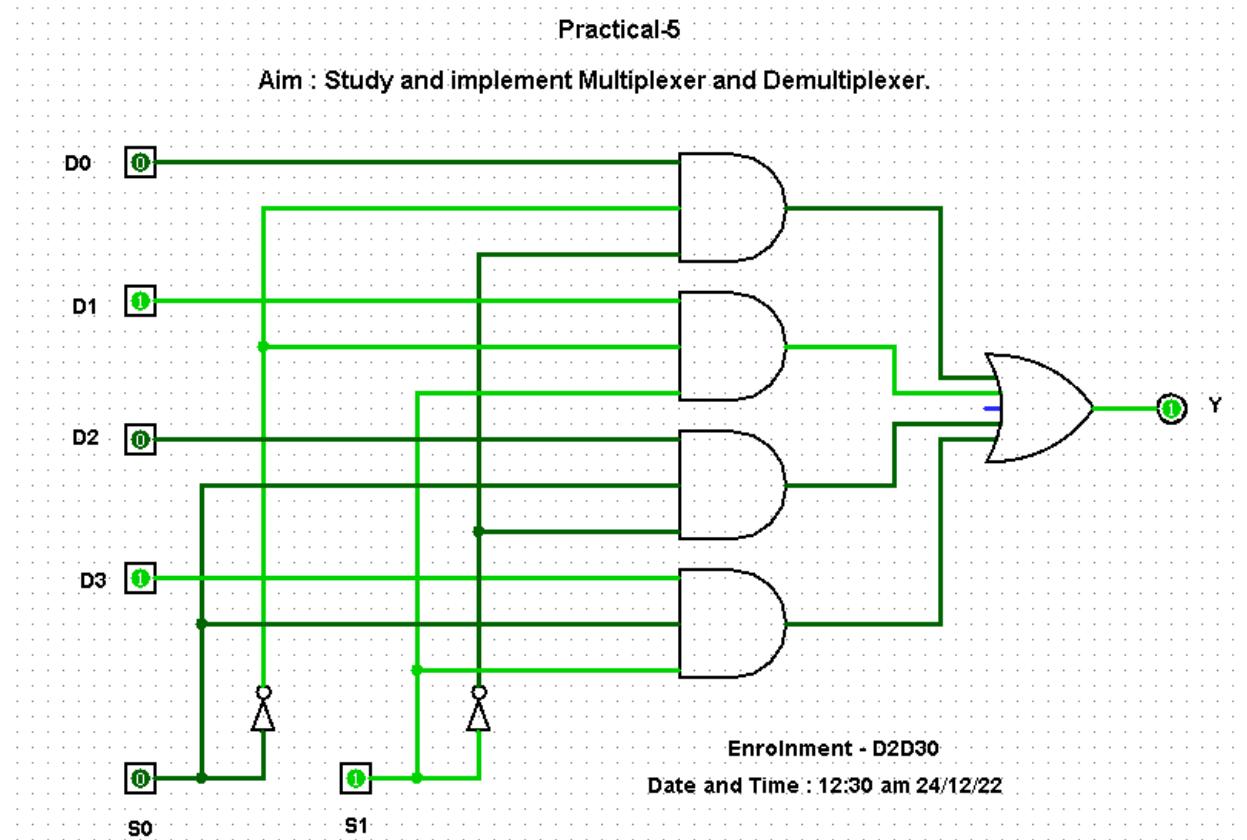
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement Multiplexer and Demultiplexer.

Code:

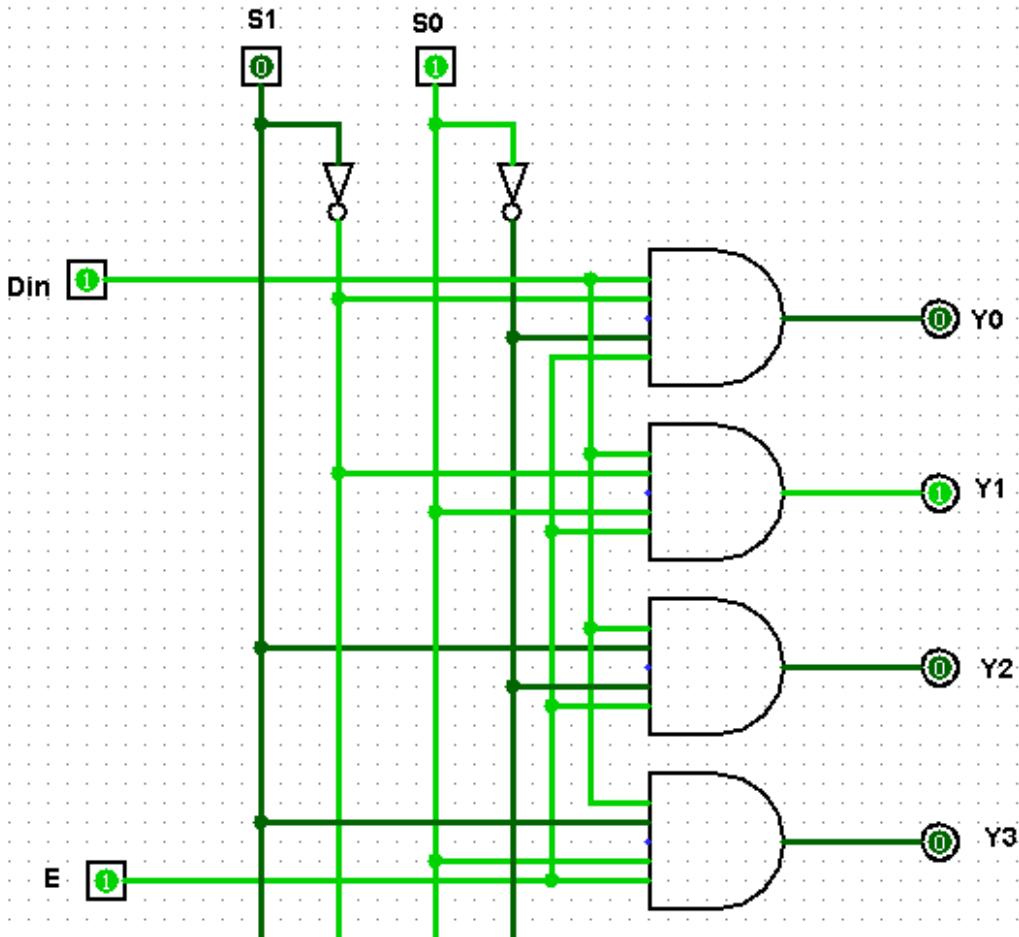
4:1 Multiplexer



1:4 Demultiplexer

Practical-5

Aim : Study and implement Multiplexer and Demultiplexer.



Enrolment - D2D30

Date and Time : 12:30 am 24/12/22

Brief Explanation & Truth Tables:

Multiplexer:

A multiplexer is a combinational circuit that has 2^n input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit.

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Demultiplexer:

A De-multiplexer is a combinational circuit that has only 1 input line and 2^N output lines. Simply, the multiplexer is a single-input and multi-output combinational circuit.

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

19. Practical 6

CO3: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

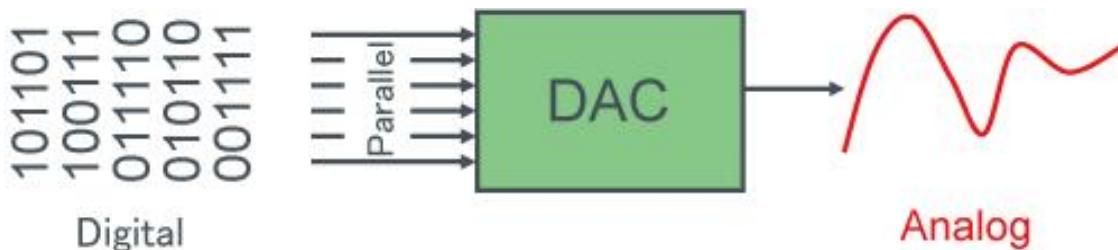
Module 2

Aim: Study and configure A to D convertor and D to A convertor.

What is Analog to Digital Converter?

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.

- Analog signals are directly measurable quantities.
- Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.



Application of Analog to Digital Converter:

ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.

- Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.
- Microcontrollers commonly use 8, 10, 12, or 16-bit ADCs, our micro controller uses an 8 or 10-bit ADC

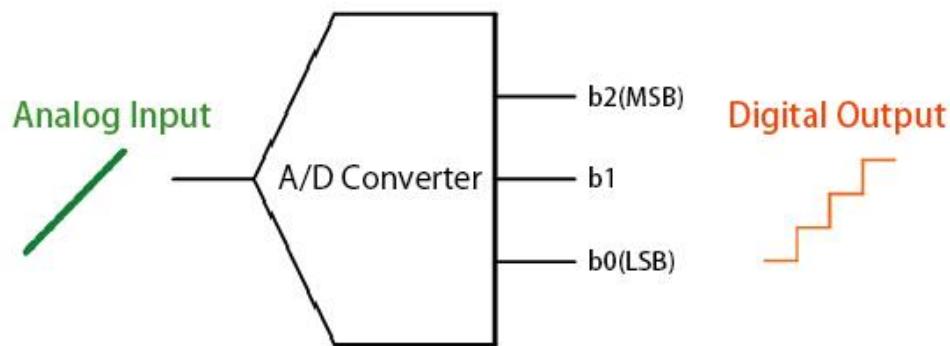
Types of Analog to Converters (ADC):

- Successive Approximation A/D Converter
- Flash A/D Converter
- Delta-Sigma A/D Converter

What is a Digital to Analog Converter?

Digital to analog converting is a process where digital signals that have a few (usually two) defined states are turned into analog signals, which have a theoretically infinite number of states. A Digital to Analog Converter, or DAC, is an electronic device that converts a digital code to an analog signal such as a voltage, current, or electric charge. Signals can easily be stored and transmitted in digital form; a DAC is used for the signal

to be recognized by human senses or non-digital systems. Converting a signal from digital to analog can degrade the signal.



Applications for Digital to Analog Converters:

An example can be found in the processing of computer data by a modem into audio-frequency tones transmitted over a telephone line. The circuit that performs this is a digital to analog converter. In music players, digital to analog converters can be used for generation of audio signals from digital information. In TVs and cell phones, digital video signals are converted into analog in order to display colors and shades.

In VoIP applications, the source is first digitized for transmission through an analog to digital converter and is then reconstructed into an analog signal using a DAC at the receiving end.

Types of Digital to Analog Converter (DAC):

- Binary Weighted Resistor D/A Converter Circuit
- Binary ladder or R–2R ladder D/A Converter Circuit
- Segmented DAC
- Delta-Sigma DAC

Analog Signal to Digital Signal Conversion Methods:

1. Sampling:

Sampling is the process of taking amplitude values of the continuous analog signal at discrete time intervals (sampling period T_s).

[Sampling Period $T_s = 1/F_s$ (Sampling Frequency)]

Sampling is performed using a Sample and Hold (S&H) circuit.

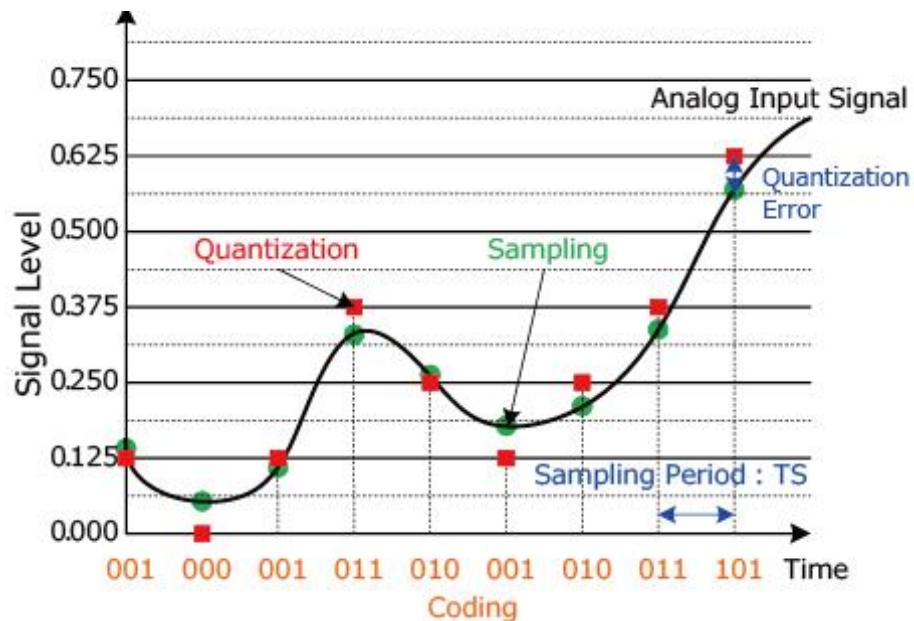
2. Quantization:

Quantization involves assigning a numerical value to each sampled amplitude value from a range of possible values covering the entire amplitude range (based on the number of bits).

[Quantization error: Sampled Value - Quantized Value]

3. Coding:

Once the amplitude values have been quantized they are encoded into binary using an Encoder.



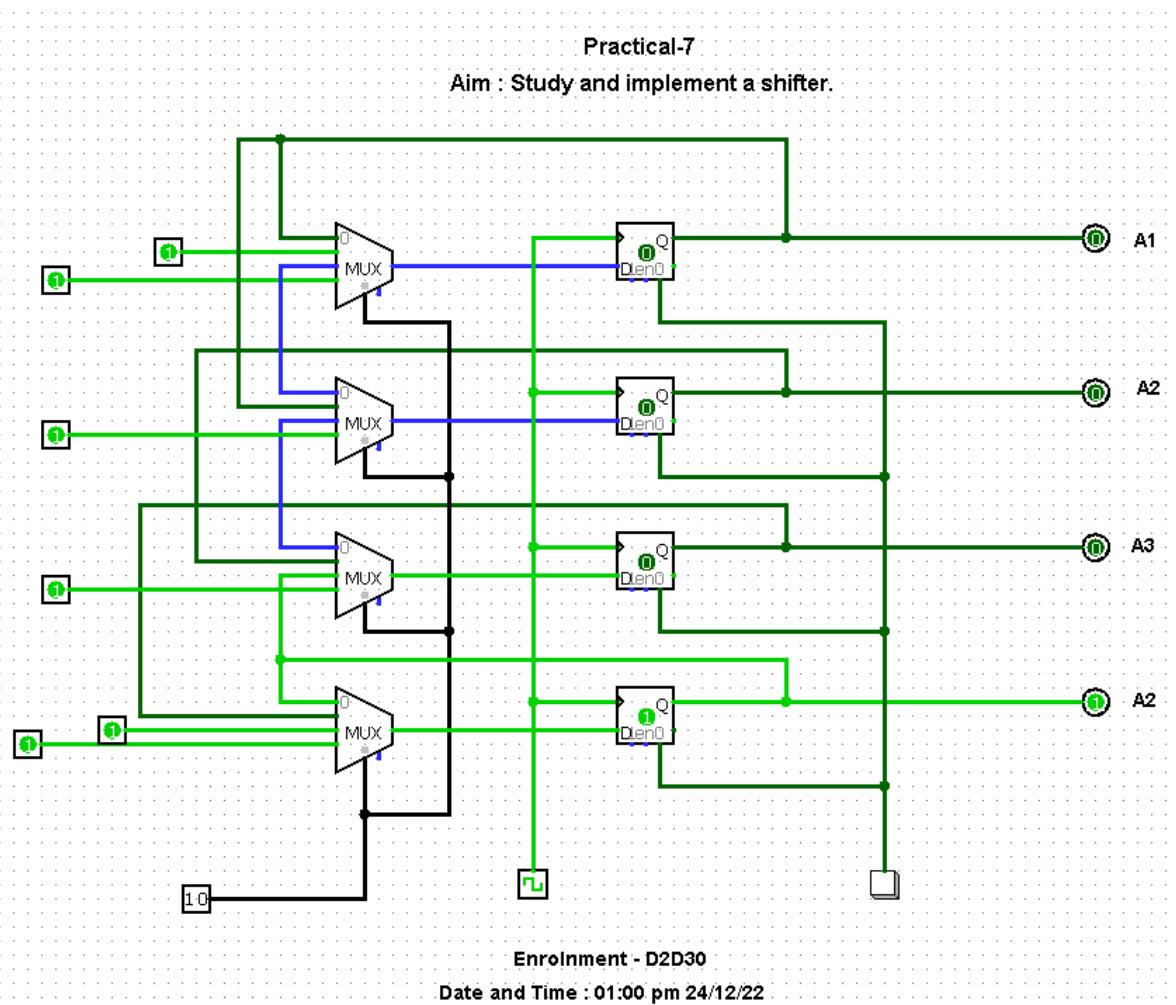
20. Practical 7

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement a shifter.

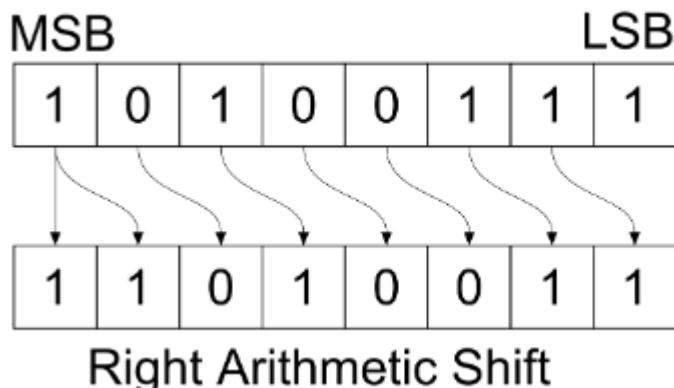
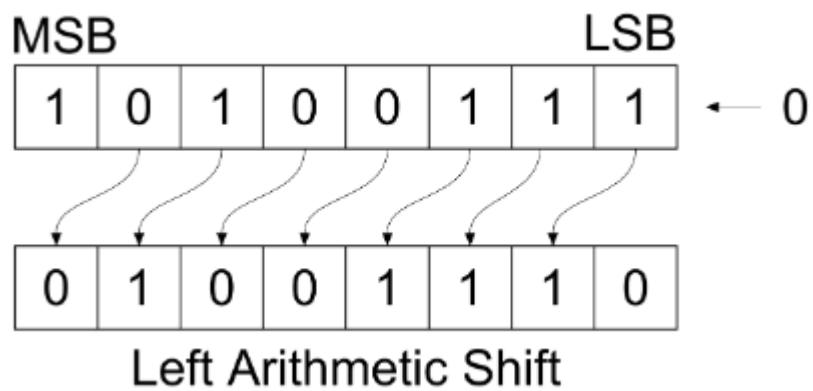
Code:



Brief Explanation & Truth Tables:

Arithmetic Shifter : is the same as a logical shifter, but on right shifts fills the most significant bits with a copy of the old most significant bit (MSB). This is useful for multiplying and dividing signed numbers Arithmetic shift left (ASL) is the same as logical shift left (LSL).

Truth Table:



21. Practical 8

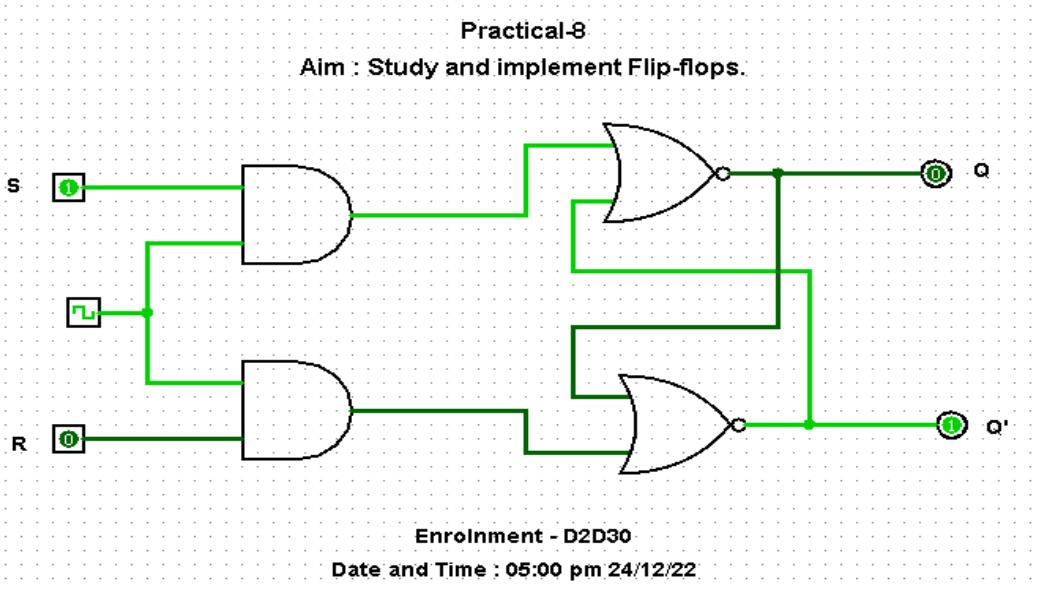
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

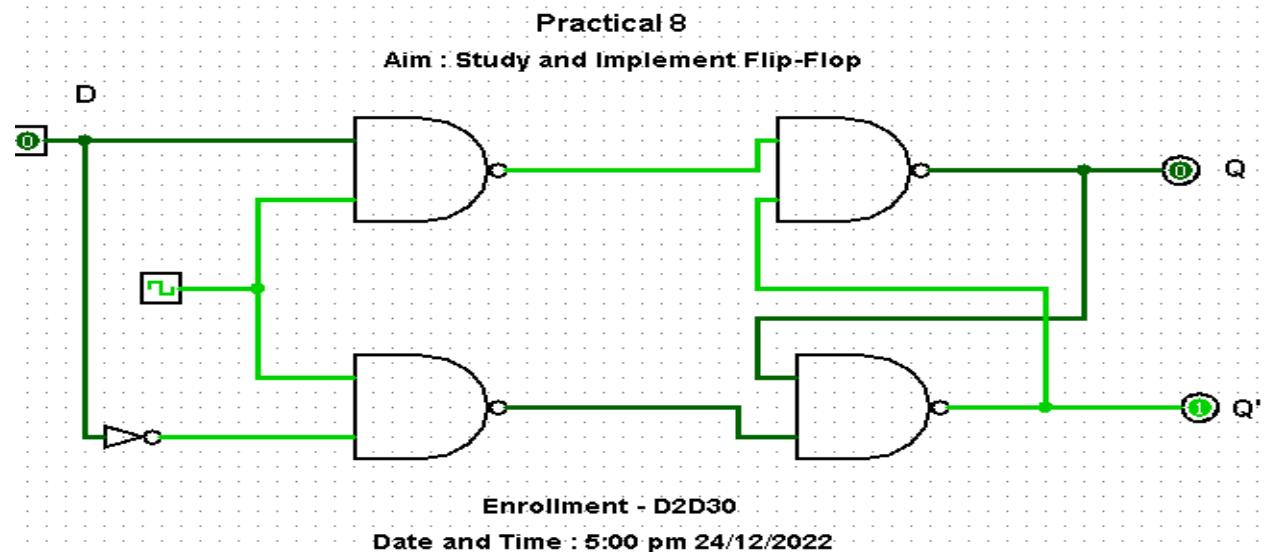
Aim: Study and implement Flip-flops.

Code:

SR Flip Flop



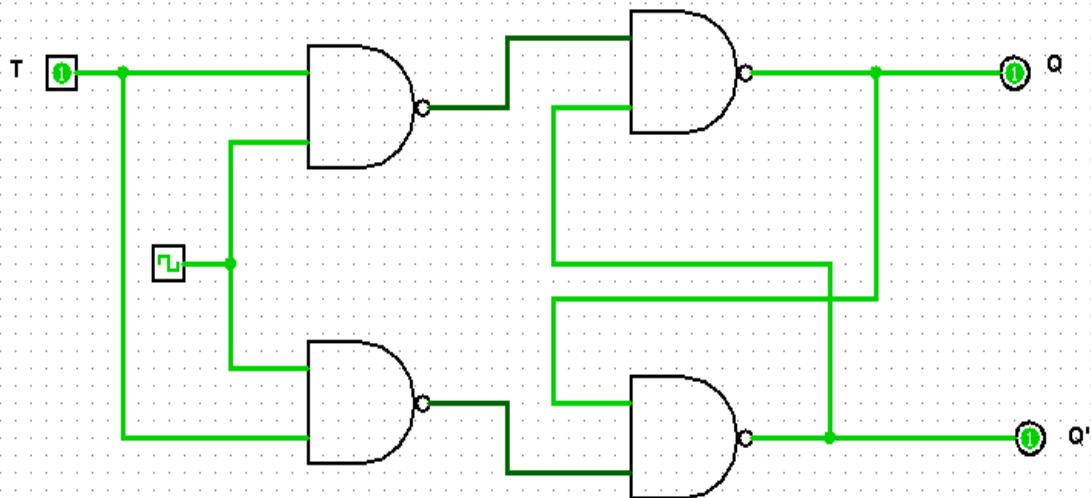
D Flip Flop



T Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



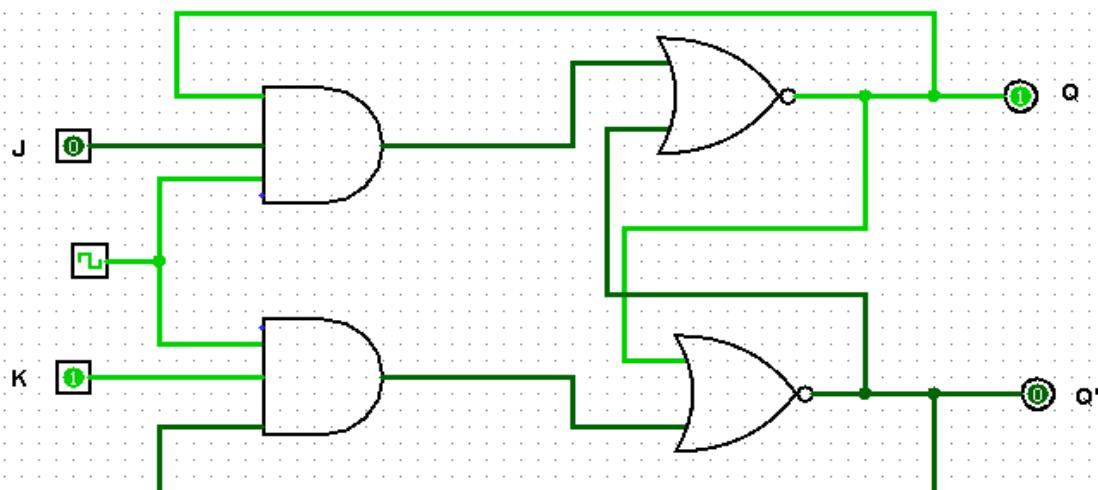
Enrolment - D2D30

Date and Time : 05:00 pm 24/12/22

JK Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



Enrolment - D2D30

Date and Time : 05:00 pm 24/12/22

Brief Explanation & Truth Tables:

SR Flip Flop

A gated SR latch requires an Enable (EN) input.

Its S and R inputs will control the state of the flip flop only when the EN is high.

When EN is low, the inputs become ineffective and no change of state can take place.

Truth Table

En	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate (Invalid)
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

D Flip Flop

It differs from the S-R latch in that has only one input in addition to EN.

When D=1, we have S=1 and R=0, causing the latch to SET when ENABLED

When D=0, we have S=0 and R=1, causing the latch to RESET when ENABLED

Truth Table

En	D	Q_n	Q_{n+1}	State
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set
1	1	1	1	
0	X	0	0	No Change (NC)
0	X	1	1	

JK Flip Flop

The JK flip flop is very versatile and also the most widely used.

The functioning of the JK flip flop is identical to that of the SR flip flop, except that it has no invalid state like that of SR flip flop.

Truth Table

En	J	K	Q _n	Q _{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	0	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

T Flip Flop

A T flip flop has a single control input, labeled T for toggle.

When T is HIGH the flip flop toggles on every new clock pulse.

When T is LOW the flip flop remains in whatever state it was before.

Truth Table

En	T	Q _n	Q _{n+1}	State
1	0	0	0	No Change (NC)
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	
0	X	0	0	No Change (NC)
0	X	1	1	

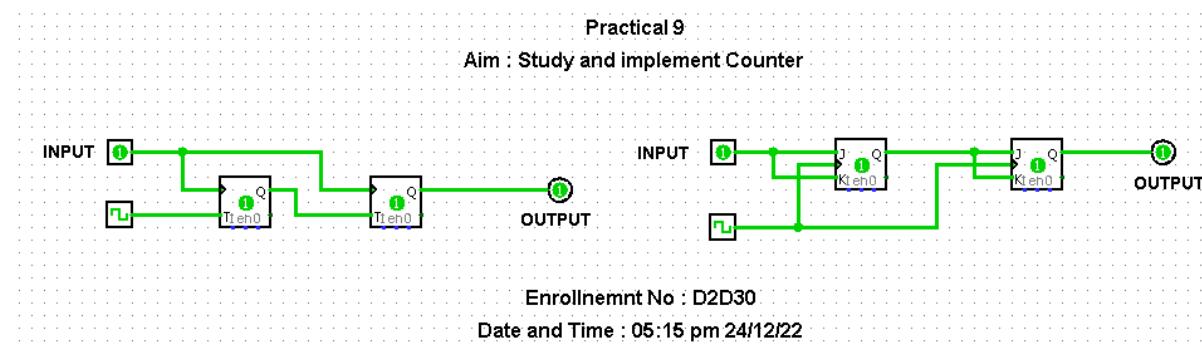
22. Practical 9

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and Implement Counter

Code:



Brief Explanation & Truth Tables:

Asynchronous Counter

The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle(T) flip-flops are being used. But we can use the JK flip-flop also with J and K connected permanently to logic

External clock is applied to the clock input of flip-flop A and Q A output is applied To the clock input of the next flip-flop.

Synchronous Counter

If the “Clock” pulses are applied to all the flip flop in counter simultaneously, Then such a counters are called synchronous counter.

In this type of counter there is no connection between the output of first FF and clock input of next FF and so on.

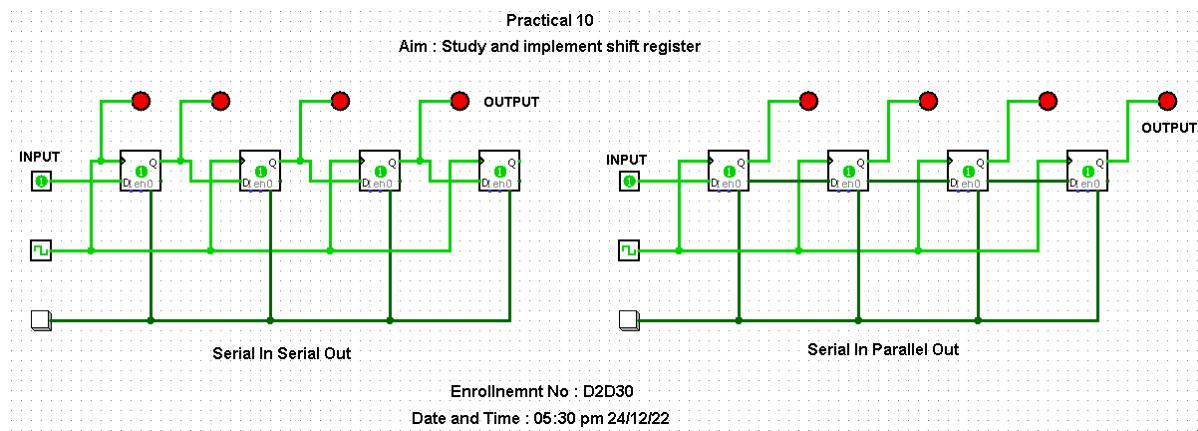
23. Practical 10

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

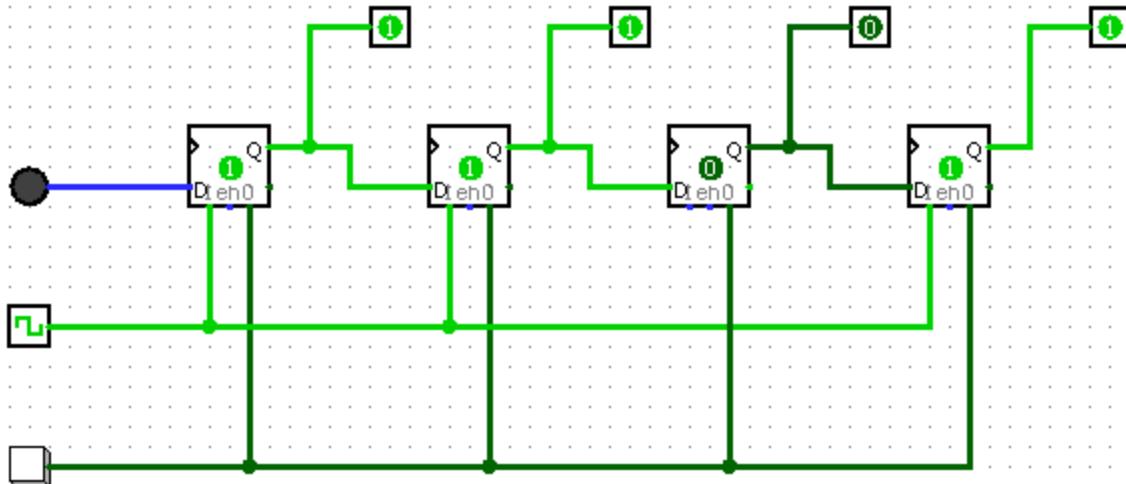
Module 3

Aim: Study and Implement a shift register

Code:



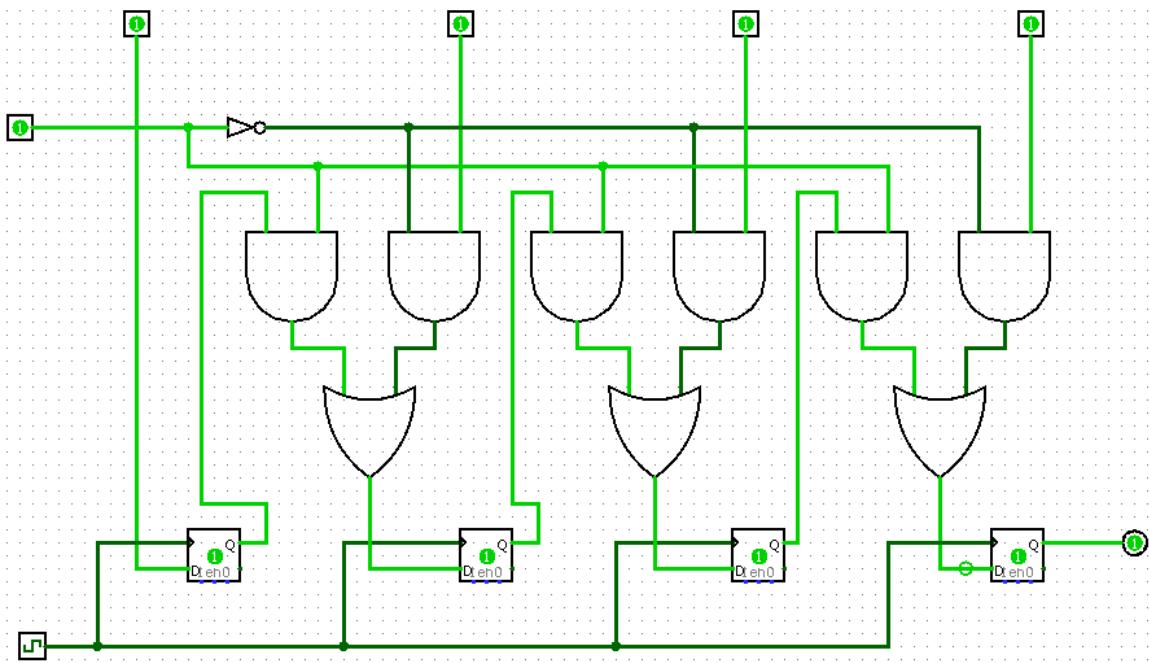
Practical 10
Aim : Study and implement shift register



Enrollment No : D2D30
Date and Time : 05:30 pm 24/12/22

Practical 10

Aim : Study and implement shift register



Enrollment No : D2D30

Date and Time : 05:30 pm 24/12/22

Brief Explanation:

A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.

Data may be shifted into or out of the register either in serial form or in parallel form.

So, there are four basic types of shift registers:

- serial-in, serial-out
- serial-in, parallel-out
- parallel-in, serial-out
- parallel-in, parallel-out

Data may be rotated left or right. Data may be shifted from left to right or right to left at will, i.e. in a bidirectional way.

Also, data may be shifted in serially (in either way) or in parallel and shifted out serially (in either way) or in parallel.

24. Practical 11

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and Implement K-Map for the given function:(SOP)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

Code:

Step 1: Finding the number of variables to build the K-map

$$\text{Number of variables} = 4(A,B,C,D)$$

So 4 variable K-map is to be used

Step 2: Filling cells of K-map for SOP with 1 respective to the min-terms for given equation

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	0	1	3	4	
	01	4	5	7	6	
	11	12	13	15	14	
	10	8	9	11	10	

Step 3: We create rectangular groups that contain total terms in the power of two like 2,4,8 and so on. Try to cover as many elements as we can cover in one group.

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	1	0	1	3	1 4
	01	4	5	7	6	
	11	12	1 13	15	14	
	10	1	8	9	11	1 10

Step 4: With the help of these groups, we find the product terms and sum of them for the SOP form $Y = ABC'D + B'D'$

9. Assignment 1

CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra

Module 1

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function: $F=A'B'C+A'BC+AB'$.
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

Assignment : 1

Module - 1

COI - Solve the give problem , using fundamental of number system .

1. State and explain De Morgan's theorem with the truth table

De Morgan Suggested two theorem that from a important part of Boolean Algebra .

$$1. \overline{AB} = \bar{A} + \bar{B}$$

The complement of product is equal to the sum of the complement

Truth table

A	B	\overline{AB}	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

$$2. \overline{A+B} = \bar{A} \cdot \bar{B}$$

The complement of a sum is equal to the product of the complement

Truth Table

A	B	$\bar{A} + B$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

2. Simplify Boolean function

$$F = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\bar{B}$$

$$\begin{aligned} &= \bar{A}C(\bar{B} + B) + A\bar{B} \\ &= \bar{A}C + A\bar{B} \end{aligned}$$

$$\therefore F = \bar{A}C + A\bar{B}$$

3. List and explain logic family

i. BIPOLAR

a) Saturated

- Register Transistor logic [RTL]
- Diode Transistor logic [DTL]
- Direct Transistor logic [DCTL]
- Integrated Injection logic [IIL]
- High Threshold logic [HTL]
- Transistor Transistor logic [TTL]

b) Unsaturated

- P - channel MOSFET (PMOS)
- n - channel MOSFET (NMOS)
- complementary MOSFET (CMOS)
- It's a group of compactable ICs with same logic level and supply voltage for performing various logic function.
- They are fabricated using a specific circuit configured which is referred a logic family.
- They are define design of the basic gate of each logic family is same.

Transistor Transistor logic (TTL)

It is named for it's independence on Transistor alone to perform basic operation.

- 4) Describe deleting and correction code
- To maintain the data integrity between Transmitter and receiver , extra bit or more than one bit are added
 - These extra bit allow the deletion and some of extra correction of errors
 - The data along with extra bit form the codes which allow only detection .

Parity code

- Even Parity Code
- Odd Parity Code

Even Parity Code

- The value of even parity bit should be 'zero' if even number of 1 present in binary code
- otherwise it should be one so that even number of ones present in even parity

Binary Code	Even parity bit	Even parity code
000	0	0 0 0 0
001	1	0 0 1 1
010	1	0 1 0 1
011	0	0 1 1 0
100	1	1 0 0 1
101	0	1 0 1 0
110	0	1 1 0 0
111	1	1 1 1 1

Odd parity code:

- The value of odd parity bit should be 'zero' if odd number of one present in binary code
- otherwise it should be one so, that odd number of ones present in odd parity

Binary code	odd parity bit	odd parity code
000	1	0000
001	0	0010
010	0	0100
011	1	0111
100	0	1000
101	1	1011
110	1	1101
111	0	1111

Hamming code

- It is useful for both detection and correction of error present in the receive data.
- This code use multiple parity bit and we have to parity bit on position.

Bit design	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁
Bit location	7	6	5	4	3	2	1
Binary location	111	110	101	100	011	010	001

- Parity P₁, check bit location 1, 3, 5, 7 and assign P₁ according to it
- Parity P₂, check bit location 2, 3, 6, 7 and assign P₂ according to it
- Parity P₃, check bit location 4, 5, 6, 7 and assign P₃

10. Assignment 2

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem

Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
 - 2.1. $F(x,y,z) = \Sigma (2,3,6,7)$
 - 2.2. $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

Assignment : 2

Module : 2

1) Explain K-map

- The map method gives us a systematic approach for simplicity a Boolean expression.
- The basis for this method is a graphical chart known as Karnaugh map (K-map).
- It contains boxes called cells. Each of the cells represents one of the 2^n position possible product that can be formed from n variables.
- Thus 2-variable map contains $2^2 = 4$ cells, a 3-variable map contains $2^3 = 8$ cells and so on for fourth.

A	B
0	0
1	1

1-variable map
(2 cells)

A	B	0	1
0	0	0	1
1	1	1	0

2-variable map
(4 cells)

A	BC	00	01	11	10
0	0	0	1	1	0
1	1	1	0	0	1

3-variable map
(8 cells)

2 Obtain the simplified expression in sum of product for the following Boolean function

$$1. F(x, y, z) = \Sigma(2, 3, 6, 7)$$

x	y	z	00	01	11	10
0			0	1	3	2
1			4	5	7	6

$$\therefore F = y$$

$$2. F(A, B, C, D) = \Sigma(4, 6, 7, 15)$$

AB	CD	00	01	11	10
00				3	2
01		4	5	7	6
11		12	13	15	14
10		8	9	11	10

$$\therefore F = \bar{A}BD + BCD$$

3

Describe adder and Subtractor :

Adder :

- The logical circuit which perform addition of two bit (SUM & CARRY) is a half adder.
- The logic circuit which perform addition of 3 bit (two significant bit and a previous carry) is full adder.

Half adder.

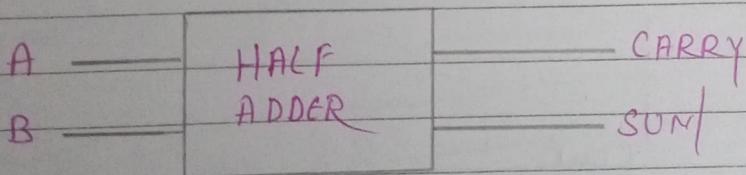
Two binary input

Two binary output \rightarrow SUM AND CARRY

Truth table

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Block Diagram



Full Adder

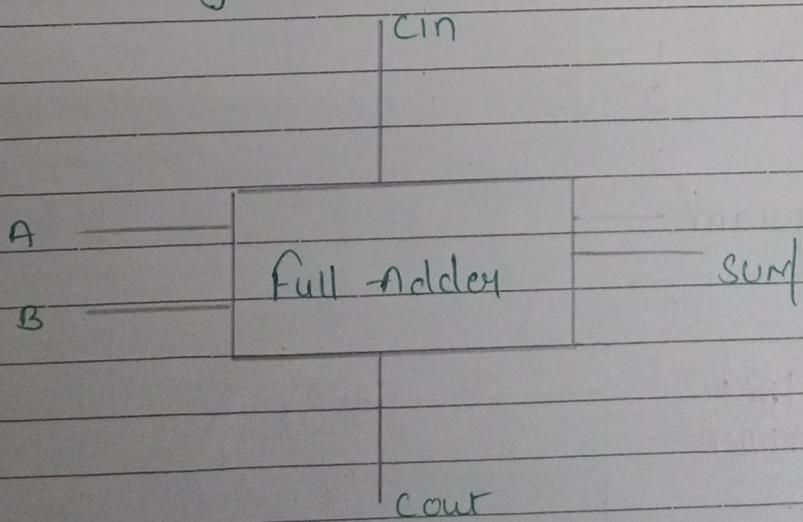
Three - binary input

Two - binary output \rightarrow SUM AND CARRY

Truth table

A	B	Cin	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Block Diagram



SUBTRACTOR

- A half subtractor is a combinational circuit that subtract two-bit and produce their difference.
- A full subtractor is a combinational circuit that subtracts between two bits taking into account Borrow.

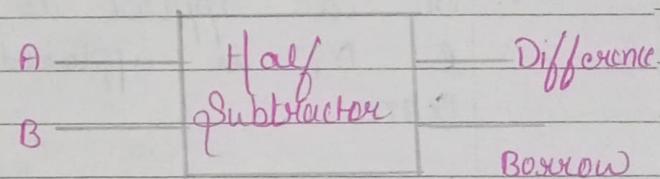
Half Subtractor

Two input, two output which is difference and Borrow

Truth Table

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Block Diagram



Full Subtractor

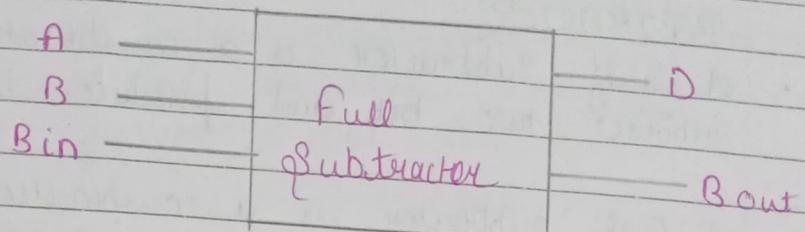
Three input

Two output - Difference, Borrow

TRUTH TABLE

A	B	Cin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Block Diagram



- 4) Explain Multiplexer & Demultiplexer

Multiplexer

To select a single data line from several data input lines and the data from the selected data line should be available.

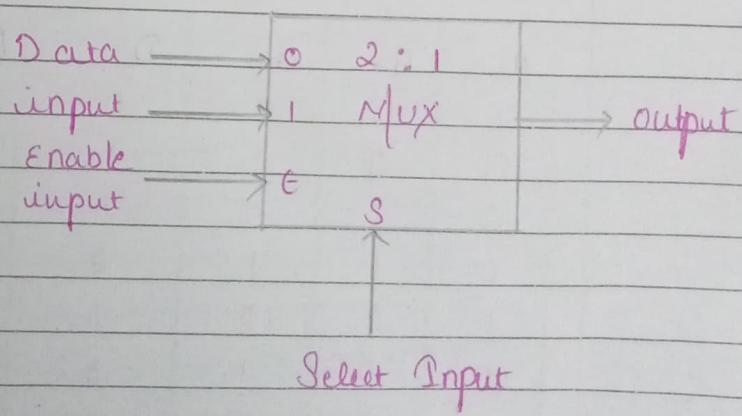
2 : 1 multiplexer

- Data is applied as an input to one AND GATE & D, is applied as an input to another AND GATE
- Output of both AND GATE is applied as input to OR GATE.

Function Table

E	S	y
1	0	D ₀
1	1	D ₁
0	X	0

Block diagram



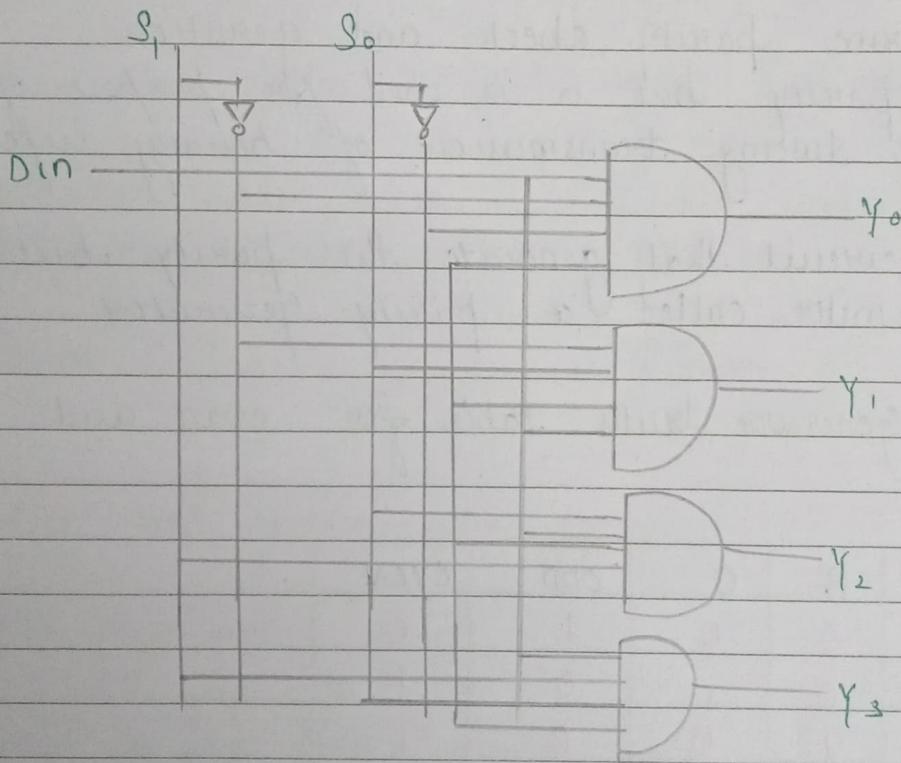
Demultiplexer

- A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines.

1:4 demultiplexer.

The single line input variable D_{in} has paths to all four outputs, but the line information is directed to only one of the output lines.

Logic Diagram



$$Y_0 = \bar{S}_1, S_0 \text{ } D_{in}$$

$$Y_1 = S_1, \bar{S}_0 \text{ } D_{in}$$

$$Y_2 = \bar{S}_1, \bar{S}_0 \text{ } D_{in}$$

$$Y_3 = S_1, S_0 \text{ } D_{in}$$

Function Table

E	S ₁	S ₀	Din	Y ₀	Y ₁	Y ₂	Y ₃
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

5

| Describe parity check and generation

| A parity bit is used for purpose of detecting
error during transmission of binary information

| The circuit that generates the parity bit is the
transmitter called a parity generator

* Parity Generator truth table for even and odd parity.

A	B	C	ODD	EVEN
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

11. Assignment 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 3

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

Assignment : 3

Module : 3

- Differentiate Sequential and combinational circuit

Combinational circuit

Sequential circuit

<ul style="list-style-type: none"> In combinational circuit the output variable are not at all time dependent on the combination of input variable Easy to design parallel adder is a combinational circuit Faster 	<ul style="list-style-type: none"> In Sequential circuit, the output variable depend not only on the present input but they also depend upon the past history of input. Hard to design Serial adder is a sequential circuit Q lower.
--	--

- list and explain flip flop

Flip flops are :

- JK flip flop
- D flip flop
- T flip flop
- SR flip flop

1) JK Flip Flop

The data input are J and K which are ANDed with J and \bar{K} respectively, to obtain S and R input

Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

2) D Flip Flop

- The input condition can be avoided by making them complement of the each other.
- This modified SR flip flop is known as D flip flop

Truth table

CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	\bar{Q}_n

3) T flip flop

- T flip flop is also known as "Toggle flip flop"
- modification of JK flip flop.

Truth table

T	S_{n+1}
0	S_n
1	\bar{S}_n

4) SR flip flop

- The circuit is similar to SR latch except enable signal represent by the clock pulse (CP)
- The edge detection circuit is a differentiation

Truth table

CP	S	R	S_{n+1}
0	X	X	S_n
↑	0	0	HOLD
↑	0	1	0
↑	1	0	1
↑	1	1	Invalid

3) List and explain following Register

→ Buffer Register

→ Controlled Buffer Register

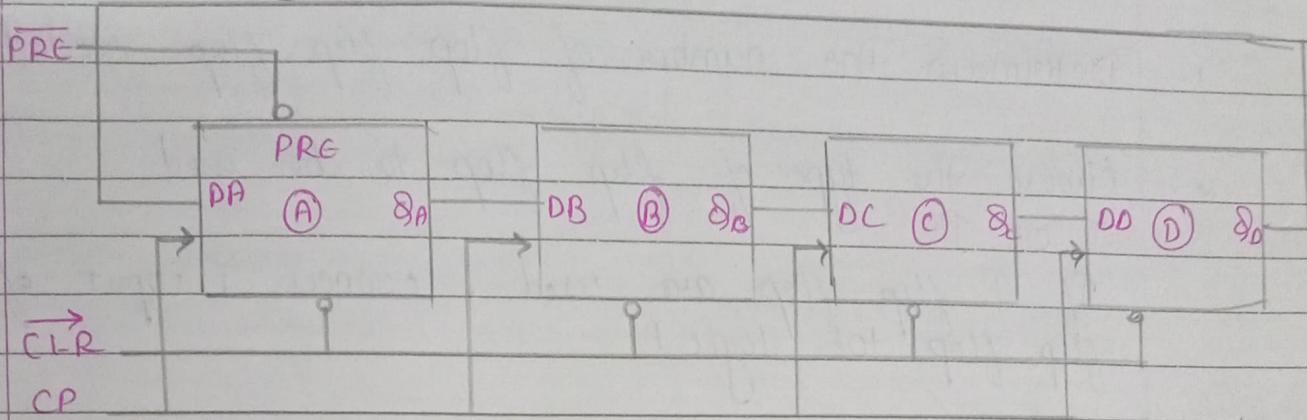
→ Shift Register

- 1) Buffer Register
 - constructed using for D flip flop. This register is called buffer register.
 - Each D flip flop is triggered with a common negative edge clock pulse
 - Input bit set up the flip flop for loading
- 2) Controlled Buffer Register
 - we can control input and output of the register by connecting tri-state device at the input and output sides of Register.
 - Tri-state switches are used to control the operations.
- 3) Shift Register
 - The Binary information of a register can be moved from stage to stage within the register.
 - This type of bit movement or shifting is essential for certain arithmetic operation and logic operation
 - This give rise of group of register called "SHIFT REGISTER"

5. Describe how to design counter using flip flop

1. Determine the number of flip flop needed.
2. Choose the type of flip flop to be used
'T' or 'JK'
If T flip flop are used, connect T input of all flip flop to logic 1.
If JK flip flop are used, connect both J and K input of all flip flop output on each clock transition.
3. Write the truth table for the counter.
4. Derive the reset logic by K-map simplification
5. Draw the logic diagram.

4) Describe Ring counter.



- The Q output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the first stage.
- The \overline{CLR} followed by PRE makes the output of the first stage to '1' and remaining output are 'zero'.
- The first clock pulse produce " $Q_B = 1$ " and remaining output "zero".
- According to the clock pulse applied at the clock input CP , a sequence of 4 stage is produced.

12. Assignment 4

CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 4

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

Assignment : 4

Module : 4

- 1. Explain weighted register / converter
- A weighted register DAC produces an analog output which is almost equal to the digital (binary) input by using binary weighted register in the inverting adder circuit.
- In short binary weighted register DAC is called as weighted register DAC
- The binary weighted currents derived from a reference voltage V_R via current scaling register $2R, 4R, 8R$.
- For on switch ; $I = \frac{V_R}{R}$ AND
For off switch ; $I = 0$
- Due to high dependence of input independent of OP-amp, summing current will flow through R_F .
- Hence, The total current through R_F can be given as ;

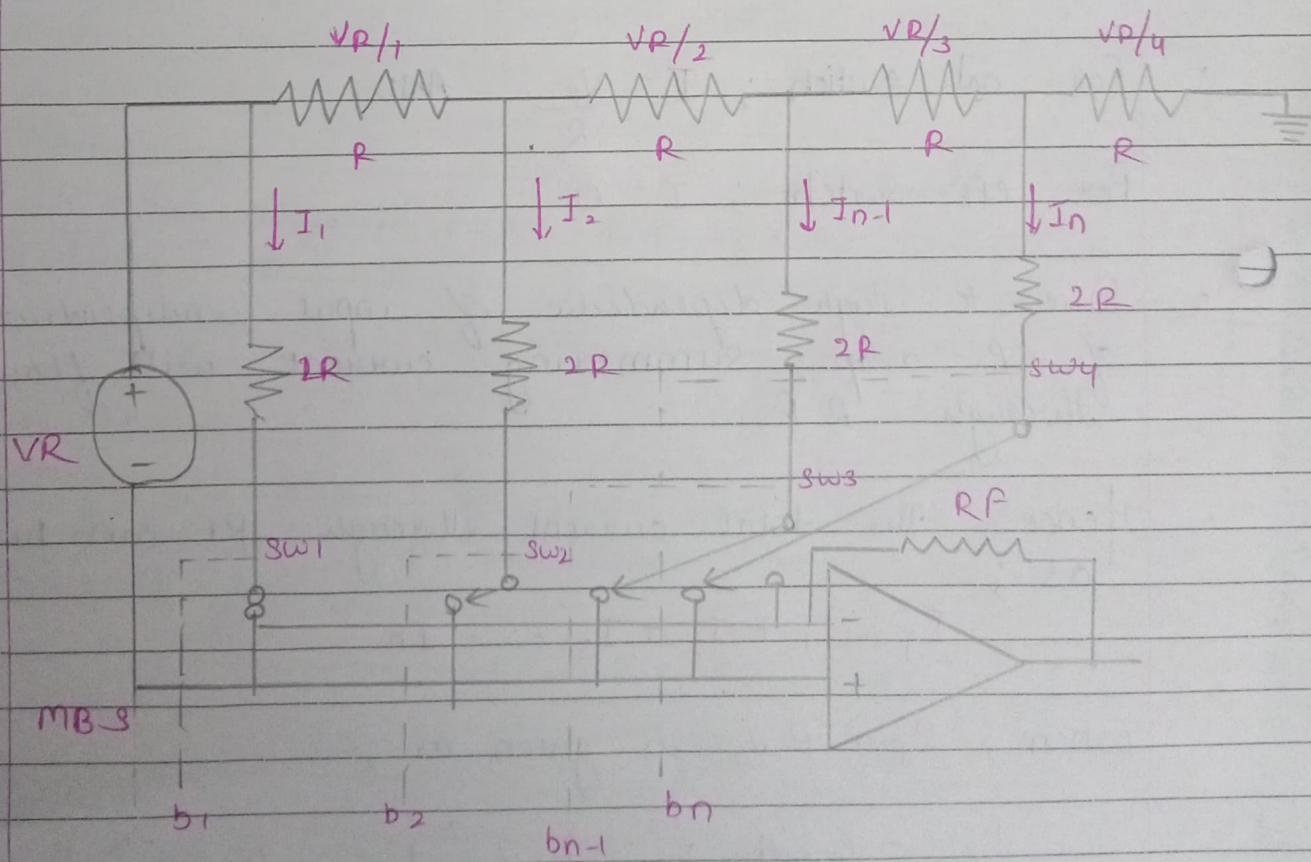
$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

when , $R_F = R \cdot V_o$ is given as ;

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})$$

2) Explain R- $\frac{1}{2}R$ Ladder D/A converter

- R/ $\frac{1}{2}R$ ladder D/A converter uses only two resistor values. This avoids resistor spread drawback of binary weighted D/A converter.
- Easier to build accurately as only two precision metal film resistors.
- Number of bits can be expanded by adding more section.
- In inverted R/ $\frac{1}{2}R$ ladder DAC, node voltage remains constant with changing input binary words.



3) Describe specification of A/D and D/A converter
 → Specification of D/A converter.

1) Resolution

- Smallest change that occurs in an analog output as a result of a change in the digital input.

$$\text{Resolution} = \text{Step Size} / \text{Full Scale} \times 100\%$$

Full Scale :

$$\text{No. of Steps} \times \text{Step Size}$$

Resolution :

$$1 / \text{number of Steps} \times 100\%$$

2) Accuracy

Specified in term of full scale error and it's linearity error.

3) Settling time

The time required for the analog output to settle to within $\pm 1/2$ LSB of the final value after a change in the digital input.

4) Monotonicity

This means that the stair case output will have no downward steps as the binary input is increased from 0 to 1.

3) Describe specification of A/D and D/A converter
→ Specification of D/A converter.

i) Resolution

- Smallest change that occurs in an analog output as a result of a change in the digital input.
- $\text{1-bit resolution} = \text{Step Size} / \text{Full Scale} \times 100\%$

• Full Scale :

$$\text{No. of Steps} \times \text{Step Size}$$

• 1-bit resolution :

$$1 - 1 \text{- bit number of Steps} \times 100\%$$

2) Accuracy

- Specified in term of full scale error and it's linearity error.

3) Settling time

The time required for the analog output to settle to within $\pm 1/2 \text{ LSB}$ of the final value after a change in the digital input.

4) Monotonicity

This means that the stair case output will have no downward steps as the binary input is increased from 0 to 1.

Specification of AD converter

- Range of input voltage
- Input independence
- Accuracy
- Conversion time
- Format of digital output

4) Explain Quantization and encoding

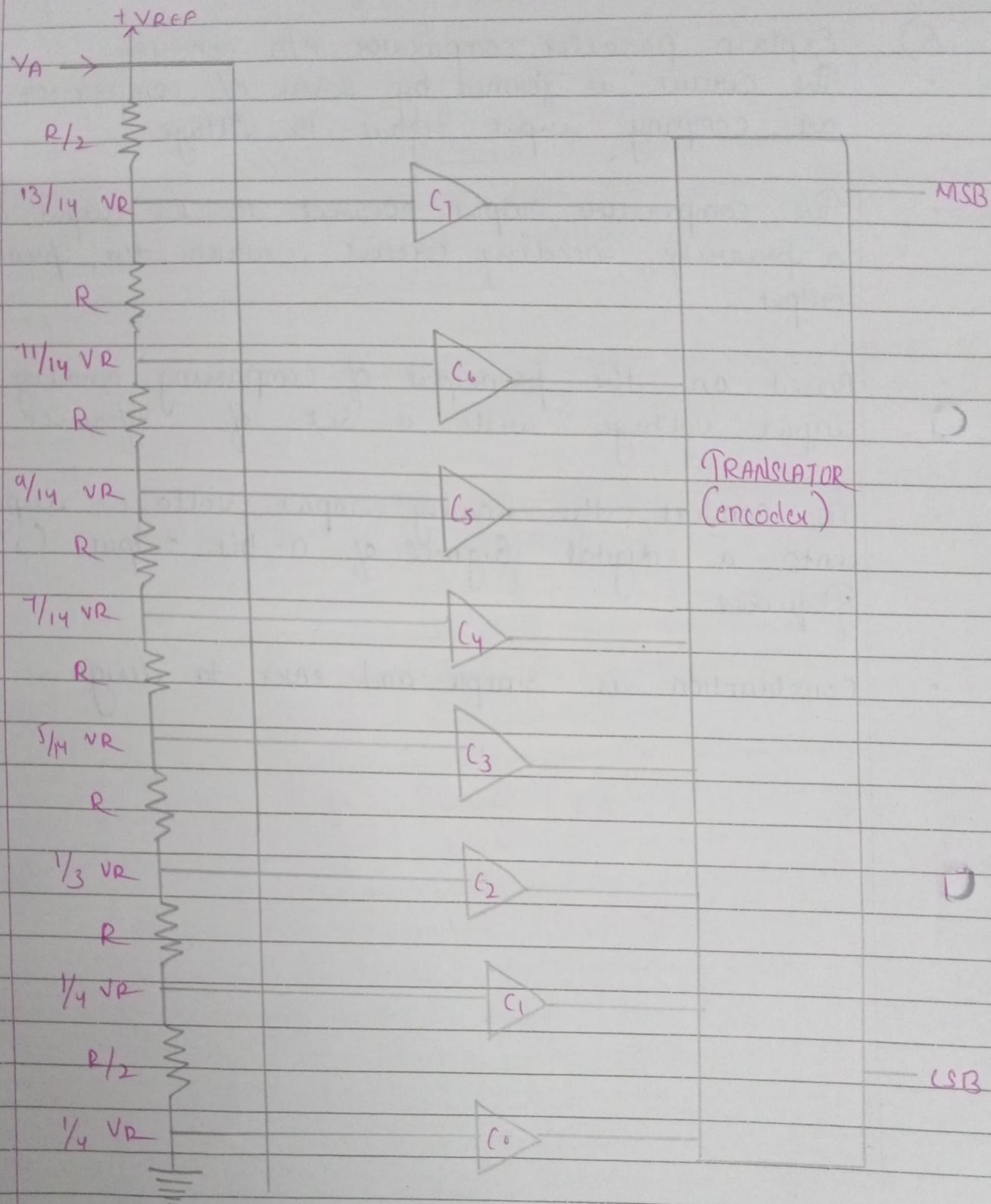
The process of mapping the sampled analog voltage value to discrete voltage level.

- which are then represented by the format of binary number.
- This is needed because the analog sample value of are real numbers.

$$q = \frac{V_{max} - V_{min}}{2^n}, I - (-I) = 0.25V$$

The value of q is more formally called the quantizer resolution.

- 5) Explain parallel comparator A/D converter.
- The circuit is formed by series of comparators each are company input signal to voltage.
- The comparators output connect to the input of the a priority encoding circuit, which produce output
- Based on the principle of comparing analog input voltage with a set of reference voltage.
- To convert the analog input voltage into a digital signal of n-bit output ($2^n - 1$) Required
- Construction is simple and easier to design.



[3-bit Flash | Parallel comparator]

13.Assignment 5

**CO5: Implement PLDs for the given logical
problem.Module 5**

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA)

Assignment : 5

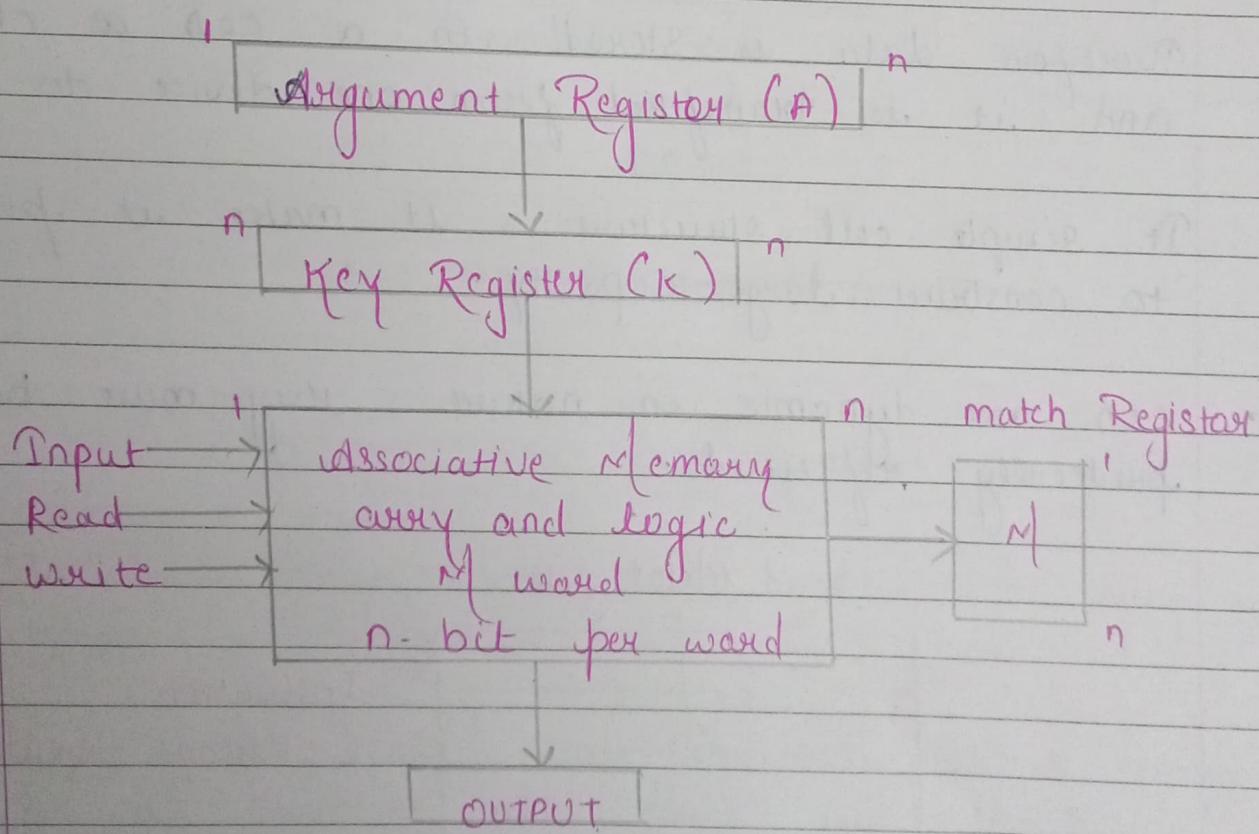
Module : 5

Explain Content Addressable memory (CAM)

The time required to find an object stored in the memory can be reduced considerably if the objects are selected.

A memory unit accessed can be the context of it is called an associative memory.

This type of memory is accessed simultaneously and in parallel on the basis of data.



(Block diagram of associative memory)

2 Explain charge coupled device memory (CCD).

charge - coupled device (CCD) memory is a type of dynamic memory in which packets of charge are continuously transferred

The structure of a nmos charge coupled device is the quite simple.

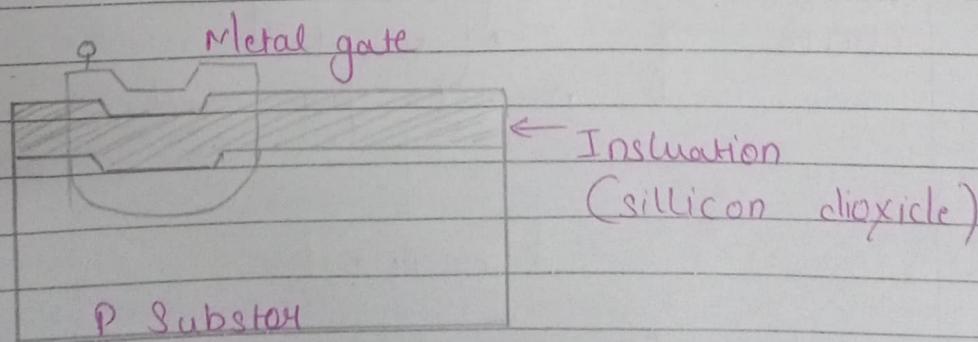
when a high voltage is applied to the metal gate hole and repel from a region.

This region called a potential well , is then capable of accepting a packet

Therefore data is stored in a CCD as charge and it is transferred from one device to another

It simple cell structure , it make it possible to construct large - capacity

CCD are dynamic in nature , they must be periodically refreshed .



3 Explain classification of memory

- Non Volatile memory

- 1) READ ONLY MEMORY (ROM)
 - i Mask Programmable ROM
 - ii Programmable ROM

- 2) READ / WRITE MEMORY (NVRAM)
 - i EEPROM
 - ii EEPROM
 - iii FLASH

- Volatile memory

- 1) READ/WRITE MEMORY (RWM)
 - a Random Access
 - i SRAM
 - ii DRAM

b Non Random Access

- i FIFO
- ii LIFO
- iii Shift Register

- The volatile memory which can be held as long as power is on
- The dynamic RAM stores the data as a charge on a capacitor after every few millisecond
- EEPROM and EEPROM are erasable memory.

4) Describe Semiconductor

- A semiconductor is a substance that has specific electrical property that enable it to serve as a foundation.
- It is typically a solid chemical element or compound that conduct electricity under certain condition but not other.
- Semiconductor are material which have a conductivity between conductor

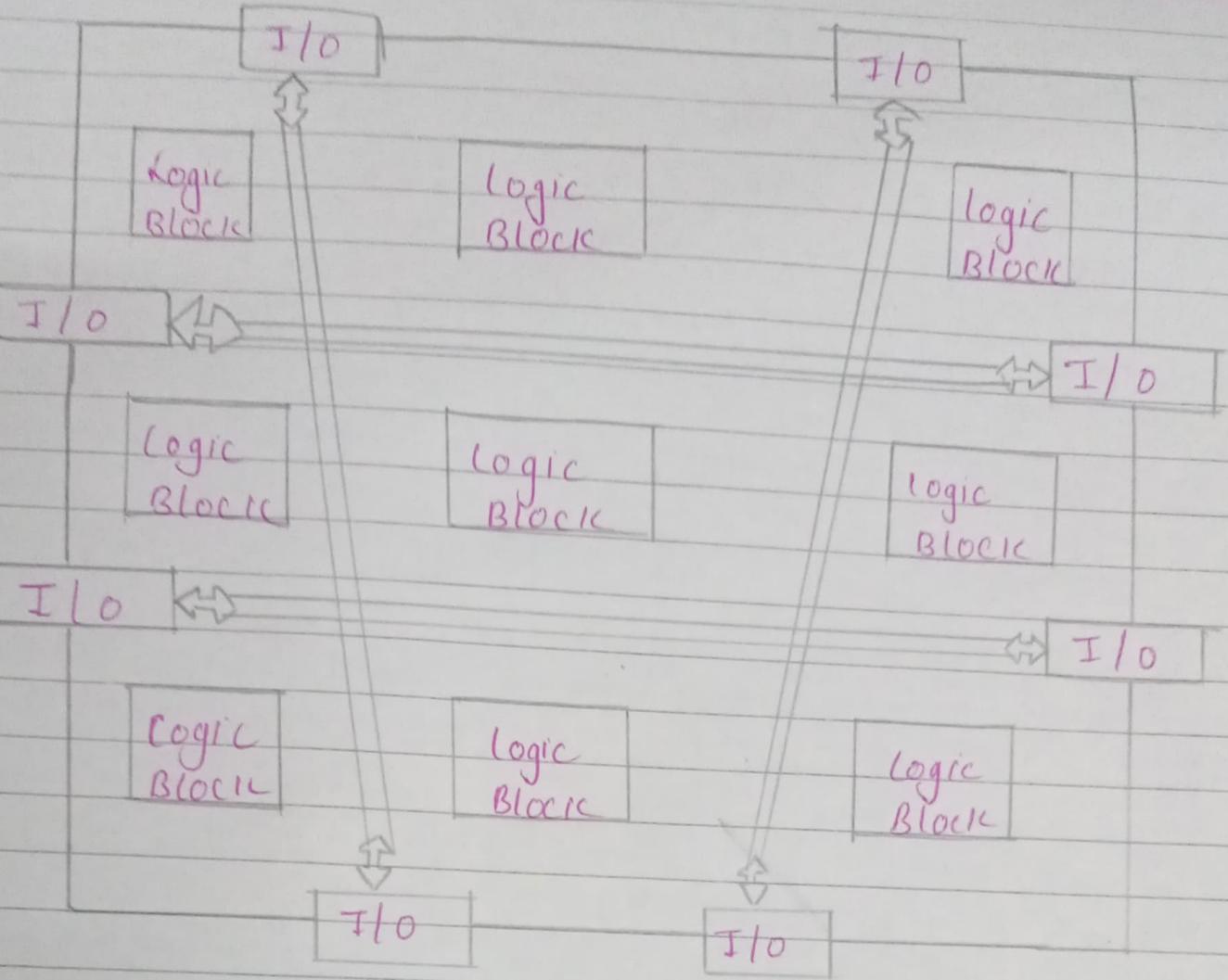
5) Explain field programmable gate array (FPGA)

- field programmable gate array (FPGA) provides the next generation in a programmable logic device

The word field is the name refer to the ability ability of the gate array to be programmed for a specific function by the user instead of a manufacture device

The word array is used to indicate the Service of column and row of gated that can be programmed.

FPGAs are called logic block or configurable logic block (CLBs)



[Basic Architecture of FPGA]

Ans