



# **Government Engineering College, Gandhinagar**

**Computer Engineering  
B.E. Semester III  
(AY 2021-22)**

**SUBJECT: Digital Fundamental ( 3130704)**



# Government Engineering College

## Sec-28 Gandhinagar

### Certificate

This is to certify that

Mr./Ms. .... Aectui ... Ratna ..... Of class

..... Division ..B..., Enrollment No ..... D.D.D.30..... Has

Satisfactorily completed his/her term work

Digital Fundamental Subject for the term ending in

...Jan..2023.

Date: -

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# **Institute Vision/Mission**

## **Vision:**

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

## **Mission:**

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

# **Computer Engineering Department**

## **Vision/Mission**

### **Vision:**

To be a premier engineering institution , imparting equality innovative solutions and environment .

### **Mission:**

- To develop human potential to its fullest extent so that intellectual and innovative engineers can merge in a wide range of professions
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and world in future .
- To produce equality engineers , entrepreneurs and leaders to meet the present and future need of society as well as environment

# Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communications skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

## PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

## POs

**Engineering Graduates will be able to:**

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## 8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1	13/09/22	14	
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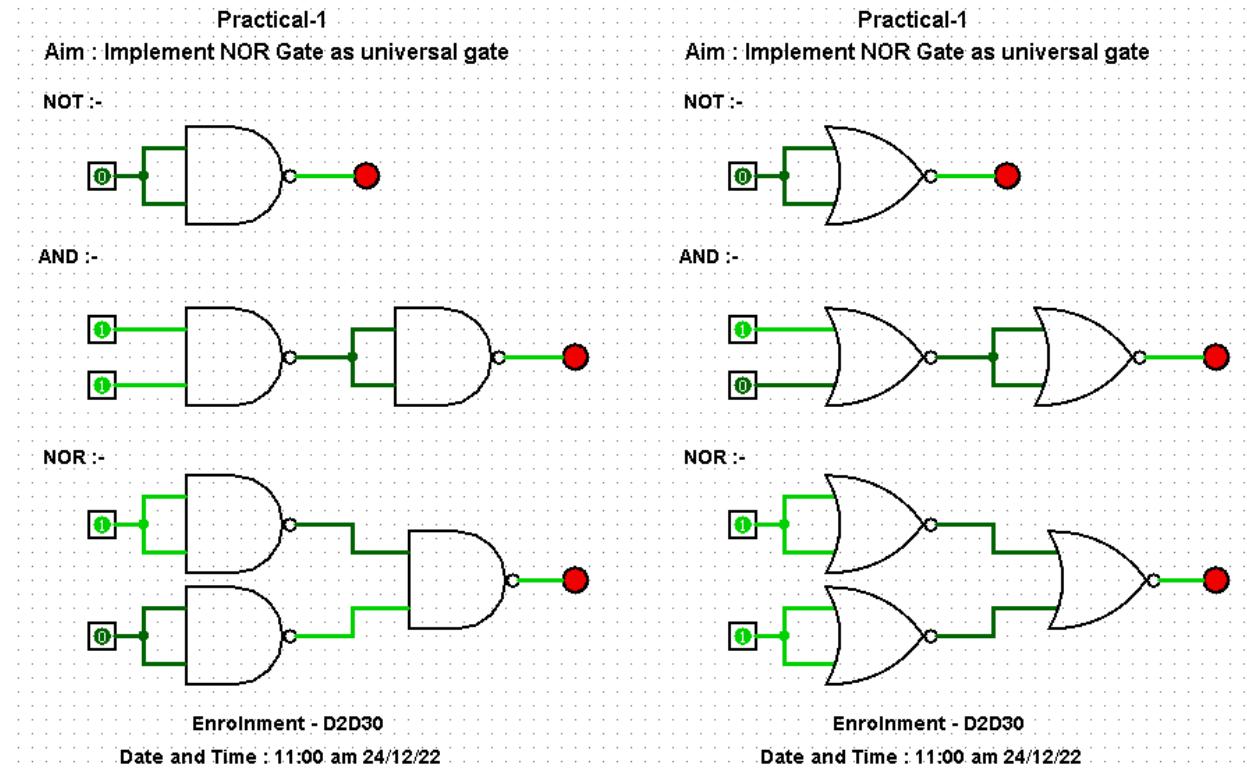
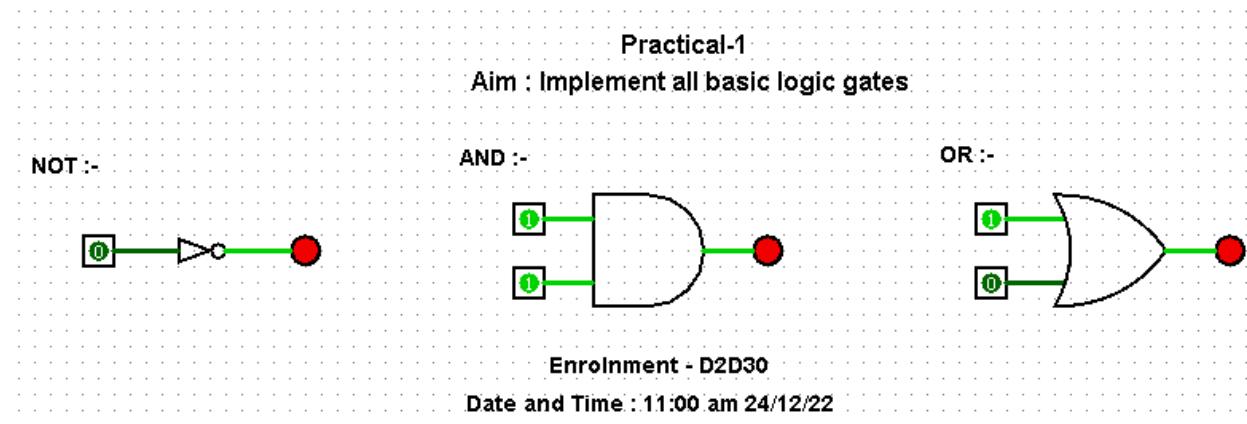
## 14.Practical 1

**CO2:** Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

### Module 1

**Aim:** Getting familiar with Logisim, Study and implement all basic logic gates.  
Implement NAND and NOR logic gates as universal gates.

**Code:**

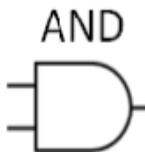


### Brief Explanation & Truth Tables:

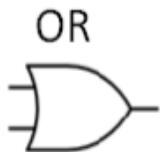
In an OR gate, the output of an OR gate attains state 1 if one or more inputs attain state 1.

In the AND gate, the output of an AND gate attains state 1 if and only if all the inputs are in state 1.

In a NOT gate, the output of a NOT gate attains state 1 if and only if the input does not attain state 1.



INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1



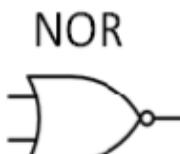
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1



INPUT		OUTPUT
A		
0		1
1		0



INPUT		OUTPUT
A	B	
0	0	1
1	0	1
0	1	1
1	1	0



INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

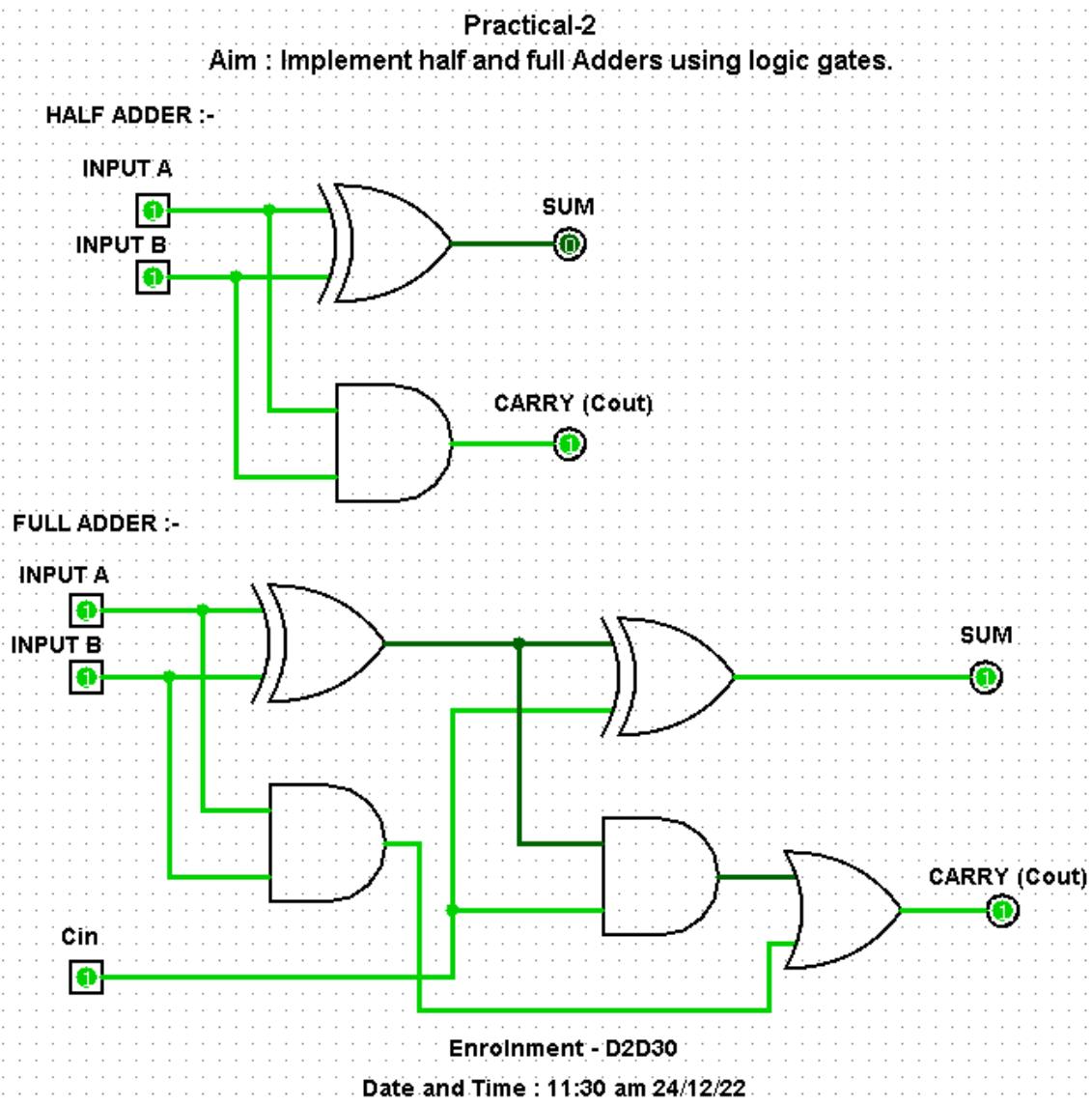
## 15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

### Module 2

Aim: Implement half and full Adders using logic gates.

Code:



### Brief Explanation & Truth Tables:

A half-adder circuit consists of two input terminals- namely A and B. Both of these add two input digits (one-bit numbers) and generate the output in the form of a carry and a sum.

Input		Output	
A	B	CARRY	SUM
0	0	0	0
1	1	1	0
0	1	0	1
1	0	0	1

The full adder adds three binary digits. Among all the three, one is the carry that we obtain from the previous addition as C-IN, and the two are inputs A and B. It designates the input carry as the C-OUT and the normal output as S

Input			Output	
A	B	C	SUM	CARRY OUT
0	0	0	0	0
1	1	1	1	1
0	1	1	0	1
1	0	1	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

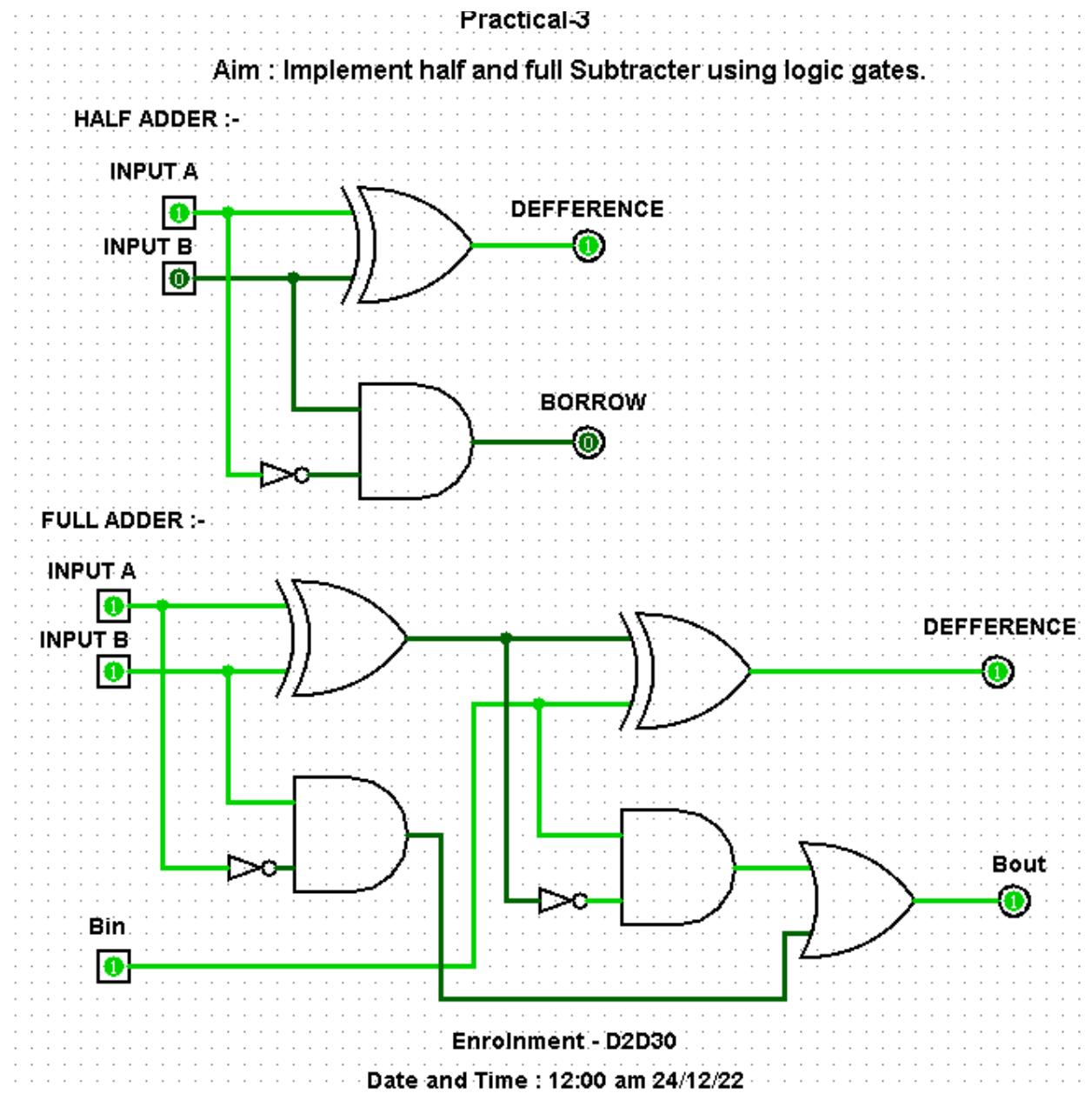
## 16. Practical 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

### Module 2

Aim: Implement half and full Subtractors using logic gates.

Code:



### **Brief Explanation & Truth Tables:**

The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively.

### **Half Subtractor Truth Tables:**

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

### **Full Subtractor Truth Table:**

Inputs			Outputs	
A	B	Borrow <sub>in</sub>	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

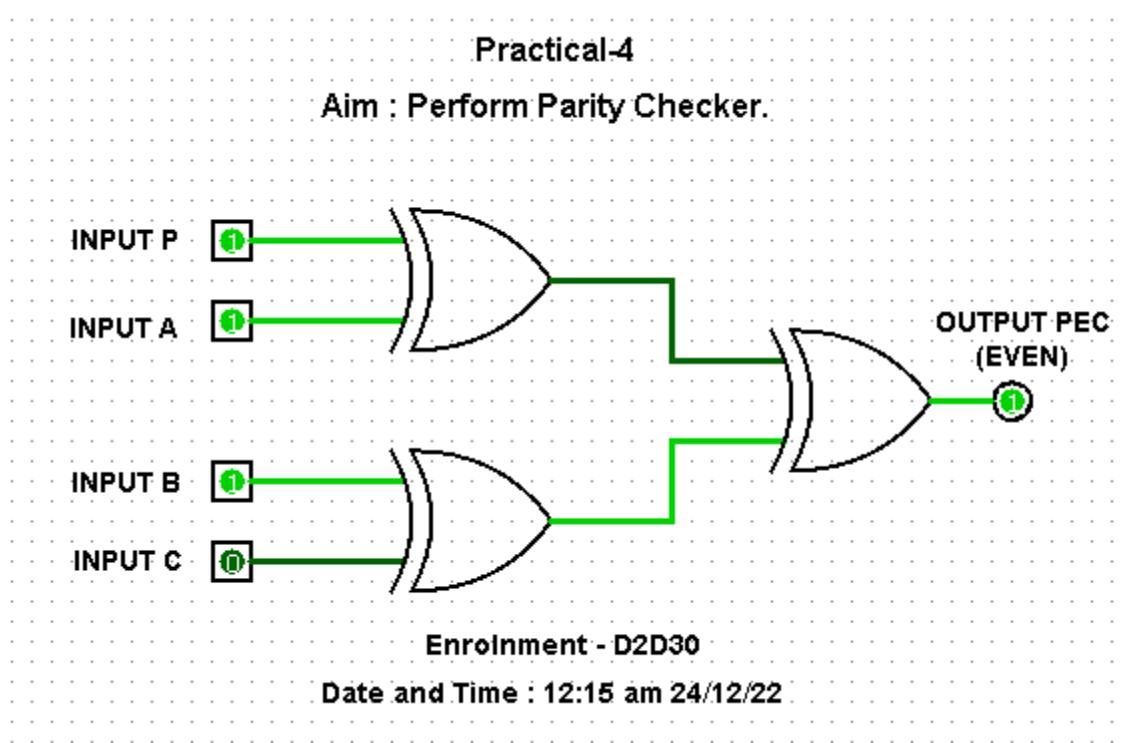
## 17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

### Module 2

Aim: Perform Parity Checker

Code:



$D_3$	$D_2$	$D_1$	$D_0$	Even-parity P	Odd-parity P
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

## 18. Practical 5

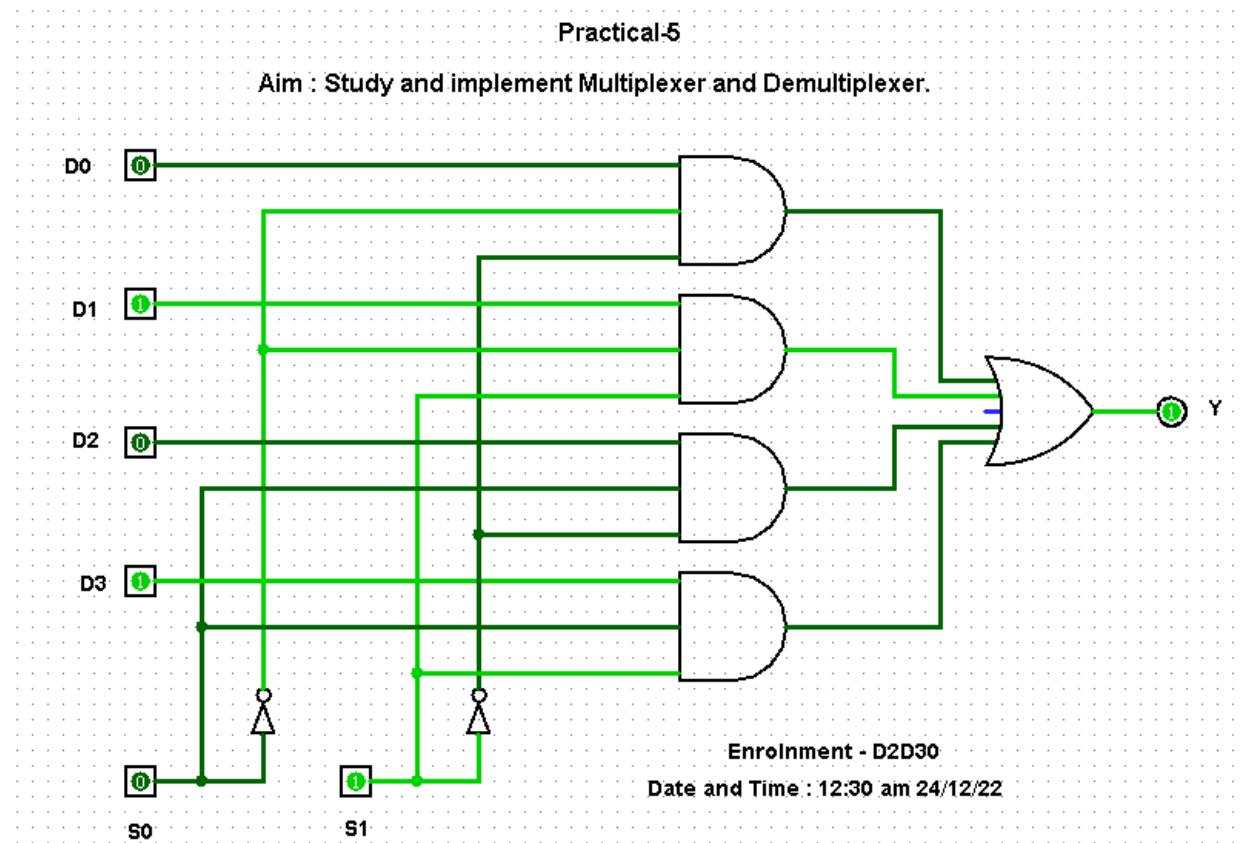
**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working.

### Module 2

**Aim:** Study and implement Multiplexer and Demultiplexer.

**Code:**

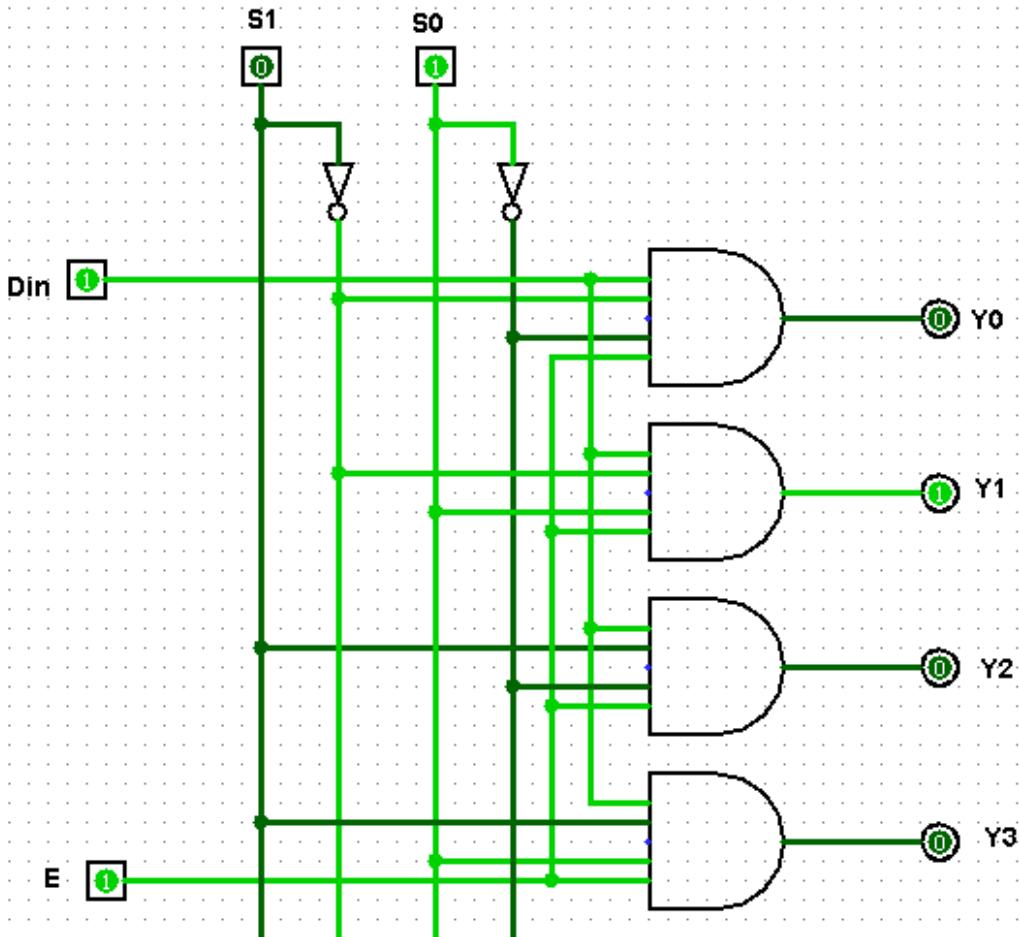
**4:1 Multiplexer**



## 1:4 Demultiplexer

### Practical-5

Aim : Study and implement Multiplexer and Demultiplexer.



Enrolment - D2D30

Date and Time : 12:30 am 24/12/22

## **Brief Explanation & Truth Tables:**

### **Multiplexer:**

A multiplexer is a combinational circuit that has  $2^n$  input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit.

INPUTS		Output
$S_1$	$S_0$	$Y$
0	0	$A_0$
0	1	$A_1$
1	0	$A_2$
1	1	$A_3$

### **Demultiplexer:**

A De-multiplexer is a combinational circuit that has only 1 input line and  $2^N$  output lines. Simply, the multiplexer is a single-input and multi-output combinational circuit.

INPUTS		Output			
$S_1$	$S_0$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	$A$
0	1	0	0	$A$	0
1	0	0	$A$	0	0
1	1	$A$	0	0	0

## 19. Practical 6

**CO3: Examine the process of Analog to Digital conversion and Digital to Analog conversion.**

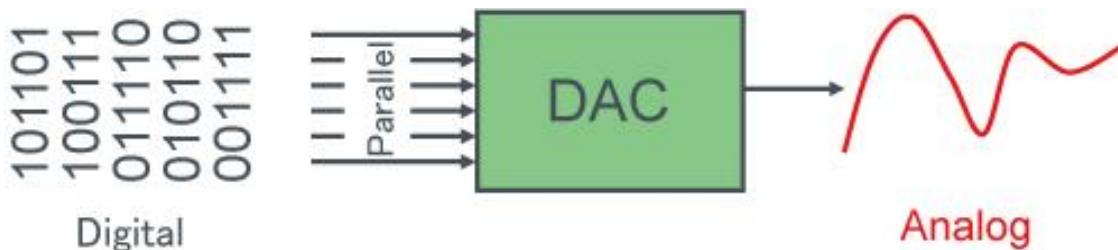
### Module 2

**Aim: Study and configure A to D convertor and D to A convertor.**

#### What is Analog to Digital Converter?

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.

- Analog signals are directly measurable quantities.
- Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.



#### Application of Analog to Digital Converter:

ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.

- Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.
- Microcontrollers commonly use 8, 10, 12, or 16-bit ADCs, our micro controller uses an 8 or 10-bit ADC

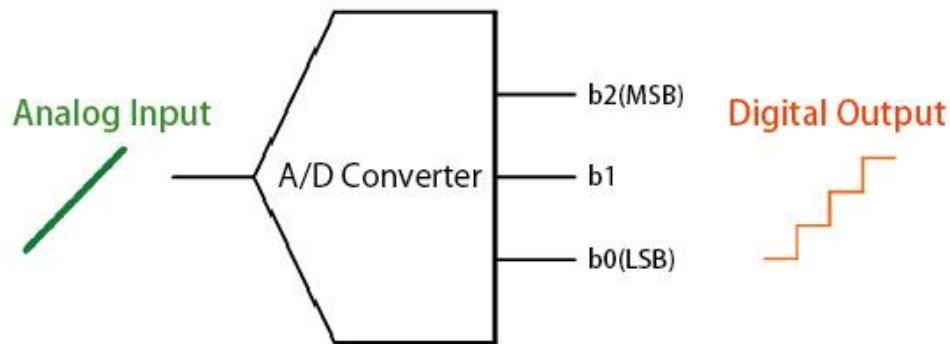
#### Types of Analog to Converters (ADC):

- Successive Approximation A/D Converter
- Flash A/D Converter
- Delta-Sigma A/D Converter

#### What is a Digital to Analog Converter?

Digital to analog converting is a process where digital signals that have a few (usually two) defined states are turned into analog signals, which have a theoretically infinite number of states. A Digital to Analog Converter, or DAC, is an electronic device that converts a digital code to an analog signal such as a voltage, current, or electric charge. Signals can easily be stored and transmitted in digital form; a DAC is used for the signal

to be recognized by human senses or non-digital systems. Converting a signal from digital to analog can degrade the signal.



### **Applications for Digital to Analog Converters:**

An example can be found in the processing of computer data by a modem into audio-frequency tones transmitted over a telephone line. The circuit that performs this is a digital to analog converter. In music players, digital to analog converters can be used for generation of audio signals from digital information. In TVs and cell phones, digital video signals are converted into analog in order to display colors and shades.

In VoIP applications, the source is first digitized for transmission through an analog to digital converter and is then reconstructed into an analog signal using a DAC at the receiving end.

### **Types of Digital to Analog Converter (DAC):**

- Binary Weighted Resistor D/A Converter Circuit
- Binary ladder or R–2R ladder D/A Converter Circuit
- Segmented DAC
- Delta-Sigma DAC

### **Analog Signal to Digital Signal Conversion Methods:**

#### **1. Sampling:**

Sampling is the process of taking amplitude values of the continuous analog signal at discrete time intervals (sampling period  $T_s$ ).

[Sampling Period  $T_s = 1/F_s$  (Sampling Frequency)]

Sampling is performed using a Sample and Hold (S&H) circuit.

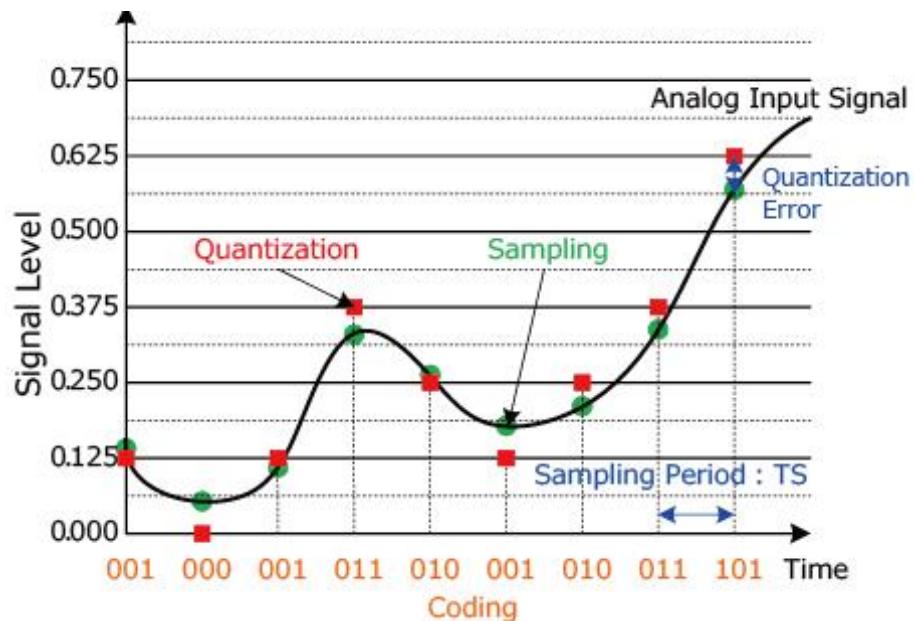
#### **2. Quantization:**

Quantization involves assigning a numerical value to each sampled amplitude value from a range of possible values covering the entire amplitude range (based on the number of bits).

[Quantization error: Sampled Value - Quantized Value]

### 3. Coding:

Once the amplitude values have been quantized they are encoded into binary using an Encoder.



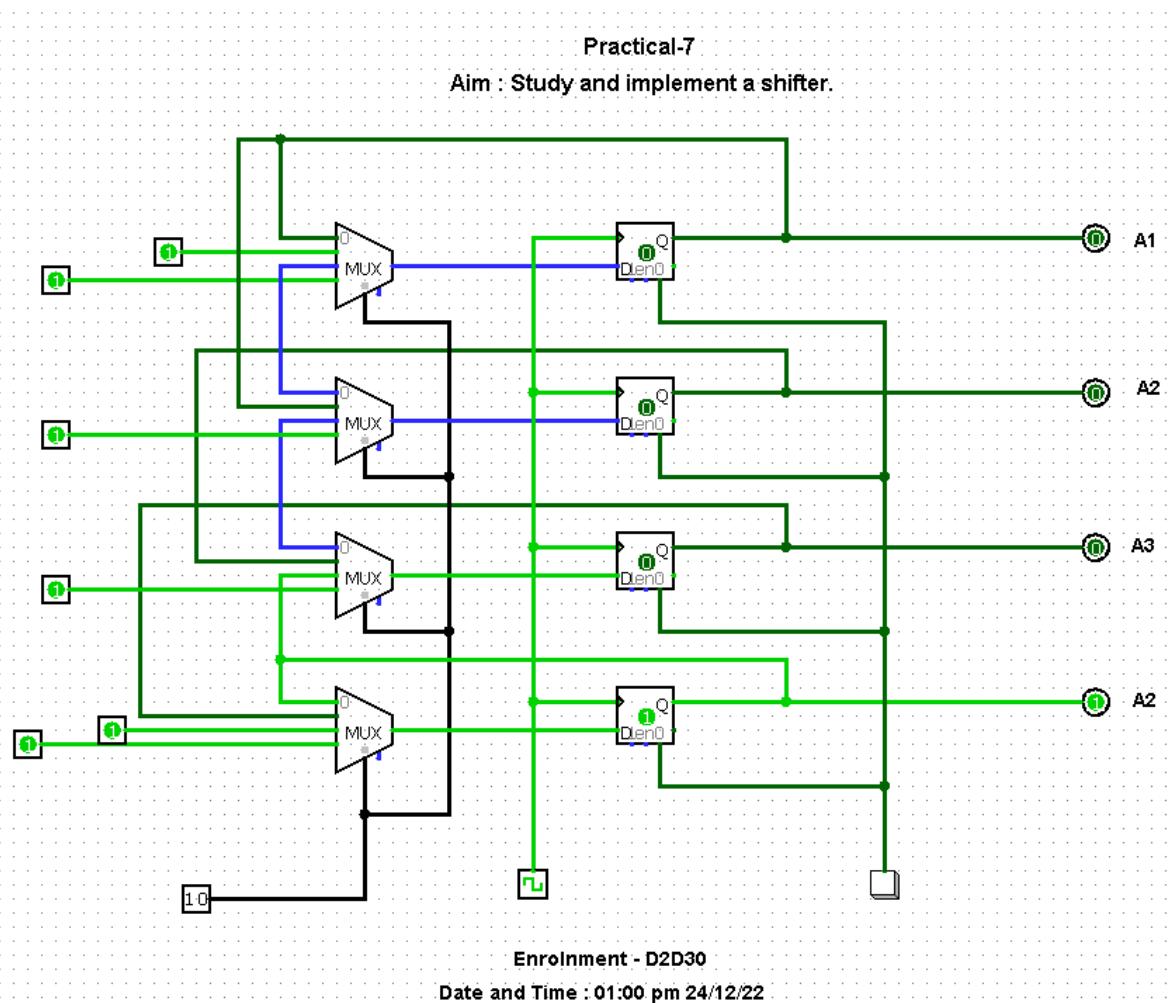
## 20. Practical 7

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

### Module 2

Aim: Study and implement a shifter.

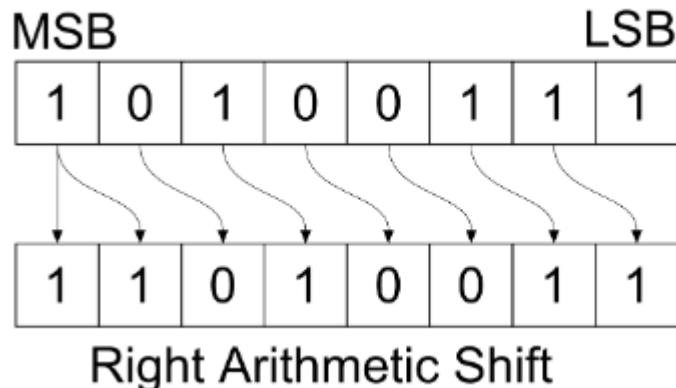
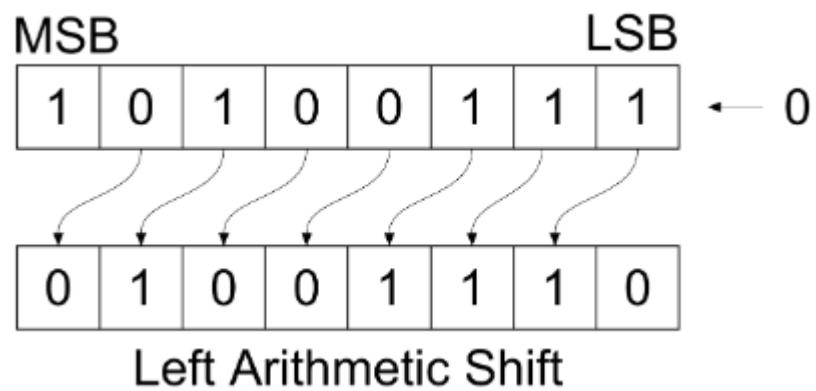
Code:



### Brief Explanation & Truth Tables:

**Arithmetic Shifter** : is the same as a logical shifter, but on right shifts fills the most significant bits with a copy of the old most significant bit (MSB). This is useful for multiplying and dividing signed numbers Arithmetic shift left (ASL) is the same as logical shift left (LSL).

### Truth Table:



## 21. Practical 8

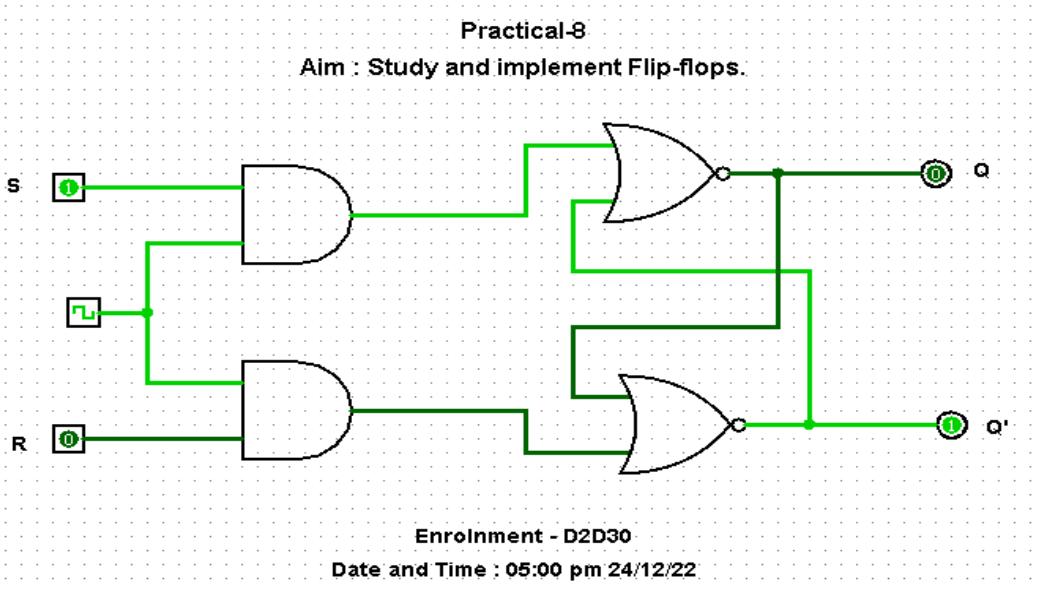
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

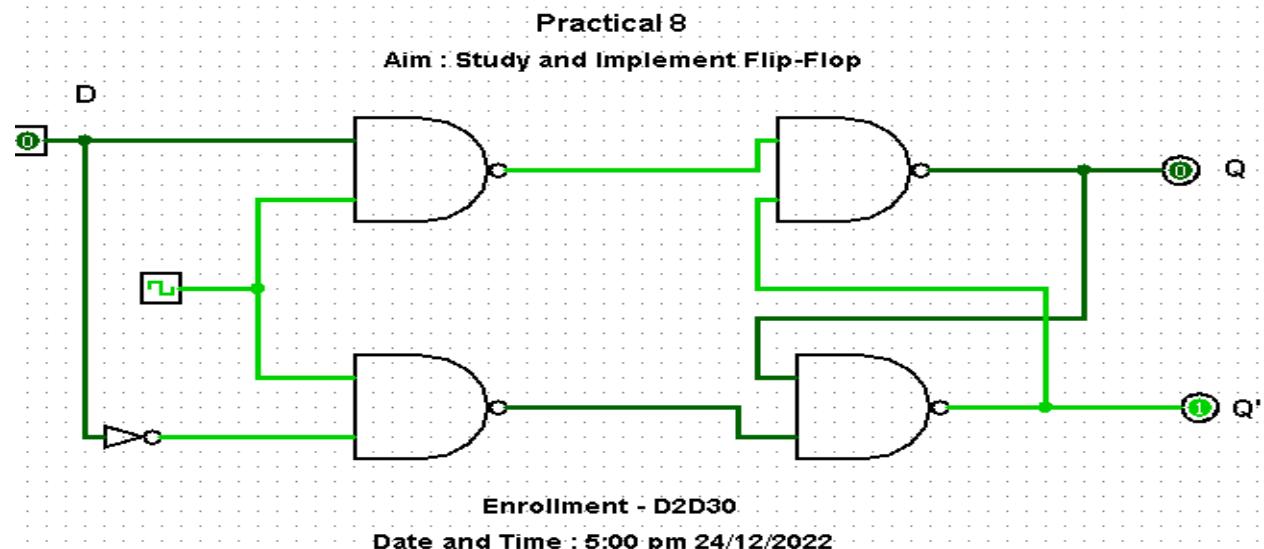
Aim: Study and implement Flip-flops.

Code:

SR Flip Flop



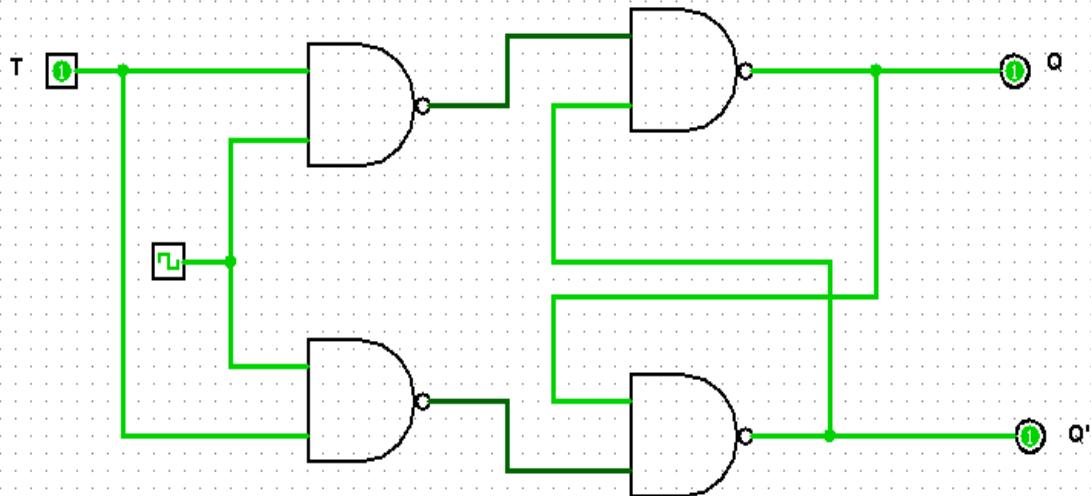
D Flip Flop



## T Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



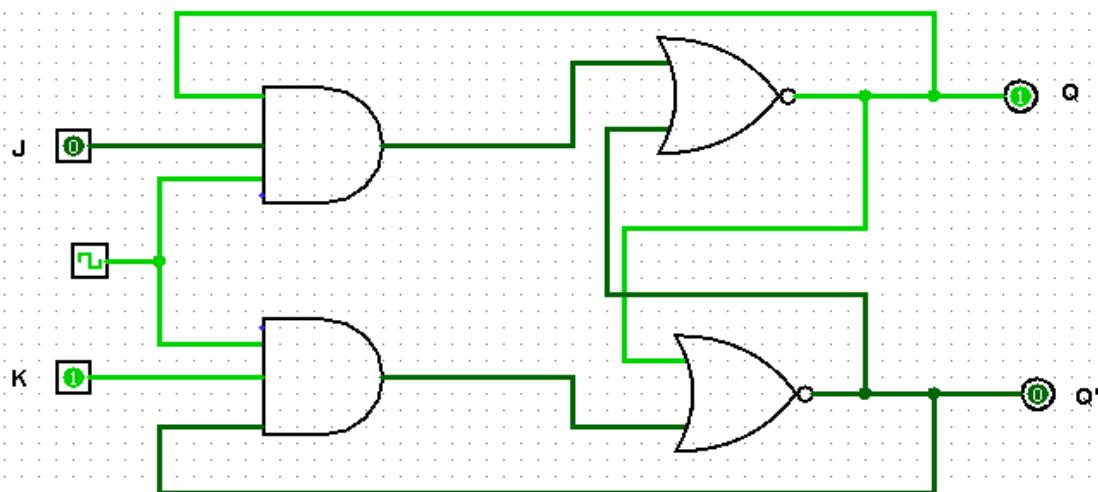
Enrolment - D2D30

Date and Time : 05:00 pm 24/12/22

## JK Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



Enrolment - D2D30

Date and Time : 05:00 pm 24/12/22

## Brief Explanation & Truth Tables:

### SR Flip Flop

A gated SR latch requires an Enable (EN) input.

Its S and R inputs will control the state of the flip flop only when the EN is high.

When EN is low, the inputs become ineffective and no change of state can take place.

#### Truth Table

En	S	R	$Q_n$	$Q_{n+1}$	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate (Invalid)
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

### D Flip Flop

It differs from the S-R latch in that has only one input in addition to EN.

When D=1, we have S=1 and R=0, causing the latch to SET when ENABLED

When D=0, we have S=0 and R=1, causing the latch to RESET when ENABLED

#### Truth Table

En	D	$Q_n$	$Q_{n+1}$	State
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set
1	1	1	1	
0	X	0	0	No Change (NC)
0	X	1	1	

## JK Flip Flop

The JK flip flop is very versatile and also the most widely used.

The functioning of the JK flip flop is identical to that of the SR flip flop, except that it has no invalid state like that of SR flip flop.

### Truth Table

En	J	K	Q <sub>n</sub>	Q <sub>n+1</sub>	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	0	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

## T Flip Flop

A T flip flop has a single control input, labeled T for toggle.

When T is HIGH the flip flop toggles on every new clock pulse.

When T is LOW the flip flop remains in whatever state it was before.

### Truth Table

En	T	Q <sub>n</sub>	Q <sub>n+1</sub>	State
1	0	0	0	No Change (NC)
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	
0	X	0	0	No Change (NC)
0	X	1	1	

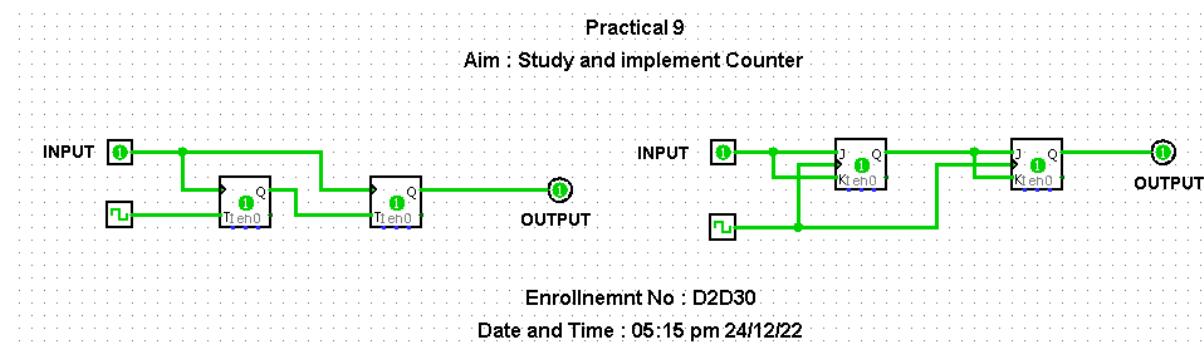
## 22. Practical 9

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working**

### Module 3

**Aim: Study and Implement Counter**

**Code:**



**Brief Explanation & Truth Tables:**

### Asynchronous Counter

The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle(T) flip-flops are being used. But we can use the JK flip-flop also with J and K connected permanently to logic

External clock is applied to the clock input of flip-flop A and Q A output is applied To the clock input of the next flip-flop.

### Synchronous Counter

If the “Clock” pulses are applied to all the flip flop in counter simultaneously, Then such a counters are called synchronous counter.

In this type of counter there is no connection between the output of first FF and clock input of next FF and so on.

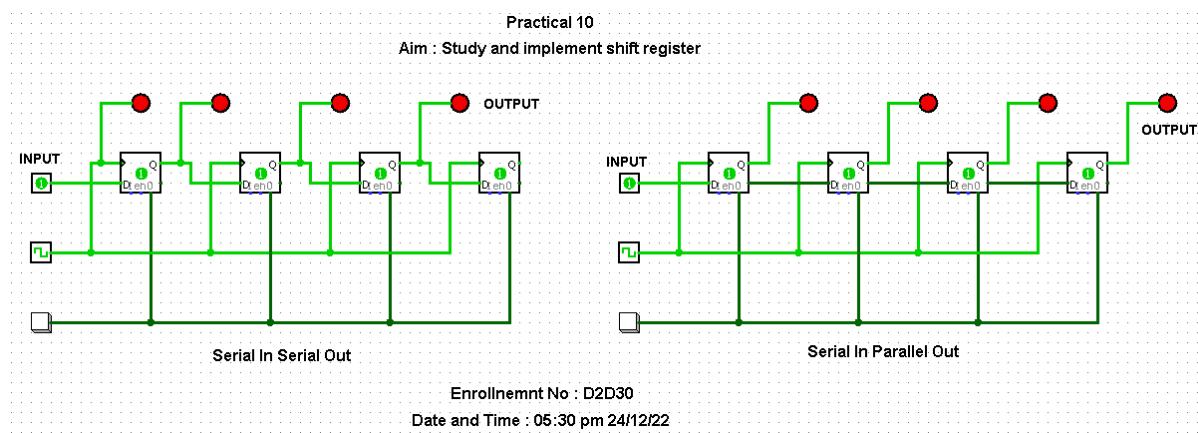
## 23. Practical 10

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

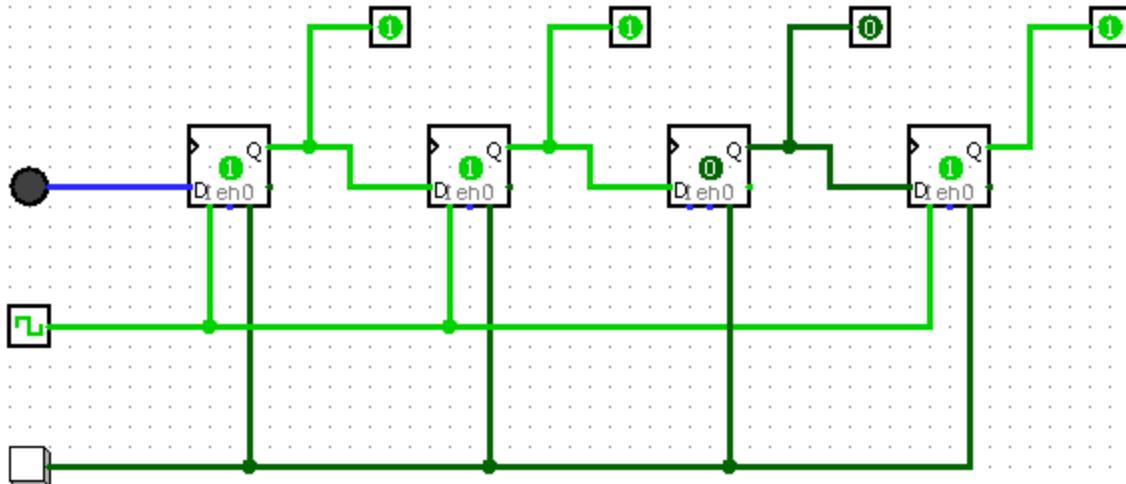
### Module 3

Aim: Study and Implement a shift register

Code:



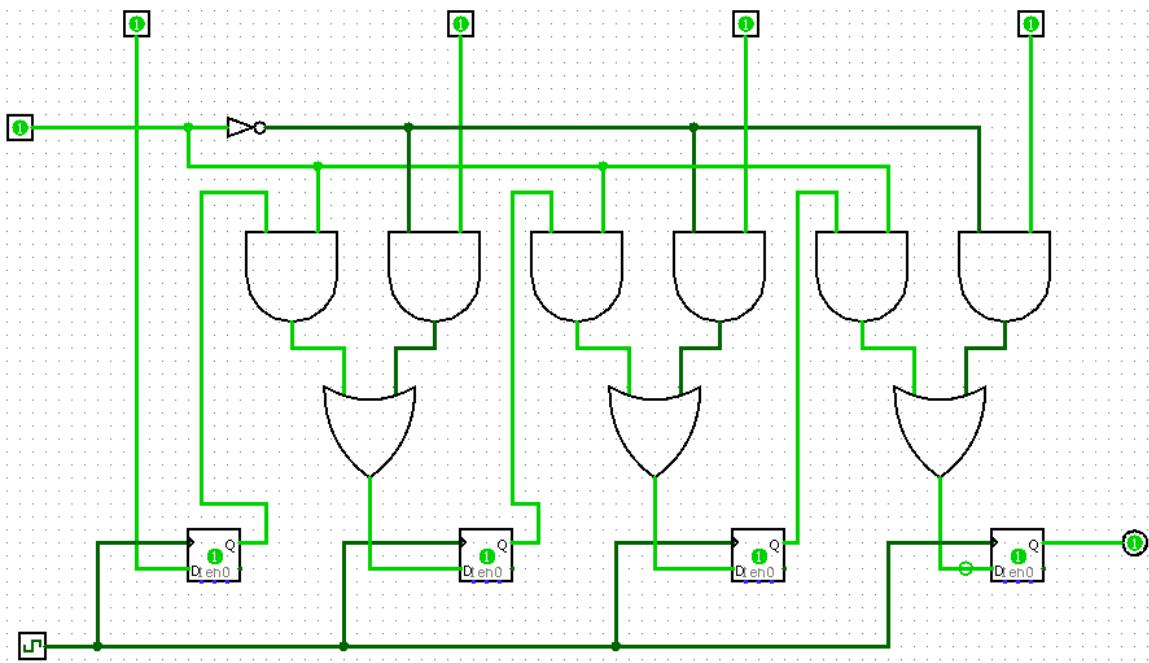
Practical 10  
Aim : Study and implement shift register



Enrollment No : D2D30  
Date and Time : 05:30 pm 24/12/22

Practical 10

Aim : Study and implement shift register



Enrollment No : D2D30

Date and Time : 05:30 pm 24/12/22

### Brief Explanation:

A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.

Data may be shifted into or out of the register either in serial form or in parallel form.

So, there are four basic types of shift registers:

- serial-in, serial-out
- serial-in, parallel-out
- parallel-in, serial-out
- parallel-in, parallel-out

Data may be rotated left or right. Data may be shifted from left to right or right to left at will, i.e. in a bidirectional way.

Also, data may be shifted in serially (in either way) or in parallel and shifted out serially (in either way) or in parallel.

## 24. Practical 11

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working**

### Module 3

**Aim: Study and Implement K-Map for the given function:(SOP)**

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

#### Code:

Step 1: Finding the number of variables to build the K-map

$$\text{Number of variables} = 4(A,B,C,D)$$

So 4 variable K-map is to be used

Step 2: Filling cells of K-map for SOP with 1 respective to the min-terms for given equation

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	0	1	3	4	
	01	4	5	7	6	
	11	12	13	15	14	
	10	8	9	11	10	

Step 3: We create rectangular groups that contain total terms in the power of two like 2,4,8 and so on. Try to cover as many elements as we can cover in one group.

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	1	0	1	3	1 4
	01	4	5	7	6	
	11	12	1 13	15	14	
	10	1	8	9	11	1 10

Step 4: With the help of these groups, we find the product terms and sum of them for the SOP form  $Y = ABC'D + B'D'$

# Digital Fundamental (3130704)

## Course Outcomes (COs)

CO-1	Solve the given problem using fundamentals of number systems and Boolean Algebra
CO-2	Analyze working of logic families and logic gates and design simple circuits using various gates
CO-3	Design and implement combinational and sequential logic circuits and verify its working
CO-4	Examine the process of Analog to digital conversion and digital to Analog conversion
CO-5	Implement PLDs for given logical problem.

## 7. Assignment Index

Sr. No	Assignment	Date	Page No.	Sign
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3	Assignment 3	30/11/22		Nisha
4	Assignment 4	14/12/22		
5	Assignment 5	30/12/22		

## **9. Assignment 1**

**CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra**

### **Module 1**

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function:  $F=A'B'C+A'BC+AB'$ .
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

## Assignment - 1

### Module 1

Q1 : Solve the given problem using Fundamentals of Number Systems and Boolean Algebra.

Q2 State and Explain De Morgan's theorem with truth tables

→ De Morgan suggested two theorems that form an important part of Boolean Algebra

$$(1) \overline{AB} = \bar{A} + \bar{B}$$

The complement of product is equal to the sum of the complements

Truth Table:

A	B	$\overline{AB}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

$$(2) \overline{A+B} = \bar{A} \cdot \bar{B}$$

The complement of a sum is equal to the product of the complements

Truth Table:

A	B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Q2 Simplify Boolean Functions

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}$$

$$= \bar{A}C(\bar{B} + B) + A\bar{B}$$

$$= \bar{A}C + A\bar{B}$$

$$[A + \bar{A} = 1]$$

$$\boxed{F = \bar{A}C + A\bar{B}}$$

Q3 List and explain Logic family

(1) Bipolar

(a) Saturated

- Register Transistor Logic [RTL]
- Diode Transistor Logic [DTL]
- Direct Coupled Transistor Logic [DCTL]
- Integrated Injection Logic [I<sup>2</sup>L]
- High Threshold Logic [HTL]
- Transistor Transistor Logic [TTL]

(b) Unsaturated

- p-channel MOSFET (PMOS)
- n-channel MOSFET (NMOS)
- Complementary MOSFET (CMOS)

It is a group of compatible ICs with the same logic level and supply voltages for performing various logic functions. They are fabricated using a specific circuit configuration which is referred as logic family. The circuit design of the basic gate of each logic family is same.

## • Transistor - Transistor Logic [TTL]

- It is named for its independence on transistors alone to perform basic logic operations

## • Schottky TTL

- A Schottky Transistor is a combination of a Transistor and a Schottky Diode that prevent the diode the transistors from saturating by diverting the excessive input current. It is also called Schottky Transistor

## • CMOS - Complementary metal oxide semiconductor

It is a type of metal-oxide semiconductor field effect transistor fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFET's for logic functions

## Q4) Describe error detecting and correcting code

- To maintain the data integrity bet<sup>n</sup> transmitter & receiver, extra bit or more than one bit are added in the data. These extra bits allows the detection and some times correction of error in data. The data along with extra bit forms the codes. Codes which allow only error detection are called error detecting and correcting code

Parity code - Even Parity code  
Odd Parity code

Even Parity code: The value of even parity bit should be zero, if even number of ones present in the binary code; otherwise, it should be one. So that, even number of ones present is even parity code.

<u>Binary Code</u>	<u>Even Parity bit</u>	<u>Even Parity code</u>
000	0	0000
001	1	0011
010	1	0101
011	0	0110
100	1	1001
101	0	1010
110	0	1100
111	1	1111

Odd Parity code - The value of odd Parity <sup>bit</sup> code, should be zero, if odd number of ones present in the binary code. Otherwise, should be one. So odd no. of ones present in parity odd parity code.

<u>Binary code</u>	<u>odd Parity bit</u>	<u>odd Parity code</u>
000	1	0001
001	0	0010
010	0	0100
011	1	0111
100	0	1000
101	1	1011
110	1	1101
111	0	1110

## → Hamming code

It is useful for both detection and correction of error present in the received data. This code uses multiple parity bits and we have to place these parity bits position of powers of 2.

Bit designation	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub> P <sub>4</sub>	D <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>
Bit location	7	6	5	4	3	2	1
Binary location number	111	110	101	100	011	010	001

Parity P<sub>1</sub> checks bit locations 1, 3, 5, 7 and assigns P<sub>1</sub> according to even or odd parity.

Parity P<sub>2</sub> checks bit locations 2, 3, 6, 7 and assigns P<sub>2</sub> according to even or odd parity.

Parity P<sub>4</sub> checks bit locations 4, 5, 6, 7 and assigns P<sub>4</sub> according to even or odd parity.

## Q5 Differentiate TTL, Schottky TTL and CMOS

Parameter	CMOS	TTL	Schottky TTL
Device used	N-channel P-channel MOSFET	Unipolar N Transistor	Schottky diode
V <sub>IH</sub> (min)	3.5 V	2 V	2 V
V <sub>IL</sub> (max)	1.5 V	0.8 V	0.8 V
V <sub>OH</sub> (min)	4.95 V	2.7 V	2.7 V
V <sub>OL</sub> (max)	0.005 V	0.4 V	0.5 V
Power	0.1 mW	10 mW	1 mW
Dissipation per gate Moore			
Fanout	50	10	50
Application	Portable instrument where battery supply is used	laboratory instruments	Voltage clamping application to prevent transistor saturation

# **10. Assignment 2**

**CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem**

## **Module 2**

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
  - 2.1.  $F(x,y,z) = \Sigma (2,3,6,7)$
  - 2.2.  $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

## Assignment 2

C02: Analyze working of logic families and logic gates and design the simple circuits using various gate for given problem.

### Module 2

Q1 Explain K-Map

- The map method gives us a systematic approach for simplifying a Boolean expression
  - The basis of this method is graphically chart known as Karnaugh map.
  - It contains boxes called cells.
- Each of cell represents one of  $2^n$  possible products that can be formed from  $n$  variables. Thus, a 2-variable map contains 4 cells ( $2^2$ ) 3-variable contains 8 cells ( $2^3$ ) and so on.

2 Variable	
A 0	0
A 1	1

[2 cells]

2 Variable	
B A 0	0
B A 1	1

[4 cells]

3 Variable	
AB 00	AB 01
CD 00	CD 01
CD 10	CD 11

[8 cells]

4 Variable	
AB 00	AB 01
CD 00	CD 01
CD 10	CD 11

[16 cells]

Q2 Obtain simplified expression in sum of product for following Boolean Functions

$$2.1) F(x_1, y_1, z) = \Sigma \{2, 3, 6, 7\}$$

	$x_1 y_1 z$	$\bar{x}_1 y_1 z$	$x_1 \bar{y}_1 z$	$\bar{x}_1 \bar{y}_1 z$	$x_1 y_1 \bar{z}$	$\bar{x}_1 y_1 \bar{z}$	$x_1 \bar{y}_1 \bar{z}$	$\bar{x}_1 \bar{y}_1 \bar{z}$
$\bar{z}$	0	1	2	3	6	7	4	5
$\bar{y}_1$	0	1	2	3	6	7	4	5
$y_1$	1	2	3	4	5	6	7	8

$$F = y_1$$

$$2.2) F(A, B, C, D) = \Sigma \{4, 6, 7, 15\}$$

	$AB$	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$
$\bar{C}\bar{D}$	0	1	2	3	4	5	6	7
$\bar{C}D$	8	9	10	11	12	13	14	15
$C\bar{D}$	16	17	18	19	20	21	22	23
$CD$	24	25	26	27	28	29	30	31

$$F = \bar{A}B\bar{D} + BCD.$$

Q3 Describe Adder and subtractor

### Adder -

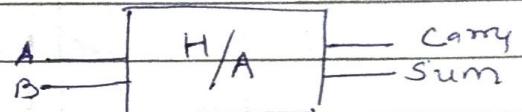
#### • Half Adder

- Two binary inputs - augend & addend bits
- Two binary outputs - sum and carry

Truth Table

Block Diagram

A	B	C +	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



#### • Full Adder

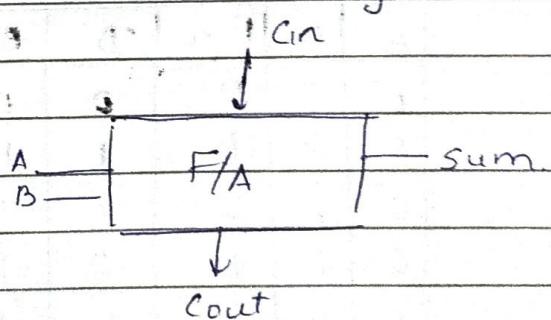
Three binary inputs : augend, adder, previous

two binary inputs : carry & sum (carry)

Truth table

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Block Diagram



## Subtractor

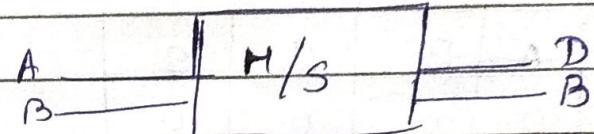
- Half Subtractor

- Two inputs and two outputs which is difference and borrow

Truth Table

A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Block Diagram



- Full Subtractor

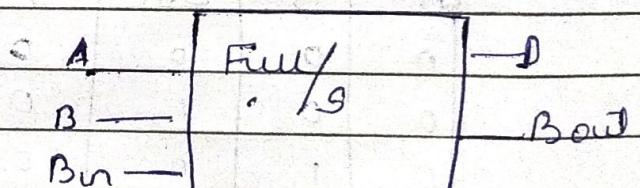
Three inputs : minuend, subtractend and borrow

Two outputs : difference and borrow

Truth Table

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Block Diagram



Q4 Explain multiplexer and De-multiplexer

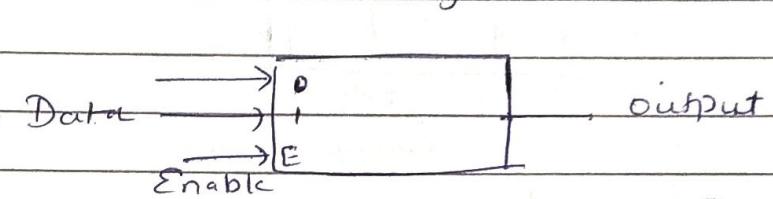
- To select single data line from several data input lines and the data from the selected data line should be available on the output. The digital circuit which does this task is a multiplexer.

### 2:1 Multiplexer

Function table

E	S	Y
I	C	D <sub>0</sub>
I	I	D <sub>1</sub>
0	X	0

Block Diagram

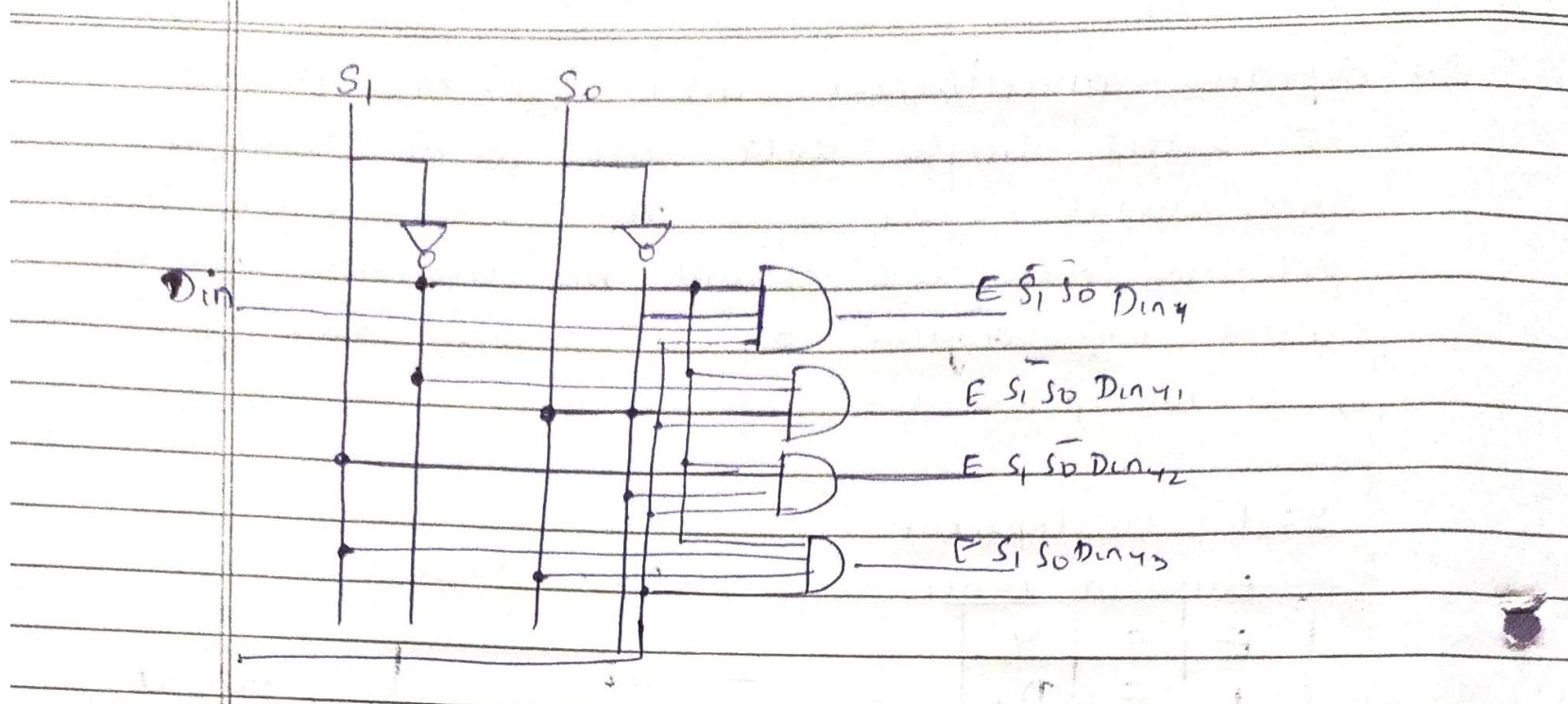


### \* De Multiplexer

- A circuit that receives information on a single line and transmits this information on one of  $2^n$  possible output lines. The selection of specific output line is controlled by values of n selection lines.

### 1:4 Demultiplexer

E	S <sub>1</sub>	S <sub>0</sub>	Din	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1



Q5 Describe Parity checker and generator

### Parity Generator

- used for purpose of detecting error during transmission and binary information

The circuit that generates the parity bit in the transmitter is called parity generator and the circuit that checks the parity in the receiver is called parity checker

A	B	C	odd parity bit	Even parity bit
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

### Parity Checker

The Three bits in the message together with the parity bit are transmitted to their destination where they are applied to parity checker circuit.

~~The parity checker for Possible error in the transmission.~~

Truth table

Decimal Equivalent	P	A	B	C	Parity error check [PEC]
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

# **11. Assignment 3**

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## **Module 3**

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

## Assignment 3

CO3 : Design and implement combinational and sequential logic circuits and verify the working.

### Module 3

Q1 Differentiate b/w

#### Sequential Circuits

- The output variables depend not only on the present input variables but they also depend upon the past history of these input variable

→ Harder to design

→ Serial adder is a Sequential circuit

→ Sequential, slower than combinational circuits

#### Combinational Circuits

- In combinational circuit, the output variables are at all times dependent on the combination of input variables

→ Easy to design

→ Parallel adder is a combinational circuit.

→ Faster in speed

(g) List and explain Flip-Flops

(a) JK Flip-Flop

(b) D Flip-Flop

(c) T Flip-Flop

(d) SR Flip-Flop

~~JK~~

### (a) JK flip flop

- The data inputs are J and K which are ANDED with  $Q$  and  $\bar{Q}$  respectively, to obtain S and R inputs

Truth Table

J	K	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$Q_n$

### (b) D-Flip Flop

- Input connections can be avoided by making them complement of each other
- This modified SR flip flop is known as D Flip Flop

Truth Table

CP	D	$Q_{n+1}$
↑	0	0
↑	1	1
0	X	$Q_n$

### (c) T-Flip Flop

- Also known as "Toggle Flip Flop".
- Modification of JK flip flop

Truth Table

T	$Q_{n+1}$
0	$Q_n$
1	$\bar{Q}_n$

#### (d) SR Flip Flop:

- It is similar to SR latch except enable signal is replaced by clock pulse (CP) followed by positive edge detector circuit.
- Edge detector circuit is differentiator.

Truth Table

CP	S	R	$Q_{n+1}$
0	X	X	$Q_n$
↑	0	0	Hold
↑	D	1	0
↑	1	0	1
↑	1	1	Invalid

Q3 List and Explain Registers

- Buffer Registers
- Controlled Buffer Registers
- Shift Registers

(a) Buffer Registers

- constructed using 4 D flip flops. This register is called buffer Registers
- Each D flip flop is triggered with common negative edge clock pulse
- Input bits set up flipflop loading

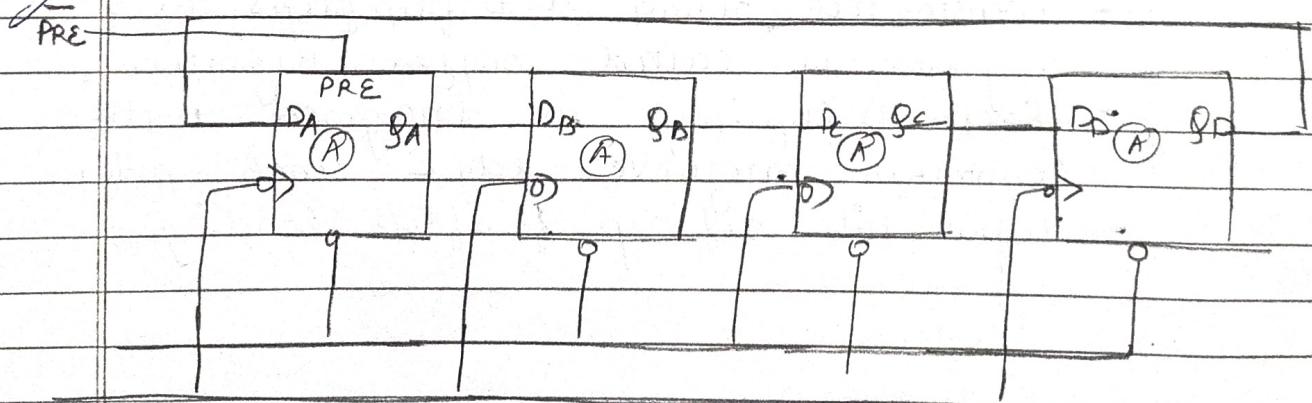
### (b) Controlled Buffer Register

- We can control input and output of register by connecting tristate devices at the input and output sides of register. So this register is called controlled buffer register.
- Tristate switches are used to control the operation.

### (c) Shift Register

- The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses.
- This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessor. This gives rise to a group of registers called 'shift Register'.

### Q4 Describe Ring Counter.



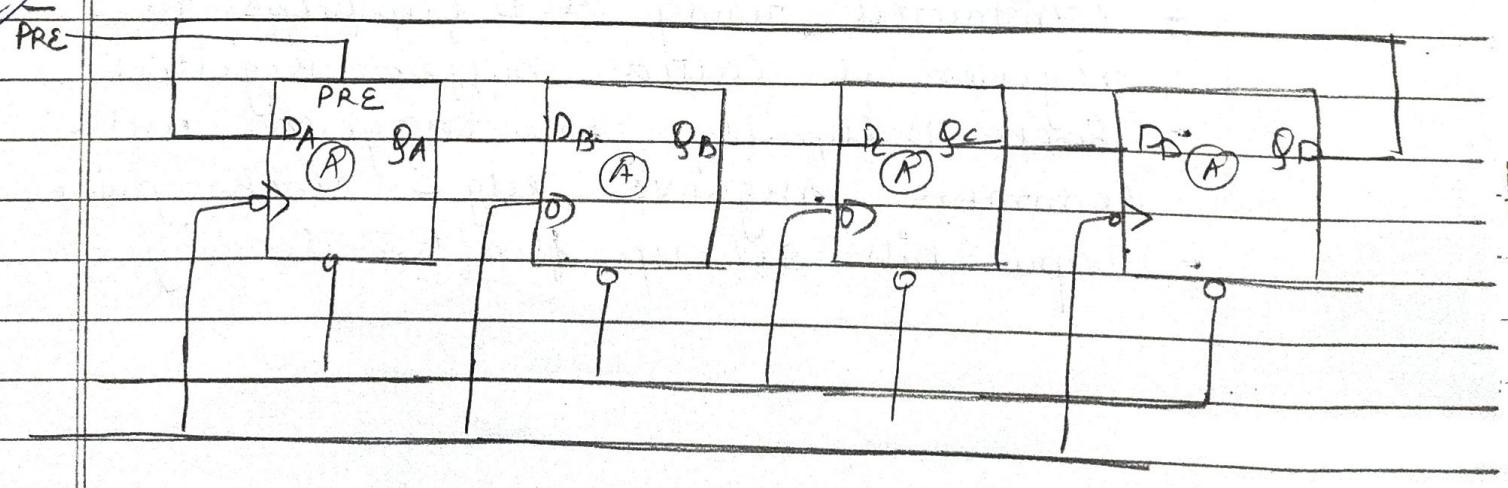
### (b) Controlled Buffer Register.

- we can control input and output of register by connecting tristate devices at the input and output sides of register. So this register is called controlled buffer register.
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### (c) Shift Register.

- The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses.
- This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessor. This gives rise to a group of register called 'shift register'.

## Q4 Describe Ring Counter.



- The Q output of each stage is connected to the input of next stage and the output of last stage is fed back to the input of first stage.
- The CLR followed by PRE makes the output of 4th stage to '1' and remaining outputs are zero i.e.  $Q_3 = 1$  and  $Q_2 = Q_1 = Q_0 = 0$ .

The first clock pulse produces  $Q_3 = 1$  and remaining are zero.

The first clock pulse produces  $Q_3 = 1$  & remaining zero.

~~According to clock pulses applied at clock input CP, a sequence of four state is produced~~

Q5 Describe how to design counters using flip flop.

- steps involved in design of asynchronous counter

- 1) Determine the number of flip flops needed
- 2) choose the types of flip flops to be used  
T or JK, If T flip flops are used connect T input of all flip flops to logic 1

If JK flip-flops to logic 1. Such connection toggles the flip-flop output on each clock transition.

- 3) write the truth table for the cursors
- 4) Devise the reset logic by K-map simplification
- 5) Draw logic diagram.

## **12. Assignment 4**

**CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.**

### **Module 4**

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

## Assignment - 4

Q4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 4:

Q1 Explain weighted resistor / converter

→ Weighted Resistor / converter - A weighted resistor DAC produces an analog output, which is almost equal to digital binary input by using binary weighted resistors in the inverting adder circuit. In short, a binary weighted resistors DAC is called as weighted Resistors DAC.

The binary weighted Resistors DAC uses an op-amp to sum n binary weighted currents derived from reference voltage  $V_R$  via current scaling resistor  $2R, 4R, 8R, 2^n R$

- For ON SWITCH ;  $I = \frac{V_R}{R}$  and

For OFF switch ,  $I = 0$

- Due to high input impedance of op-amp, summing current will flow through  $R_f$ . Hence the total current through  $R_f$  can be given as

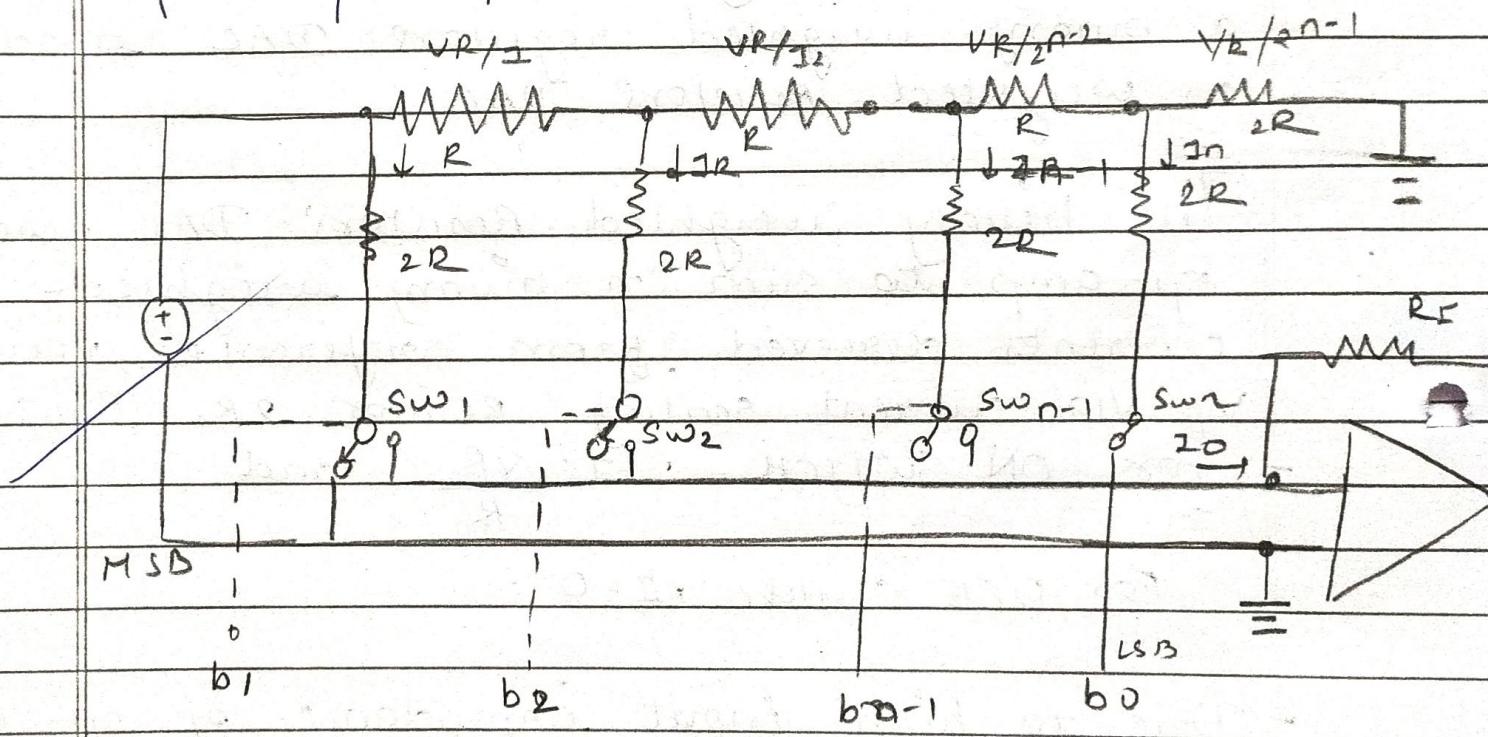
$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

when  $R_f = R$ ,  $V_o$  is given as,

$$V_o = -V_R(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Q2 Explain R-2R ladder D/A converter

- R-2R ladder D/A converter uses only two resistors value. This avoids resistance spread drawback of binary weighted D/A converter.
- Easier to build accurately as only two precision metal film resistors are required.
- Number of bits can be expanded by adding more sections of same R/2R values.
- In ~~vers~~ inverted R/2R ladder DAC, node voltage remains constant with changing input binary words. This avoids any slow-down effect by stray capacitance.



Q3 Describe specification of A/D & D/A converters

\* Specification of A/D D/A

1) Resolution

- smallest change that occur in analog output as a result of a changes in digital input.
- % Resolution = step size / full scale  $\times 100\%$ .
- Full scale = No. of steps  $\times$  step size
- % Resolution =  $1/\text{No. of steps} \times 100\%$ .

2) Accuracy

- Specified in terms of full scale error and linearity error.

3) Settling time

- The time required for analog output to settle to within  $\pm \frac{1}{2}$  LSB of the final value after a change in digital input.

4) Monotonicity

- This means that staircase output will have no downward steps as binary input is incremented from 0 to full scale value.

5) Temperature sensitivity

- The analog output voltage for any fixed digital input varies with temperature.

## \* Specifications of A/D converter:

1. Range of Input voltage
2. Input impedance
3. Accuracy
4. Conversion time
5. Format of digital output.

Q4 Explain quantization and encoding.

### - Quantizing / Encoding.

- Process of mapping the sampled analog voltage values to discrete voltage levels which are then represented by binary numbers. This is needed because the analog sample values are real numbers that occur on continuum.

$$q = \frac{V_{max} - V_{min}}{2^N}$$

$$= \frac{1 - (-1)}{8}$$

$$= 0.25 \text{ V}$$

Value of  $q$  is more formally called the quantizer's Resolution.

Q5 Explain parallel Comparator A/D converters.

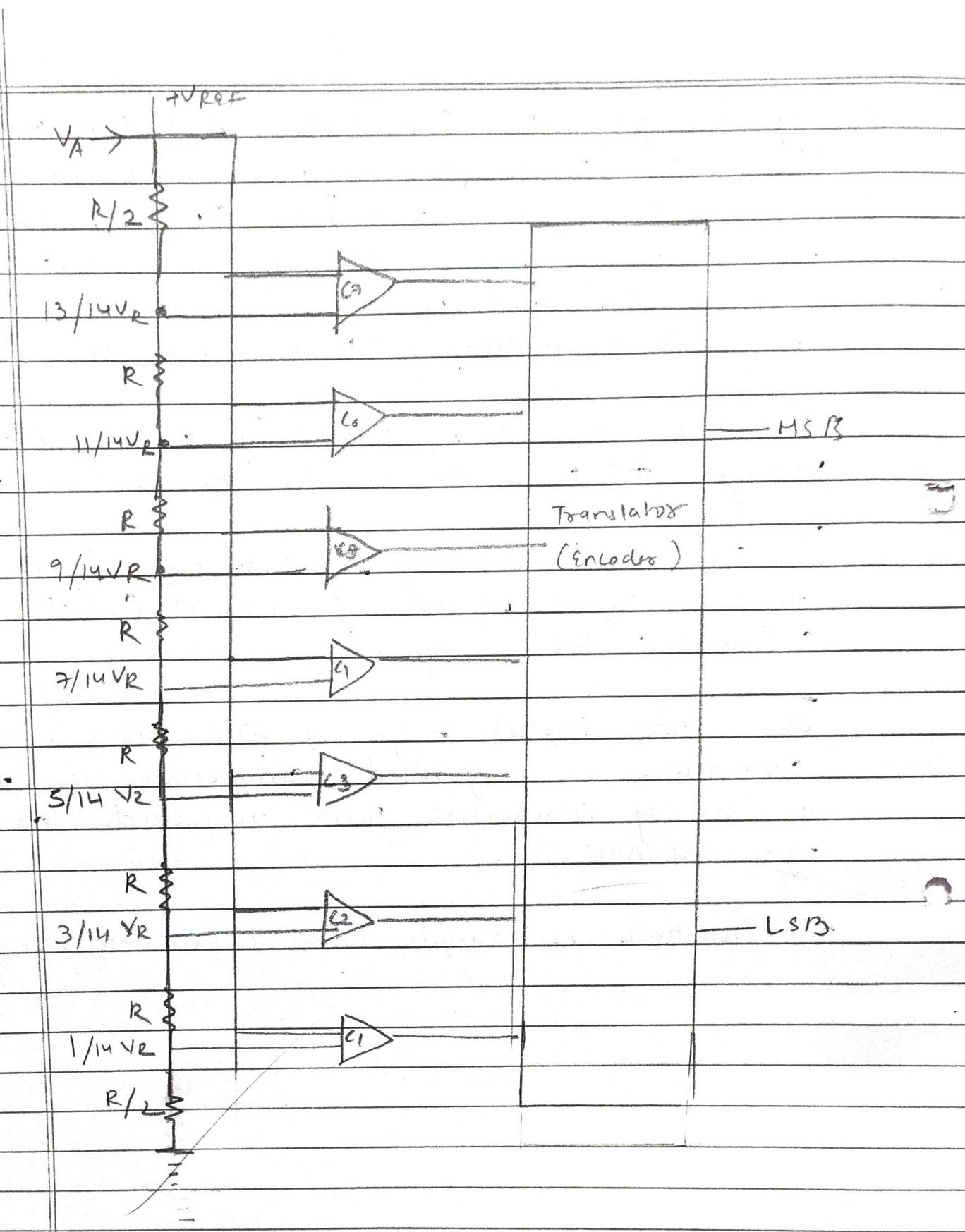
→ This circuit is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to input of a priority encoder circuit which then produces binary outputs.

- Based on principle of comparing analog input voltage. ~~the~~ to with a set of reference voltage

To convert the analog input voltage into a digital signal of  $n$ -bit output. ( $2^n - 1$ ) Comparators are required.

It is the fastest type of ADC because the conversion is performed simultaneously through a set of comparators hence referred as flash type of ADC

Construction is simple and easier to design.



## **13.Assignment 5**

**CO5: Implement PLDs for the given logical  
problem.Module 5**

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA)

## Assignment 5

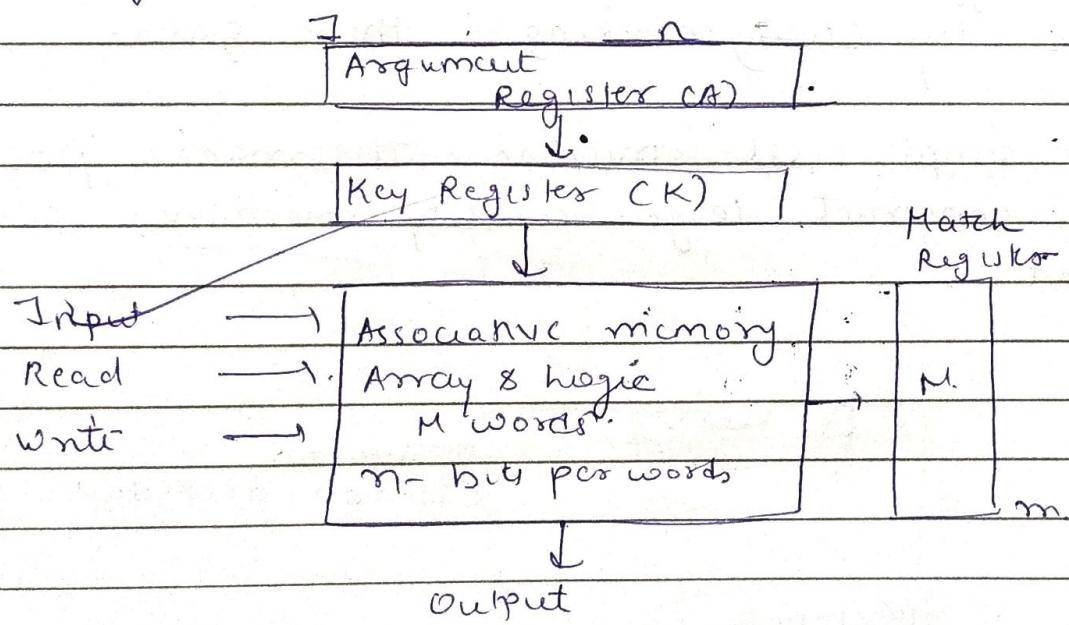
Cos: Implement PLD's for logical problem.

### Module 5

Q1 Explain content addressable memory [CAM].

The time required to find an object stored in memory can be reduced considerably if objects are selected based on their contents, not on their locations. A memory unit accessed by the content is called an associative memory or content addressable memory [CAM].

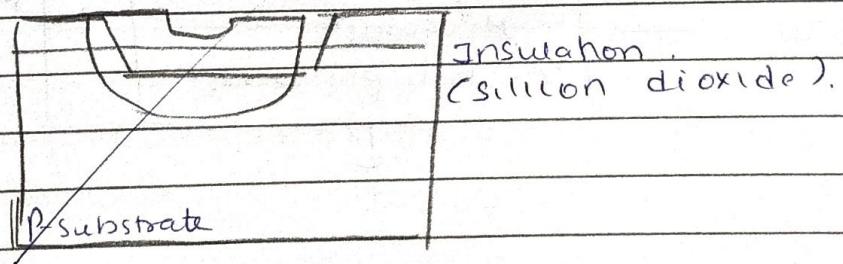
This type of memory is accessed simultaneously and in parallel on the basis of data content rather than by specific address or location.



Q2 Explain charge coupled device memory [CCD].

- It is a type of dynamic memory in which packets of charge are continuously transferred from one MOS device to another. The structure of a MOS charge coupled device is quite simple.
- When a high voltage is applied to metal gate, in the P-type substrate. This region called a potential well, is then capable of accepting a packet of negative charge electrons. Therefore, data is stored in CCD as charge, and it is transferred from one device to an adjacent one by closing clocking their gates.

It simple cell structure. It makes possible to construct large capacity memories at low cost.



Q3 Explain classification of memory

Non-Volatile memory

i) Read Only Memory [ROM]

: (i) Mask Programmable ROM

(ii) Programmable ROM

ii) Read / Write Memory [NVRAM]

(i) EEPROM.

(ii) EEPROM

(iii) FLASH.

Volatile memory

i) Read / Write memory (RWM)

a) Random Access:

i) SRAM

ii) DRAM

b) Non-Random Access

(i) FIFO

(ii) LIFO

(iii) Shift Registers

- The volatile memories which can hold data as long as power is on are called static Ram [SRAMs]

- The dynamic RAM [DRAM's] stores the data as a charge on the capacitor after every few milliseconds to hold the data even power is off

#### Q4 Describe Semiconductors?

- It is a substance that has specific electrical properties that enable it to serve as a foundation for computers and other electronic devices.

- It is typically a solid chemical element or compound that conducts electricity under certain conditions but not others.

- Semiconductors are materials which have a conductivity between conductors and non-conductors or insulators

- Semiconductors can be pure elements such as silicon or germanium or compounds such as gallium arsenide or cadmium selenide

Q5 Explain Field Programmable Gate Array.  
[FPGA]

- It provides the next generation in the programmable logic devices
- The word field in the name refers to the ability of gate arrays to be programmed for a specific function by user instead of by the manufacturer of device.
- The word array is used to indicate a series of columns and rows of gates that can be programmed by the end user.
- The programmable logic blocks of FPGA, are called logic's blocks or configurable logic blocks [CLBs].

Programmable  
/ Input/Output Block

