



Government Engineering College

Sec-28 Gandhinagar

Sem: - 3

Subject: - Digital Fundamental

Subject Code: - 3130704



Government Engineering College

Sec-28 Gandhinagar

Certificate

This is to certify that

Mr./Ms. ... Rupnarmi ... Aath Of class

..... CE .. Division ... A., Enrollment No. 210130107055. Has

Satisfactorily completed his/her term work in

Digital Fundamentals Subject for the term ending in

2022-2023

Date: - 7/11/2022

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department

Vision/Mission

Vision:

- To achieve excellence for providing value based education in computer Engineering through innovation, teamwork and ethical practices.

Mission:

- To produce computer science and engineering graduates according to the needs of industry government, society and scientific community.
- To develop partnership with industries, government agencies and R&D organizations
- To motivate students/graduates to be entrepreneurs.
- To motivate students to participate in reputed conferences, workshops, symposiums, seminars and related technical activities.

Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	Solve the given problem using fundamentals of numbers system and Boolean Algebra
CO-2	Analyse working of logic families and logic gates and design the simple circuits
CO-3	Design and implement combinational and sequential logic circuits and
CO-4	Examine the process of Analog to Digital conversion and digital to
CO-5	Implement PLDS for the given logical problem.

7. Assignment Index

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8. Practical Index

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14. Practical 1

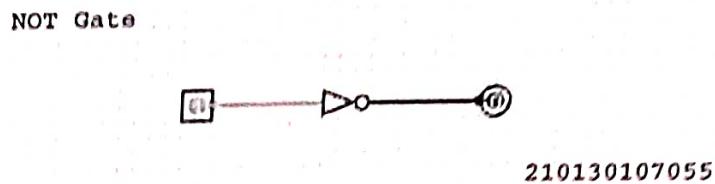
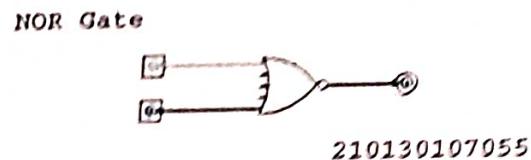
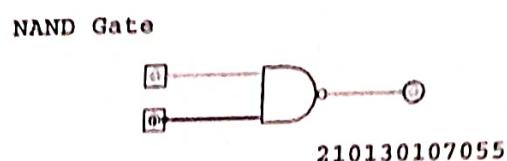
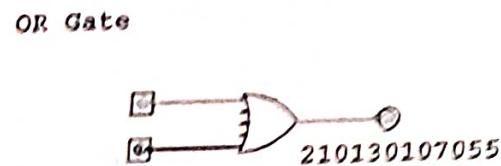
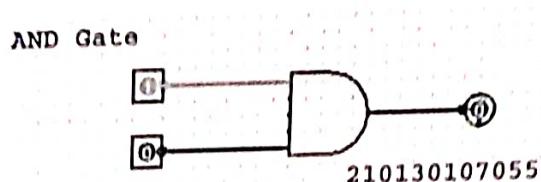
CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

Module 1

Aim: Getting familiar with Logisim, Study and implement all basic logic gates.
Implement NAND and NOR logic gates as universal gates.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



XOR Gate



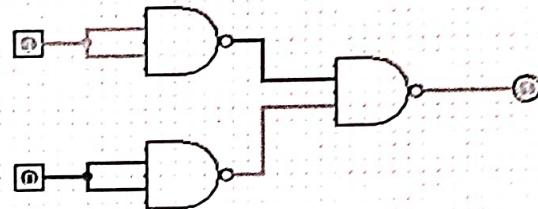
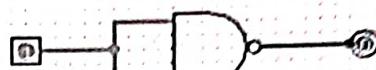
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XNOR Gate



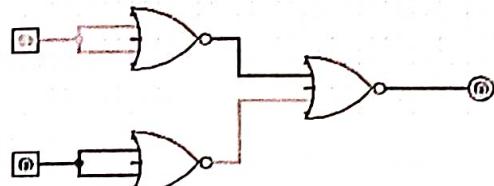
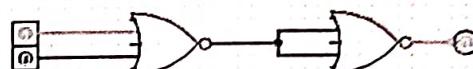
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NAND Gate as Universal Gate



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NOR Gate as Universal Gate



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15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

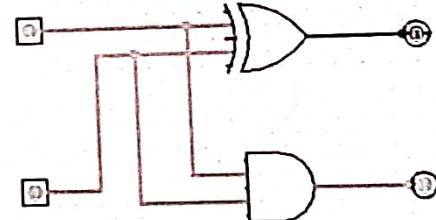
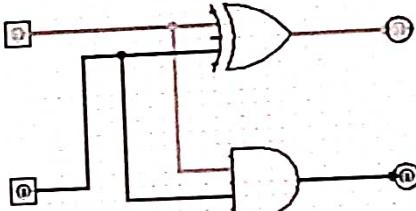
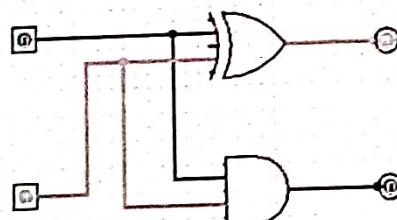
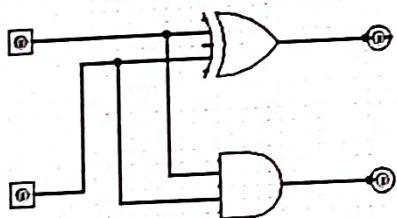
Module 2

Aim: Implement half and full Adders using logic gates.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

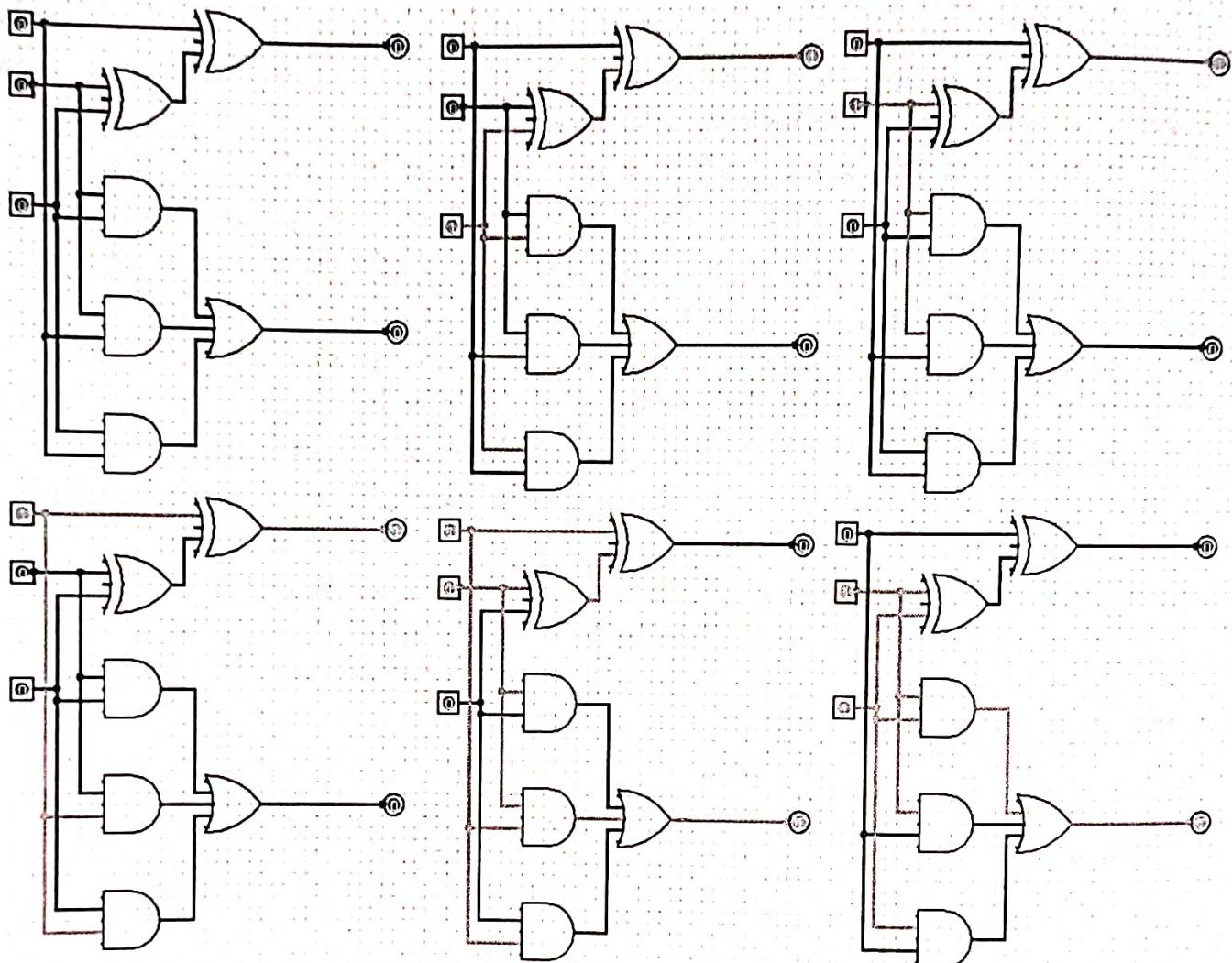
HALF Adder



date & time :27-12-22 12:26

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FULL Adder



date & time :27-12-22 1:20 210



16. Practical 3

C03: Design and implement Combinational and Sequential logic circuits and verify its working.

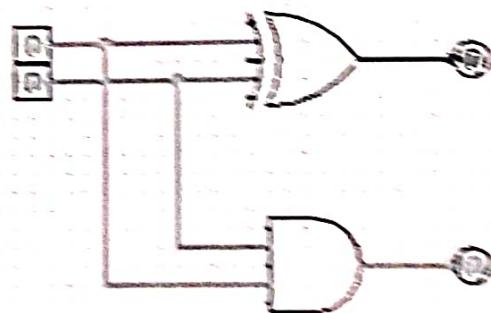
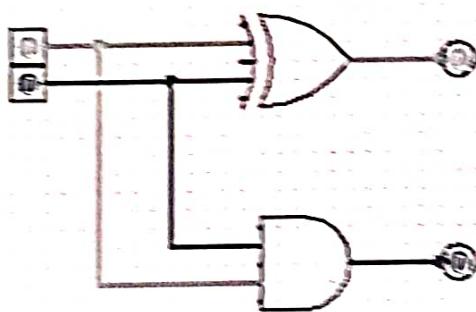
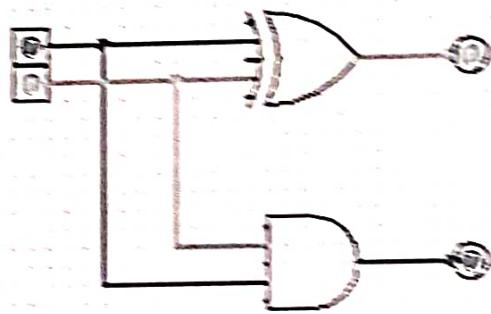
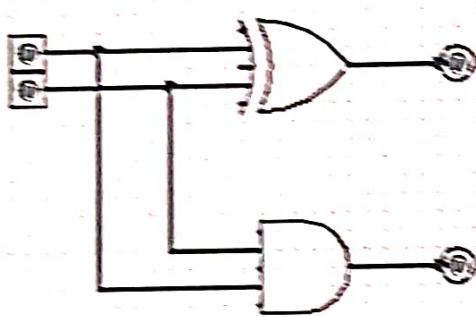
Module 2

Aim: Implement half and full Subtractors using logic gates.

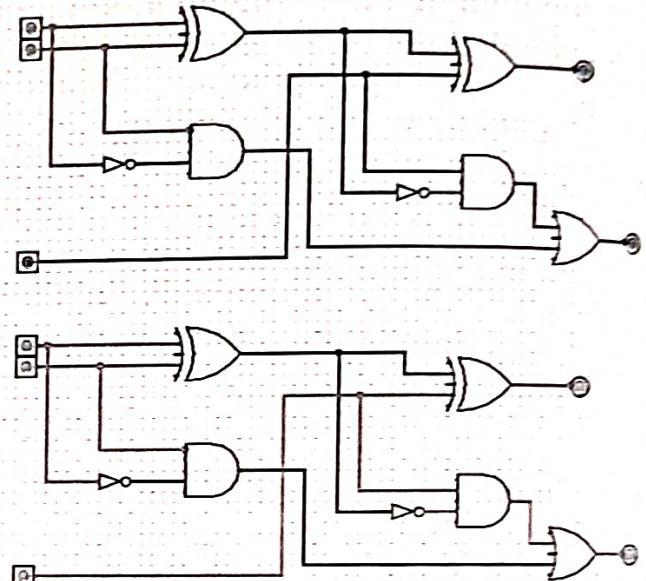
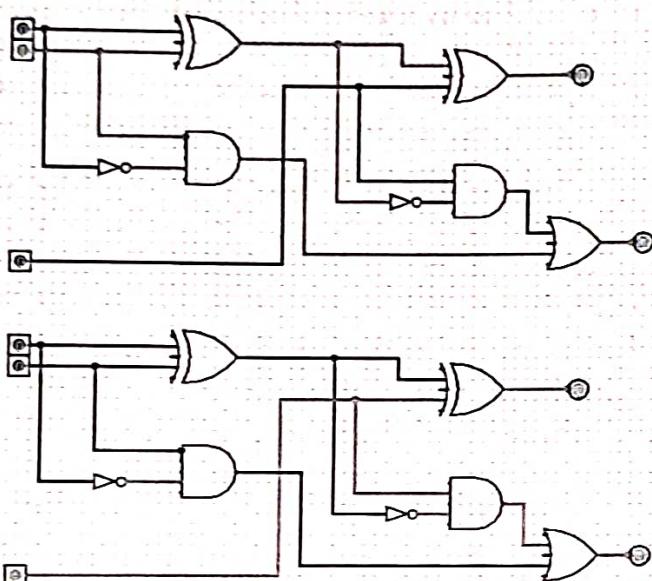
Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

Half Subtractor



FULL Substractor



date & time 15-12-22 5 34

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17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

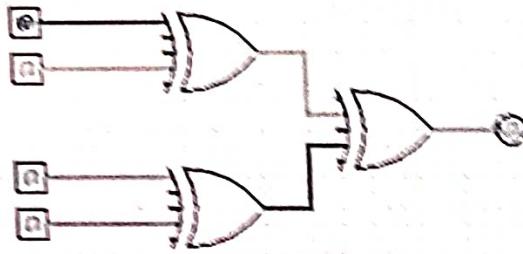
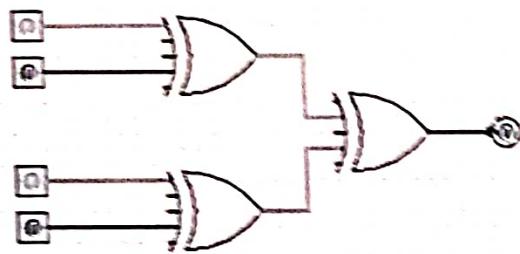
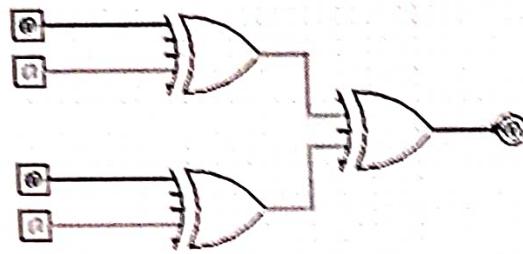
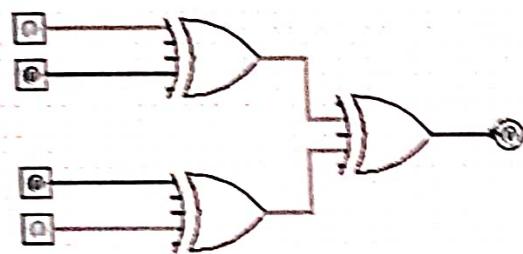
Module 2

Aim: Perform Parity Checker.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

Parity Checker



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18. Practical 5

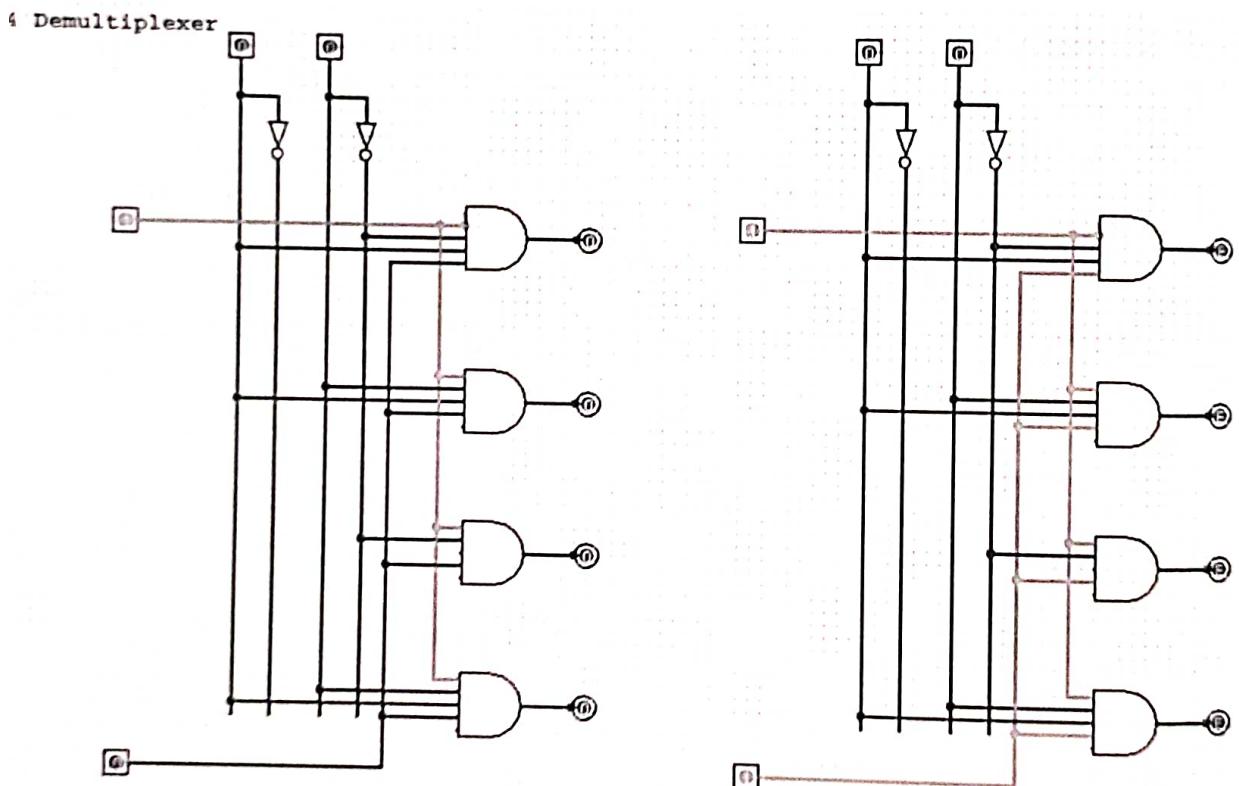
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement Multiplexer and Demultiplexer.

Code:

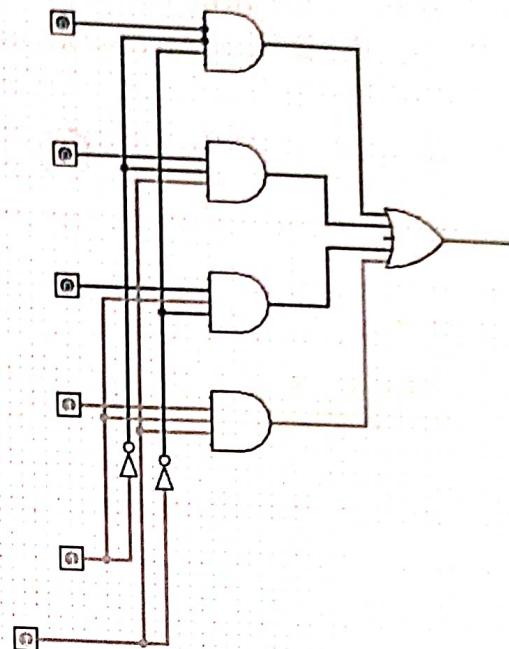
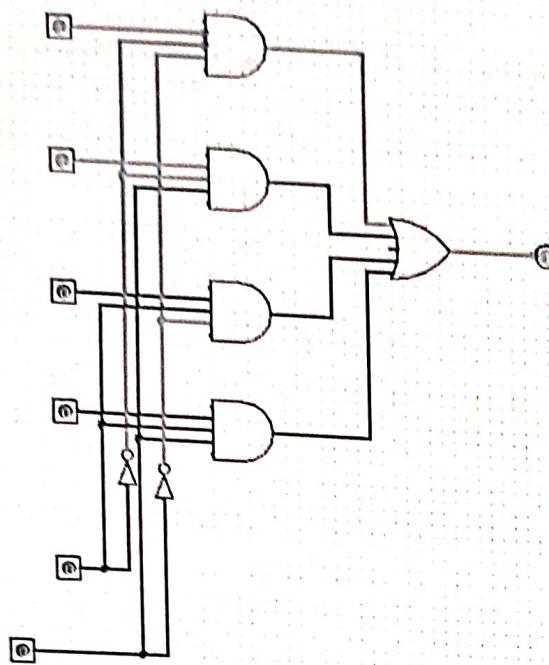
Output snapshot: (In output include practical details and execution date & time with your enrollment number)



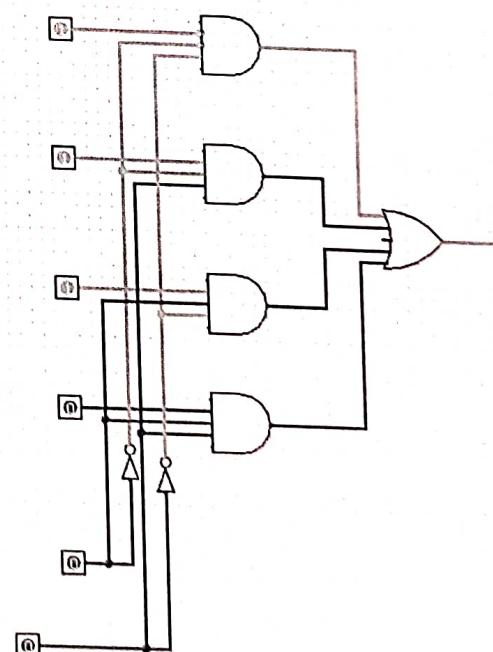
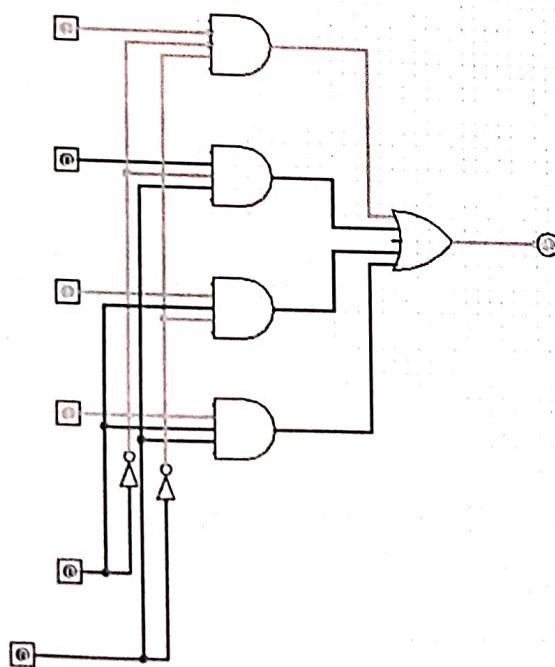
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4:1 Multiplexer



2101



date & time 23-12-22 9:30

21

19. Practical 6

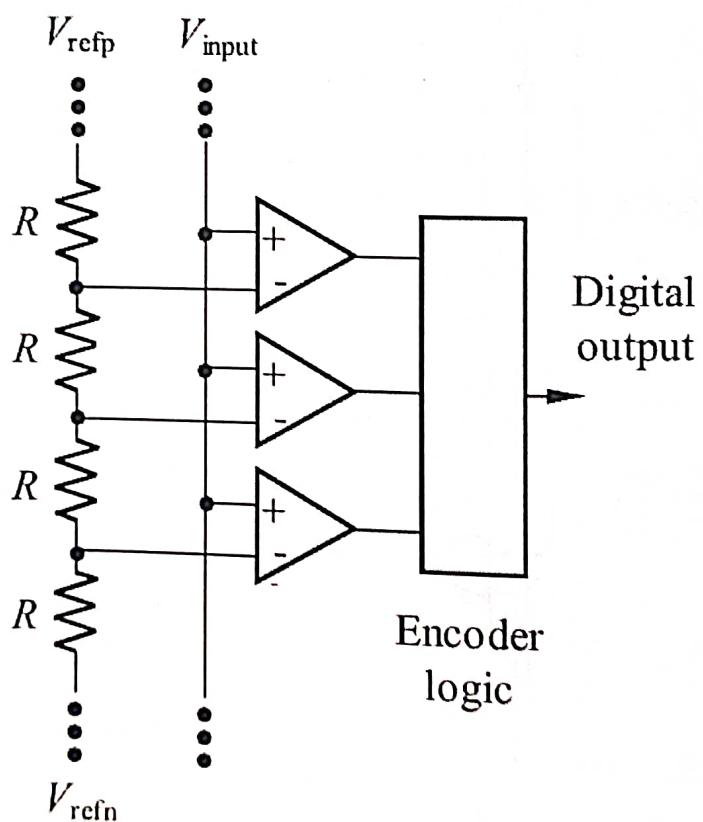
CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion

Module 4

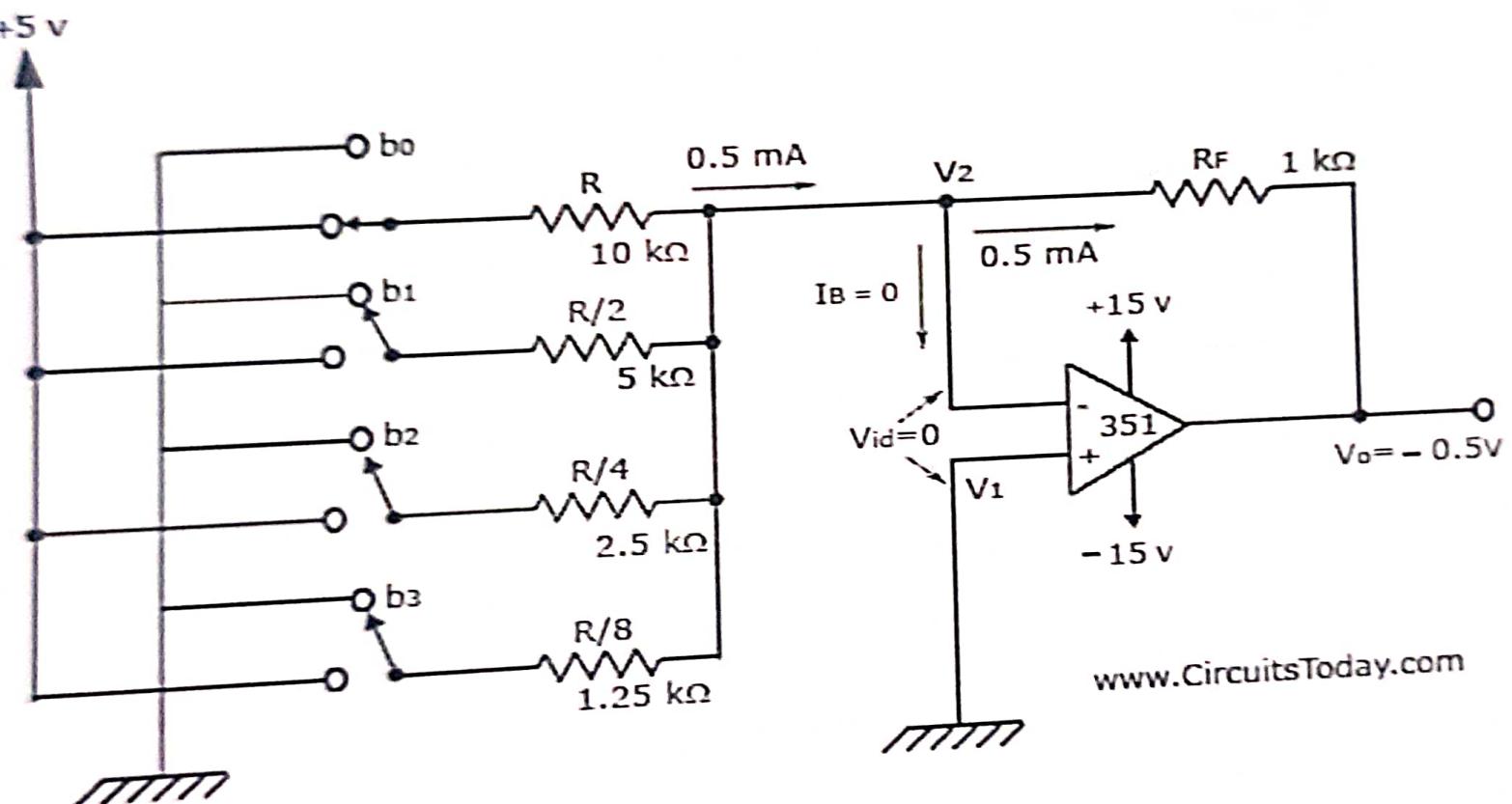
Aim: Study and configure A to D convertor and D to A convertor.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



D/A Converter With Binary Weighted Resistors



20. Practical 7

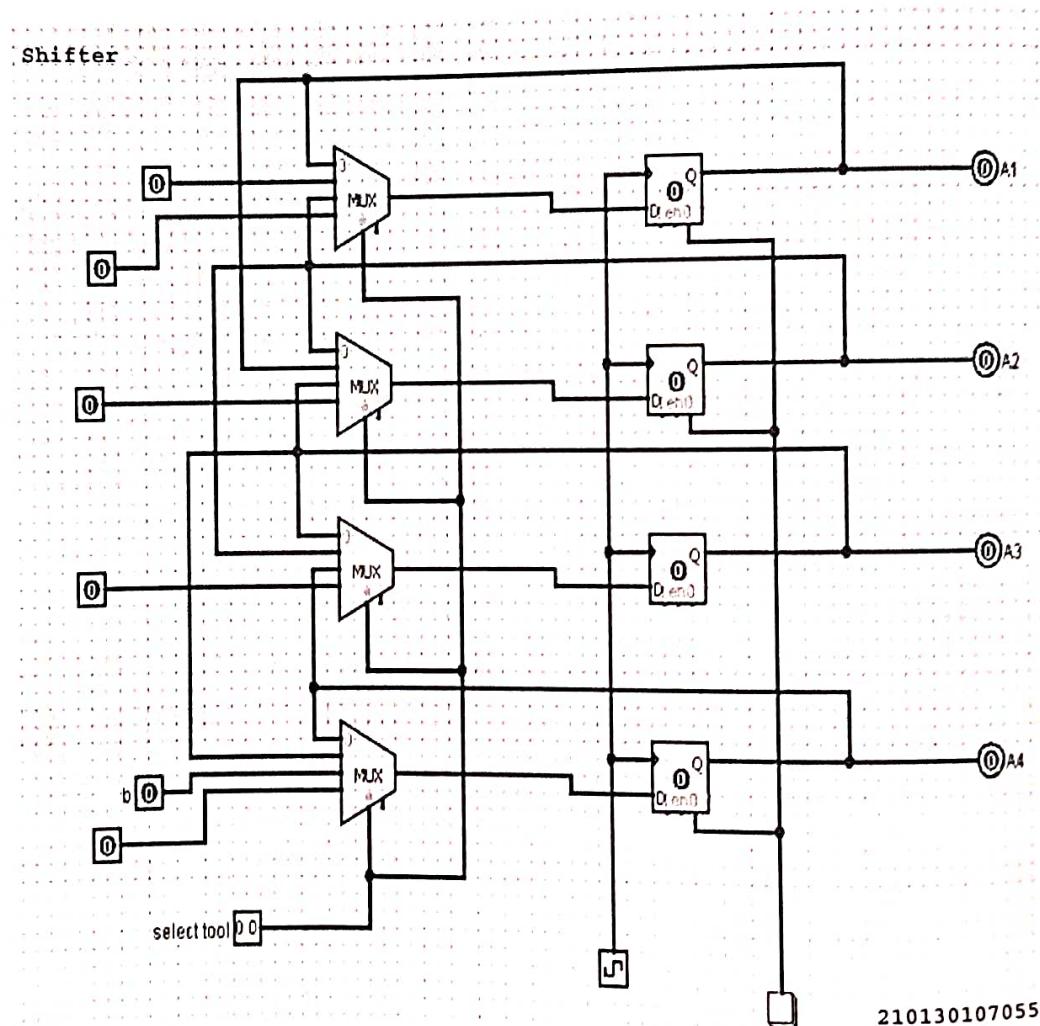
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and implement a shifter.

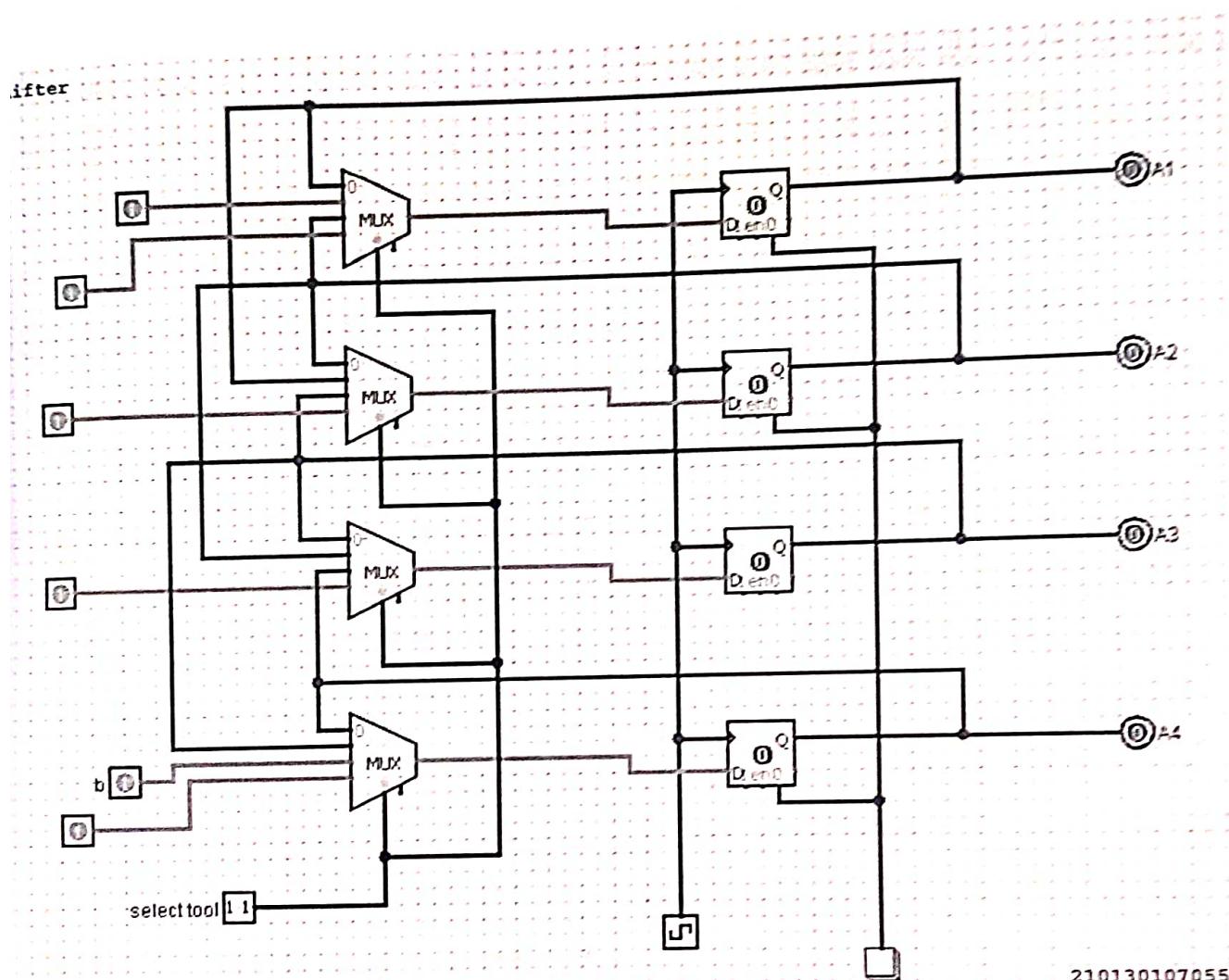
Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



DE

Assignment - 1



date & time 27-12-22 4:57

21. Practical 8

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

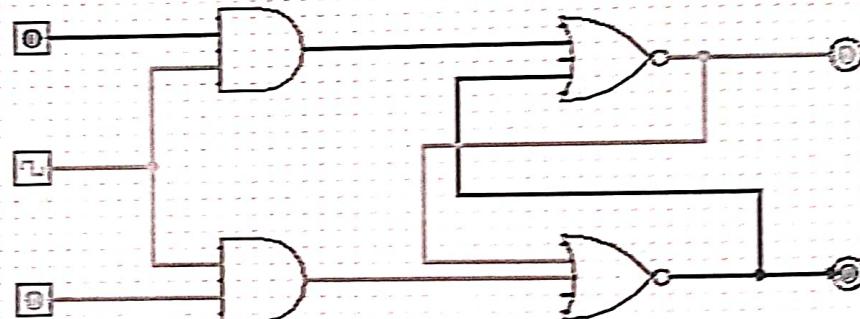
Module 3

Aim: Study and implement Flip-flops.

Code:

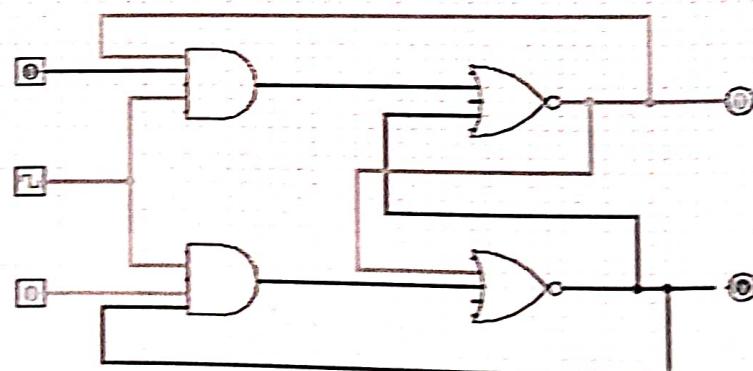
Output snapshot: (In output include practical details and execution date & time with your enrollment number)

S-R Flip Flop



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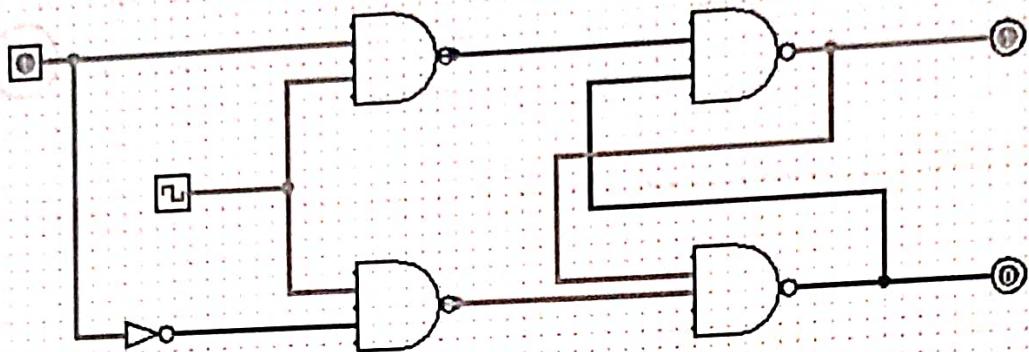
J-K Flip Flop



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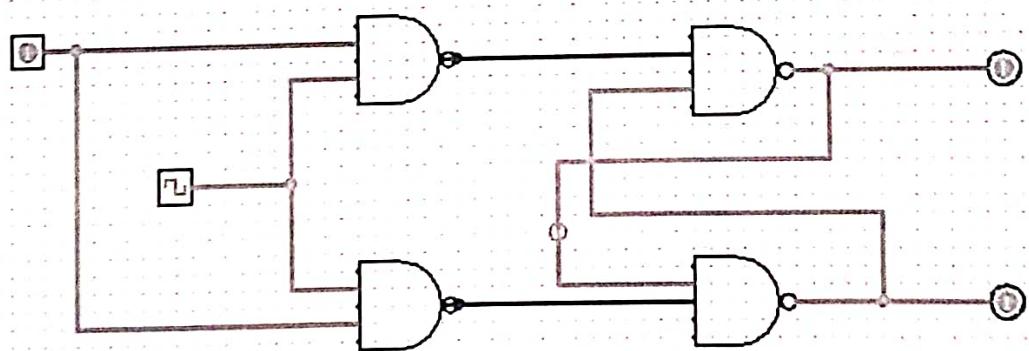
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D Flip Flop



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T Flip Flop



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22. Practical 9

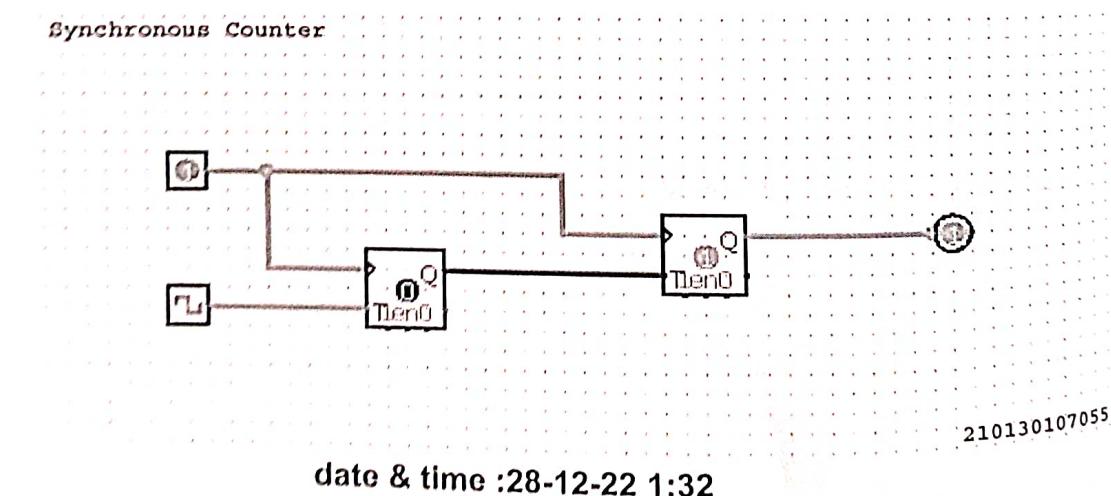
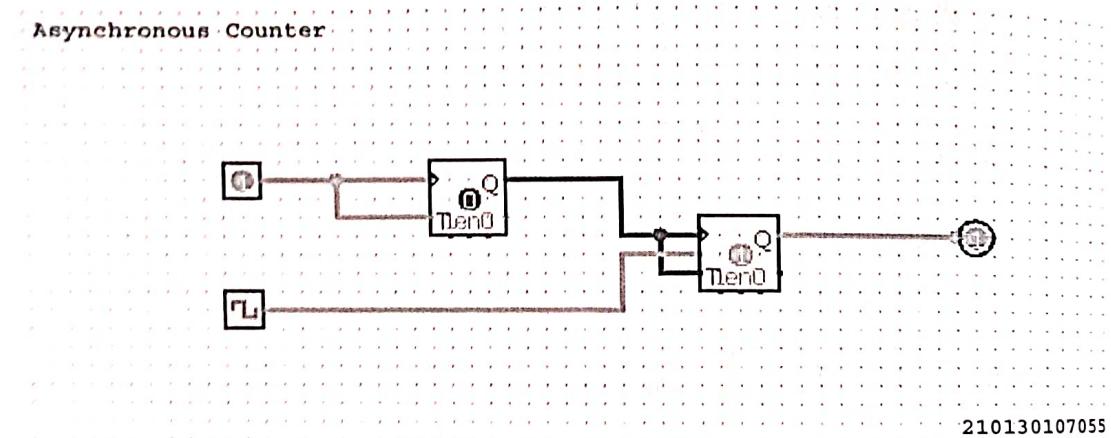
CO3: Design and Implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and implement Counter.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



23. Practical 10

COE: Design and implement Combinational and Sequential logic circuits and verify its working.

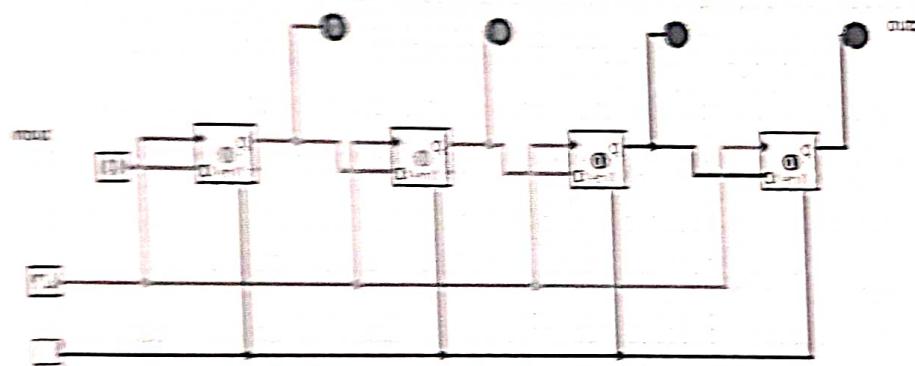
Module 3

Aim: Study and implement a shift register.

Code:

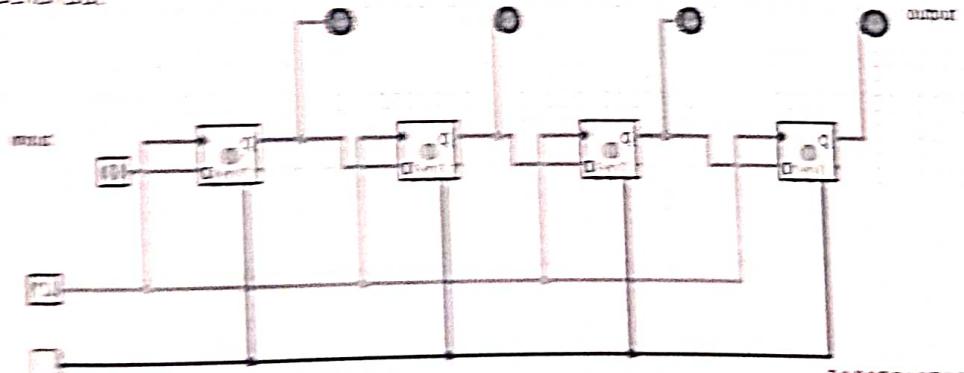
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Serial In Serial Out



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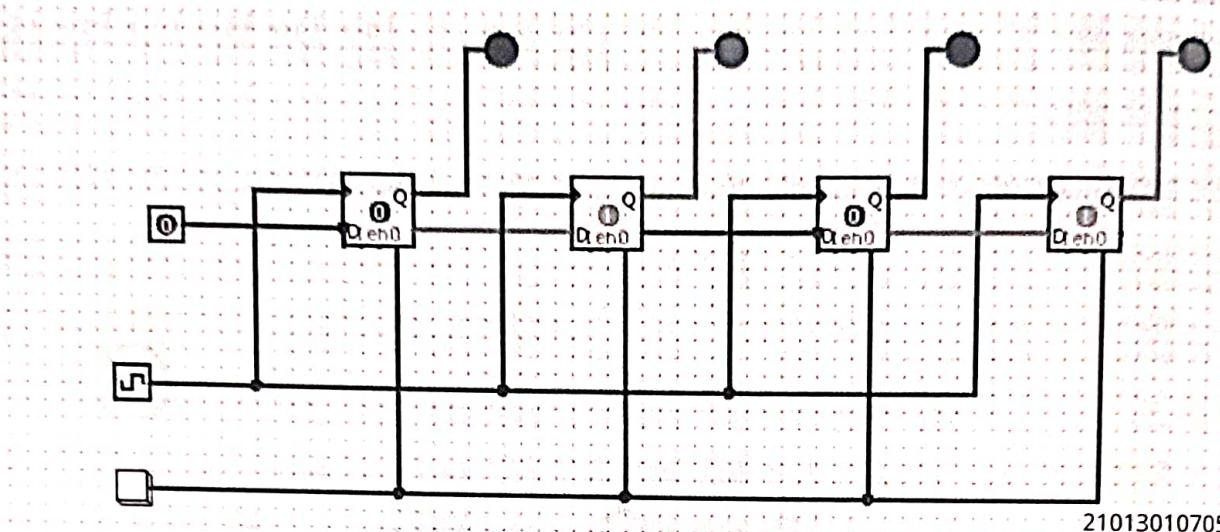
Serial In Serial Out



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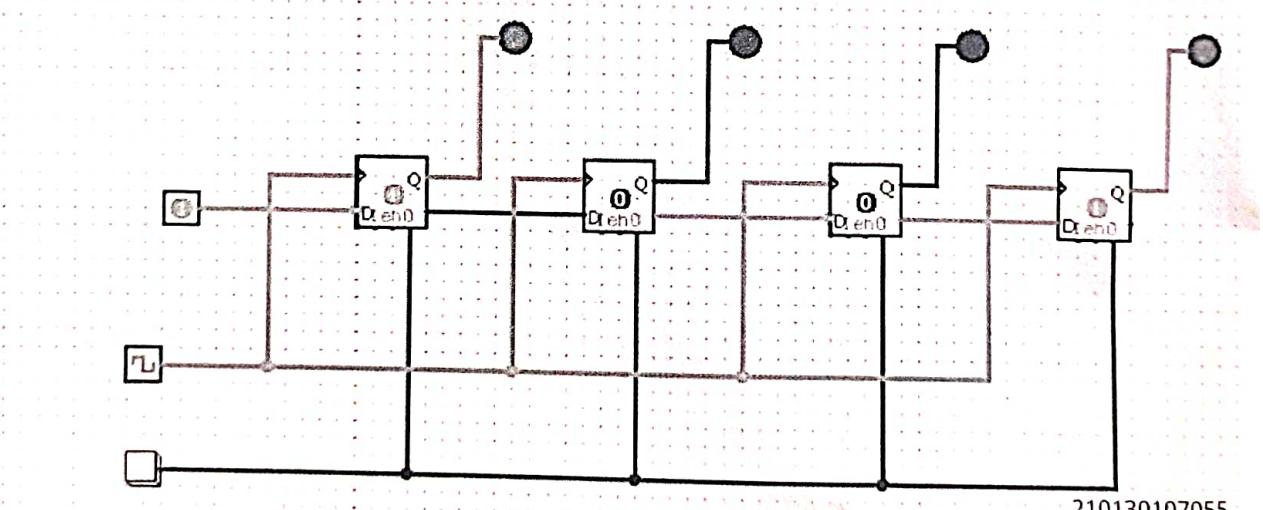
2019-2020

Serial InParallel Out



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Serial InParallel Out



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24. Practical 11

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 2

Aim: Study and implement K-Map for the given function:(SOP)

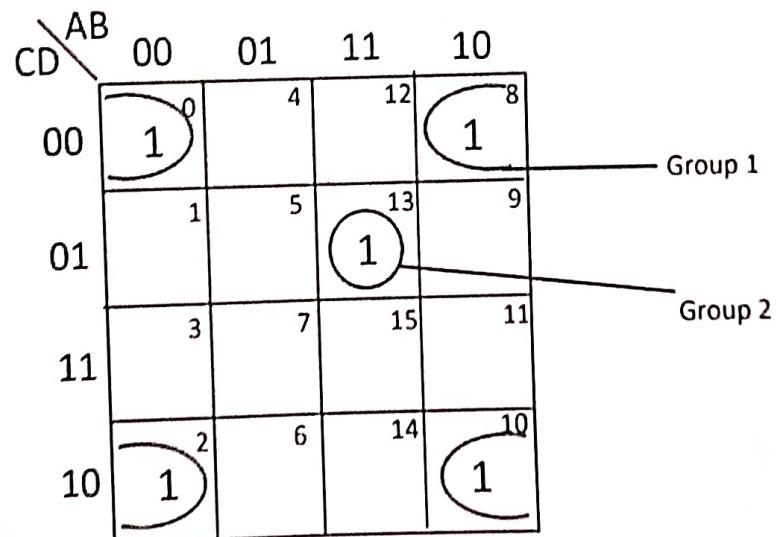
$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

$$F(A,B,C,D) = \sum(0,2,8,10,13)$$



First consider group 1,

Group's Product term = $B'D'$

Now, consider group 2,

Group's Product term = $ABC'D$

To obtain final solution we add product term of Group 1 and Group 2,

Ans : $F(A,B,C,D) = B'D + ABC'D$

Q
2
c/1/2)

DE

Assignment:- I

D) State and explain De Morgan's theorems with truth tables.

$$\rightarrow \text{Luw 1} = \overline{A+B} = \bar{A}\bar{B}$$

\rightarrow This law states that the complement of sum of variables is equal to the product of their individual complement.

A	B	$A+B$	$(\bar{A}+\bar{B})$	\bar{A}	\bar{B}	$\bar{A}\bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

\rightarrow Hence, Law 1 is proved from the above truth table.

$$\text{Luw 2: } \bar{AB} = \bar{A} + \bar{B}$$

\rightarrow This law states that the complement of product of variables is equal to the sum of individual complement.

A	B	AB	\bar{AB}	$\bar{A} + \bar{B}$	$\bar{A}\bar{B}$
0	0	0	1	1	1
0	1	0	1	0	1
1	0	0	1	1	0
1	1	1	0	0	0

\rightarrow Hence, Law 2 is proved from the above truth table.

2) Simplify Boolean function: $F = A'B'C + A'B'C + AB'$

$$\begin{aligned}
 F &= A(CB + B') + AB' \\
 &= AC + AB'
 \end{aligned}$$

3) List & explain logic family.

Characteristic	ECL	TTL	CMOS
Power input	moderate-high	moderate	low
Fanout limit	very high	High	moderate
Circuit density	moderate	moderate-high	high ^{fast}
Circuit type per family	moderate	High	high

- 4) Describe error detecting & correcting code
- Error-detecting codes:
 - noise can alter or distort the data in transmission
 - The data may get changed to as well as to is
 - Because digit system must be accurate to the digit, errors can pose a serious problem.
 - single bit errors should be detect & correct by different schemes.
 - Parity, check sums and block parity are few ex. of error detecting code.
 - Parity:-
 - Parity bit is the simplest technique.
 - two type of parity - odd parity and even parity
 - Odd parity, the parity is set to 1 or 0 at the transmitted.

even parity, the parity is set to 0 or 1 at the trans. mitter such that the total number of 1 bits in the word including the parity is an even number.

Detect a single bit error but can not detect two or more errors within the same word. In any practical system, there is always a finite probability of the occurrence of single errors.

Check sums:- simple parity can not detect two errors within words.

Added to the sum of previously transmitted words.

At the transmission, the check sum up to that time is sent to the receiver.

The receiver can check its sum with the transmitted sum.

If the two sums are the same then, no errors were detected at the receiver end.

This type of transmission is widely used in teleprocessing system.

Block parity:-

Q-1 Draw parity column.

	Parity Column
0101011	0
1001010	1
0110111	0
1101001	0
1000110	1
0111011	1
0111010	0 ← Parity Row

Q.2

Differentiate TTL, Schottky, TTL, CMOS.

parameters

CMOS

TTL

device

n-channel

Bipolar junction

use

un p-channel

Transistor

V_H(min)

3.5 V

2 V

V_I(max)

1.5 V

0.8 V

V_{OH}(min)

4.0 V

2.7 V

V_{OL}(max)

0.005 V

0.4 V

High level

V_{NH} = 1.45 V

0.4 V

noise margin

0.7 V

Low level

V_{NL} = 1.45 V

0.4 V

noise

0.7 V

margins

better than

less than CMOS

immunity

TTL

10 ns

propagation

70 ns

delay



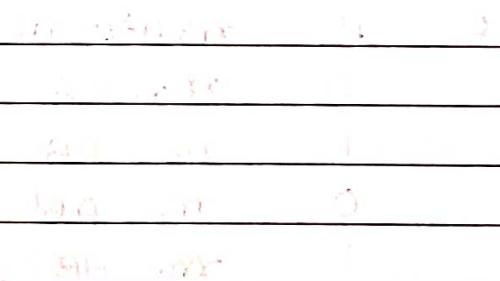
~~Switching less turn~~
speed TTL
~~Fun-out SO~~
power
supply 3-15V
voltage

Faster than
(MOS)
~~10~~
Fixed 5V

Application portable instrument & laboratory
battery supply
is used

~~JK~~
6/12

IC 74123 is a dual JK flip-flop integrated circuit.
It contains two JK flip-flops with three-state outputs.



IC 74123 is a dual JK flip-flop integrated circuit.
It contains two JK flip-flops with three-state outputs.
Mainly used in digital logic design, interfacing, etc.

Assignment-2

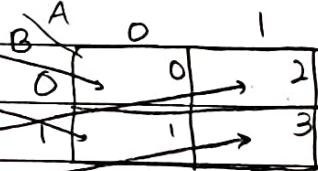
Q2

Explain K-map:-

The Karnaugh map method is a systematic method of simplifying the Boolean expression.

- The K-map is a chart or a graph, composed of an arrangement of adjacent cells, each representing a particular combination of variable in sum-of-products form.
- The output values placed in each cell are derived from the minterms of a Boolean function.
- Two-variable K-map:-
 - The two-variable expression can have $2^2 = 4$ possible combination of the input variables A and B.
 - Each of these combinations, $A'B'$, $A'B$, AB' and AB is called minterm.

A	B	minterm
0	0	$m_0 = A'B'$
0	1	$m_1 = A'B$
1	0	$m_2 = AB'$
1	1	$m_3 = AB$



→ Three-variable K-map

→ A function in three variable expressed in the standard SOP form can have eight possible combination: $A'B'C'$, $A'B'C$, $A'BC'$, $A'BC$, ABC' , $A'BC$, $AB'C'$, $AB'C$.

		A	B	C	00	01	11	10
		0		0	0	2	6	4
		1		1	1	3	7	5

min term number

Q. 2) obtain the simplified expression in SOP for the following Boolean functions:-

i) $F(x,y,z) = \Sigma(2,3,6,7)$

		A	B	C	00	01	11	10
		0		0	0	1	1	0
		1		1	1	0	0	1

Final Boolean expression: $y_2' + y_2 : y_1 \oplus 2$

ii) $F(A,B,C,D) = \Sigma(4,6,7,15)$

		A	B	C	D	00	01	11	10
		0		0	0	1	1	1	0
		1		1	1	0	0	0	1

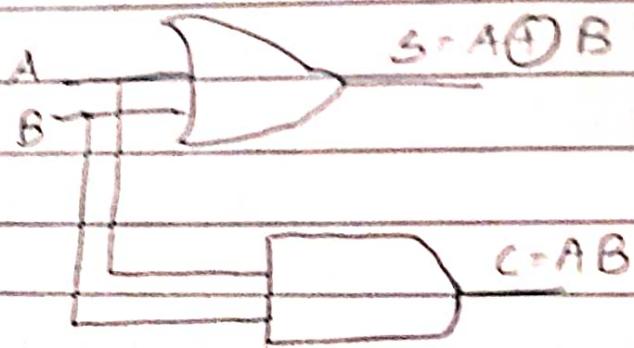
Final Boolean expression: $B(CD') + A'B'(CD) + A'BC'D$

Q. 3) Describe adder & subtractor:-

→ i) Half adder:-

→ A combination circuit that which adds two one-bit binary numbers is called a half-adder.

input			
A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



The sum column resembles like an output of the XOR gate.

The carry column resembles like an output of the AND gate.

FULL adder:-

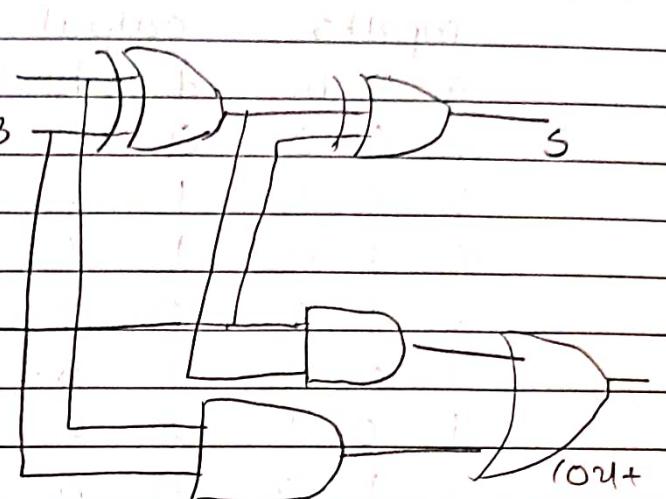
The full adder adds the bits A and B and the carry from the previous column called carry-in or in and outputs the sum bits and the carry-out cout.

$$\begin{aligned}
 S &= A'B'c_{in} + ABC_{in} + AB'C_{in} + A'BC_{in} \\
 &= (A'B' + A'B)c_{in} + (AB + A'B')c_{in} \\
 &= (A \oplus B)c_{in} + (B \oplus B)c_{in} \\
 &= A \oplus B \oplus c_{in}
 \end{aligned}$$

$$\begin{aligned}
 \text{cout} &= A'Bc_{in} + AB'c_{in} + ABC'_{in} + A'BC_{in} \\
 &= AB + (A \oplus B)c_{in}
 \end{aligned}$$

input output

A	B	cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



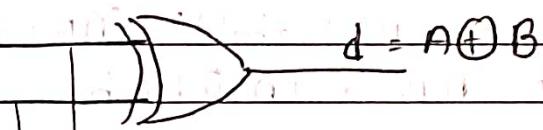
→ Half Subtractor:-

→ Subtracts one bit from the other and produces the difference.

→ Other output is to specify if it is borrowed.

inputs outputs

A	B	d	b
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



→ Full Subtractor:-

→ Full Subtractor is a combination circuit with 3 inputs (A, B, b_i)

→ Subtraction = A - B - b_i

Inputs Output

A B b_i d b

0 0 0 0 0

0 0 1 1 1

0 1 0 1 1

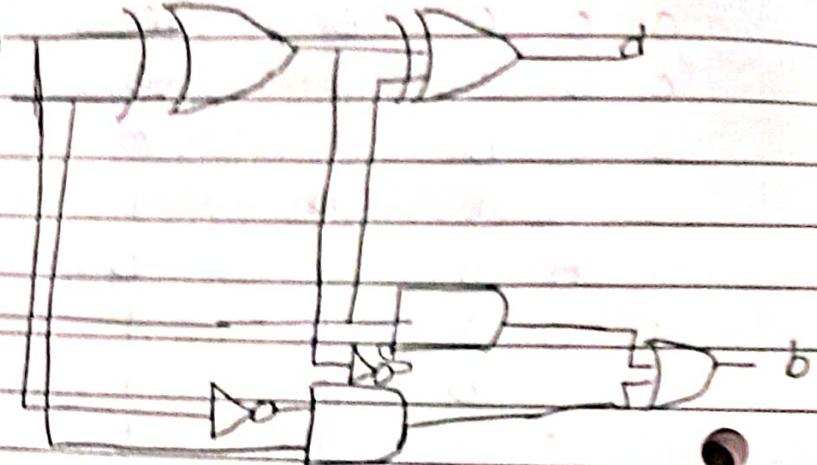
0 1 1 0 1

1 0 0 1 0

1 0 1 0 0

1 1 0 0 0

1 1 1 1 1



$$\begin{aligned}
 d &= A'B'b_i + A'Bb_i' + AB'b_i + ABb_i \\
 &= (AB' + A'B)b_i + (AB + A'B')b_i \\
 &= (A \oplus B)b_i + (A \oplus B)'b_i \\
 &= A \oplus B b_i
 \end{aligned}$$

$$\begin{aligned}
 b &= A'B'b_i + A'Bb_i' + A'Bb_i + ABb_i \\
 &= A'B(b_i + b_i') + (AB + A'B')b_i
 \end{aligned}$$

$$b = A'B + (A \oplus B)'b_i$$

Q.4 Explain multiplexed & demultiplexed.

multiplexer:-

→ A multiplexer(MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.

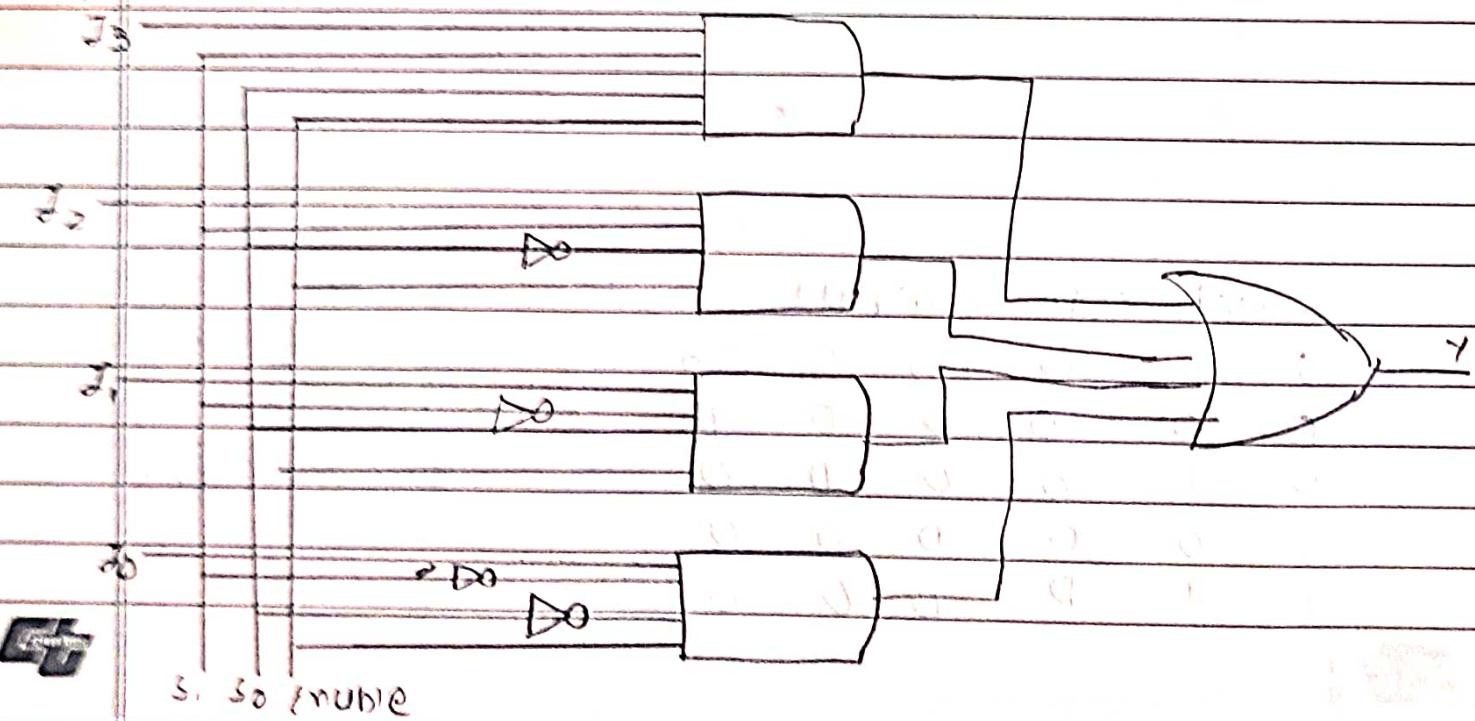
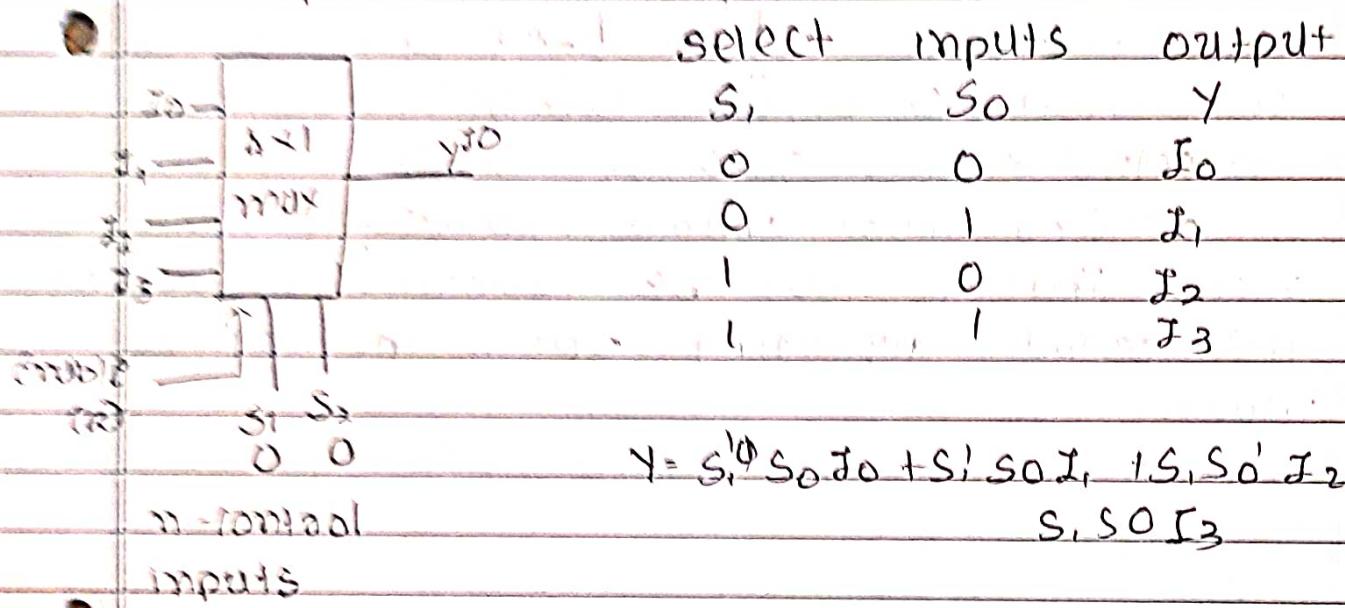
→ Consider an integer 'm', which is contained by the following relation:-

$m = 2^n$, where m and n are both integers.



- A $m \times 10 = 1$ multiplexer has
 - m inputs: $J_0, J_1, J_2, \dots, J_{m-1}$
 - one output: y
 - n control inputs: $S_0, S_1, S_2, \dots, S_{n-1}$
 - one enable control input
- each J_i may be equal to one of the inputs s_i depending upon the control inputs.

2ⁿ inputs



→ Demultiplexer:

A demultiplexer (DEMUX) is a device that allows digital information from one source to be output onto a multiple lines for transmission over different destination. Consider an integer 'm' which is constrained by the following relation:

$$m = 2^n, \text{ where } m \text{ and } n \text{ are both integers.}$$

→ A 1-to-m demultiplexer has:

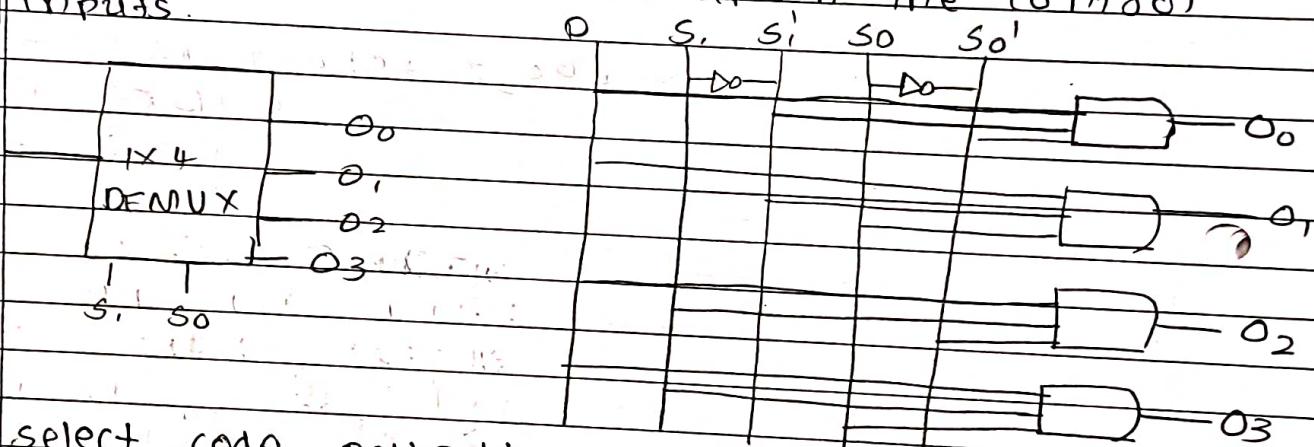
One input: D

m outputs: $O_0, O_1, O_2, \dots, O_{m-1}$

n control inputs: $S_0, S_1, S_2, \dots, S_{n-1}$

(one or more enable inputs)

→ such that D may be transferred to one of the output, depending upon the control inputs.



Select code output

S_1	S_0	O_3	O_2	O_1	O_0
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	D	0	0
1	1	D	0	0	0

- Q.S) describe parity checker & generator:-
- i) parity checker:
 - The three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit.
 - The parity checker circuit checks for possible errors in the transmission.
 - Since the information was transmitted with even parity, the four bits received must have an even no of 1's. An error occurs during the transmission if the four bits received have an odd no of 1's.
- four bit parity error check.

P A B C PEC

0 0 0 0 0

0 0 0 1 1

0 0 1 0 1

0 0 1 1 0

0 1 0 0 1

0 1 0 1 0

0 1 1 0 1

0 1 1 1 1

1 0 0 0 1

1 0 0 1 0

1 0 1 0 0

1 0 1 1 1

1 1 0 0 0

1 1 0 1 1

1 1 1 0 1

1 1 1 1 0

$$PEC = \bar{P}\bar{A}(\bar{B}C + BC + \bar{B}\bar{A})$$

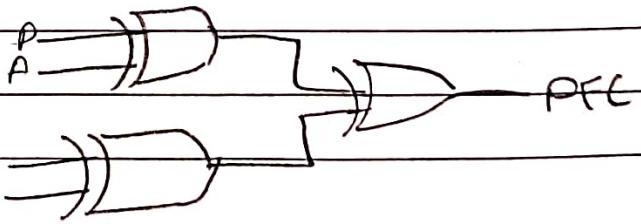
$$+ \bar{P}A(\bar{B}C + BC + \bar{B}\bar{A})$$

$$+ PA(\bar{B}\bar{C} + BC)$$

K-map:

PA	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	1	0	0
10	0	0	1	1

$$PEC = (P \oplus A) \oplus C(C \oplus B)$$



→ Parity generation:
 → Binary data, when transmitted or processed
 is susceptible to noise that can alter
 its 1s to 0s and 0s to 1s
 → To detect such errors, an additional bit
 called parity bit is added to the data bits
 and the word containing the data bits
 and the parity bit is transmitted.

even parity odd parity

0	0	1	1	1	0	1	0	1
---	---	---	---	---	---	---	---	---

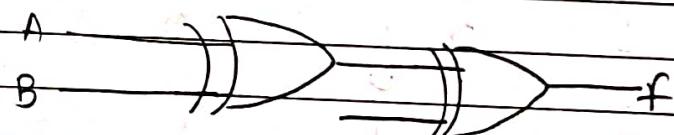
Input Output

A	B	C	F	A'B	AB	BC	AC	ABC
0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	1	0	0
0	1	0	1	1	1	0	1	0

$$f = A'B'C + A'BC' + ABC + AB'C'$$

$$f = \overline{A} \oplus \overline{B}$$

$$f = A \oplus B \oplus C$$



Kiss

6/11/2023

Assignment - 3

Q.1 Differentiate sequential & combination circuits.



combination circuit	sequential circuit
In combination circuit the output variable at any instant of time is dependent only on the present input variable.	In sequential circuit output variable at any instant of time is dependent not only on the present state.
memory unit is not required in this circuit.	memory unit is required in this circuit.
combinational circuits use fuses because the delay bet ⁿ the input and output is propagation delay.	sequential circuits do slower than combinational circuits.

Q.2 List & explain flip flop.

- A flip-flop known formally as bistable multivibrator has two stable states.
- Following are flip-flop.

i) S-R flip flop

- A gated S-R latch requires an EN input
- This type of flip-flop responds to the changes in input only as long as the also called level triggered.

EN S R Qn Qn+1 STATE

1 0 0 0 0 NO S

1 0 0 1 1 change

1 0 1 0 0 reset

1 0 1 1 0

1 1 0 0 1 set

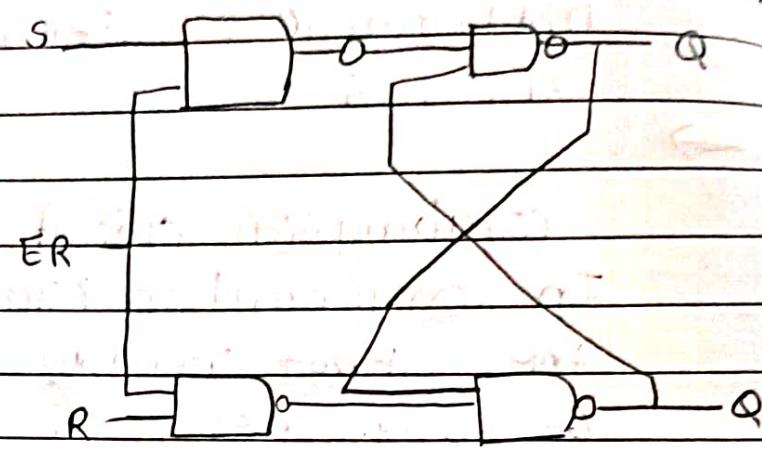
1 1 0 1 1

1 1 1 0 X invalid

1 1 1 1 X

0 X X 0 0 NO

0 X X 1 1 change



ii) D flip-flop:-

→

EN D Qn Qn+1 STATE

1 0 0 0 0 Reset

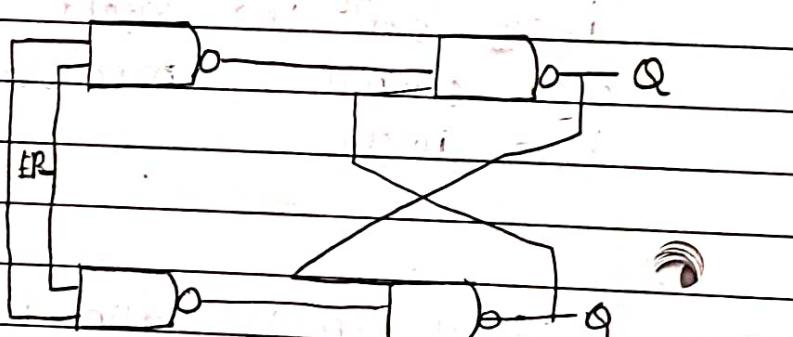
1 0 1 0

1 0 1 1 set

1 1 1 1

0 X 0 0 NO

0 X 1 0 change



→ It differs from the S-R latch in that

→ it has only one input in addition to EN.

→ we can say that the output Q follows the

D input when EN is HIGH.

ii) J-K flip-flop:

→ The J-K flip-flop is very versatile and

also the most widely used.

En J K On Qn+1 STATE

1 0 0 0 0 no

1 0 0 1 1 change

1 0 1 0 0 Reset

1 0 1 1 0

1 1 0 0 1 set

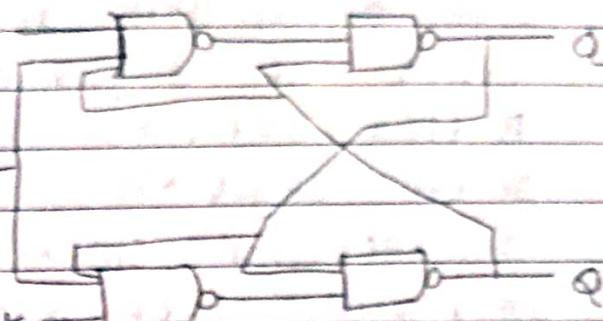
1 1 0 1 1

1 1 1 0 1 toggle → The function is identical

1 1 1 1 0

0 x x 0 0 no except that this has no neutral

0 x x 1 1 change state like that.



iv) T flip-flop:-

En T Qn Qn+1 STATE

1 0 0 0 no

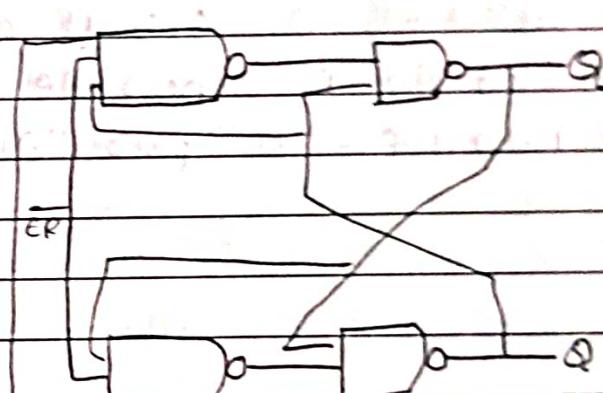
1 0 1 1 change

1 1 0 1 toggle

1 1 1 0

0 x 0 0 no

0 x 1 1 change



→ AT flip-flop has a single control input labeled T for toggle.

→ Although T flip-flops are not widely available commercially it is easy to convert a JK flip-flop to the functional equivalent of a T flip-flop by just connecting J and K together and labeling the common connection as T.

Q.3

List & explain registers.

→ TYPES OF REGISTERS.

1. Buffer register

2. Shift register

3. Bidirectional shift register

4. Universal shift register

→ Shift register

A number of FFS connected together such that data may be shifted into and shifted out of them is called a shift register.

→ There are four basic types of shift register

1. serial-in, serial-out

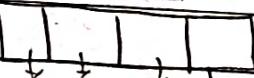
2. parallel-in, serial-out

3. serial-in, parallel-out

4. parallel-in, parallel-out



serial-in, serial-out



parallel-in, parallel-out

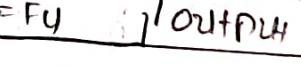
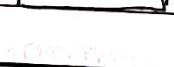
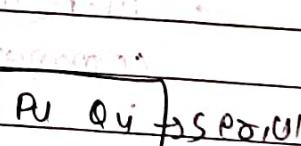
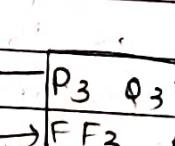
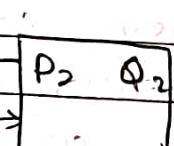
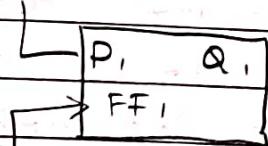


serial-in, parallel-out



parallel-in, serial-out

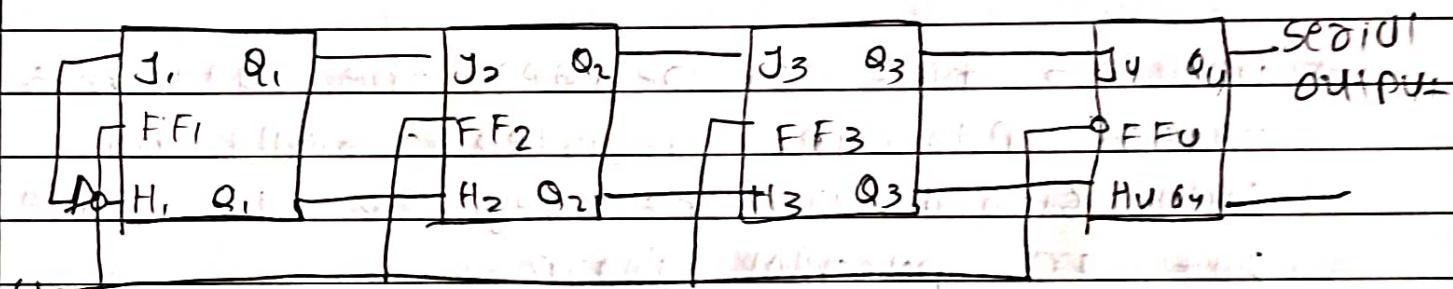
+ serial-in, serial-out



with four stages, i.e. four FFs, the register can store up to four bits.

Serial data is applied at the D input of the first FF. The Q output of the first FF is connected to the D input of the second FF. So after four clocking

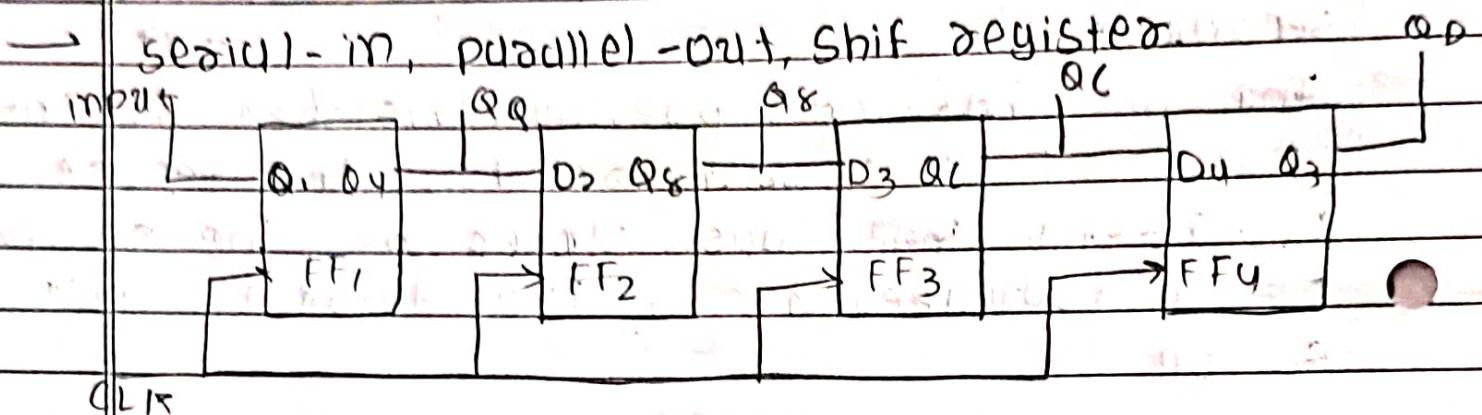
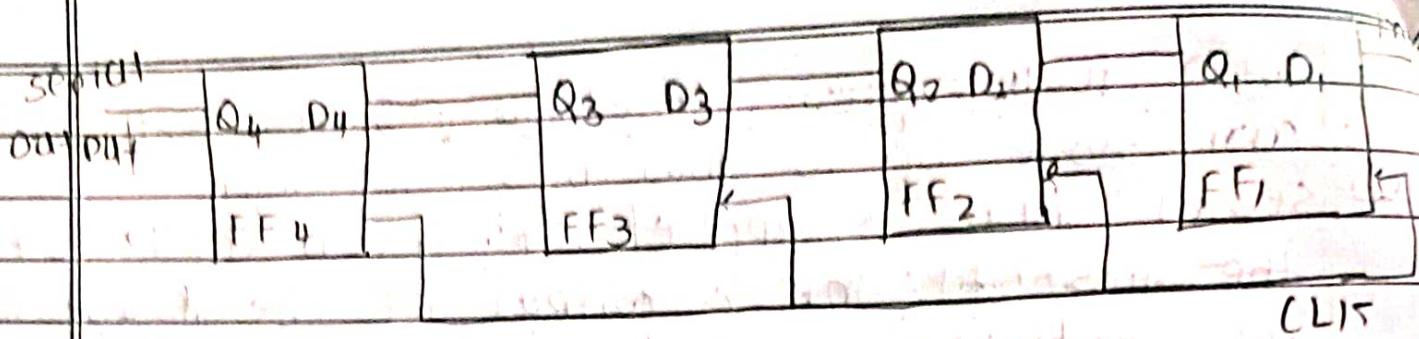
The bit that was previously stored by the first FF is transferred to the second FF. The bit that was stored by the second FF is transferred to the third FF, and so on.



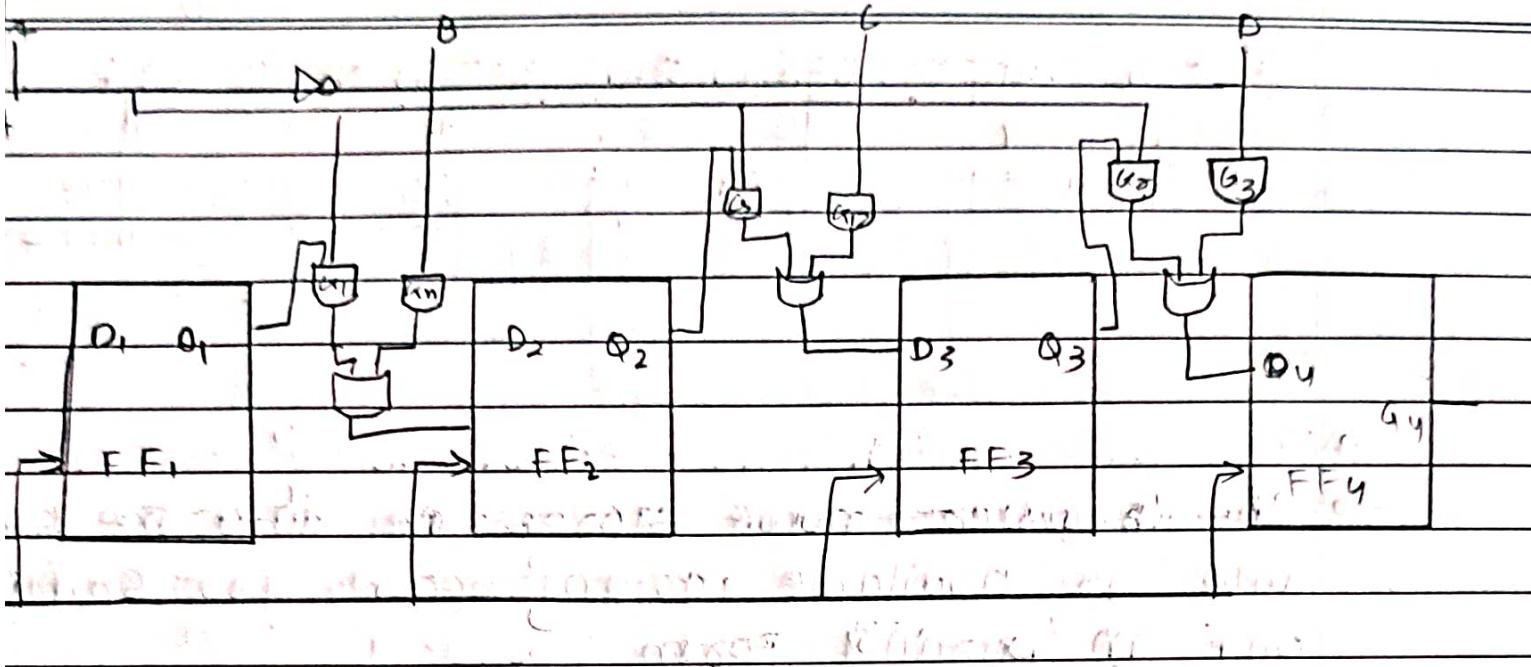
A shift register can also be constructed using J-K FFs as shown in above figure.

The data is applied at the J input of the first FF. The complement of this is fed to the K input of FF.

The Q output of the first FF is connected to J input of the second FF, the Q output of the second FF to J input of the third FF and so on.



- in this type of register, the data bits are entered into the register serially, but the data stored in the register is shifted out in parallel form.
- The serial-in, parallel-out, shift register can be used as a serial-in, serial-out, shift register if the output is taken from Q-terminal of the last FE.
- parallel-in, serial-out, shift register.
- there are four data lines A, B, C and D through which the data is entered into the register in parallel form.
- The signal shift load allows the data to be entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q_4 .

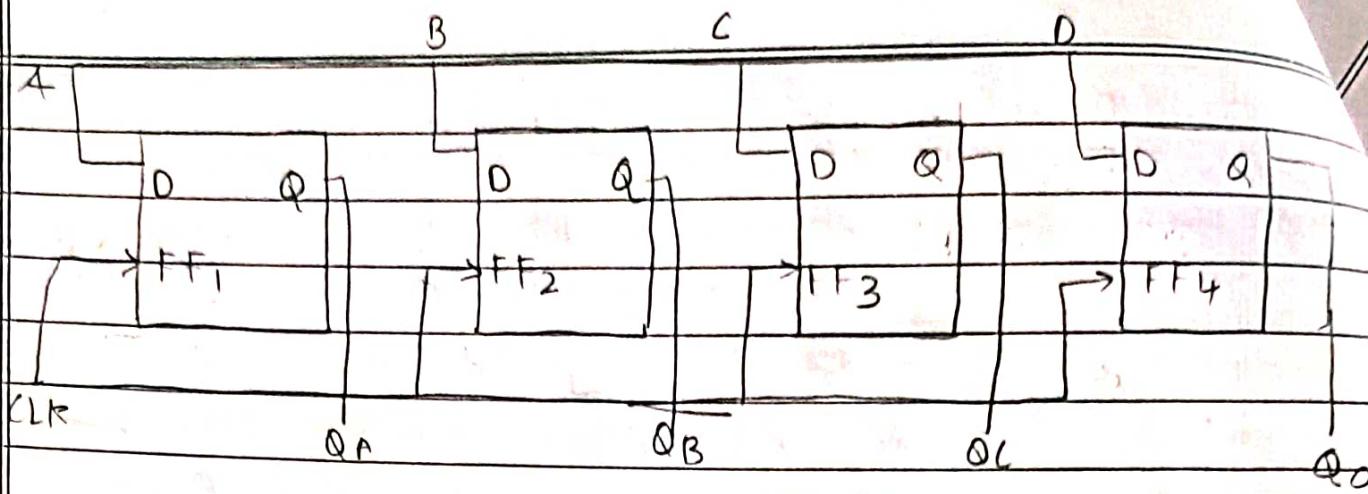


when Shift Load line is HIGH, gates G₁, G₂ and G₃ are disabled but gates G₅, G₆ and G₇ are enabled allowing the data bits to shift right from one stage to the next. The OR gate allows either the normal shifting operation or the parallel entry depending which NAD gates are enabled by the level on the shift load input.

parallel-in, parallel-out, shift register. In a parallel-in, parallel-out, shift register the data is entered into the register in parallel form, and also the data is taken out of the register in parallel form.

Data is applied to the D input terminals of the FFS.

When a clock pulse is applied to terminal of the FFS of the FFS.



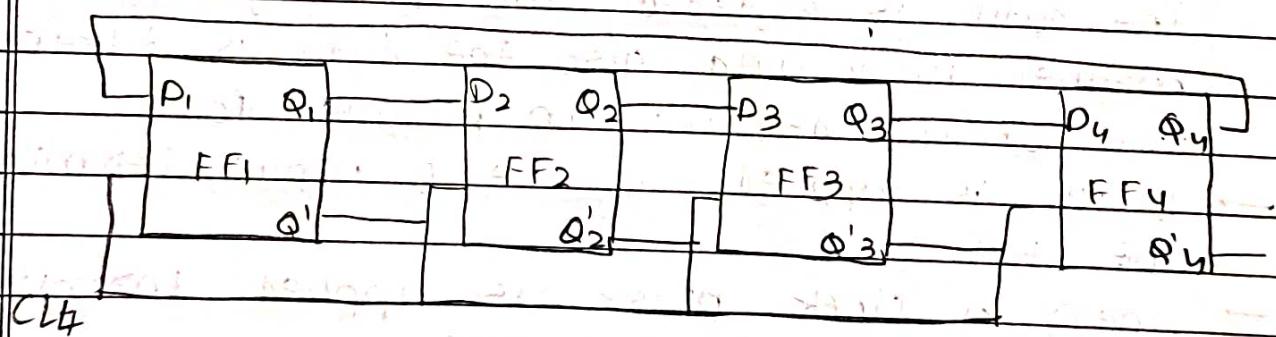
→ the register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

Q.4

Describing counter

→ This is the simplest shift register counter. The basic ring counter using D FFs is shown in Fig.

→ The FFs are arranged as in a normal list register i.e. Q output of each or each stage is connected to the D input of the next stage but the Q output of the last FF is connected, and therefore, the name ring counter.



state diagram sequence table

	Q ₁	Q ₂	Q ₃	Q ₄	After clock pulse
0001	1	0	0	0	0000
0000	0	1	0	0	0001
0001	0	0	1	0	0010
0010	0	0	0	1	0011
0011	0	0	1	1	0100
0100	0	1	0	0	0101
0101	0	0	0	1	0110
0110	0	0	1	0	0111
0111	0	1	0	0	1000
1000	1	0	0	0	0001

In most instances, only single 1 is

in the register and is made to

circulate around the register as

long as clock pulses are applied initially.

The first FF is preset to a 1.

The sequence repeats after four clock pulses.

Describe how to design counters using flip-flops.

Step 1: Number of flip-flops:-

Based on that describe of the problem, determine the required number n of the FFS - the smallest value of n is such that the number of states $N \leq 2^n$ and desired counting sequence.

Step 2: State diagram.

Draw the state diagram showing all the possible states.

Step 3: choice of flip-flops and excitation table:

Select the type of flip-flops to be used and write the excitation table.

Step 4:- minimal expressions for excitations:

Obtain the minimal expressions for the excitations of the FFS using k-maps for the excitation of the flip-flop in terms of the present states and inputs.

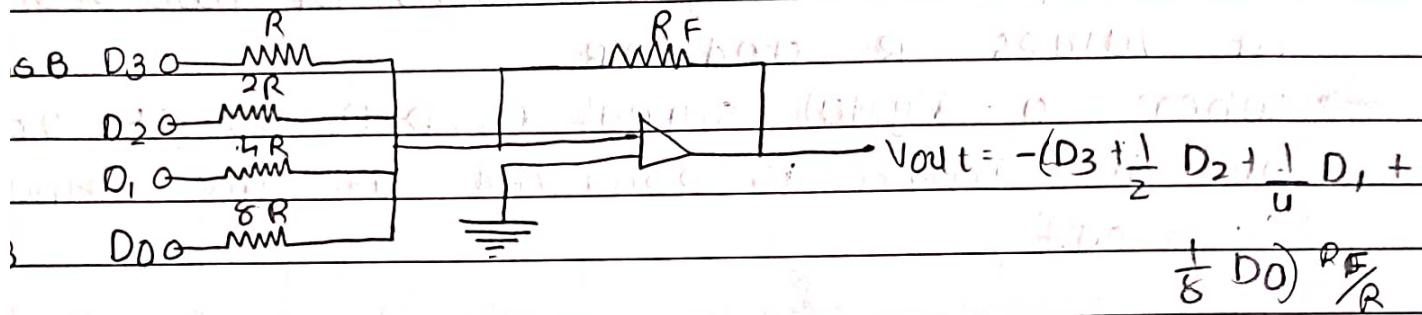
Step 5:- logic diagram:-

Draw the logic diagram based on the minimal expressions.

6/1/2>

Assignment: 4

Explain weighted resistor converter.



The diagram shown is the weighted-resistor DAC is shown in figure.

The operational amplifier is used to produces weight sum of the digital inputs where the weights are proportional to the weights of the bit positions of input.

since the op-amp is connected as an inverting amplifier, each input is amplified by factor equal to the ratio each input is amplified by a factor equal to the ratio to which it is connected.

The msb D_3 is amplified by R_F/R , D_2 is amplified by $R_F/2R$, D_1 is amplified by $R_F/4R$, D_0 the lsb is amplified by $R_F/8R$.

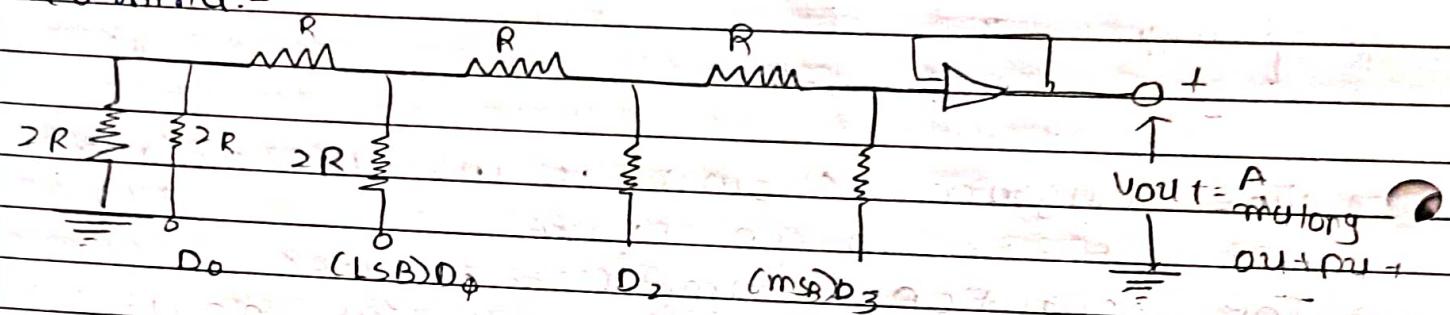
since the op-amp adds and inverts

$$V_{out} = -(D_3 + D_2/2 + D_1/4 + D_0/8) \times \left(\frac{R_F}{R}\right)$$

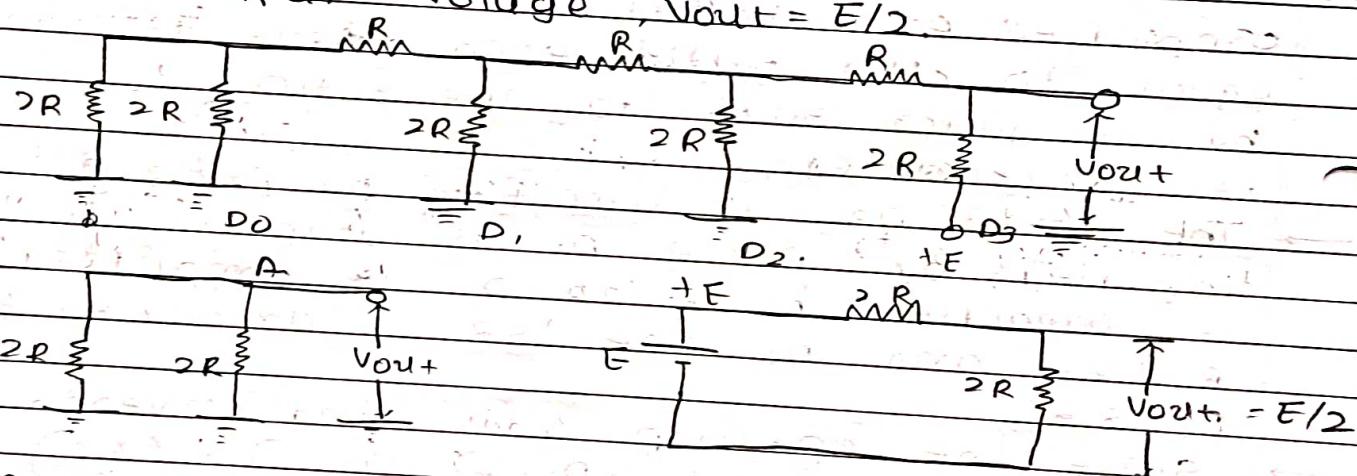
Explain R-2R ladder D/A converter -

It uses a ladder network containing series-parallel combinations of two resistors of values R and $2R$.

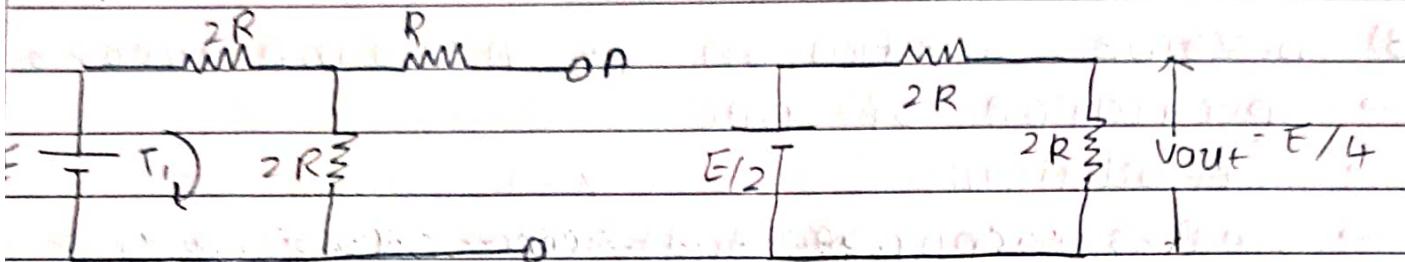
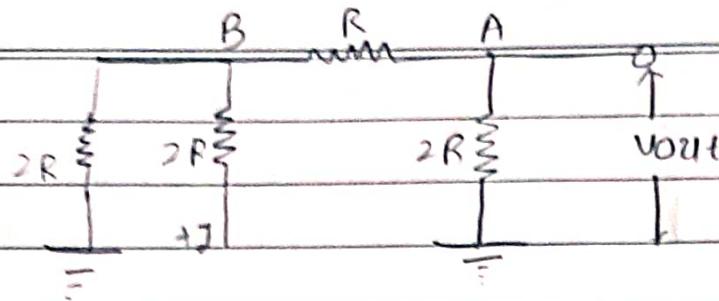
When a digital signal D_0, D_1, D_2, D_3 is applied at the input it produces at the output terminal:-



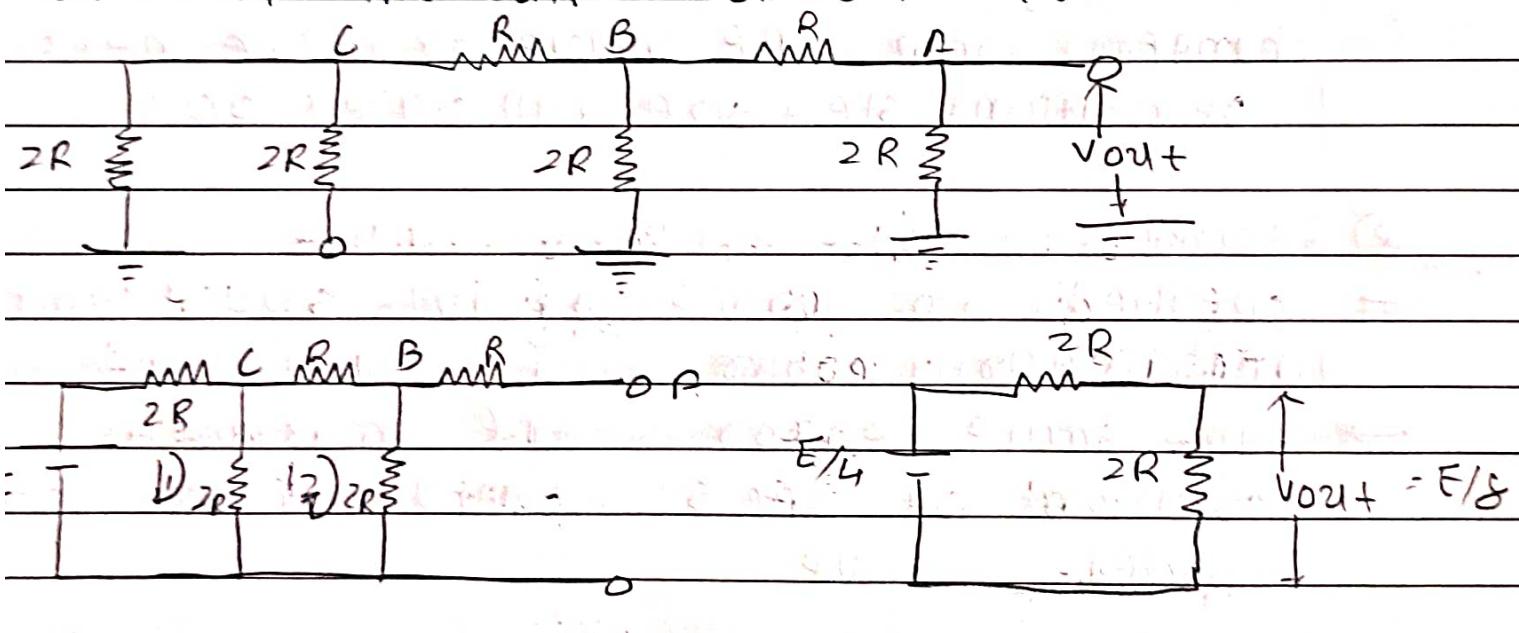
Case 1: when the input is 1000
Below figure illustrates the procedure to calculate V_{out} when the input is 1000.
The output voltage, $V_{out} = E/2$.



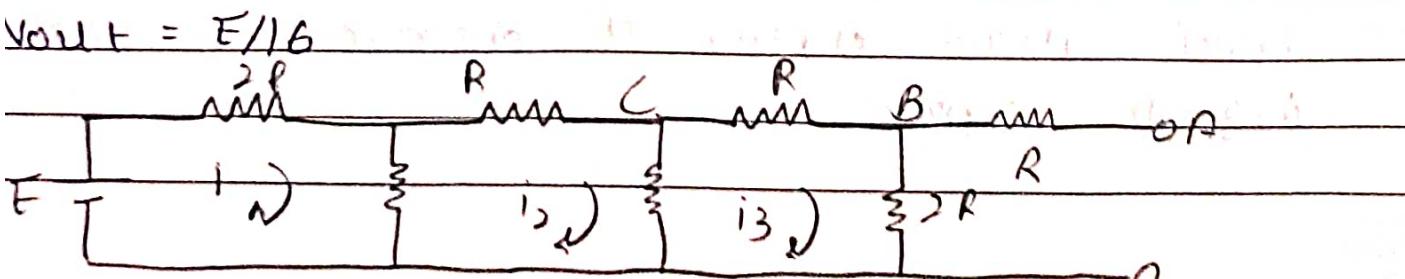
Case 2: when the input is 0100
Below figure illustrates the procedure to calculate V_{out} .

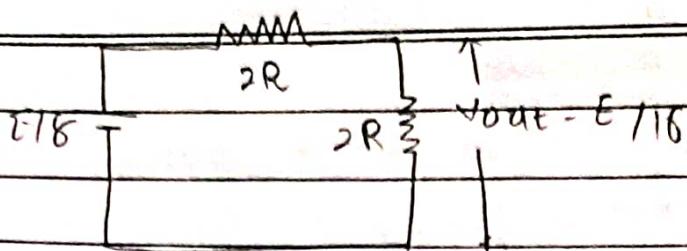


case 3:- when the input is 0100. Below figure illustrates the procedure to calculate V_{out} . Here, we find that to left of terminal C, $R_{eq} = 2R$, The output voltage, $V_{out} = E/8$



case 4: when the input is 0000. Below fig illustrate the procedure to calculate V_{out} .





Q 3) Describe specification of A/D & D/A converter.

→ Specification of DAC

→ i) Resolution:-

smallest change that can occur in an analog output as a result of a change in the digital input.

→ Equals to the weight of the LSB and also referred to as the step size.

→ Step size is the amount by which V_{out} will change as the digit input value is changed from one value to the next.

$$\text{Resolution} = \text{Step size} / \text{full scale} \times 100\%.$$

Q2) Accuracy:-

→ Specified in terms of full-scale error or linearity error.

→ Full-scale error is the maximum deviation of DAC's output from its expected value.

Q3) Settling time:

→ the time required for the analog output to settle to within $\pm 1/2$ LSB of the final value after a change in the digital input.

offset voltage:-

Ideally the output of a DAC should be zero when the binary input is zero.

monotonicity:-

This means that the staircase output will have no downward steps as the binary input is incremented from 0 to full-scale value.

specification of ADC.

Range of input voltage

Input impedance

Accuracy

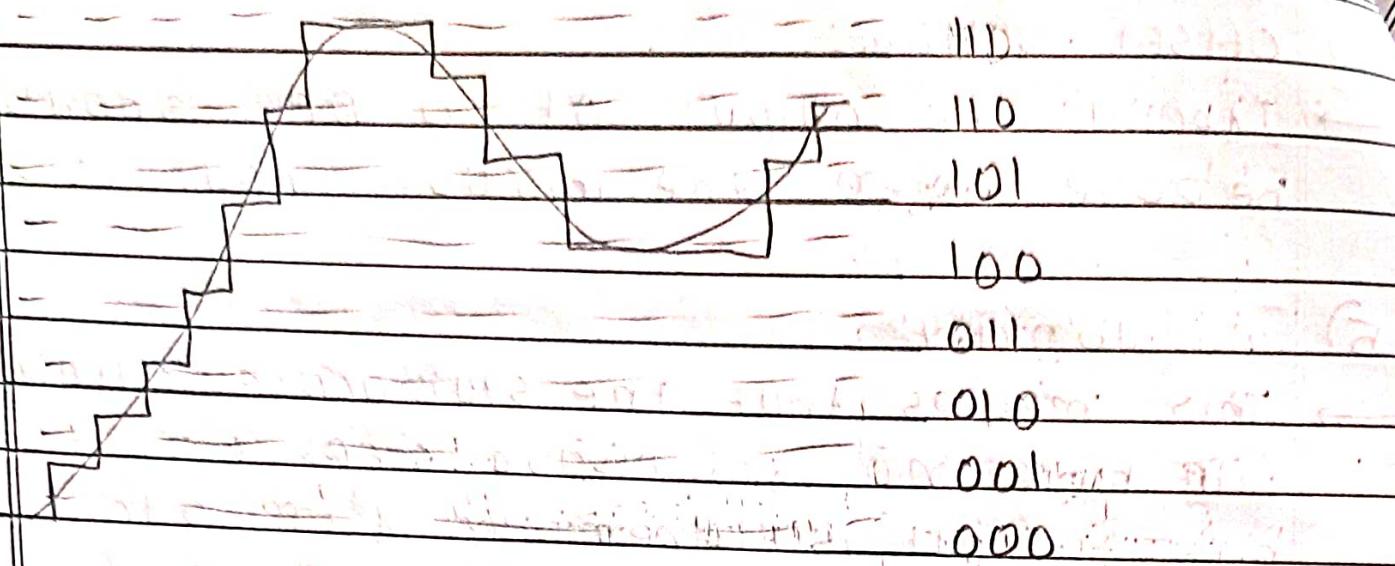
conversion time

format of digital output.

Explain quantization and encoding.

In a digital-to-analog converter, the possible number of digital inputs is fixed. Therefore, the whole range of analog voltage is required to be represented suitably in 2^n intervals.

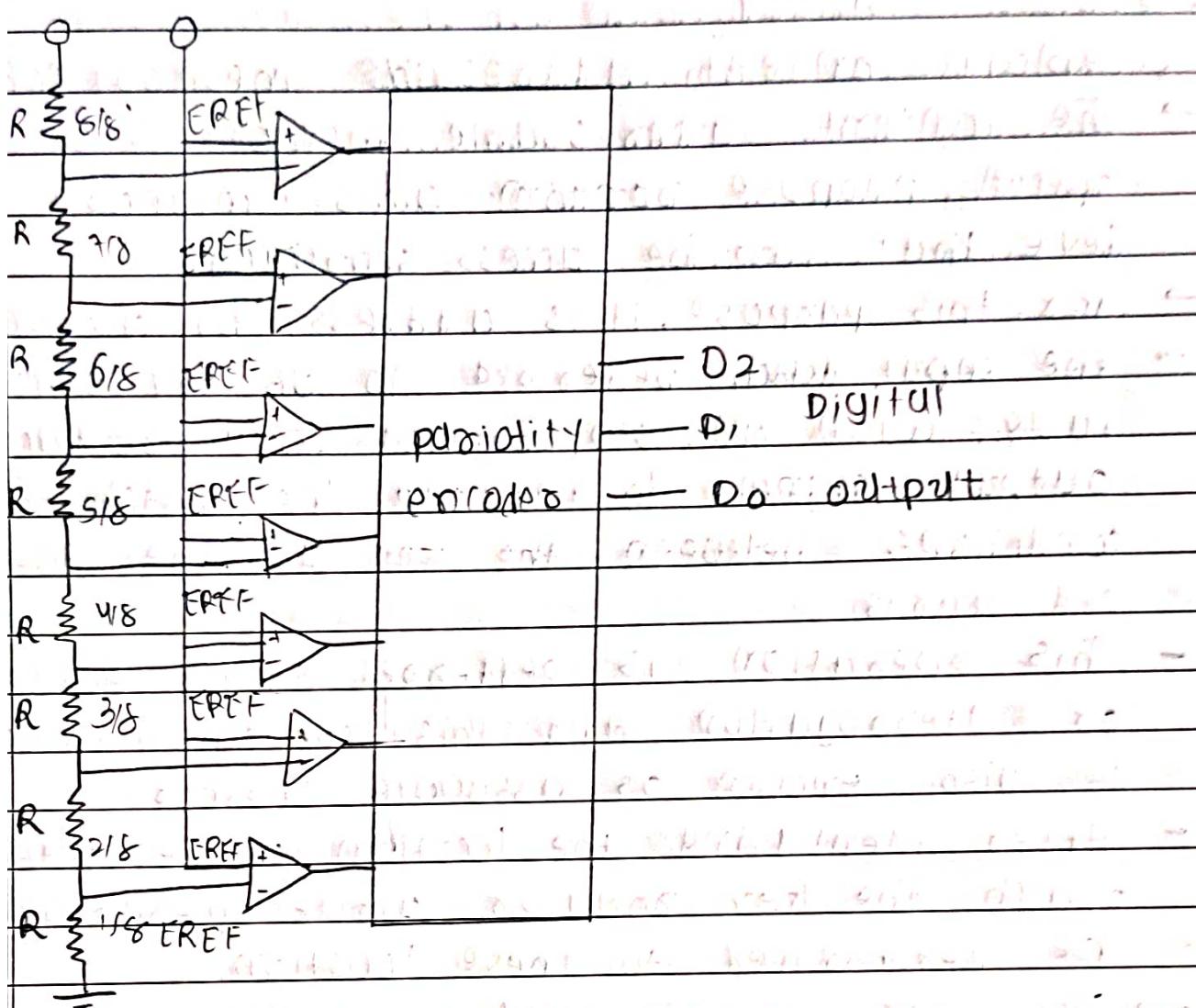
This process is known as quantization. Consider an analog voltage in the range of V_{min} to V_{max} and a 3-bit digit. The whole range of analog voltage is divided into $2^3 = 8$ intervals. Each interval is assigned a 3-bit binary value.



- From this, we observe that the whole range of voltage in one interval is represented by only one digital value.
- Therefore, there is an error affected to ds quantization error, involved in this process of quantization.

- Explain parallel comparator A/D converter.
- The flash type A/D converter is the fastest type of A/D converter.
 - This type of converter utilizes the parallel differential comparators that compare reference voltages with the analog input voltage.
 - A reference voltage V_{ref} is connected to a voltage divider that divides it into 7 equal increment levels.
 - For any given analog input, one comparator and those below it will have a HI to LL output.

Flash converter



the digital output represents the voltage that is closest in value to the analog input.

$$\left(\frac{7R}{7R+R}\right) \times E_{REF} = \frac{7}{8} E_{REF}$$

similarly, the voltage applied to the inverting input of the second comparator is

$$\left(\frac{6R}{6R+R}\right) \times E_{REF} = \frac{6}{7} E_{REF}$$

The flash converter uses no clock signal, because there is no timing or sequencing period.

$\frac{1}{6}$ bits

Assignment 5

Q.1

Explain content addressable memory (CAM)

The content addressable memory is a special purpose random access memory device that can be accessed searching.

→ for this purpose, it is addressed by associating the input data, referred to as key, simultaneously with all stored words in parallel output signals to indicate the match conditions between the key and the stored words.

- This operation is referred to as association or interrogation and this type of memory is also known as associate memory.

- After identifying the location whose contents match the key and/or write operation can be performed to these locations.

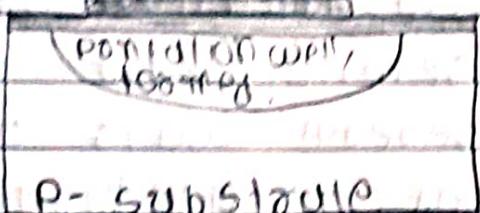
→ The key to be used may either consist of the entire data or only some specific bits of the data word.

→ If one is interested in finding out engineers in the list, the CPM is able to check every memory location simultaneously by using the codes form for engineers as the key.

→ On the other hand the key will consist of the combination of the codes corresponding to engineer and Indian National

→ All the memory location with engineers of Indian nationality operation.

Explain charge coupled device memory.



POTENTIAL WELL FORMING

The CCD memory is type of dynamic memory, in which packets of charges are continuously transferred from one mos device to another.

The structure of mos devices is quite simple. When a high voltage is applied to the metal gate holes are repelled from oxygen called a potential well.

Data in the form of charge is transferred from one device to another one by clocking their gates.

The CCD memory is inherently serial. Parallel memories are constructed in the form of shift registers.

By controlling the timing of the clock signals update.

The principal advantage of the CCD memory is that single cell structure makes it possible to construct large capacity memories at low cost.

Q.3

Explain classification of memory.

→ The table shows the classification of semiconductor memory devices. The semiconductor devices can be categorized in several ways according to their functional and architectural characteristics.

Classification of semiconductor memories

Non-volatile memory → volatile memory.

Read only memory	Read/write memory	Random Access	non-Random Access
mask ROM, EEPROM	(RAM)		
programmable ROM			
programmable ROM	• EEPROM	• SRAM	• FIFO
	• FLASH	• DRAM	• LIFO

Q.4

Describe - semiconductors.

- A semiconductor is a substance whose resistivity lies between the conductors and insulators. The property of resistivity is not the only one that decides a material as a semiconductor but it has few properties as follows.
- Semiconductor resistivity is ^{less} ~~more~~ than conductor and ^{more} ~~less~~ than insulator.
- Semiconductors have negative temperature coefficient. The resistance in semiconductors increase with the decrease in temperature and vice versa.

THE WATERTOWER HAD BEEN BUILT ON THE
WILLIAMS PROPERTY, WHICH WAS OWNED BY THE
LAW IN 1888. HE SOLD IT TO THE CITY OF BIRMINGHAM.

THE WATERTOWER

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