



# **Government Engineering College**

## **Sec-28 Gandhinagar**

**Sem: - 3**

**Subject: - Digital Fundamental**

**Subject Code: - 3130704**



# Government Engineering College

## Sec-28 Gandhinagar

### Certificate

This is to certify that

Mr./Ms. .... Lalkiya Dipal K ..... Of class

..... CE ..... Division A ....., Enrollment No. .... 210130107054 .... Has

Satisfactorily completed his/her term work in

..... DF ..... Subject for the term ending in

..... Jan ..... 2022.

Date: - 07 / 01 / 2023

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# **Institute Vision/Mission**

## **Vision:**

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

## **Mission:**

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

# **Computer      Engineering      Department**

## **Vision/Mission**

**Vision:**

**Mission:**

# Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

## PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

## POs

**Engineering Graduates will be able to:**

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

# **Digital Fundamental (3130704)**

## **Course Outcomes (COs)**

CO-1	
CO-2	
CO-3	
CO-4	
CO-5	

## **7. Assignment Index**

Sr. No	Assignment	Date	Page No.	Sign
1	Assignment 1			
2	Assignment 2			
3	Assignment 3			
4	Assignment 4			
5	Assignment 5			

## 8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1			
2	Practical 2			
3	Practical 3			
4	Practical 4			
5	Practical 5			
6	Practical 6			
7	Practical 7			
8	Practical 8			
9	Practical 9			
10	Practical 10			
11	Practical 11			

# **9. Assignment 1**

**CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra**

## **Module 1**

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function:  $F = A'B'C + A'BC + AB'$ .
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

# 10. Assignment 2

**CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem**

## Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
  - 2.1.  $F(x,y,z) = \Sigma (2,3,6,7)$
  - 2.2.  $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

# **11. Assignment 3**

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## **Module 3**

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

# **12. Assignment 4**

**CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.**

## **Module 4**

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

# **13. Assignment 5**

**CO5: Implement PLDs for the given logical problem.**

## **Module 5**

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA).

# 14. Practical 1

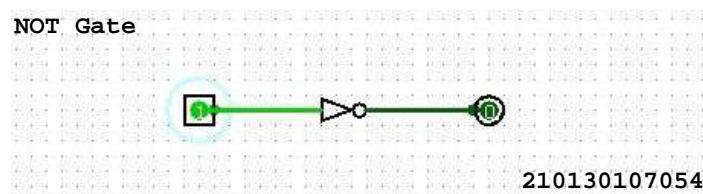
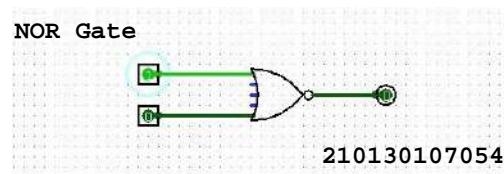
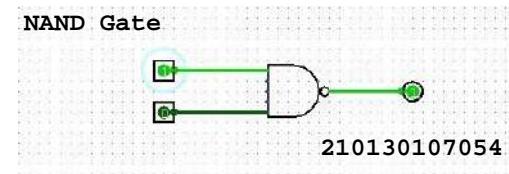
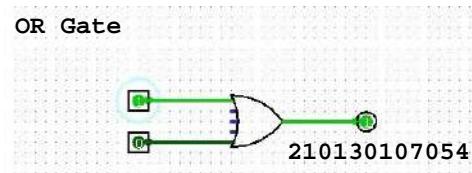
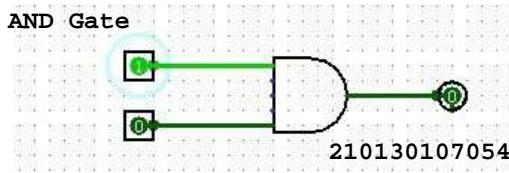
CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

## Module 1

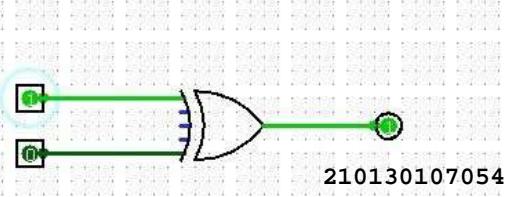
Aim: Getting familiar with Logisim, Study and implement all basic logic gates. Implement NAND and NOR logic gates as universal gates.

### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

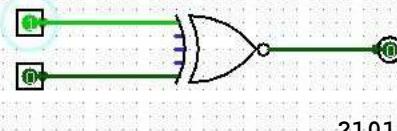


**XOR Gate**



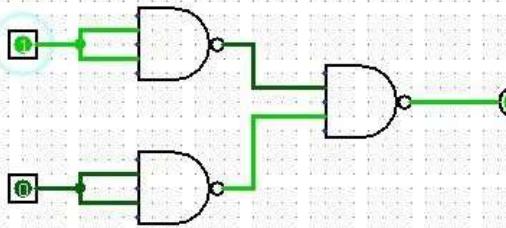
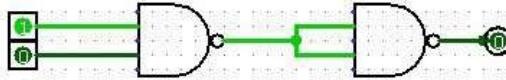
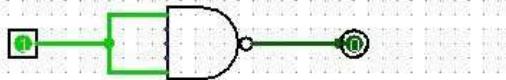
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**XNOR Gate**



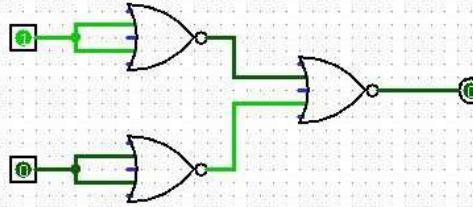
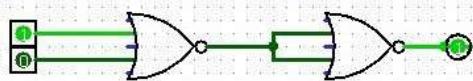
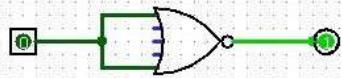
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**NAND Gate as Universal Gate**



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**NOR Gate as Universal Gate**



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# 15. Practical 2

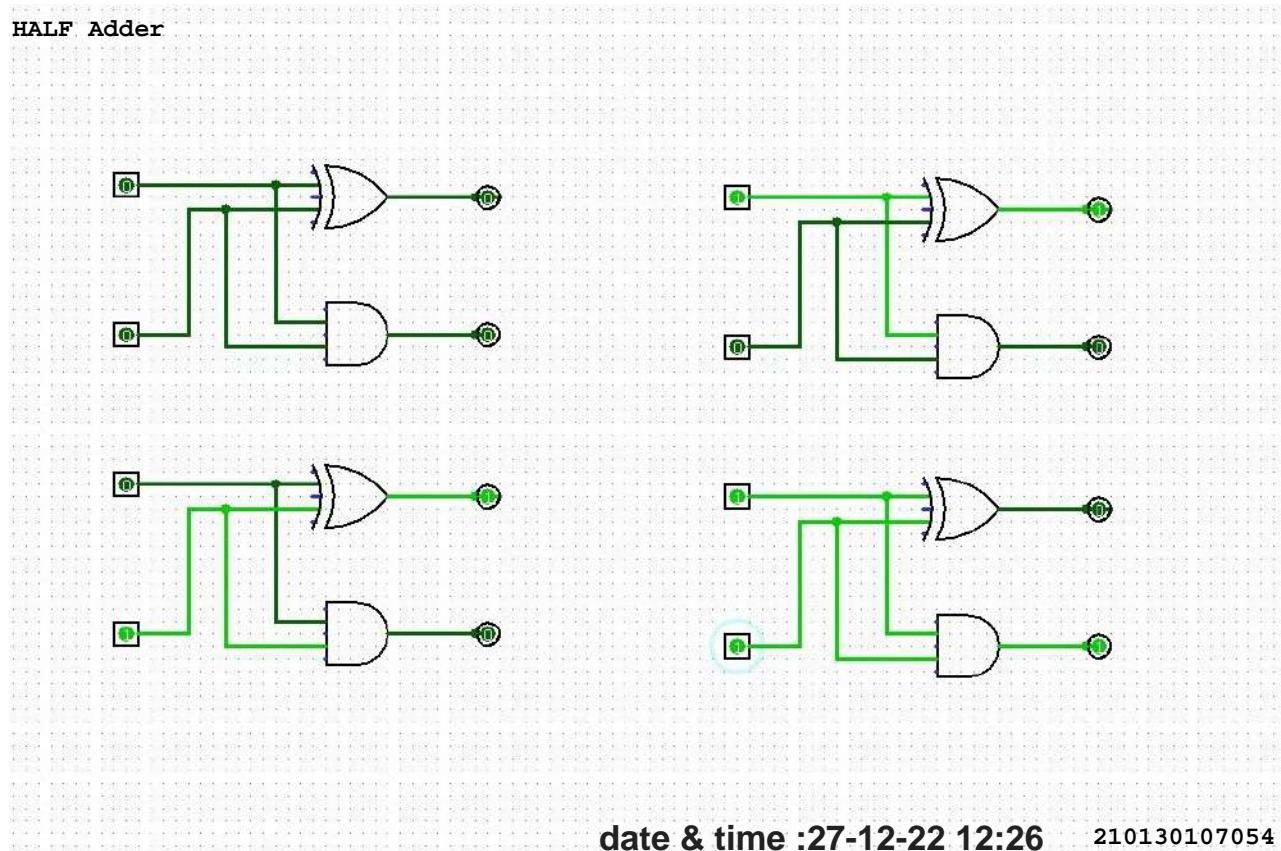
**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## Module 2

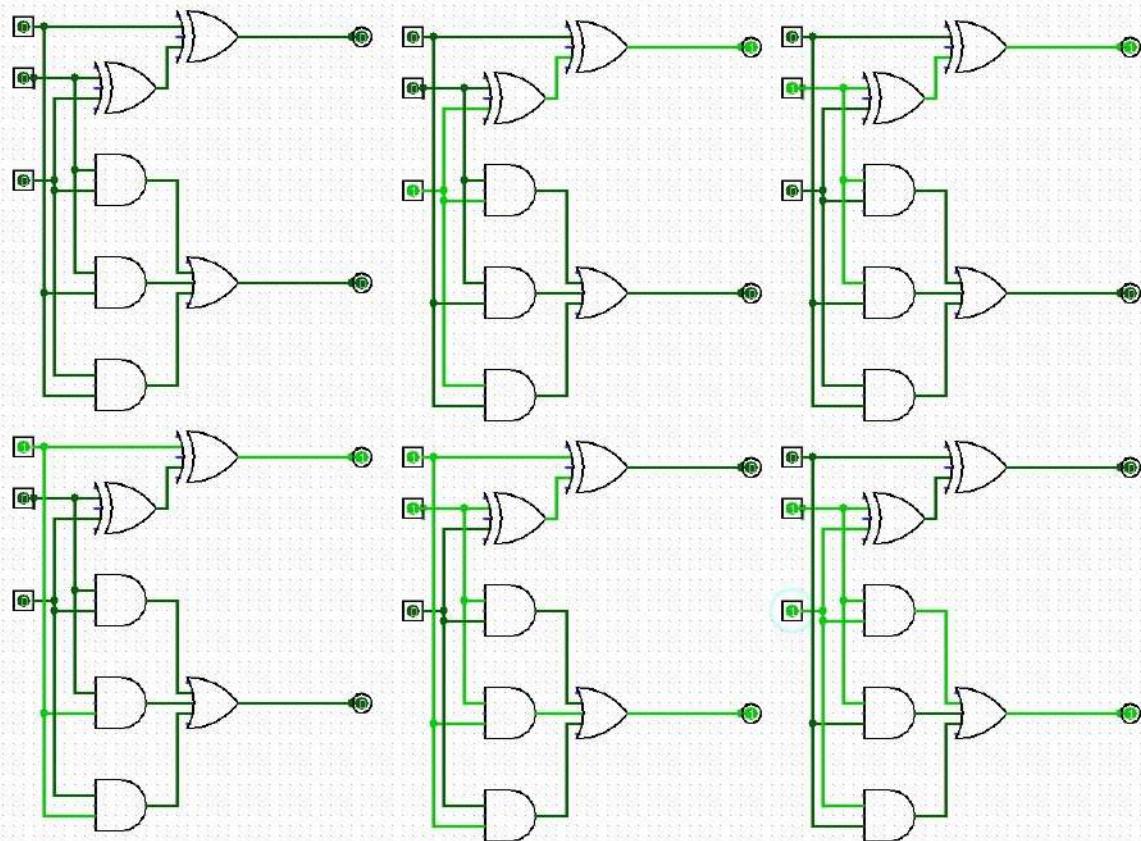
**Aim: Implement half and full Adders using logic gates.**

**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



### FULL Adder



date & time :27-12-22 1:20 210130107054



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# 16. Practical 3

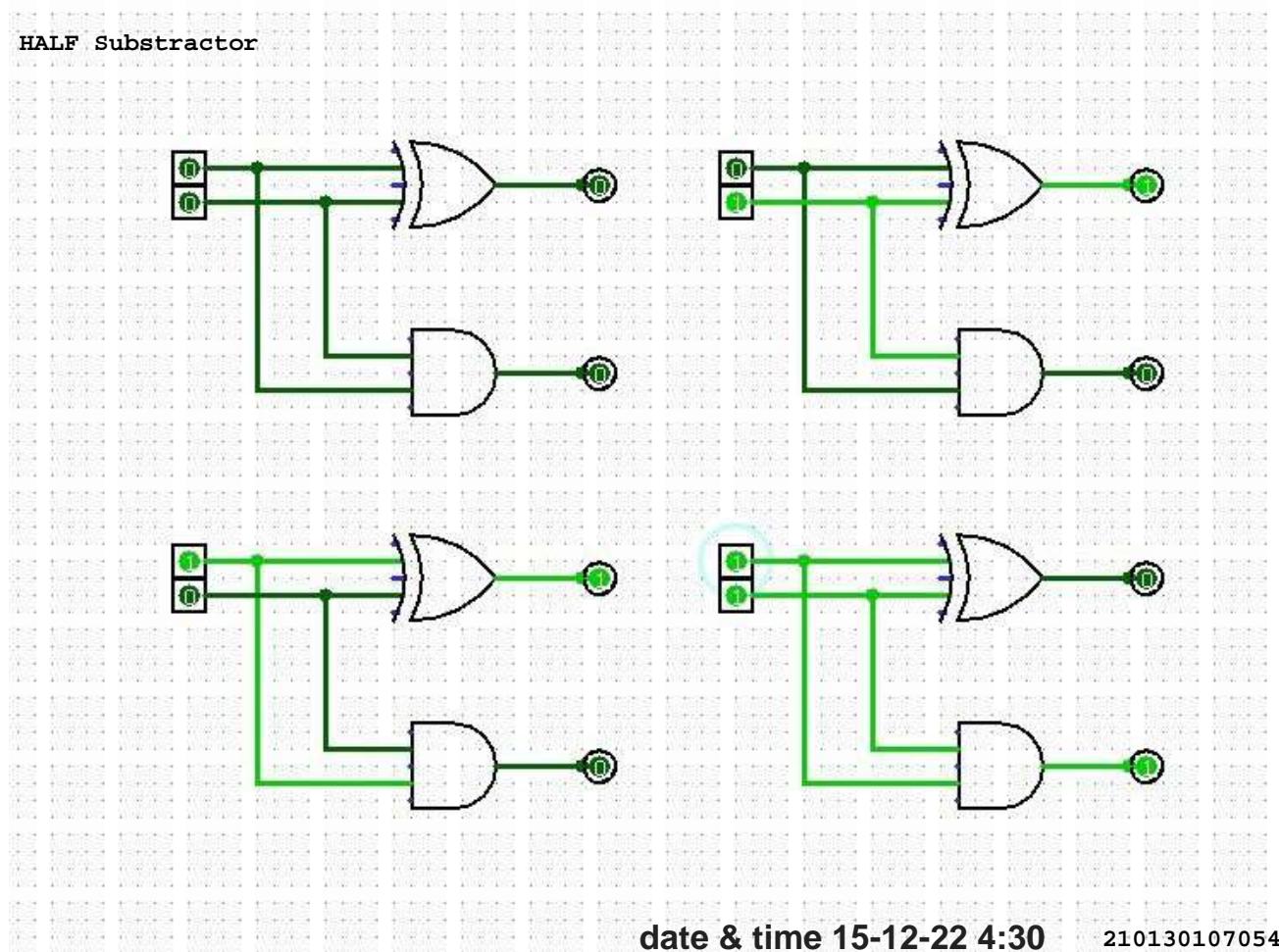
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

## Module 2

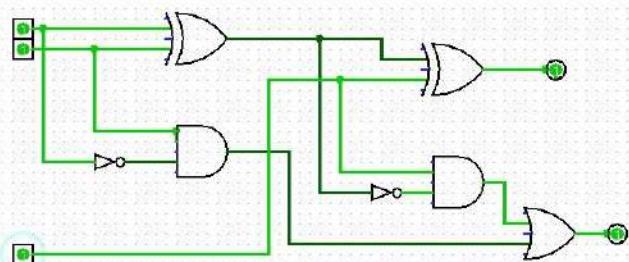
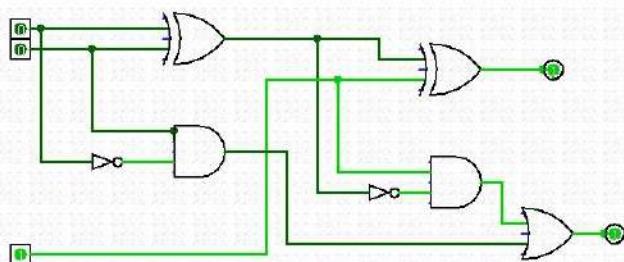
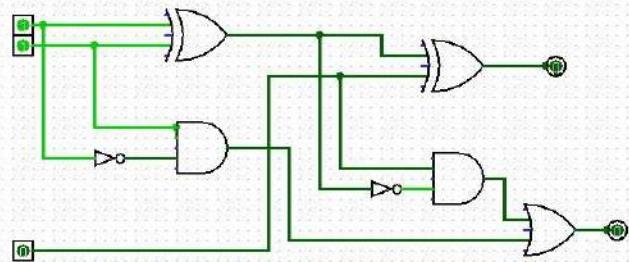
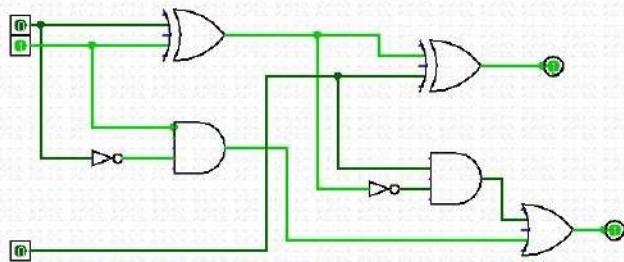
Aim: Implement half and full Subtractors using logic gates.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



**FULL Substractor**



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# 17. Practical 4

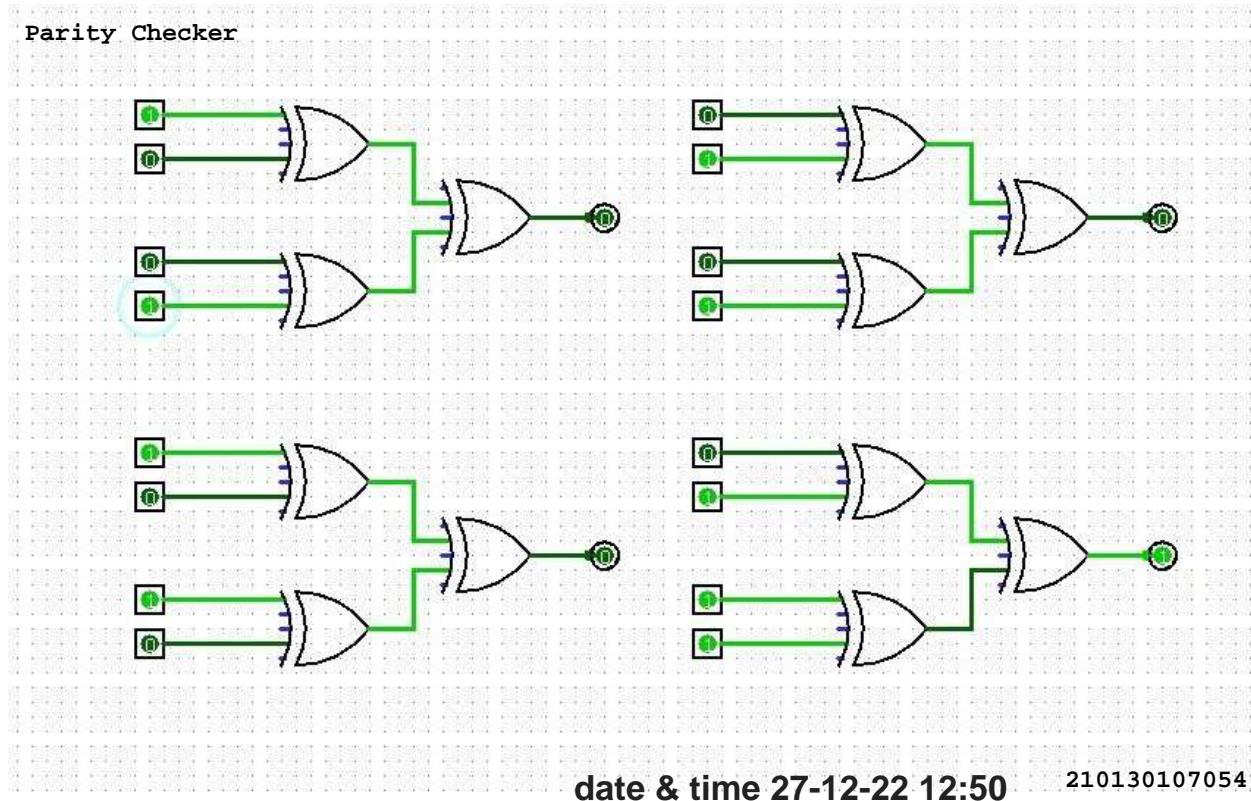
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

## Module 2

Aim: Perform Parity Checker.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



# 18. Practical 5

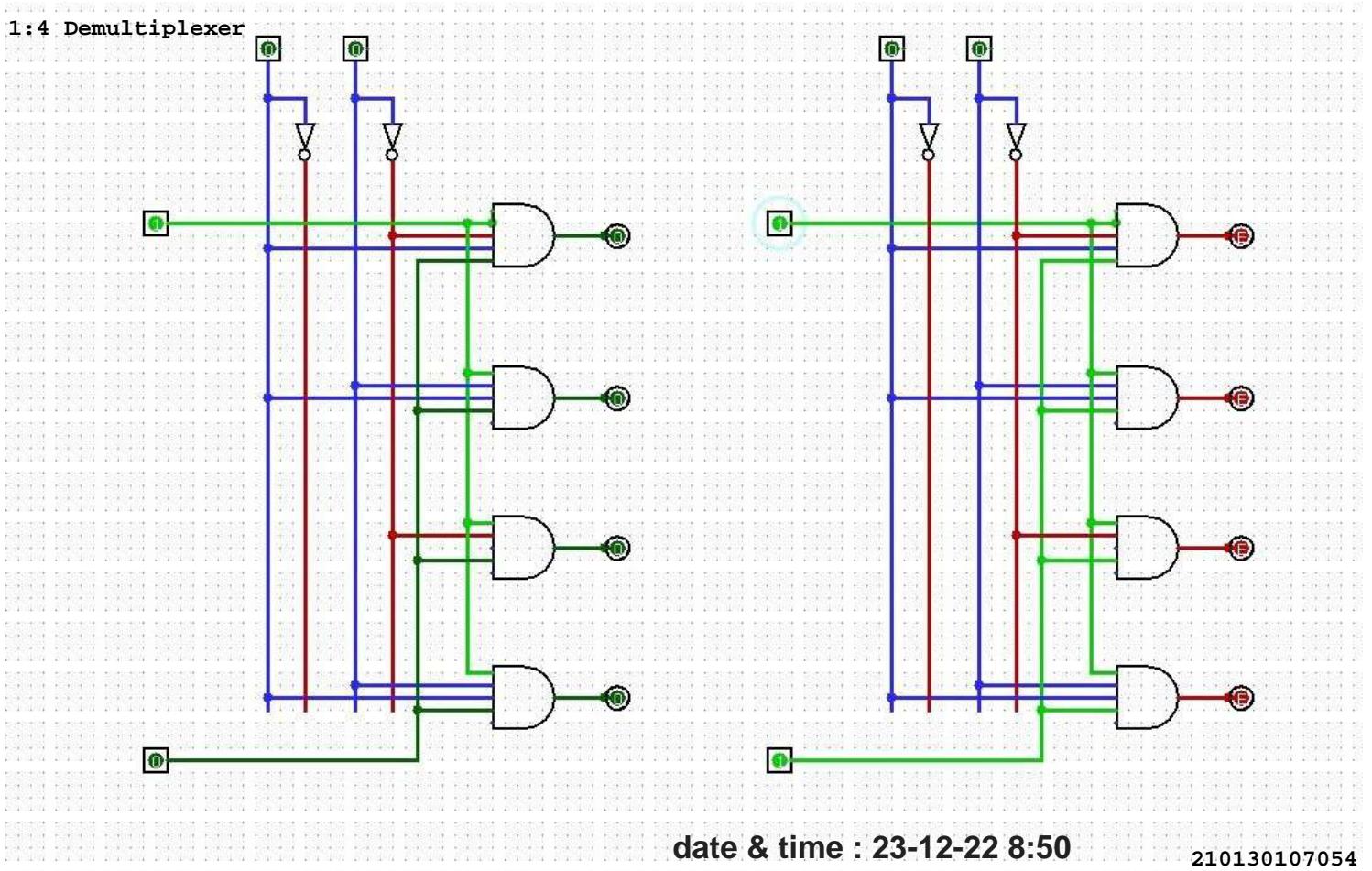
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

## Module 2

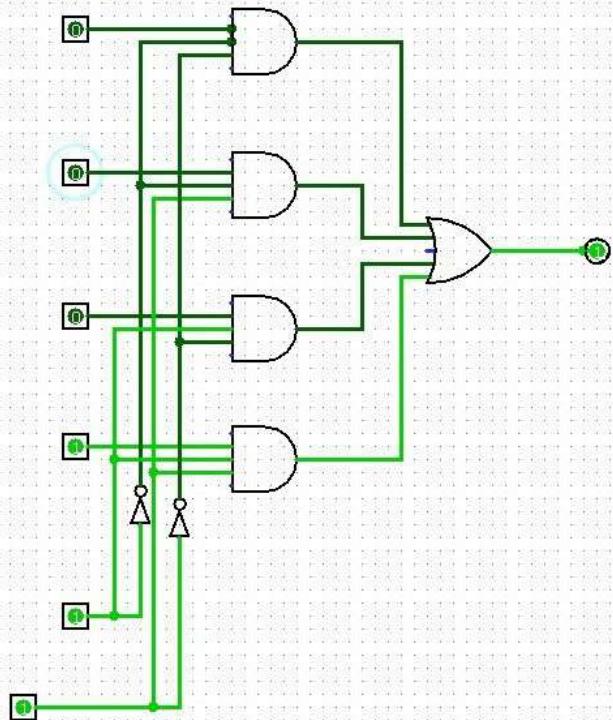
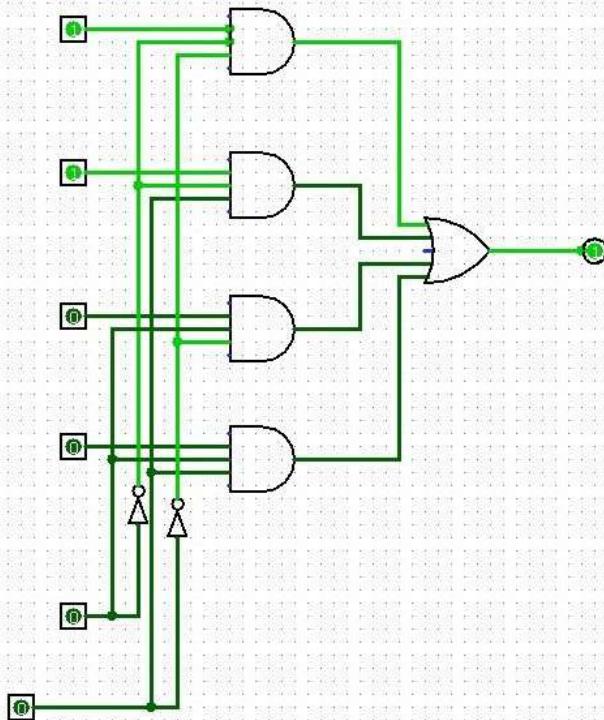
Aim: Study and implement Multiplexer and Demultiplexer.

### Code:

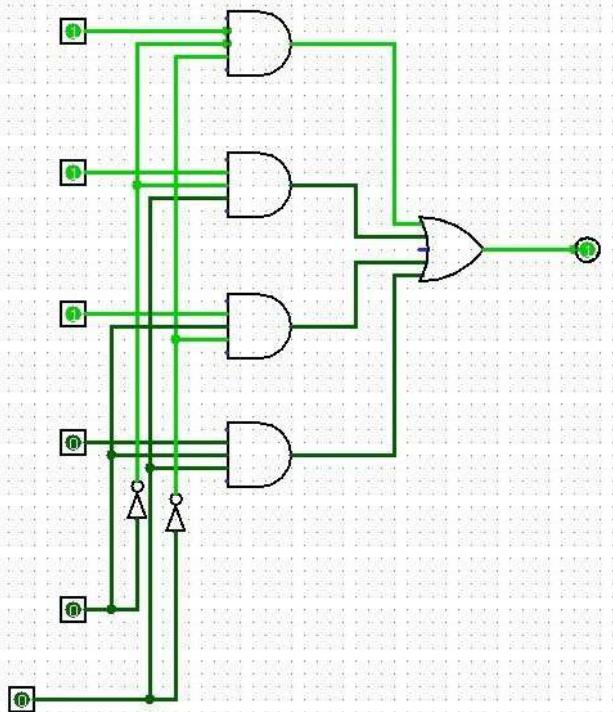
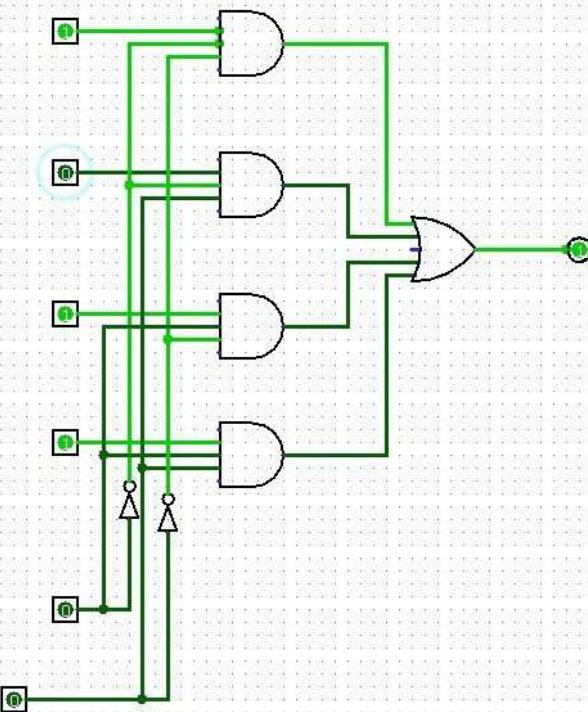
Output snapshot: (In output include practical details and execution date & time with your enrollment number)



#### 4:1 Multiplexer



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# 19. Practical 6

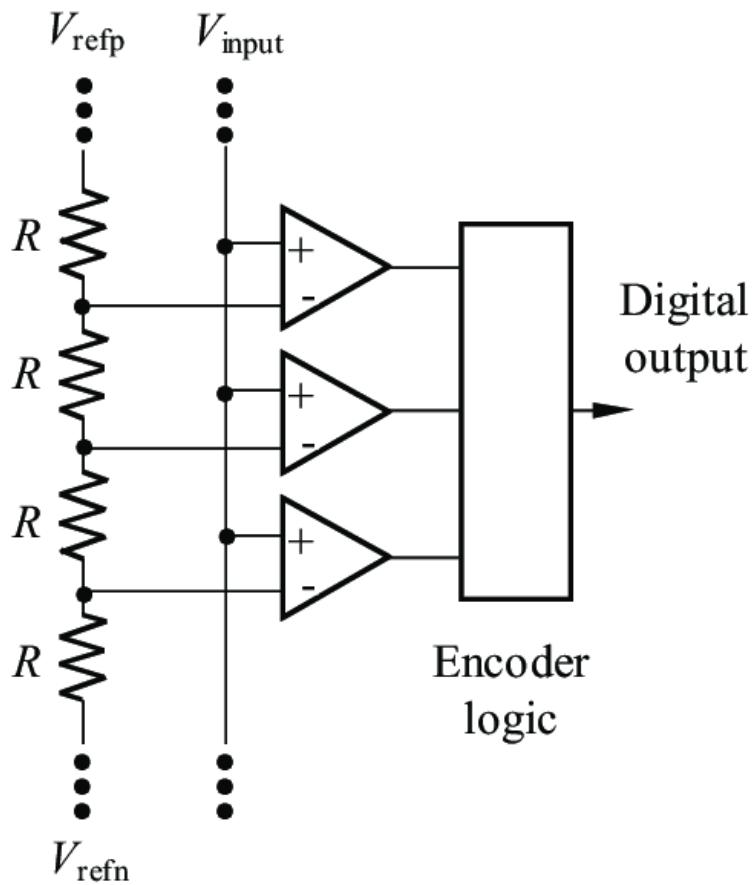
CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion

## Module 4

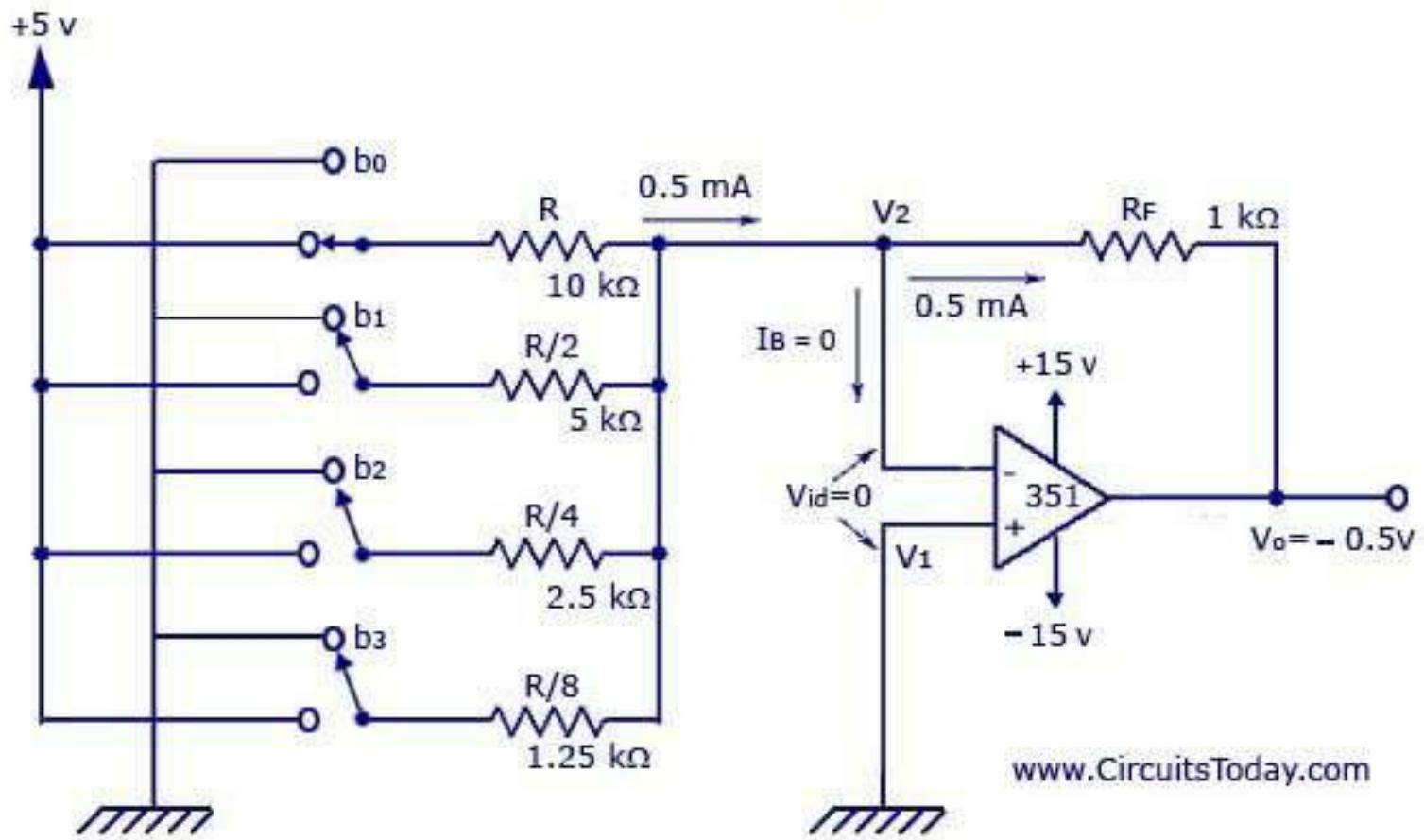
Aim: Study and configure A to D convertor and D to A convertor.

### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



## D/A Converter With Binary Weighted Resistors



# 20. Practical 7

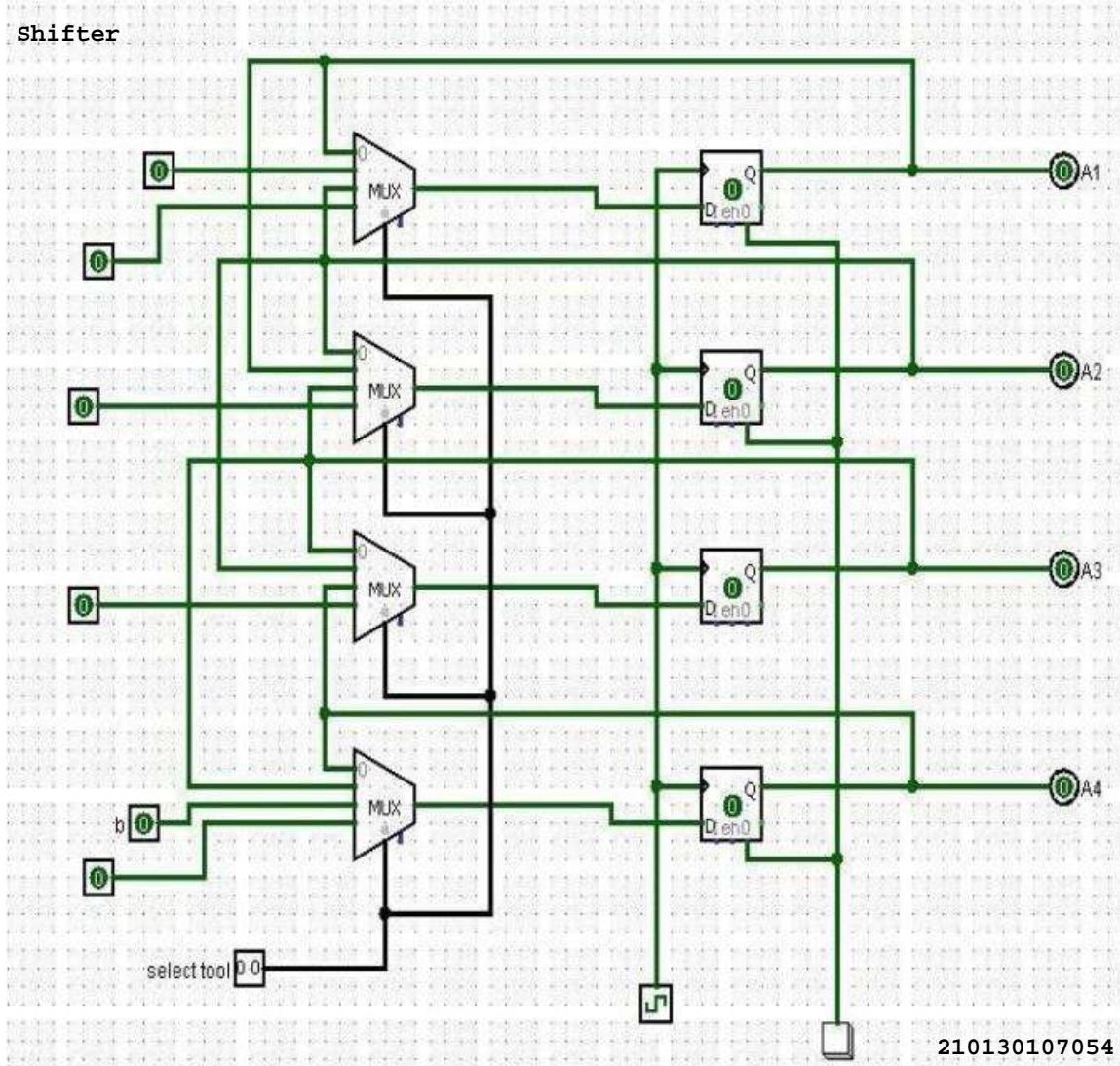
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

## Module 3

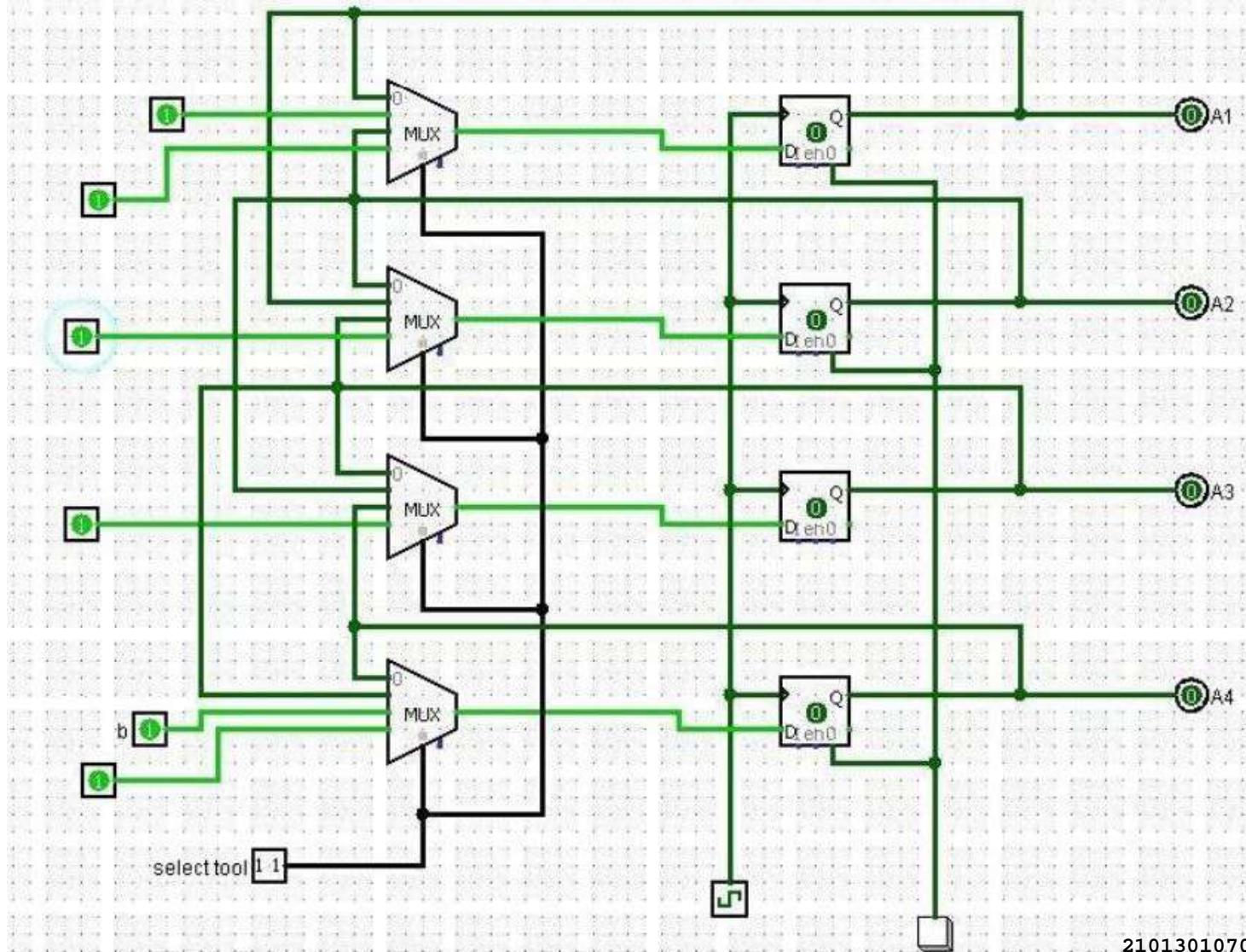
Aim: Study and implement a shifter.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



Shifter



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# 21. Practical 8

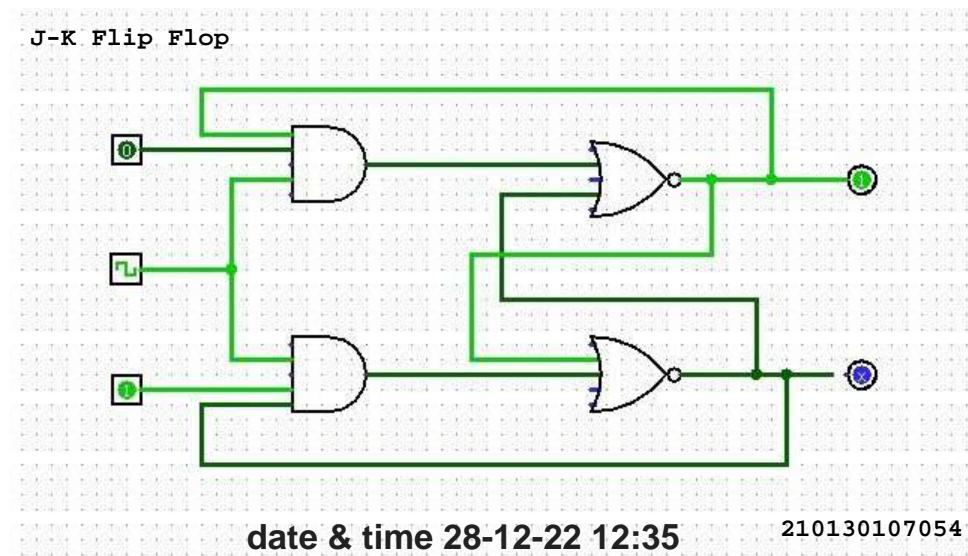
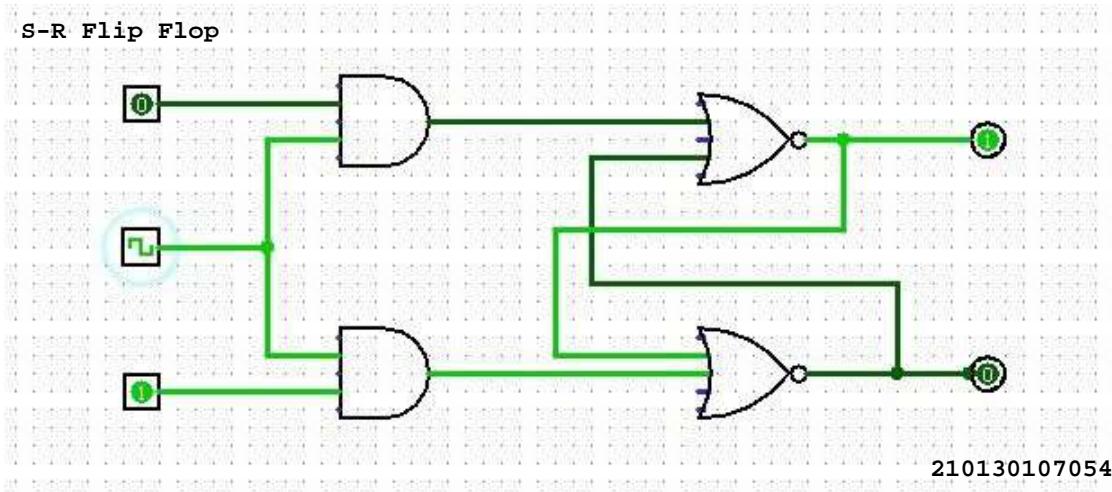
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

## Module 3

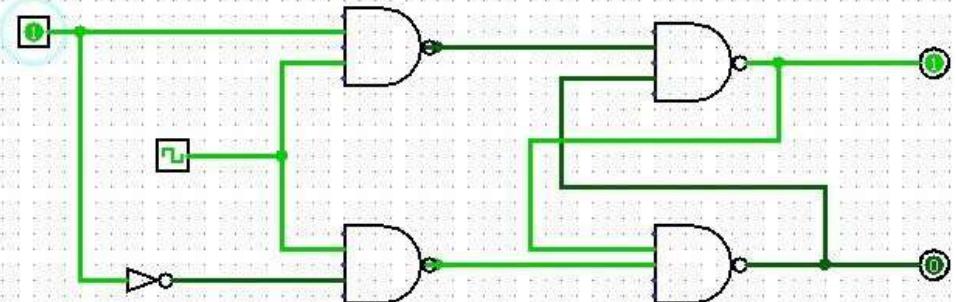
Aim: Study and implement Flip-flops.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

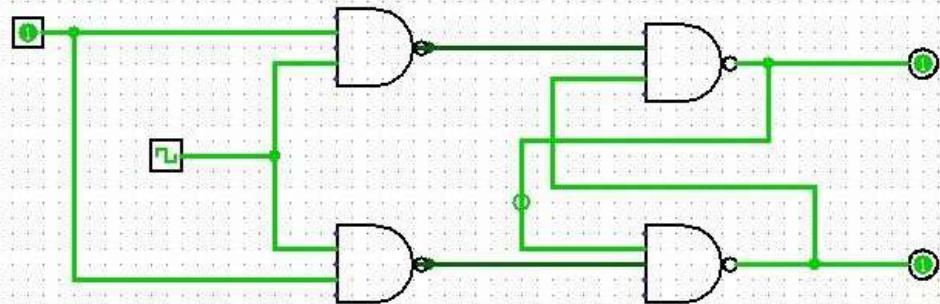


**D Flip Flop**



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**T Flip Flop**



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# 22. Practical 9

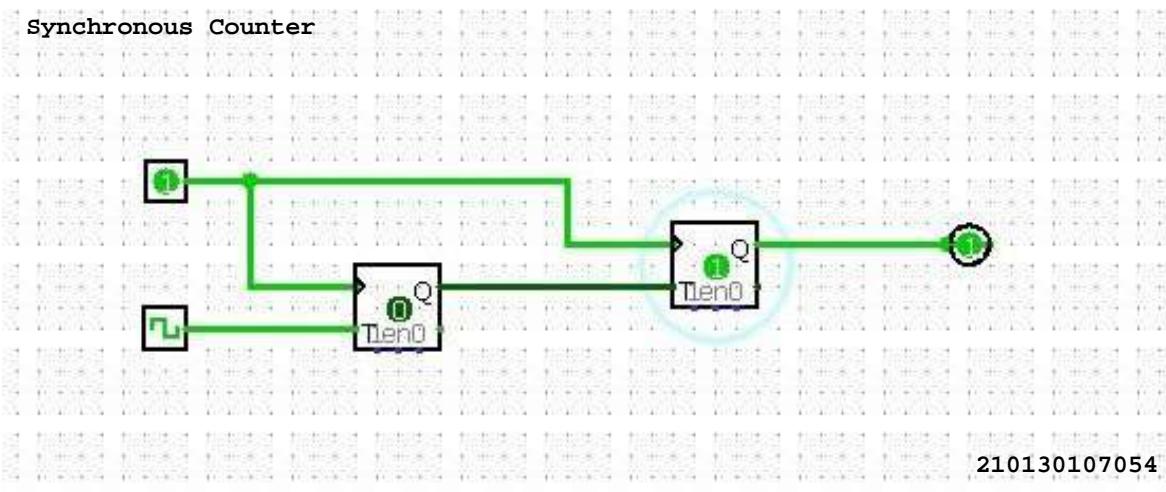
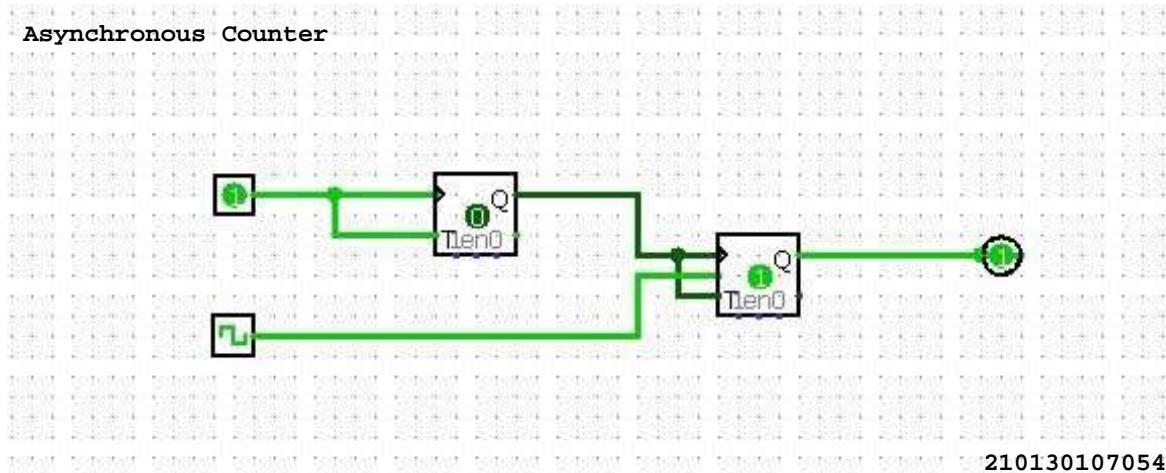
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

## Module 3

Aim: Study and implement Counter.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)



# 23. Practical 10

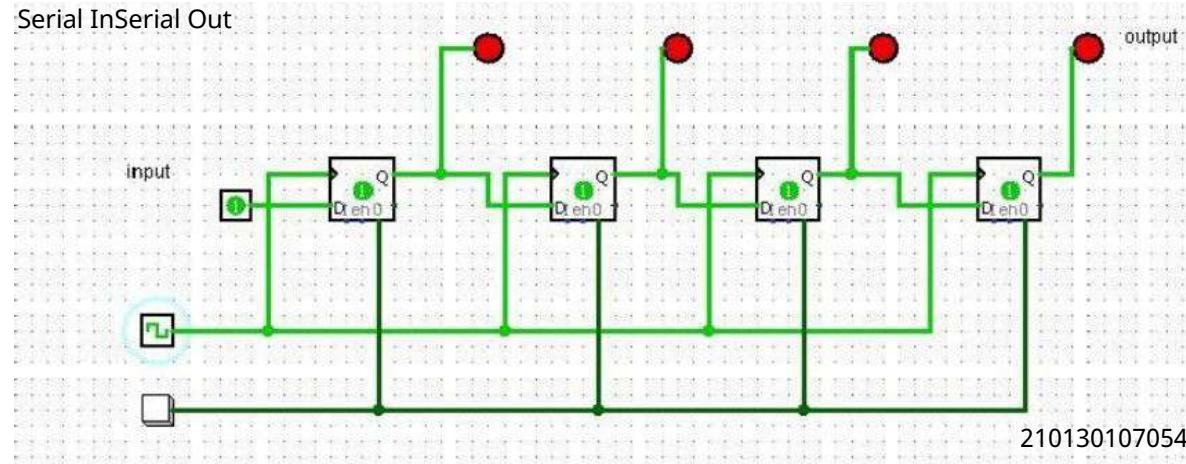
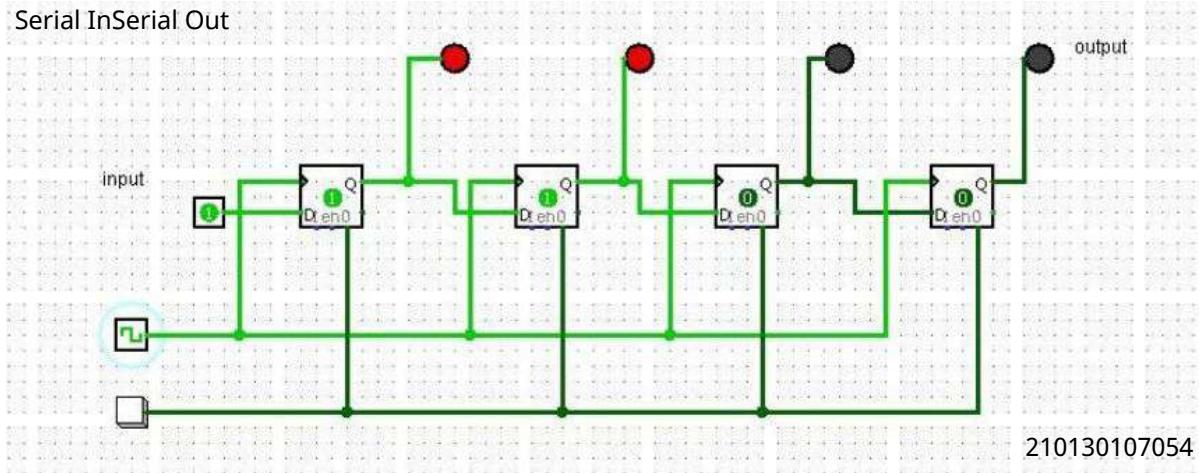
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

## Module 3

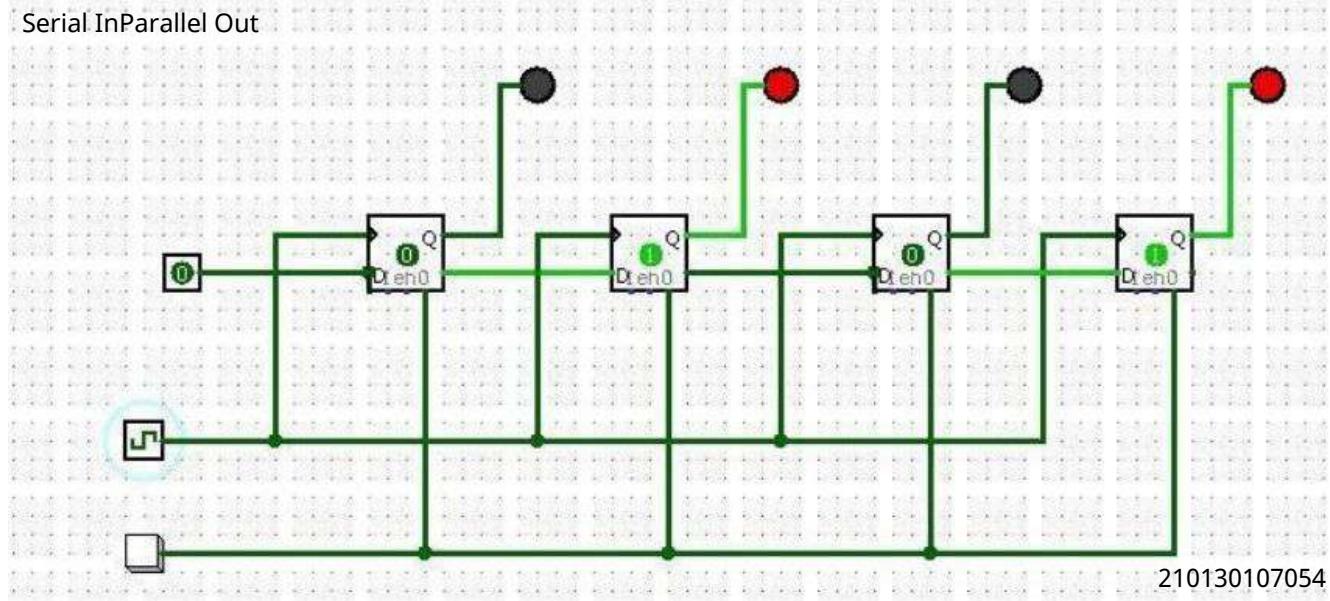
Aim: Study and implement a shift register.

Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

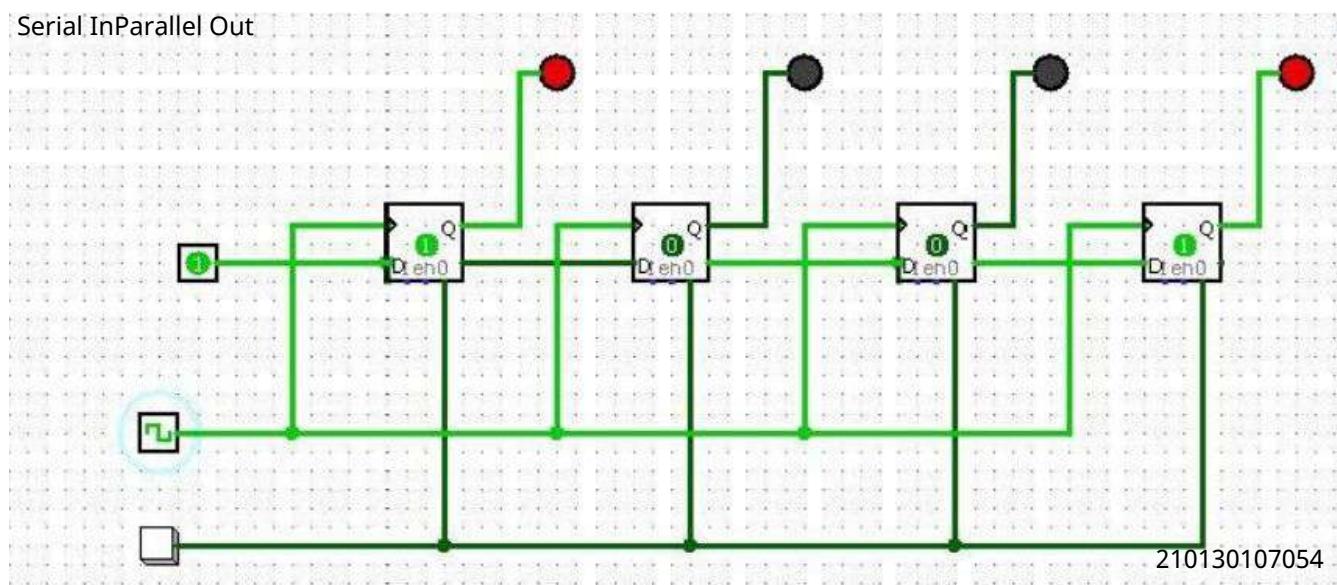


Serial InParallel Out



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Serial InParallel Out



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# 24. Practical 11

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working**

## Module 2

**Aim: Study and implement K-Map for the given function:(SOP)**

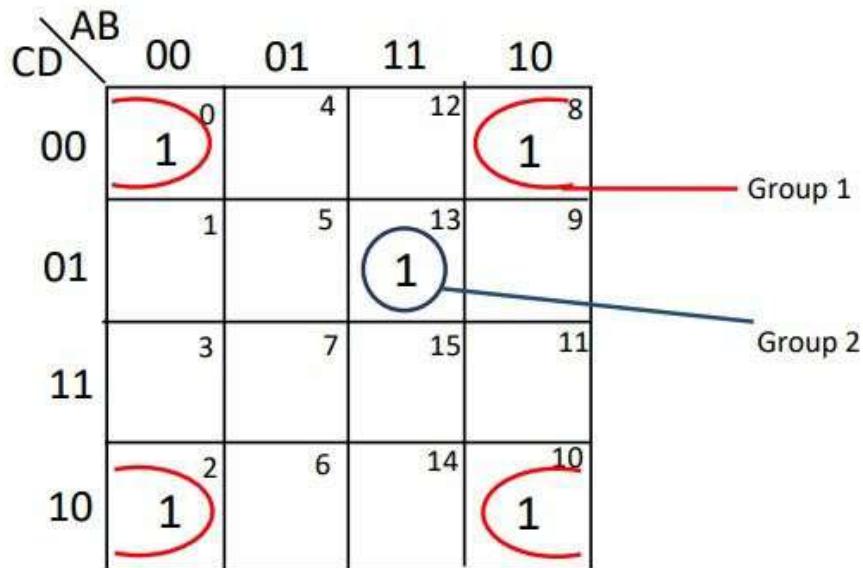
$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

$$F(A,B,C,D) = \sum(0,2,8,10,13)$$



First consider group 1,

Grou's Product term =  $B'D'$

Now, consider group 2,

Group's Product term =  $ABC'D$

To obtain final solution we add product term of Group 1 and Group 2,

Ans :  $F(A,B,C,D) = B'D + ABC'D$

## Assignment - I

P-1 State and explain De Morgan's theorems with truth tables.

$$\rightarrow \text{Law 1 : } \overline{A+B} = \bar{A} \cdot \bar{B}$$

- This law states that the complement of a sum of variables is equal to the product of their individual complements.

A	B	$A+B$	$(\bar{A}+\bar{B})$	$\bar{A}$	$\bar{B}$	$\bar{A} \cdot \bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

$\rightarrow$  Hence, Law 1 is proved from the above truth table.

$$\text{Law 2 : } \bar{A} \cdot \bar{B} = \bar{A} + \bar{B}$$

A	B	$A \cdot B$	$\bar{A} \cdot \bar{B}$	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Hence, Law 2 is proved from the above truth table.

P-2 Simplify Boolean function  $F = A'B'C + A'BC + AB'$

$$F = AC(B + B') + AB'$$

$$= AC + AB'$$

Ques-3 List & Explain logic family.

Characteristic	ECL	TTL	GA
1) Power input	Moderate - high	Moderate	L
2) Frequency limit	Very high	high	Mod
3) Circuit density	Moderate	Moderate - high	High
4) Circuit type Protamity	Moderate	high	high

Ques-4 Describe error detecting & correcting

→ Error detecting:

- Noise can alter or distort the data in transmission.
- The 1s may get changed to 0s and 0s to 1s.
- Because digital systems must be accurate to the digit, errors can pose a serious problem.
- Single bit error should be detect & correct by different schemes.
- Parity, check sum and block parity are examples of error detecting codes.

=) Parity:

- Parity bit is the simplest technique.
- two types of parity = odd and even

→ Ex : 0110 binary number has "1" as odd parity and "0" as even parity.

- Detect a single-bit error but can not detect two or more errors within the sum word.
- In any practical system, there is always a finite probability of the occurrence of single error.

⇒ Check sums :-

- Simple parity can not detect two errors within the sum words.
- Added to the sum of previously transmitted words.
- At the transmission, the check sum up to that time is sent to the receiver.
- The receiver can check its sum with the transmitted sum.
- This type of transmission is used in teleprocessing system.

⇒ Block parity :-

0 1 0 1 1 0 1 1	0	0 1 0 1 1 0 1 1	0	0 1 0 1 1 0 1 1	0
1 0 0 1 0 1 0 1	1	1 0 0 1 0 1 0 1	1	1 0 0 1 0 1 0 1	1
0 1 1 0 1 1 1 0	0	0 1 1 0 0 1 1 0	0	0 1 1 0 1 1 1 0	0
1 1 0 1 0 0 1 1	0	1 1 0 1 0 0 1 1	0	1 0 0 0 0 0 1	0
1 0 0 0 1 1 0 1	1	1 0 0 0 1 1 0 1	1	1 0 0 0 1 1 0 1	1
0 1 1 1 0 1 1 1	1	0 1 1 1 0 1 1 1	1	0 1 1 1 0 1 1 1	1
↓		0 1 1 1 0 1 1 0	0	0 1 1 1 0 1 1 0	0
↓		Parity column			

## → Error correcting code:

- The 7-bit 'hamming code' To transmit four data bits, three bits located at positions  $2^0, 2^1$  and  $2^2$  left are added to make a 7-bit code which is then transmitted.
- The word format could be as shown:  
 $P_1 \ P_2 \ D_3 \ D_4 \ D_5 \ D_6 \ D_7$   
 where the  $D$ -bits are the data bits,  
 $P$  bits are the parity bits.  
 $P_1$  is to be set a 0 or 1 so that it is even parity bits 1, 3, 5 and 7.  
 $P_2$  is to be set a 0 or 1 so that it is even parity bits 2, 3, 5 and 7  
 $P_4$  is to be set a 0 or 1 so that it is even parity 4, 5, 6 and 7

## Ques - 5 Differentiate TTL, schottky TTL, CMOS

Parameter	CMOS	TTL	Schottky TTL
Device used	n-channel & p-channel	Bipolar junction transistor	Schottky diode
$V_{IH}$ (min)	3.5 V	2 V	2 V
$V_{IL}$ (max)	1.5 V	0.8 V	0.81 V
$V_{OH}$ (max)	4.95 V	2.7 V	2.7 V

Vol (max)	0.005 V	0.4 V	0.5 V
power dissipation	0.1 mW	10mW	2 mW
pin gate			
fan-out	50	10	50
Application	portable instrument where battery Supply is used	laboratory instrument	voltage clamping application to prevent transition saturation

✓  
6/11/23

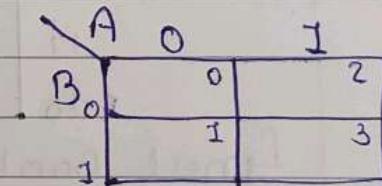
## Assignment - 2

Ques-1 Explain k-map.

- The Karnaugh map method is a systematic method of simplifying the Boolean expression
- The k-map is chart on arrangement of adjacent cells, each representing a particular combination of variables in sum
- The output values placed in each cell are derived from the minterms of a Boolean function.
- ⇒ Two-variable k-map:

- the two-variable expression can have  $2^2 = 4$  possible combinations of the input A and B
- Each of these combinations  $A'B'$ ,  $A'B$ ,  $AB'$  and  $AB$  is called minterm

A	B	minterm
0	0	$m_0 = A'B'$
0	1	$m_1 = A'B$
1	0	$m_2 = AB'$
1	1	$m_3 = AB$



⇒ Three-variable k-map:

- A function in three variable expressed in the standard SOP form can have eight possible combinations.

	AB	00	01	11	10	min term number
C	0	0	2	6	4	5
	0	1	3	7	5	9
	1					

Ques-2 Obtain the simplified expressions in SOP form for following Boolean functions:

(i)  $f(x, y, z) = \Sigma(2, 3, 6, 7)$

	xy	00	01	11	10
z	0	1	3	7	5
	0	1	4	8	6
	1	2			

Final Boolean expression:  $Az' + A'y'z$

(ii)  $F(A, B, C, D) = \Sigma(4, 6, 7, 15)$

	AB	CD	00	01	11	10
	00	1	5	13	9	
	01	2	7	14	10	
	11	4	8	16	12	
	10	3	7	15	11	

Final Boolean expression:  $BcD' + A'b'c'd$

Ques-3 Describe adder & Subtractor

i) Half adder:

- A combinational circuit which adds two bits binary numbers is called a half adder.

- The sum column resembles like an output XOR gate and carry column like AND

A	B	sum	carry			
0	0	0	0	A:		$S = A \oplus B$
0	1	1	0	B:		$C = A \cdot B$
1	0	1	0			
1	1	0	1			

### ii) Full adder:

The full adder adds the bits A and B and the carry from the previous column called carry-in and outputs the sum bits and carry-out count.

B	cin	s	cout			
0	0	0	0	A:		$S$
0	1	1	0	B:		
1	0	1	0			
1	1	0	1			$cout$
0	0	1	0			
0	1	0	1			
1	0	0	1			
1	1	1	1			

### (iii) Half subtractor:

A	B	d	b			
0	0	0	0	A:		$d = A \oplus B$
0	1	1	1	B:		
1	0	1	0			
1	1	0	0			$b = A \cdot B$

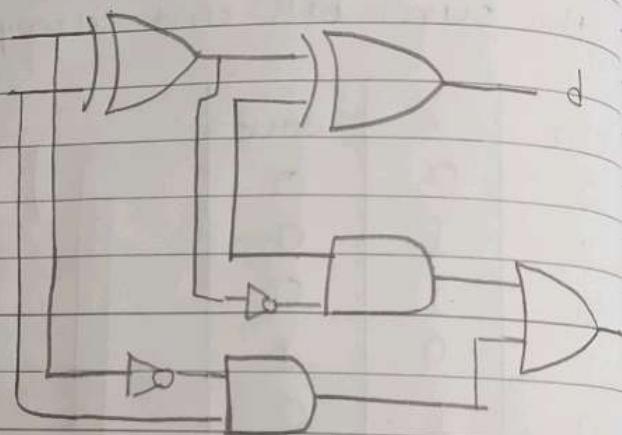
- subtracts one bit from the other and the difference.
- other output is to specify if I is less than or equal to J.

$A \rightarrow m$  to 1  
and  $n$  to 1

#### (iv) full subtractor:

- full subtractor is a combinational circuit.
- input ( $A, B, b_i$ )
- subtraction =  $A - B - b_i$

A	B	$b_i$	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



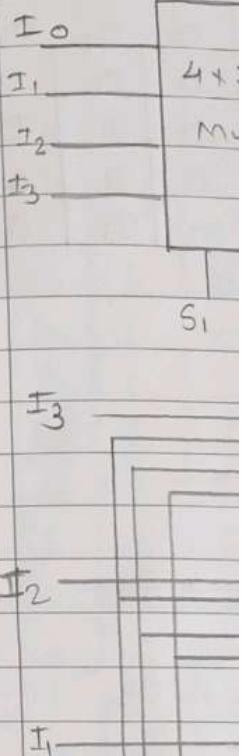
Ques - 4 Explain Multiplexer & demultiplexer.

$\rightarrow$  i) Multiplexer:

- A multiplexer is a device that allows digital information from several sources to be routed onto a single transmission line over that line to a common destination.

- Consider an integer 'm', which is contained in the following relation:

$$M = 2^n \text{ where } n \text{ is the number of bits.}$$



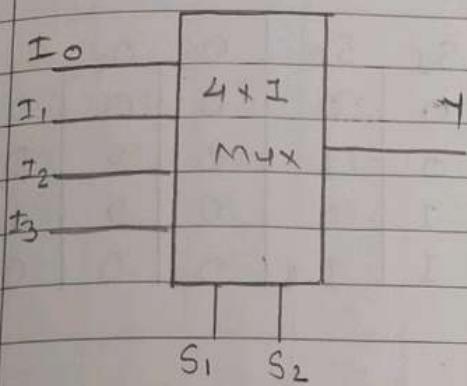
$I_0$

$S_1 S_0$

ii) Demultiplexer

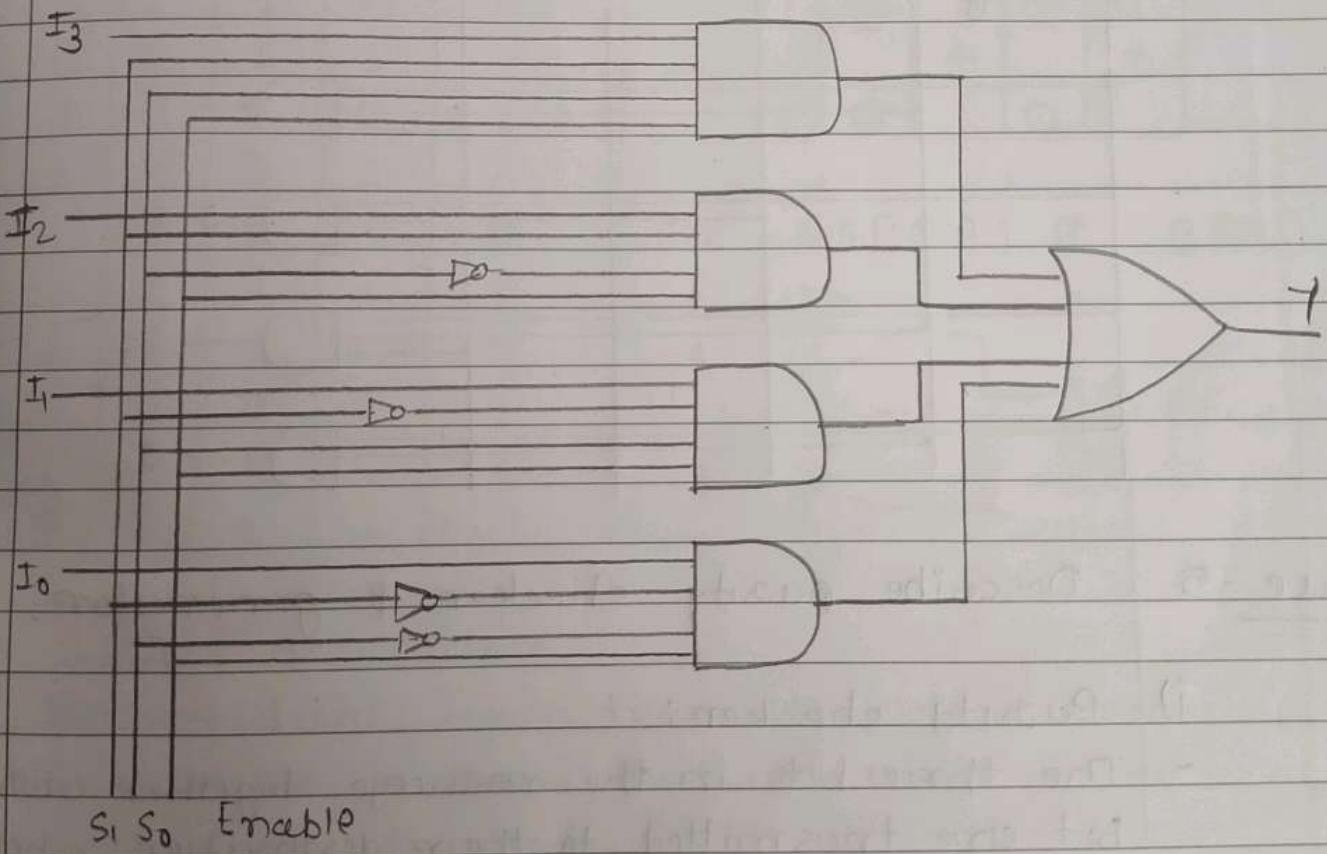
- A demultiplexer takes information from a single source and distributes it to multiple destinations.

→ A  $m$  to  $1$  multiplexer has  $m$  inputs, one output and  $n$  control inputs.



$S_1$	$S_2$	$T$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

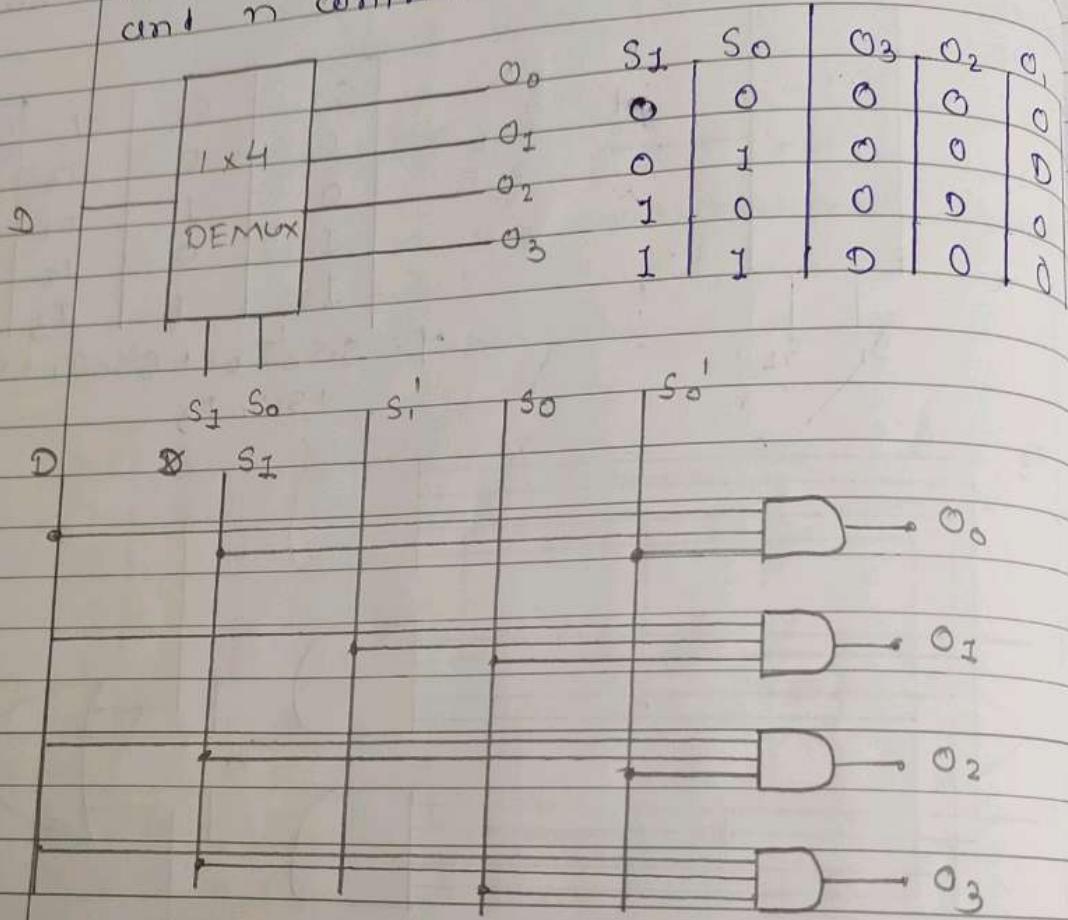
$$T = S_1 S_0' I_0 + S_1' S_0 I_1 + S_1 S_0 I_2 + S_1' S_0' I_3$$



## ii) Demultiplexer:

- A demultiplexer is a device that allows digital information from one source to be routed onto a multiple lines for transmission over different destinations.

- A  $j$ -to- $m$  demultiplexer has one input and  $n$  control inputs.



Ques - 5 Describe parity checker & generator.

### i) Parity checker:

- The three bits in the message together with bit one transmitted to their destination, where applied to the parity checker circuit.
- The parity checker circuit checks for possible errors in the transmission.
- Since the information was transmitted with the four bits received must have an even number of 1's.

four bit

P.E.C

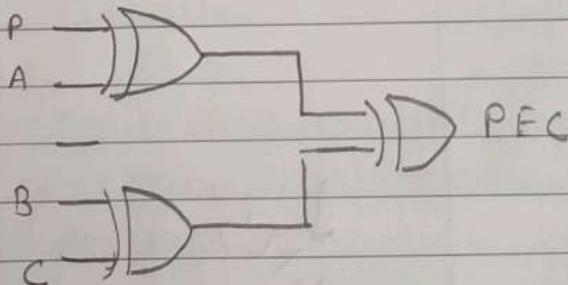
P	A	B	C	P.E.C
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

$$\begin{aligned} \text{P.E.C.} = & \bar{P}\bar{A}C\bar{B}C + B\bar{C} + \bar{P}A(C\bar{B}\bar{C} + BC) \\ & + \bar{A}PA C\bar{B}C + \bar{B}\bar{C} + P\bar{A}C\bar{B}\bar{C} \\ & + BC \end{aligned}$$

k-map:

			BC	
			PA	
	00	01	11	10
00	0	1	1	1
01	1	0	1	1
11	1	1	0	1
10	1	0	0	0

$$\text{P.E.C.} = (AP \oplus A) \oplus (B \oplus C)$$



(iii) Parity generator:

- Binary data, when transmitted and processed is susceptible to noise that can alter its 1s to 0s and 0s to 1s.
- to detect such errors, an additional bit called parity bit is added to the data bits and the word containing the data bits and the parity bits is transmitted.
- At the receiving end the no of 1s in the word received are counted and the error detected.

even parity

0	0	1	1
---	---	---	---

odd parity

0	0	1	0
---	---	---	---

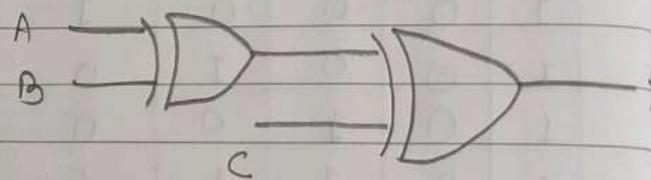
detect parity bit

input			output
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

C	AB	00	01	11	10
		0	1	1	1

$$f = A'B'C + A'B'C' + ABC + AB'C'$$

$$f = A \oplus B \oplus C$$



6/1/23

## Assignment - 3

P-1 Differentiate sequential & combinational circuit.

### Combinational circuit

- The output variables at any instant of time are dependent only on the present input variables.

- Memory unit is not required in this circuit.

- Combinational circuits are faster.

- Combinational circuits are easy to design.

### Sequential circuit

- In sequential circuits, the output is dependent not only on the present state.

- Memory unit is required in sequential circuit.

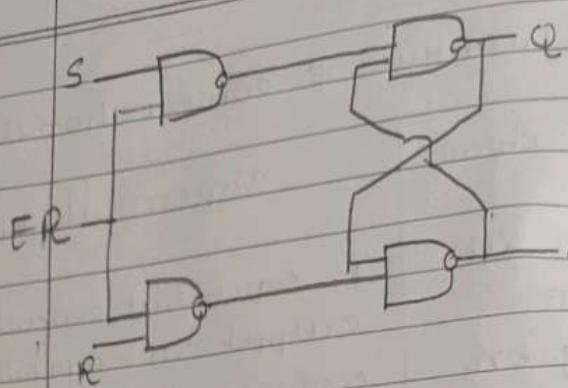
- Sequential circuits are slower than combinational circuits.

- Sequential circuits are computationally harder to design.

P-2 List & explain flip flop.

i) S-R flip flop:

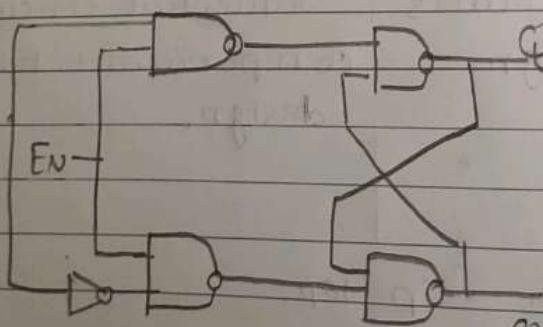
- A gated S-R latch requires an EN input
- This type of ff responds to the changes in inputs only as long as the clock is High, these type of ff are also called level triggered.



En	S	R	Q <sub>n</sub>	Q <sub>n+1</sub>
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	X
0	X	X	0	0
0	X	X	1	1

### ii) D - Flip Flop:-

- It differs from the S-R latch in that it has one input in addition to EN
- We can say that the output Q follows the D when EN is high.



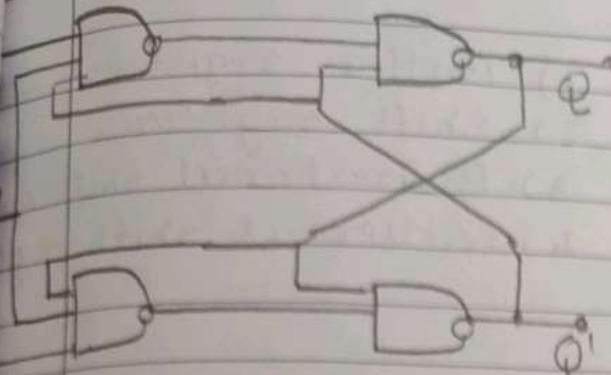
En	D	Q <sub>n</sub>	Q <sub>n+1</sub>
1	0	0	0
1	0	0	1
0	1	0	1
1	1	1	1
0	X	0	X
0	X	1	1

### iii) J-k flip flop:-

- The J-k flip flop is very versatile and also widely used
- The functioning is identical to that of the S-R ff, except that it has no invalid states like

En  
1  
1  
1  
0  
0

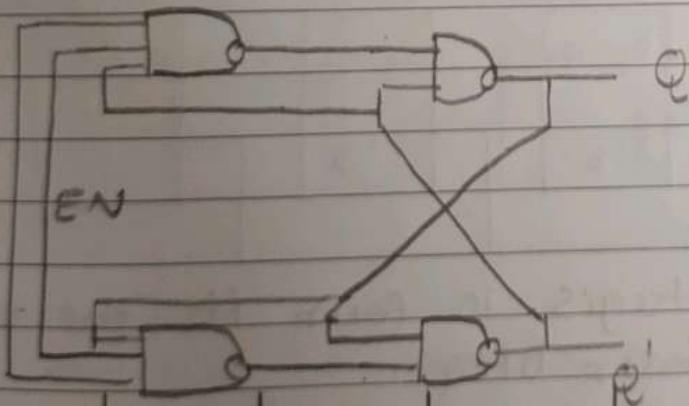
iv)  $\bar{F}$



En	J	K	$Q_n$	$Q_{n+1}$	State
1	0	0	0	0	No change
1	0	0	1	1	Reset
1	0	1	0	0	Set
1	0	1	1	0	Toggle
1	1	0	0	1	No change
1	1	0	1	1	?
1	1	1	0	1	Toggle
0	x	x	0	0	No change
0	x	x	1	1	?

iv) T - flip flop :

- A T flip-flop has a single control input, tabled T for toggle
- Although T - ff are not widely available commercially it is easy to convert a J-k ff to the functional equivalent of a T ff.



En	T	$Q_n$	$Q_{n+1}$	State
1	0	0	0	No change
1	0	1	1	?
1	1	0	1	Toggle
1	1	1	0	?
0	x	0	0	No change
0	x	1	1	?

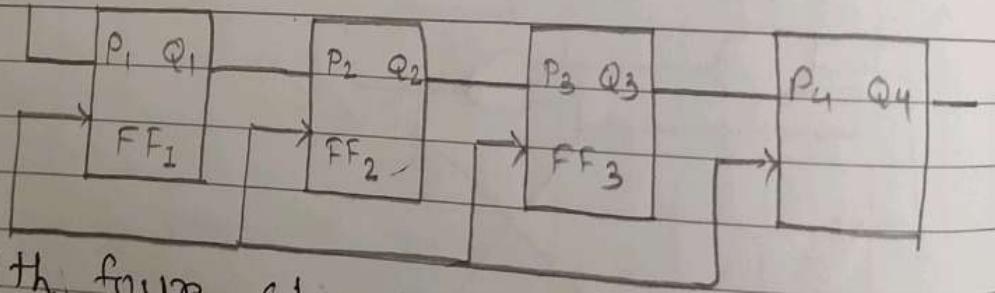
Ques-3 List & Explain registers.

- Types of registers:
- 1) Buffer registers
  - 2) Shift registers
  - 3) Bidirectional shift
  - 4) Universal shift

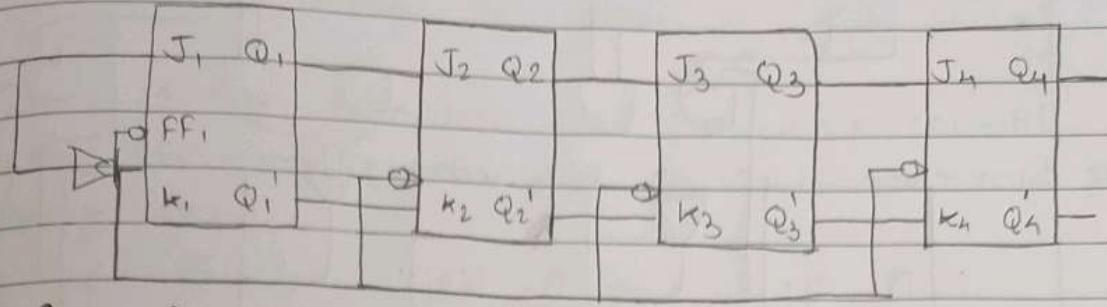
i) Shift register:

- A number of FFs connected together such that data may be shifted into and shifted out is called a shift register.
- four basic types of shift register:
  1. serial-in, serial-out
  2. serial-in, parallel-out
  3. parallel-in, serial-out
  4. parallel-in, parallel-out

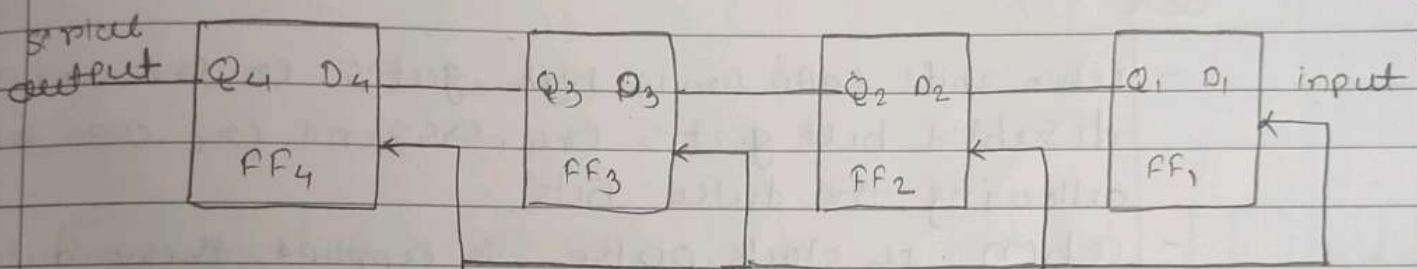
→ Serial-in, serial-out:



- with four stages ie four FFs, the register stores up to four bits.
- Serial data is applied at the D input of first FF. The Q output of the first FF is connected to the D input of the second FF.
- When serial data is transferred into a each new bit is clocked into the first FF the positive edge of each clock pulse

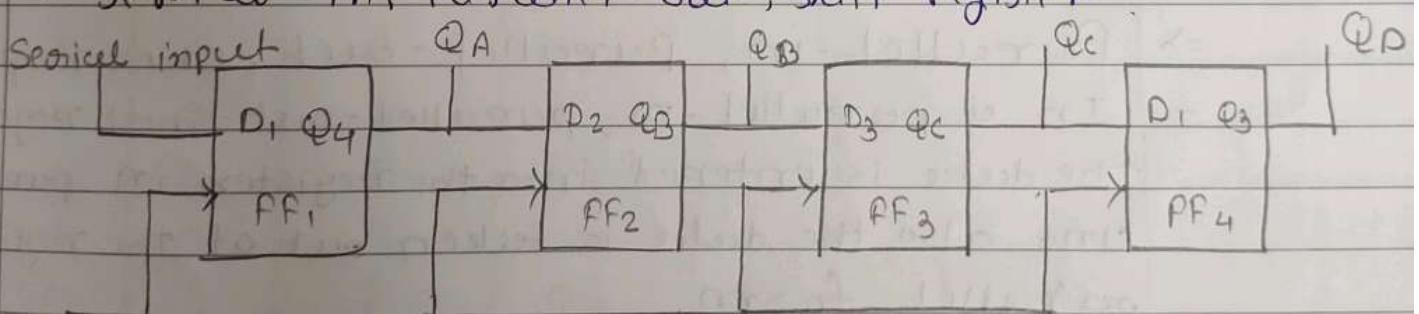


- A shift register can also be constructed using J-K FFs as shown in above figure.
- The data is applied at the j input of the first FF, the complement of this is fed to the k input of FF.



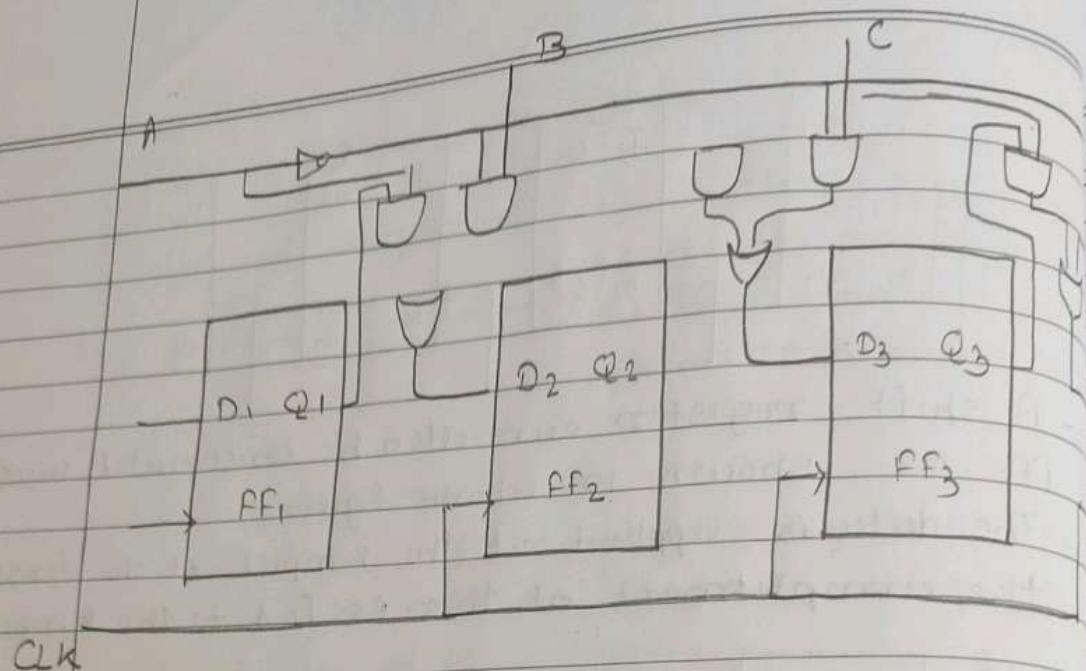
4-bit serial in, serial-out shift register

→ serial - in, parallel - out, shift register



CLK

- in this type of register, the data bits are entered into the register serially but the data stored in the register is shifted out in parallel form.
- The serial in, parallel - out, shift register can be used as a serial - in, serial - out, shift register if the output is taken from Q terminal of the last FF.

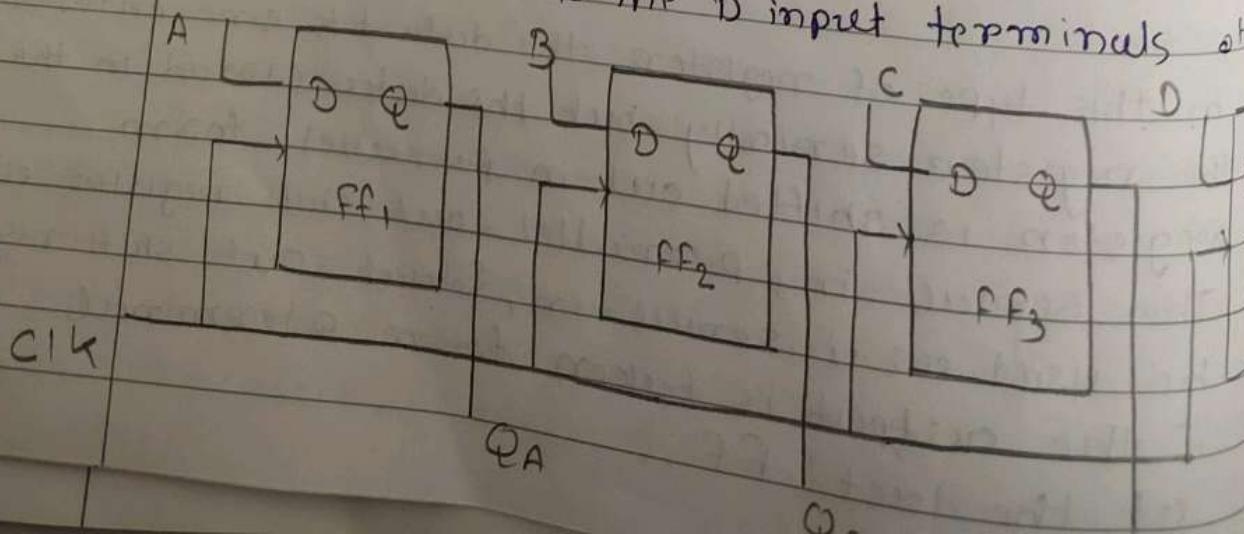


CLK

- when shift LOAD line is high, gates G<sub>1</sub>, G<sub>2</sub>, and G<sub>3</sub> are disabled but gate G<sub>4</sub>, G<sub>5</sub>, and G<sub>6</sub> are enabled, allowing the data bits.
- when a clock pulse is applied, these data bits are shifted to the Q output terminals Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> and therefore, data is inputted in one step.

CLK

- ⇒ Parallel-in, parallel-out, shift register
- In a parallel-in, parallel-out shift register the data is entered into the registers in parallel and also the data is taken out of the registers in parallel form.
- Data is applied to the D input terminals of

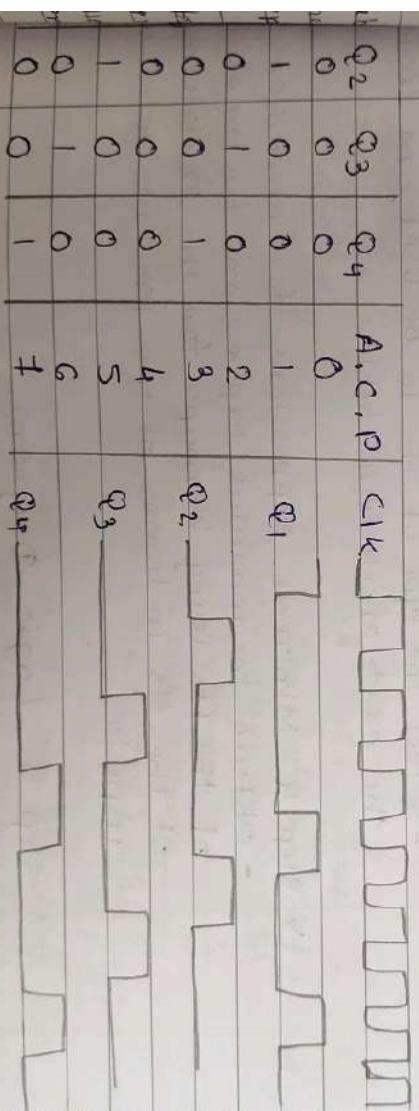
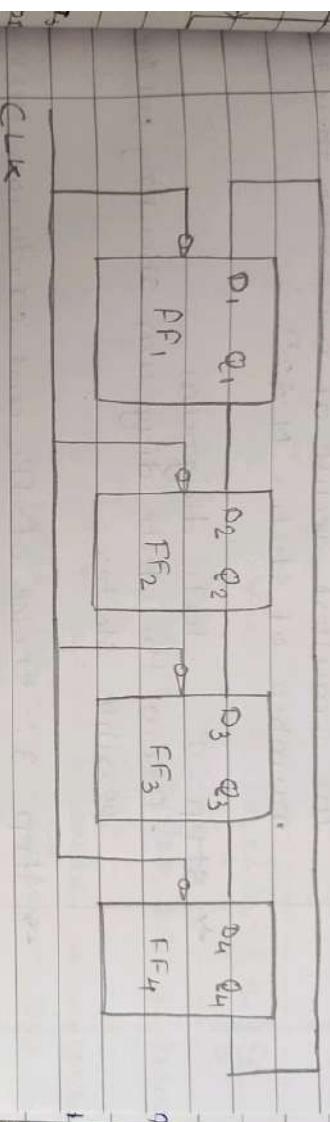


CLK

↳ This is  
↳ The  
↳ regi

Q4 Describe ring counter.

- > This is the simplest shift register counter.
- > The bits were arranged as in a normal shift register



- in most instances, only single 1 is in the register and is made to circulate around the register as long as clock pulses are applied initially.
- So the initial state is 0000. After each clock pulse the contents of the register are shifted to Q<sub>1</sub>.
- The sequence repeats after four clock pulses.

Ques-5 Describe how to design counters using

→ Step-1: Number of FFs:-

- Based on the description of the problem determine the required number  $n$  of FFs. The smallest value of  $n$  is such that number of states  $N \leq 2^n$

→ Step-2: State diagram

- Draw the state diagram showing all possible states.

→ Step-3:- choice of FFs and excitation table

- Select the type of FFs to be used and draw the excitation table.

→ Step 4: Minimal expressions for excitation

- Obtain the minimal expressions for the inputs of the FFs using K-maps for the excitation of the FFs in terms of the present states inputs.

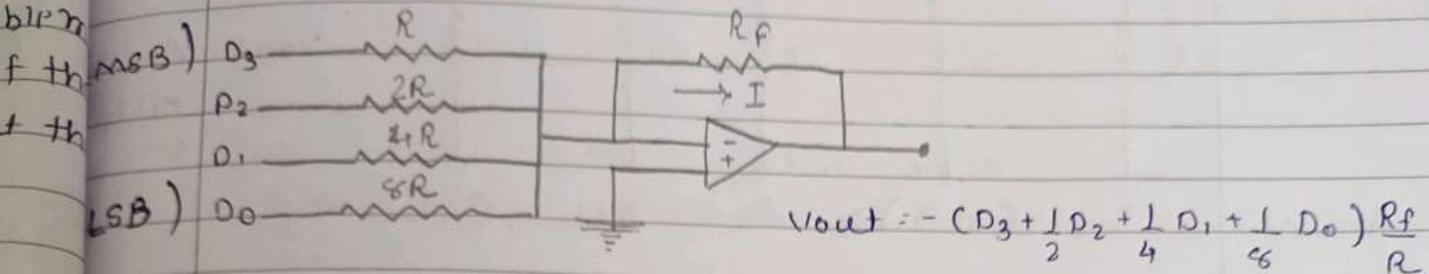
→ Step 5: Logic Diagram:

- Draw the logic diagram based on the minimal expression.

$f_1/2$   
 $f_1/1$   
6

## Assignment - 4

Q-1 Explain weighted resistor DAC converter.



- The diagram of the weighted-resistor DAC is shown in figure.
- The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit positions of input.
- The MSB  $D_3$  is amplified by  $R_f/R$ ,  $D_2$  is amplified by  $R_f/2R$ ,  $D_1$  is amplified by  $R_f/4R$ ,  $D_0$  is amplified by  $R_f/8R$ .
- Since the op-amp adds and inverts

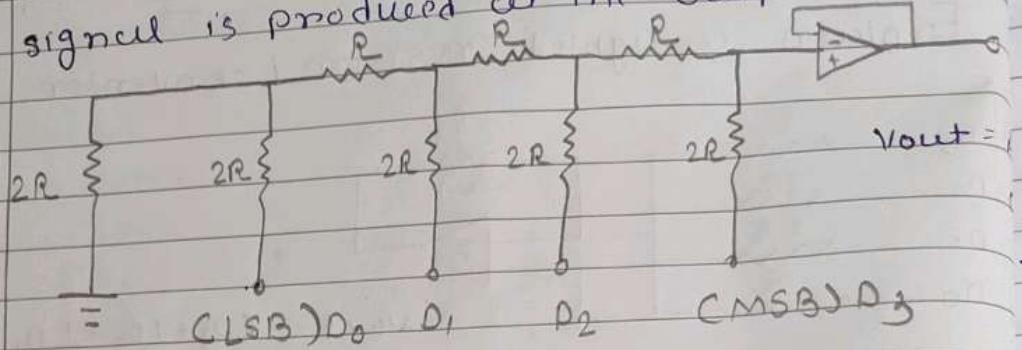
$$V_{out} = -\left(D_3/2 + D_2/4 + D_1/8 + D_0\right) \times \left(\frac{R_f}{R}\right)$$

- The main disadvantage of this type of DAC is, that a different valued precision resistor must be used for each bit position of the digital input.

Q-2 Explain R-2R ladder DAC converter.

- It uses a ladder network containing series-parallel combinations of two resistors of values  $R$  and  $2R$ .
- When a digital signal  $D_3 D_2 D_1 D_0$  is applied at the input terminals of the DAC, an equivalent closed

signal is produced at the output terminal



→ Case 1

- Below

$V_{out}$

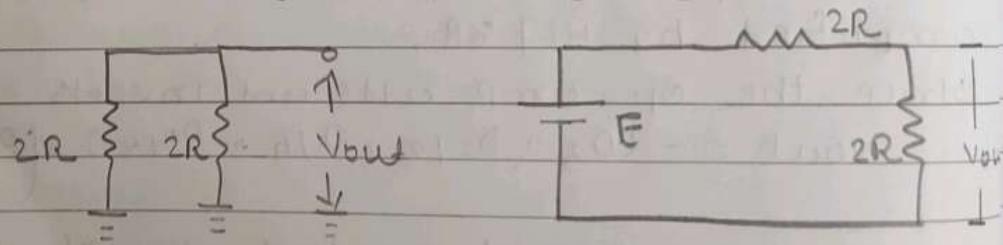
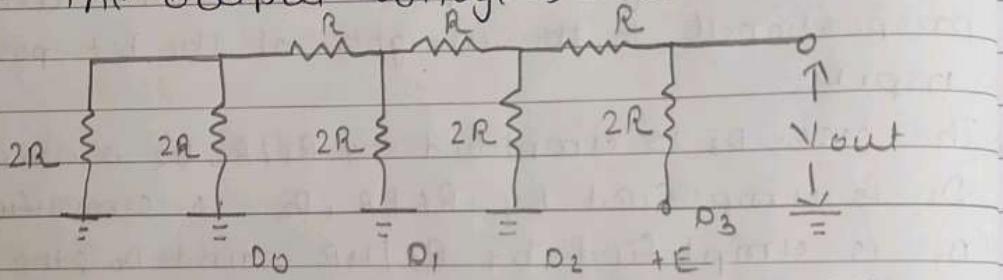
- Her

the

→ Case 1: when the input is 1000

- below figure illustrates the procedure + calculate  $V_{out}$  when the input is 1000

- The output voltage,  $V_{out} = E/2$



→ Case 2

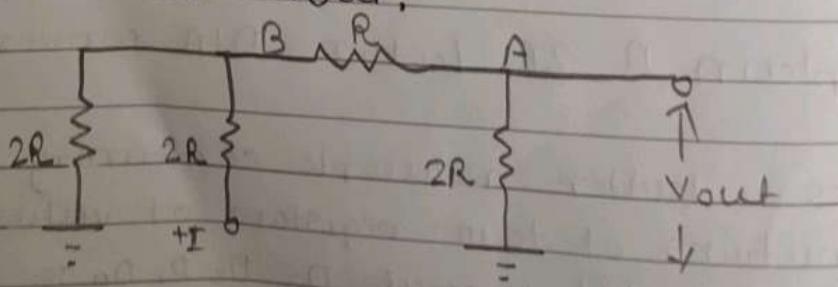
- below

$V_{out}$

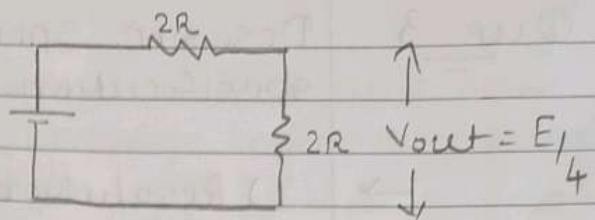
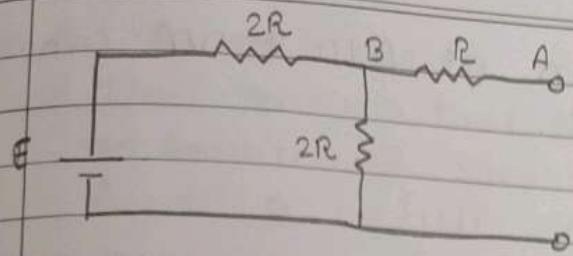
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→ Case 2: when the input is 0100

- Below figure illustrates the procedure calculate  $V_{out}$ .

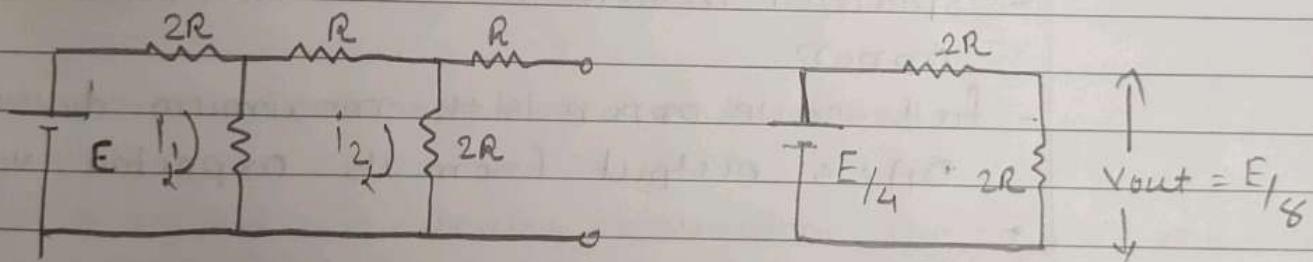
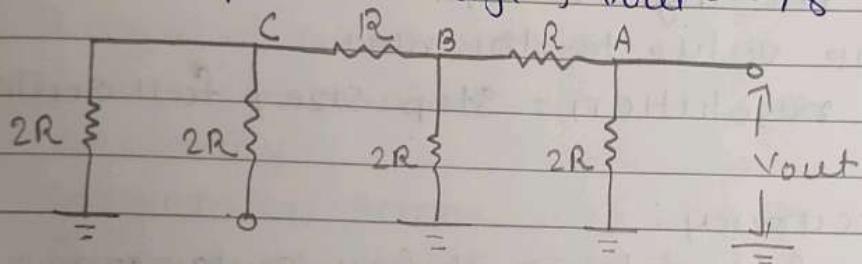


E<sub>18</sub>



→ Case 3: when the input is  $E_{10}$

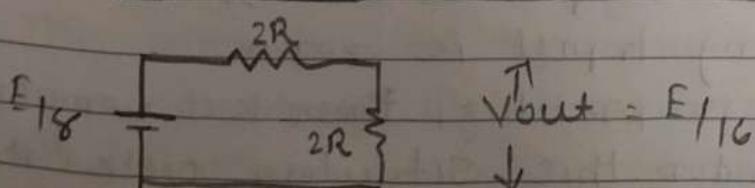
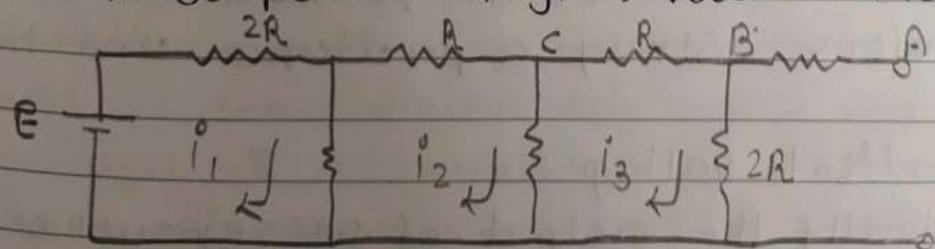
- Below figure illustrates the procedure to calculate  $V_{out}$ .
- Here, we find that to left of terminal C,  $r_{eq} = 2R$ , the output voltage,  $V_{out} = E/8$



→ Case 4: when the input is  $E_{001}$

- below figure illustrates the procedure to calculate  $V_{out}$

- The output voltage,  $V_{out} = E/16$



Ques - 3

Describe Specification of A/D & D/A converter  
specification of DAC.

→ 1) Resolution:

- smallest change that can occur in an analog output as a result of a change in the digital input → 6)
- Equals to the weight of the LSB and also known as the step size.
- Step size is the amount by which  $V_{out}$  will change as the digital input value is changed from one value to the next.

$$\text{resolution} = \text{Step size} / \text{full scale} \times 10^3$$

→ 2) Accuracy:

- specified in terms of full-scale error and error.
- full-scale error is the maximum deviation of DAC's output from its expected value.

→ 3) Setting time:

- The time required for the analog output to settle within  $\pm 1/2$  LSB of the final value after a change in the digital input.
- It is because of the presence of switches, devices, stray capacitance and inductance.

→ 4) Offset voltage:

- Ideally the output of DAC should be zero when the binary input is zero.
- However, in practice, there is a very small voltage under this situation called the offset voltage.

→ 5) monotonicity:

- This means that the staircase output will have no downward steps as the binary input is increment from 0 to full-scale value.

→ 6) Temperature sensitivity:

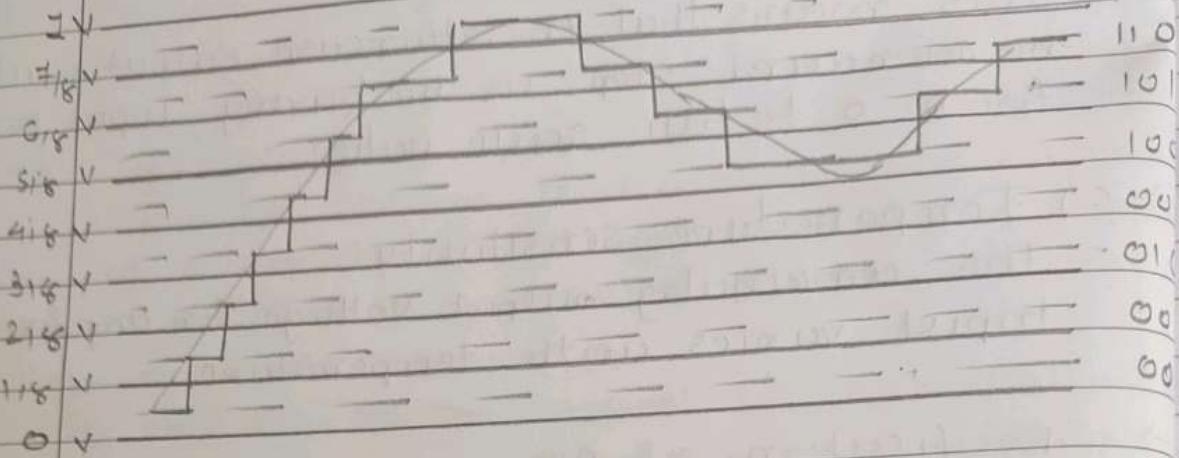
- The analog output voltage for any fixed digital input varies with temperature.

→ Specification of ADC.

- Range of input voltage
- Input impedance
- Accuracy
- Conversion time
- Format of digital output.

Q-4 Explain quantization and encoding.

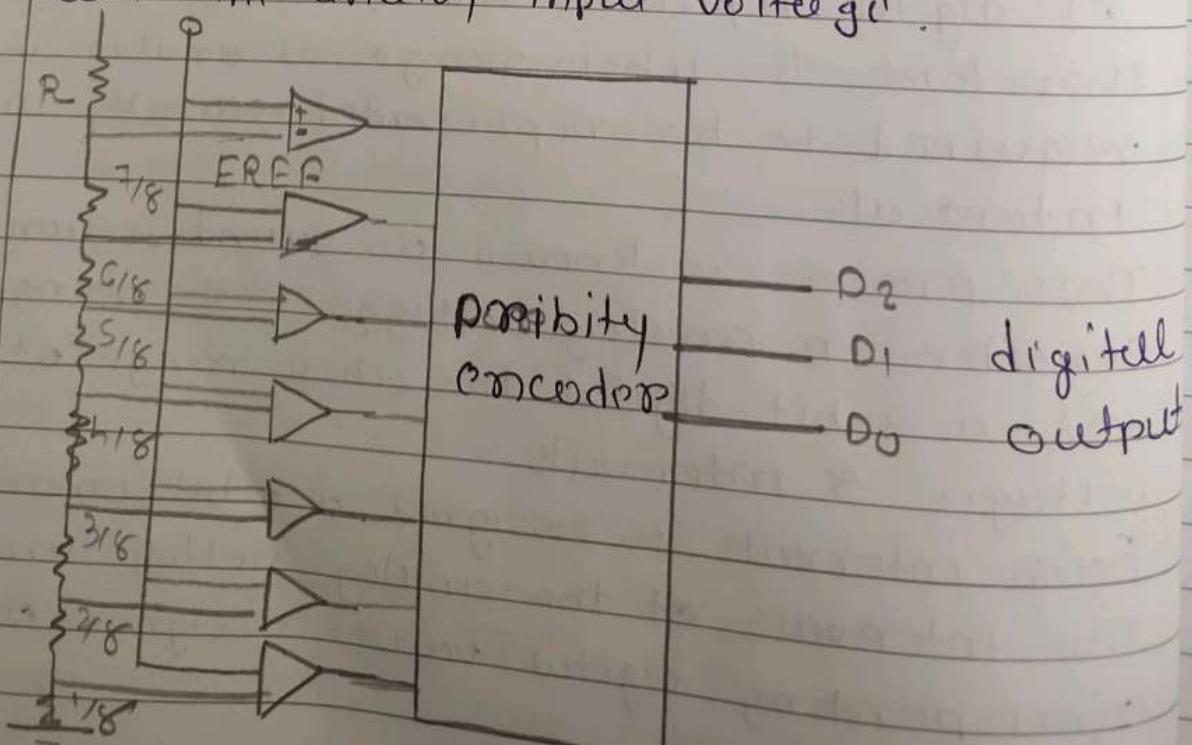
- In a digital-to-analog conversion, the possible numbers of digital inputs is fixed.
- Therefore, the whole range of analog voltage is required to be represented suitably in  $2^n$  intervals.
- This process is known as quantization.
- Consider an analog voltage in the range of 0 to V and a 3-bit digital the whole range of analog voltage 8 intervals.
- Each intervals is assigned a 3-bit binary value.
- The intervals of the analog voltage and their corresponding digital values assigned are shown in figure.



- Therefore, there is an error referred to as quantization error, involved in this process of quantization →

Ques-5 Explain parallel comparator A/D converter

- The flash type A/D converter is the fastest type of converter.
- This type of converter utilizes the parallel bit comparators that compare reference voltage with the analog input voltage.



- All comparators outputs are connected to appropriate encoder, which produces a digital output corresponding to the input having producer in this case is the one that represents the largest input.
- Thus, the digital output represents the voltage that is closest in value to the analog input.

$$\left( \frac{FR}{FR + R} \right) \times E_{REF} = \frac{1}{8} E_{REF}$$

- Similarly, the voltage applied to the inverting terminal of the second comparator is

$$\left( \frac{GR}{GR + R} \right) \times E_{REF} = \frac{6}{8} E_{REF}$$

- The flash converter uses no clock signal, bcz there is no timing or sequencing period.

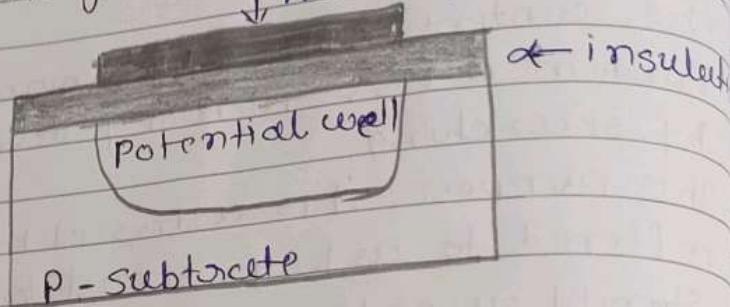
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## Assignment - 5

Q-1 Explain content addressable memory.

- The content addressable memory is a special purpose random access memory device that can be accessed by searching.
- In this purpose, it is addressed by associating the input data referred to as key, simultaneously with all the stored words.
- This operation is referred to as association and this type of memory is also known as associative memory.
- The key to be used may either consist of the entire data word.
- A CAM has the ability to search out data on the basis of its contents and therefore can be a powerful asset in many applications.
- If one is interested in finding out engineers, then CAM is able to check every memory location simultaneously by using the word form.
- On the other hand, the key will consist of the combination of the codes corresponding to engineer and Indian national.
- All the memory locations with engineers of Indian nationality will be identified and the remaining data can then be retrieved by using the read operation.
- To do the same search process with a conventional memory, each memory word is to be read out and compared with the key.

Ques-2 Explain charge coupled device memory  
↓ metal gate



- > The CCD memory is type of dynamic memory which packets of charges are continuously transferred from one mos device to another.
- > The structure of mos device is quite simple.
- > When a high voltage is applied to the metal gate holes are repelled from a region.
- > Data in the form of charge is transferred from one device to an adjacent one by clocking gates.
- > The CCD memory is inherently serial.
- > By controlling the timing of the clocks applied.
- > The principle advantage of this CCD memory is that, its single cell structure makes it to construct large capacity memory at low cost.

Ques-3 Explain classification of memory.

- > The table shows the classification of semiconductor memory devices. The semiconductor devices are categorized in several ways according to functional and architectural aspects.

## Classification

Non-Volatile memory

ROM

- Mask -  
Rom

- programmable  
Rom

Read/Write me. Random access non-Random access

- EEPROM
- EEROM
- FLASH

Volatile memory

RWEM

- SRAM
- DRAM
- FIFO
- LIFO
- Shift register

## p-4 Describe Semiconductors

- > A semiconductor is a substance whose resistivity lies between the conductor and insulators.
- > The property of resistivity is not the only one that decides a material as a semiconductor, but it has few properties as follows..
  - Semiconductors have resistivity which is less than insulators and more than conductors.
  - Semiconductors have negative temperature coefficient.
  - The conducting properties of a semiconductor change when a suitable metallic impurity is added to it, which is very important property.
  - The transistor has replaced the bulky vacuum tube from which the size and cost of the device got decreases.

## Semi-conductors

intrinsic

Extrinsic

P-type

n-type

Ques - 5 Explain Field programmable Gate Array.

- Field programmable gate array provides generation in the programmable logic device.
- The word field in the name refers to the ability of the gate array to be programmed specific function by the user instead of by manufacturer of the device.
- As compared to standard gate arrays, the programmable gate arrays are larger.
- The basic cell structure for FPGAs is more complicated than basic cell structures of arrays.
- The programmable logic blocks of FPGAs are called logic blocks.
- The basic architecture of FPGAs consists of an array of logic blocks with programmable row and column interconnecting channels surrounded by programmable blocks.

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14.

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