



# **Government Engineering College Sec-28 Gandhinagar**

**Sem: - 3**

**Subject: - Digital Fundamental**

**Subject Code: - 3130704**



# Government Engineering College

## Sec-28 Gandhinagar

### Certificate

This is to certify that

Mr./Ms. Tank Gunjan D... Of class

..... Division ...B..., Enrollment No.... D2D31..... Has

Satisfactorily completed his/her term work in

Digital Fundamental..... Subject for the term ending in

20/Jan/2022.

Date: -

A handwritten signature in black ink, which appears to read "Narayan Patel".

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# Institute Vision/Mission

## **Vision:**

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

## **Mission:**

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

# **Computer      Engineering      Department**

## **Vision/Mission**

**Vision:**

**Mission:**

# Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

## PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

## POs

**Engineering Graduates will be able to:**

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of

mathematics, natural sciences, and engineering sciences.

**3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

**6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**12. Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## Digital Fundamental (3130704)

### Course Outcomes (COs)

CO-1	Solve the given problem using Fundamentals of Number system and Boolean algebra.
CO-2	Analyze working of logic families and logic gates and design circuit using various gates.
CO-3	Design and implement combinational and sequential logic circuit and verify its working.
CO-4	Examine the process of Analog to digital conversion and digital to analog conversion.
CO-5	Implement PLDs for the given logic problem.

## 7. Assignment Index

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## 8. Practical Index

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# 9. Assignment 1

**CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra**

## Module 1

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function:  $F = A'B'C + A'BC + AB'$ .
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

# ASSIGNMENT - 1

- Q-1) State and explain De Morgan's theorem with Truth table.
- The De Morgan suggested two theorem that form an important part of Boolean algebra.
  - 1) complement of product = sum of complement individual variable

$$\overline{AB} = \overline{A} + \overline{B}$$

A	B	$\overline{AB}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

- 2) complement of sum = product of complement of individual variable

A	B	$\overline{A+B}$	$\overline{AB}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

(Q-2) simply Boolean functions  $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}$

$$\begin{aligned} & \bar{A}\bar{B}C + \bar{A}BC + A\bar{B} \\ &= \bar{A}C(\bar{B} + B) + A\bar{B} \\ &= \bar{A}C + A\bar{B} \end{aligned}$$

(Q-3) list and explain logic families.

- A logic family of integrated circuit is a group of logic gates constructed using one of several different designs, usually with compatible logic levels and power supply characteristic with family

- TTL
- CMOS
- ECL

#### \* TTL (Transistor - Transistor logic)

- power input moderate
- frequency limit high
- circuit density moderate high

#### \* CMOS

- power input low
- frequency limit moderate
- circuit density very high

#### \* ECL

- power input moderate high
- frequency limit very high
- circuit density moderate

(Q-4) Describe error detecting & correcting code.

#### \* ERROR DETECTING

- When binary data is transmitted and processed, it is susceptible to noise that can alter or distort its contents.
- Because digital systems must be accurate to the digit, errors can pose a serious problem.

#### \* Parity

- The simplest technique for detecting errors is that of adding an extra bit, known as parity bit, to each word being transmitted.
- There are two types of parity - odd parity & even

#### \* check sums

- simple parity cannot detect two errors within the same word.
- as each word is transmitted, it is added to the sum of the previously transmitted words, and retained at the transmitter end.

#### \* Block parity

- when several binary words are transmitted or stored in succession, the resulting collection of bits can be regarded as a block of data.

### \* ERROR CORRECTING :

- A code is said to be an error correcting code, if the correct code word can always be deduced from an erroneous word.
- If the location of an error correction is determined, then by complementing the erroneous digit, the message can be corrected.

### \* 7 bit hamming code

Q-5) Differentiate TTL, shottcky TTL, cmos

characteristics	TTL	CMOS
power input	moderate	Low
frequency limit	High	moderate
circuit density	moderate	High very high
circuit types	High	High
per family		

# 10. Assignment 2

**CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem**

## Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
  - 2.1.  $F(x,y,z) = \Sigma (2,3,6,7)$
  - 2.2.  $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

# ASSIGNMENT - 2

(Q-1) Explain K-map.

- The Karnaugh map (K-map) method is a systematic method of simplifying the boolean expression.
- The K-map is a chart or a graph, composed of an arrangement of adjacent cells, each representing a particular combination of variables in sum or product.

\* Two variable K-map

$$2^2 = 4$$

$$m_0 = \bar{A}\bar{B}, m_1 = \bar{A}B, m_2 = A\bar{B}, m_3 = AB$$

	A	0	1
B	0	0	2
1	1	1	3

\* Three variable K-map

$$2^3 = 8$$

$$m_0 = \bar{A}\bar{B}\bar{C}, m_1 = \bar{A}\bar{B}C, m_2 = \bar{A}BC, m_3 = \bar{A}B\bar{C}, m_4 = A\bar{B}\bar{C}, m_5 = A\bar{B}C$$

$$m_6 = ABC, m_7 = A\bar{B}\bar{C}$$

C	AB	00	01	11	10
0	0	2	6	4	
1	3	7	5	1	

\* Four variable K-map

$$m_0 = \bar{A}\bar{B}\bar{C}\bar{D}, m_1 = \bar{A}\bar{B}\bar{C}D, m_2 = \bar{A}\bar{B}CD, m_3 = \bar{A}\bar{B}C\bar{D}, m_4 = A\bar{B}\bar{C}\bar{D}, m_5 = A\bar{B}\bar{C}D$$

$$m_6 = \bar{A}BC\bar{D}, m_7 = \bar{A}BCD$$

CD	AB	00	01	11	10
		00	1	4	12
01	0	2	5	13	9
	1	3	7	15	11
11	0	2	6	14	10
	1	3	7	15	12

(Q-2) obtain the simplified expressions sum of products for the following Boolean Functions:

$$2.1 \quad F(x,y,z) = \Sigma(2,3,6,7)$$

$$2.2 \quad F(A,B,C,D) = \Sigma(4,6,7,15)$$

$$* \quad F(x,y,z) = \Sigma(2,3,6,7)$$

	$\bar{x}\bar{y}$	$\bar{x}y$	$\bar{x}\bar{y}$	$xy$	$x\bar{y}$	
$\bar{z}A$	0	1	9	1	6	4
$\bar{z}B$	1	1	3	1	7	5

$$F(x,y,z) = \bar{y}$$

$$* \quad F(A,B,C,D) = \Sigma(4,6,7,15)$$

	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$	$\bar{A}\bar{B}$	$\bar{A}B$	$AB$	$A\bar{B}$
$\bar{C}\bar{D}$	0	1	4	12	1	5	13	9
$\bar{C}D$	1	3	1	15	1	7	15	11
$CD$	3	1	7	1	14	1	10	1
$C\bar{D}$	2	1	6	14	10			

$$F(A,B,C,D) = BC\bar{D} + \bar{A}BC + A\bar{B}C\bar{D}$$

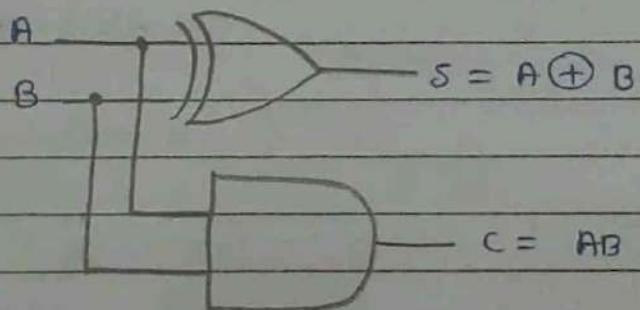
(Q-3) Describe adder and subtractor.

- \* Adder is combinational circuit which is used to add Binary bits. (sum).
- \* Subtractor is used to subtract the Binary bits.

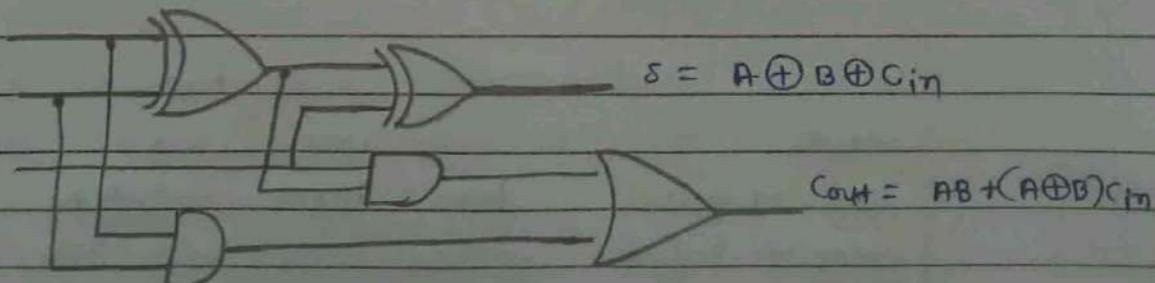
ADDER	SUBTRACTOR
Half	Half
Full	Full

### ADDER

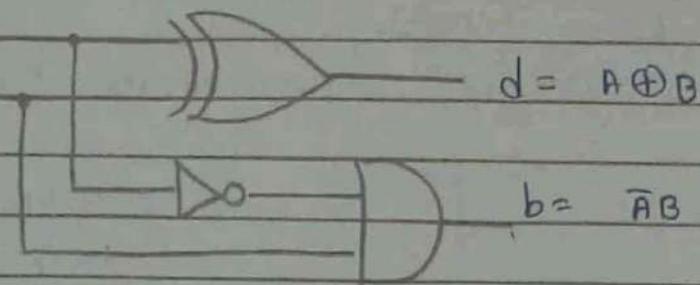
- \* Half Adder :- it adds two inputs and produces sum and carry.



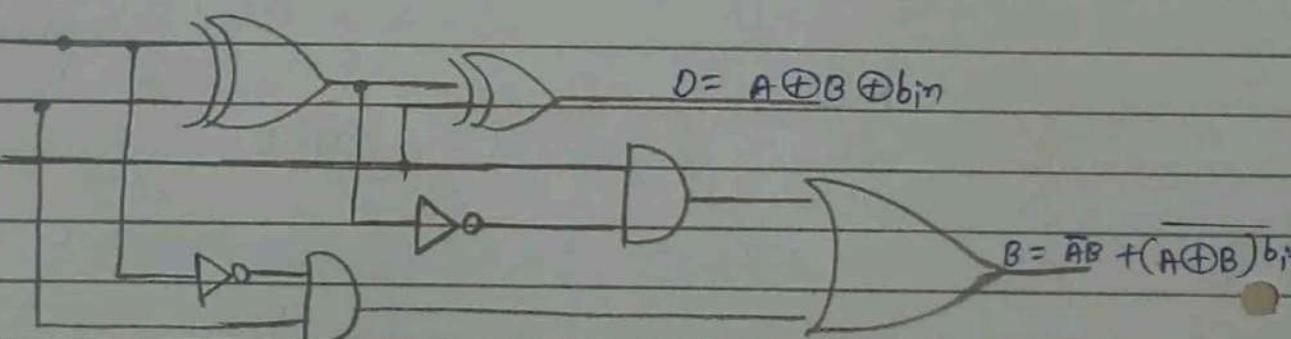
- \* Full Adder :- it adds together two binary bits , plus a carry in digit to produce a sum and carry out digit.



\* HALF SUBTRACTOR :- it subtracts one bit from the other and produces difference.



\* FULL SUBTRACTOR :- it performs subtraction involving 3 bits, A, B & Bin. and produces difference and Bout Borrow.

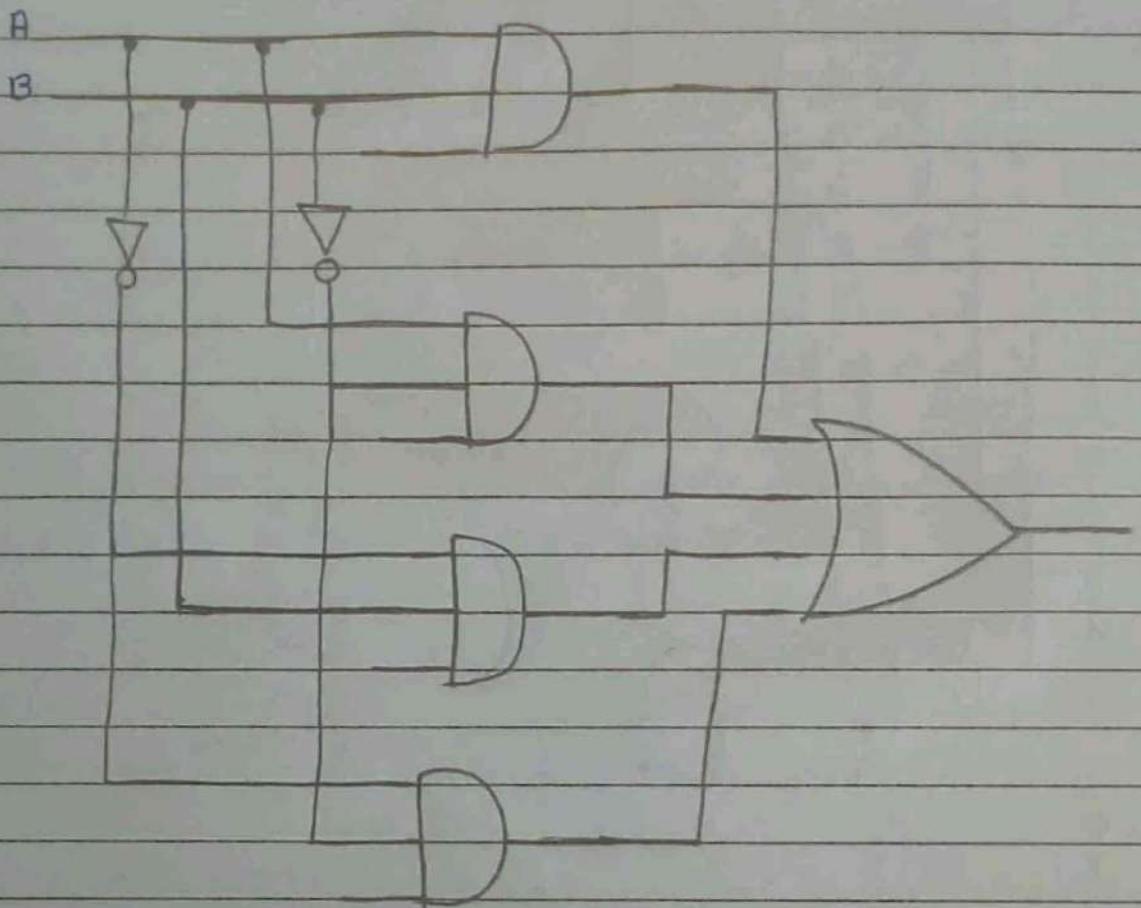


Q-4) Explain multiplexers & demultiplexers

### MULTIPLEXER

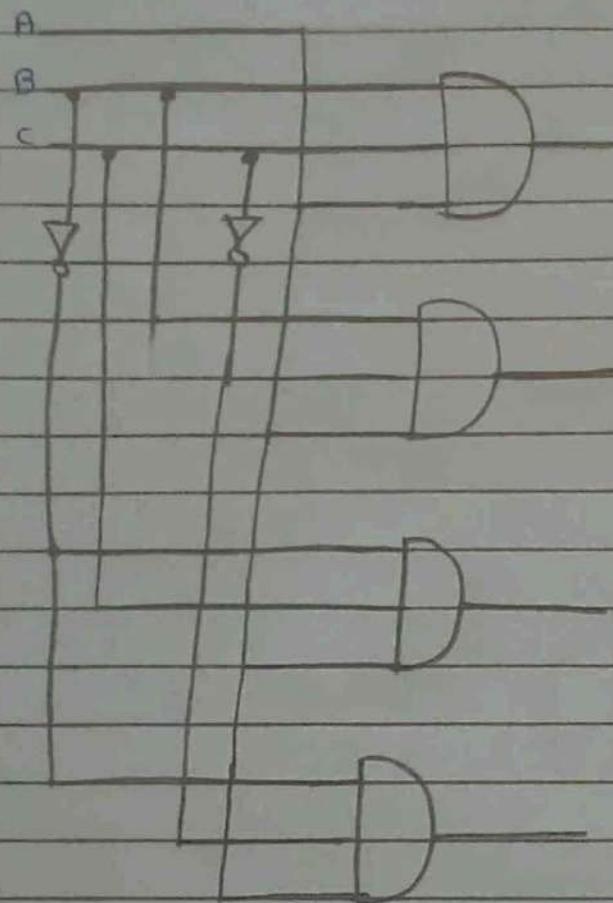
- it is a combinational circuit has a maximum of  $2^n$  data inputs, 'n' selection lines, and a single output line. one of these data inputs will be connected to the output based on the values of the selection lines.

### 4x1 MUX



### \* Demultiplexer

- a demultiplexer performs reverse operation of multiplexer
- it takes a single input and distributes it over several o/p.
- demux is 1 to N device



(Q-5) Describe parity checker and generator.

Parity generator :- The parity generator is a combination circuit at the transmitter. It takes an original message as input and generates the parity bit for that message and the transmitter. In this generator transmits message along with its parity bit.

Parity checker :- Parity check is an error correction process in network communication that ensures data transmissions between communication nodes are accurate.

# 11. Assignment 3

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## Module 3

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

# ASSIGNMENT- 3

(Q-1)

Differentiate Sequential & combinational circuits.

## Combinational circuit

- here, the output variables at any instant of time are dependent only on the present input variables.

- memory units is not required in combinational circuits.

- it is faster

- it is easy to design.

## sequential circuit

- here, the output variables at any instant of time are dependent not only on the present input variables but also on the present state.

- memory units is required to store the past history of the input variables in sequential circuits.

- it is slower

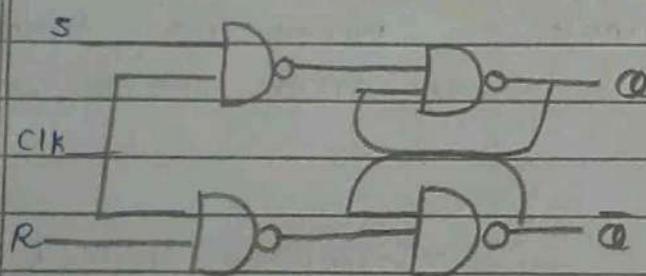
- comparatively harder to design.

(Q-2) List and Explain Flip Flops.

- Flip Flop is used to store data.

- SR Flip Flop
- JK Flip Flop
- D Flip Flop
- T Flip Flop

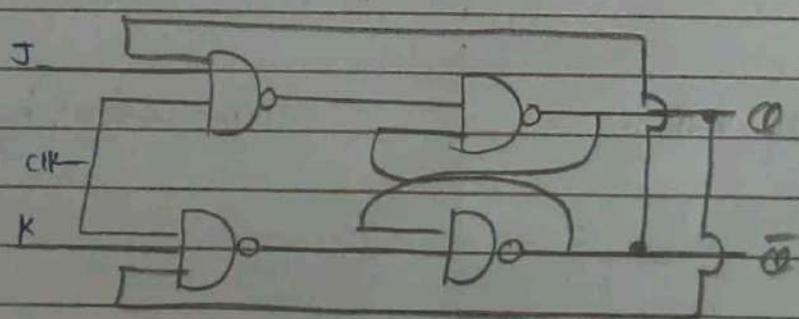
\* S-R Flip Flop



Truth table

A	B	Output
0	0	invalid
0	1	1
1	0	0
1	1	Hold

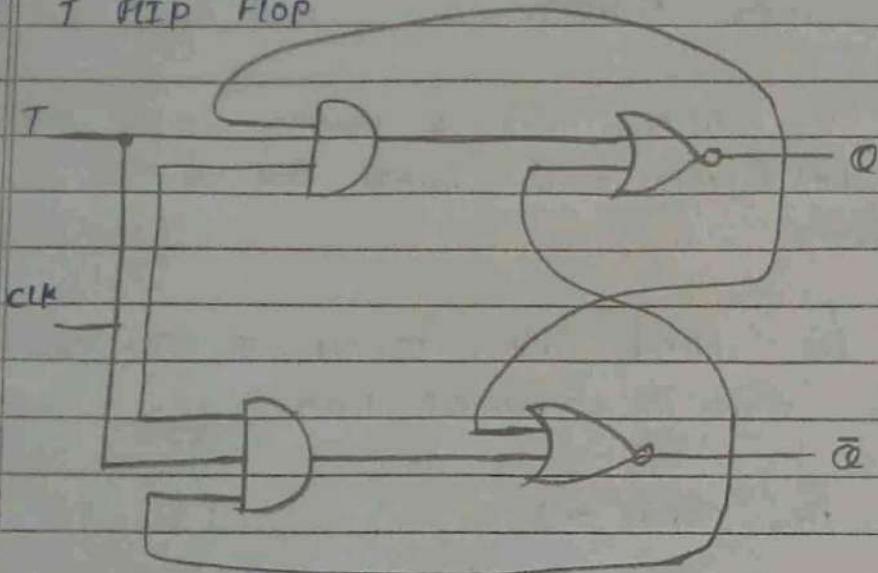
\* JK Flip Flop



Truth table

J	K	Q(n+1)
0	0	Hold
0	1	0
1	0	1
1	1	on

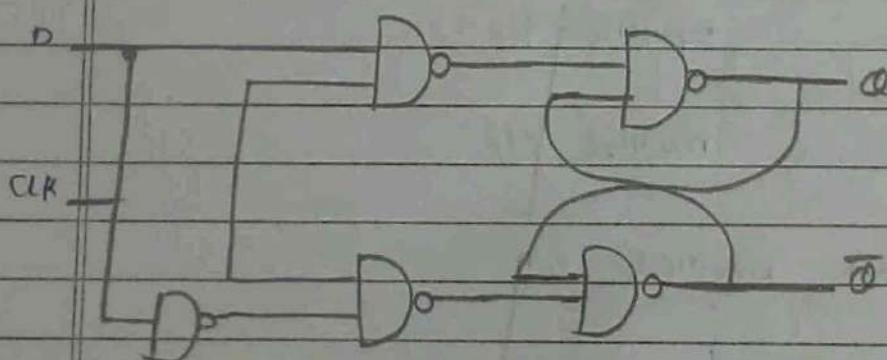
\* T FLIP FLOP



T 4th table

T	$Q_n$	$(Q_{n+1})$
0	0	0
0	1	1
1	0	1
1	1	0

\* D Flip Flop



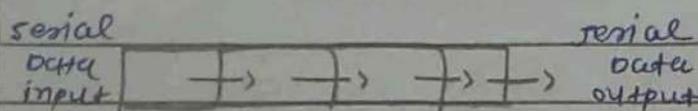
D 4th table

D	$Q_n$	$(Q_{n+1})$
0	0	0
0	1	1
1	0	0
1	1	1

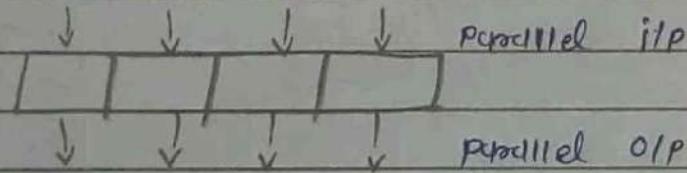
(1)-3) List & Explain Register.

- A number of flip-flops connected together such that data may be shifted into and shifted out of them is called shift register.
  - Data may be shifted into or out of the register either in serial form or parallel form.

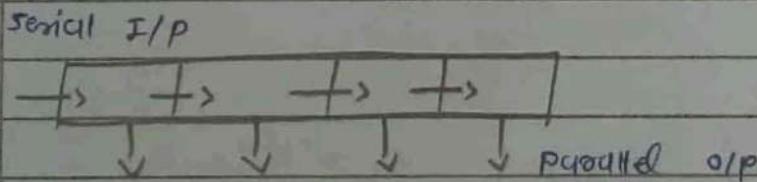
## 2) Social in, social out



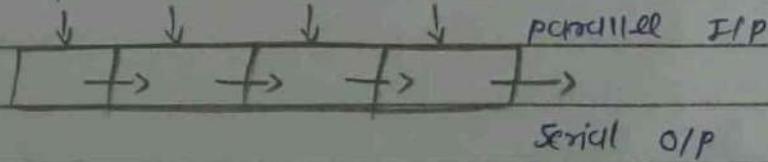
2) Parallel port input Parallel input



3) Serial input parallel o/p

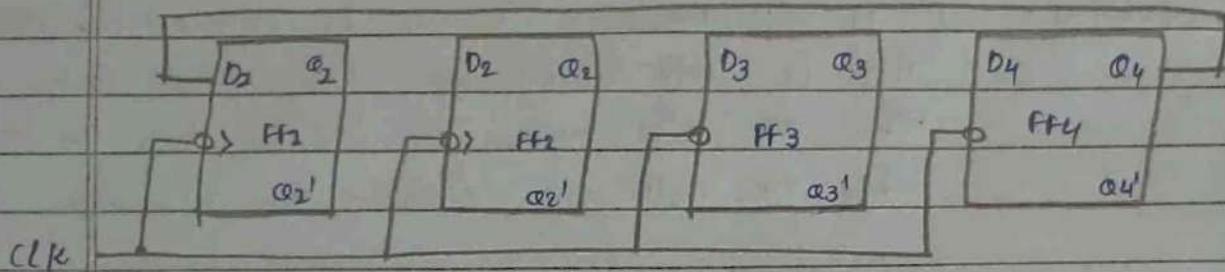


4) parallel I/P serial O/P

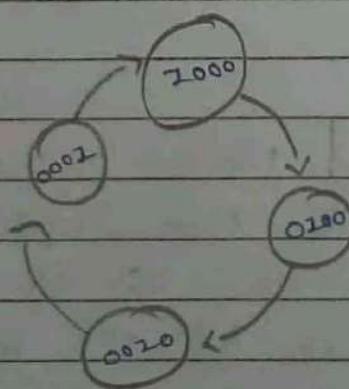


(Q-4) Describe ring counter.

- This is the simplest shift register counter. The basic ring counter using D FFs is shown arranged as in a normal shift register.



- In most instances, only single 1 is in the register and is made to circulate around the register as long as clock pulses are applied initially the first FF is present to a 1.
- So, the initial state is 2000. After each clock pulse, the contents of the registers are shifted to the right by one bit and Q4 is shifted to an output.



(Q-5) Describe how to design counter using Flip Flops.

Operations for Asynchronous Counter.

1 condition 1: when both flip flop are in rest condition

operation: The o/p of both flip flops Q<sub>A</sub> Q<sub>B</sub> will be 0.

2 condition 2: when the first negative clock edge passes

operation: 1<sup>st</sup> FF will toggle, o/p will be from 0 to 1. o/p of this FF will taken by clock input of the next FF. This o/p will taken as positive edge by 2<sup>nd</sup> clock. This i/p will not change the 2<sup>nd</sup>'s o/p.

3 condition 3: when the 2<sup>nd</sup> negative clock edge is applied.

operation: The 2<sup>nd</sup> FF will toggle again, o/p of this FF will change from 1 to 0. This o/p will taken as negative edge clock by 2<sup>nd</sup> FF. This i/p will change the 2<sup>nd</sup>'s FF's o/p state.

4 condition 4: when the 3<sup>rd</sup> negative clock edge is applied.

operation: The 1<sup>st</sup> FF will toggle again, o/p will change from 0 to 1. This will taken as positive edge by 2<sup>nd</sup> FF. This o/p will not change the 2<sup>nd</sup> FF's output state.

5 condition 5: when the fourth negative clock edge is applied

operation: The FF will toggle again, and o/p will be change from 1 to 0. This o/p will taken as a negative edge clock by 2<sup>nd</sup> FF. This i/p will change the o/p state of the 2<sup>nd</sup> FF.

# 12. Assignment 4

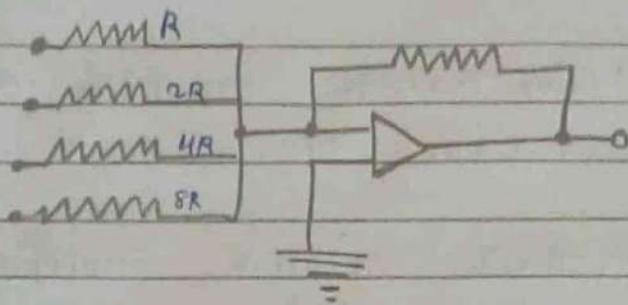
**CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.**

## Module 4

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

# ASSIGNMENT-4

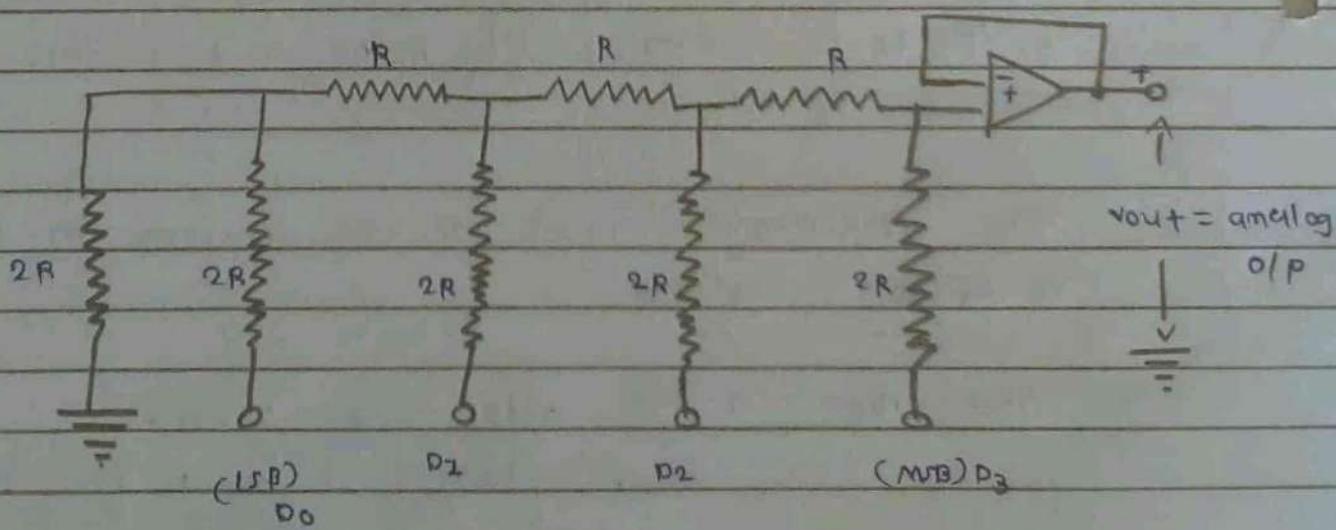
(Q-2) Explain weighted resistor converter.



- The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit positions of inputs.
  - since the op-amp is connected as an inverting amplifier, each input is amplified by a factor equal to the ratio of the feedback resistance divided by the input resistance to which it is concerned.
  - The MSB  $p_3$  is amplified by  $R_1/R_3$ ,  $p_2$  is amplified by  $p_1/R_2$ ,  $p_1$  is amplified by  $R_2/4R$  and  $p_0$ , the LSB is amplified by  $R_1/8R$ .
  - The inverting terminal of the op-amp in figure c acts as a virtual ground.
  - since the op-amp adds and inverts.
- $$V_{out} = \left( \frac{p_3}{R_3} + \frac{p_2}{R_2} + \frac{p_1}{R_1} + \frac{p_0}{R_0} \right) \times \left( \frac{R_f}{R} \right)$$
- The main disadvantage of type of DAC is that a different valued precision resistor must be used for each bit position of the digital I/P.

(Q-2) Explain R-2R ladder D/A converter.

- The R-2R ladder type DAC is the most popular DAC. It
- uses a ladder network containing series parallel combinations of two resistors of values  $R$  and  $2R$ .
- The operational amplifier configured as voltage followers is used to prevent loading.
- Figure shows the circuit diagram of a R-2R ladder type DAC having 4 bit digital i/p.
- When a digital signal  $D_3 D_2 D_1 D_0$  is applied at the input terminals of the DAC, an equivalent analog signal is produced at the o/p terminal.



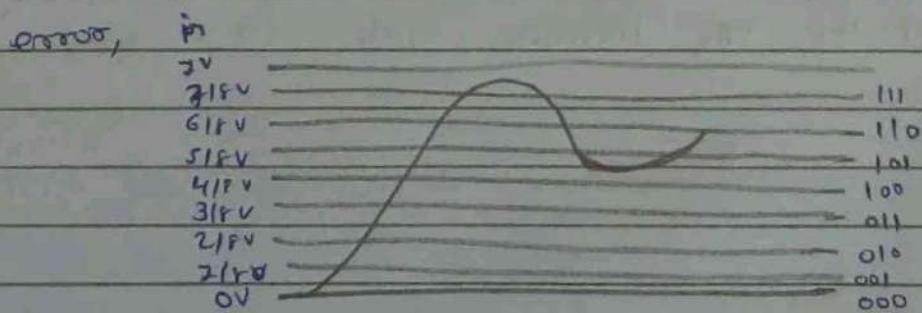
(Q-3) Describe specification of A/D & D/A converter.

- the resolution of a DAC is defined as the smallest change that occurs in an analog output result of a change in the digital I/P
- The resolution of a DAC is also defined as the reciprocal of the no. of discrete steps in the full scale o/p of the DAC
- the resolution is always equal to the weight of the LSB and is also referred to as the step size
- the step size is the amount by which  $V_{out}$  will change as the digital input value is changed from one value to the next
- the step size of the DAC is the same as the proportionality factor in the DAC i/p o/p relationship.
- Although resolution can be expressed as the amount of voltage or current per step, it is also useful to express it as a percentage of full scale o/p.
  
- $\% \text{ resolution} = \frac{\text{Step size}}{\text{Full scale}} \times 100\%$ .
  
- cost of the DAC increase with the no. of I/P bits.

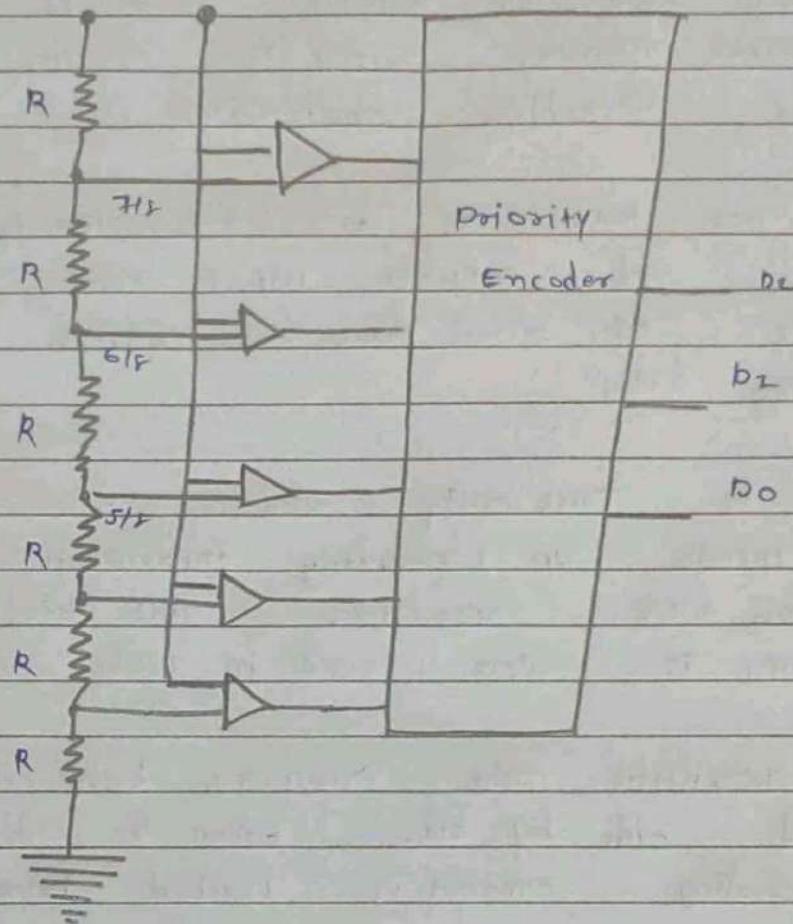
Q-4)

Explain quantization and encoding.

- in a digital to analog converter, the possible number of digital o/p is fixed.
- in contrast, in an analog to digital converter the input analog voltage, can have any value in a range, but the digital o/p can have only  $2^N$  discrete values for an N bit A/D converter.
- therefore, the whole range of analog voltage is required to be represented suitably in  $2^N$  intervals.
- this process is known as quantization.
- consider an analog voltage in the range of 0 to V and a 3 bit digital o/p for any voltage in this range.
- let us divide the whole range of analog voltage in 8 intervals of the size  $s = V/8$ .
- each interval is assigned a 3 bit binary value.
- The intervals of the analog voltage and their corresponding digital values assigned.
- From this, we observe that the whole range of voltage in an interval is represented by only one digital value.
- Therefore, there is an error referred to as quantization error.



(Q-5) Explain parallel comparator A/D converter.



- The A/D converter is the fastest type. This utilizes parallel different comparators that compare reference voltage with I/P voltage.
- advantage is conversion time is less, disadvantage is it requires  $2^{n-1}$  comparators,  $2^n$  resistors and priority encoder.
- here it requires  $7(=2^3-1)$  comparators. A reference voltage  $E_{ref}$  is connected to voltage divider into 7 equal increment levels.
- For any analog I/P, one comparator and all below will have high voltage applied to the inverting terminal of the uppermost comparator.

$$\left( \frac{7R}{7R+R} \right) \times E_{ref} = \frac{7}{8} \times E_{ref}$$

# 13. Assignment 5

**CO5:** Implement PLDs for the given logical problem.

## Module 5

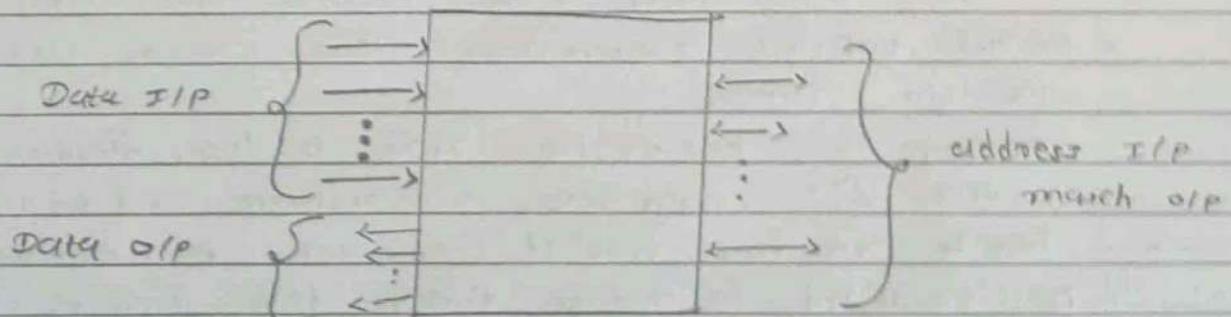
1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA).

## ASSIGNMENT - 5

(Q-2)

Explain content addressable memory.

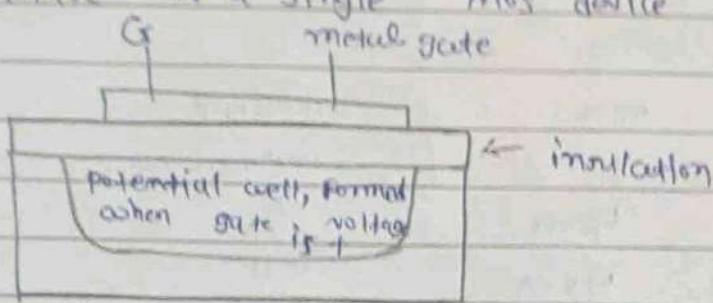
- Content addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications.
- It is also known as associative memory or associative storage and compares input search data against a table of stored data and returns the address of matching data.
- CAM is frequently used in networking devices where it speeds up forwarding information base and routing table operations. This kind of associative memory is also used in cache memory.
- In associative cache memory, both address and content is stored side by side. When the address matches, the corresponding content is fetched from cache memory.



Q-2

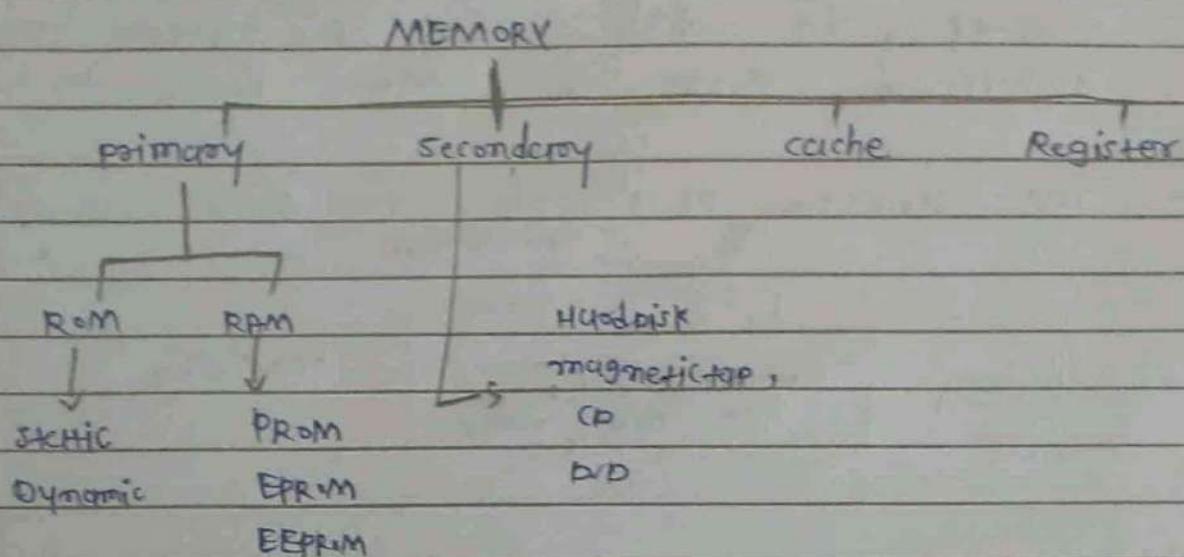
Explain charge coupled device memory (CCD)

- The charge coupled device memory is a type of dynamic memory, in which packets of charges are continuously transferred from one MOS device to another.
- The structure of a single MOS device is below.



- The CCD memory is inherently serial. Practical memories are constructed in the form of shift registers, each shift register being a line of cells.
- By controlling the timing of the clock signals applied to the shift registers, data can be accessed one bit at a time from a single register or several bits at a time from multiple registers.
- Advantage of CCD is single cell structure makes it possible to construct large capacity memories at low cost.

(Q-3) Explain classification of memory



### \* RAM

- Data is not permanent but it can be altered any no. of times
- it is a high speed memory
- The CPU can access the data stored on it
- large size with higher capacity.

### \* ROM

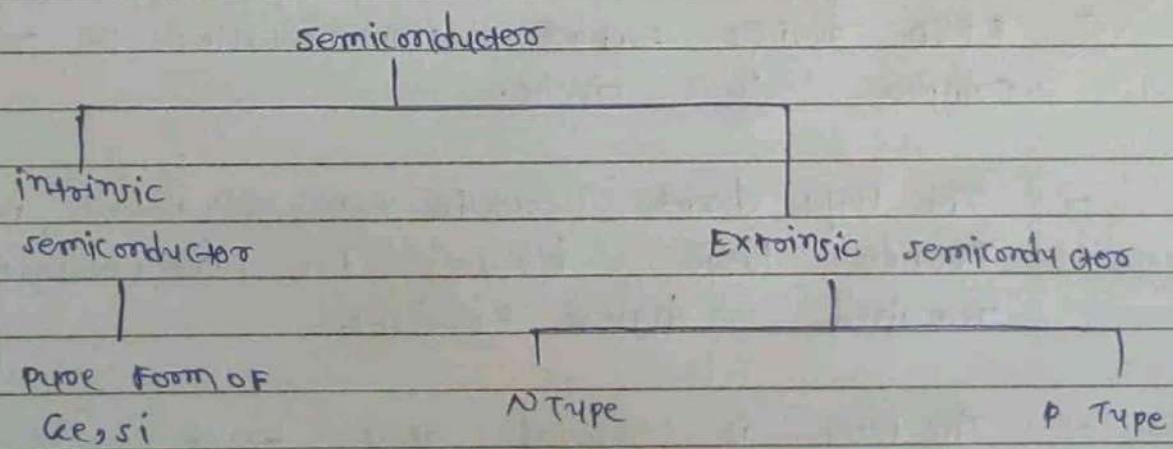
- Data is permanent. it can be altered but only a limited no. of times that too at slow speed
- it is much slower than the RAM.
- small size with less capacity.

(Q-4) Describe semiconductors.

- Semiconductor devices can display a range of useful properties, such as passing current more easily in one direction than the other, showing variable resistance, having sensitivity to light or heat. Because the electrical properties of a semiconductor material can be modified by doping and by the application of electrical fields or light, devices made from semiconductors can be used for amplification.

### Properties of semiconductor

- Resistivity
- Conductivity
- Temperature coefficient of resistance
- Current flow



- The conductivity of devices depends mainly on the majority of carriers. Hence in the p-type semiconductor holes are subject to current conduction on the contrary, in the case of n-type semiconductor, electrons are responsible for current conduction.

(Q-5) Explain field programmable gate array (FPGA).

- The programmable logic devices are based on similar basic architecture the programmable logic cell or the programmable logic array.
- To increase the effective size and to add more functionality in a single programmable device, alternative architectures have been developed which are known as field programmable gate arrays.
- The logic densities of FPGAs are much higher than those of CPLDs.
- From modern thousands digital circuit with 200 of 1000 of gates is not too large.
- FPGA devices support implementation of relatively large complex logic circuits.
- The FPGA doesn't contain AND, OR panels, instead they provide logic blocks for implementation of the required digital functions.
- The FPGA is composed of a no. of relatively independent configurable logic blocks.
- There are a number of manufacturers of FPGA devices.
- The basic FPGAs consist of an array of configurable logic blocks.

# 14. Practical 1

**CO2:** Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

## Module 1

**Aim:** Getting familiar with Logisim, Study and implement all basic logic gates.  
Implement NAND and NOR logic gates as universal gates.

### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

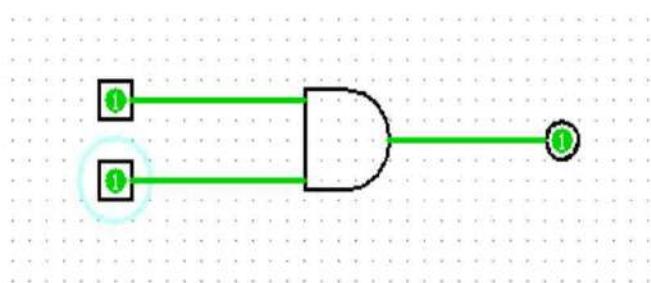
## Basic Gate :

### AND GATE :

- and gate has two or more inputs but only one output
- here if both inputs are 1 then output is 1 else output is 0(zero).
- NOTATION :  $c = A * B$

### Truth Table

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

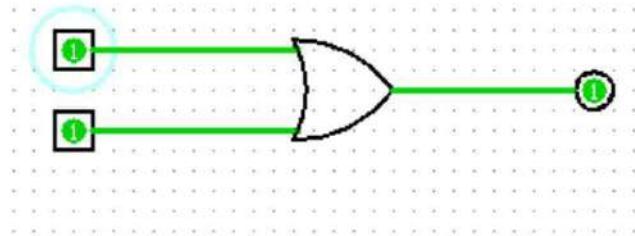


## OR GATE :

- or gate has two or more inputs but only one output
- here, if both inputs are 0 then the output is 0.
- NOTATION :  $A + B$

## Truth Table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

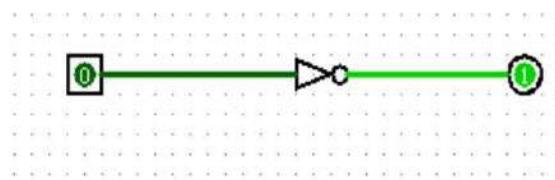


## NOT GATE :

- It is also called an “inverter”.
- Here output is always a complement of input.
- If the input is 1 then the output is 0.
- If the input is 0 then the output is 1.
- NOTATION :  $c = A'$

## Truth Table

A	C
1	0
0	1

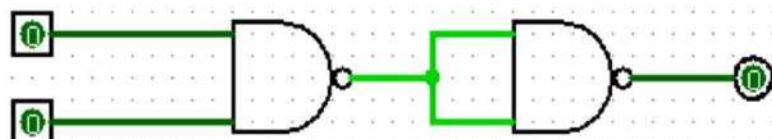


## Universal Gate :

### Using Nand gate

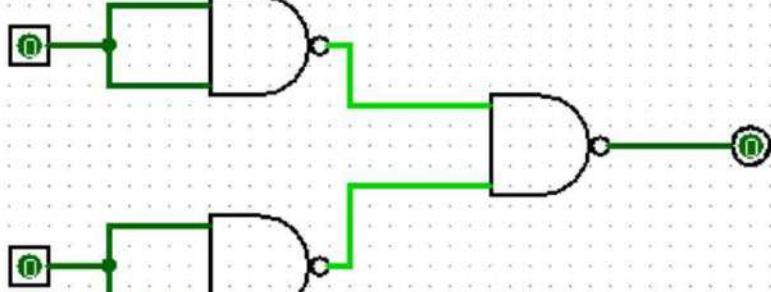
#### AND GATE :

Notation:  $A * B$



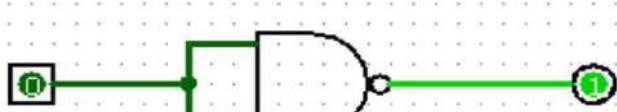
#### OR GATE :

Notation :  $A + B$



## NOT GATE :

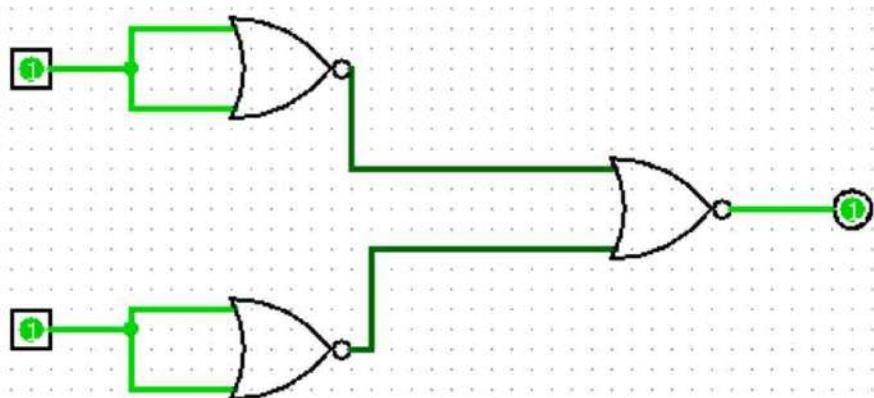
*Notation: A'*



## Using Nor gate

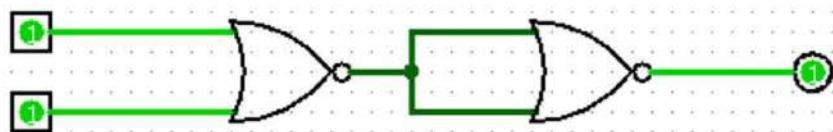
## AND GATE :

*Notation: A \* B*



## OR GATE :

Notation :  $A + B$



## NOT GATE :

Notation:  $A'$



# 15. Practical 2

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## Module 2

**Aim:** Implement half and full Adders using logic gates.

**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

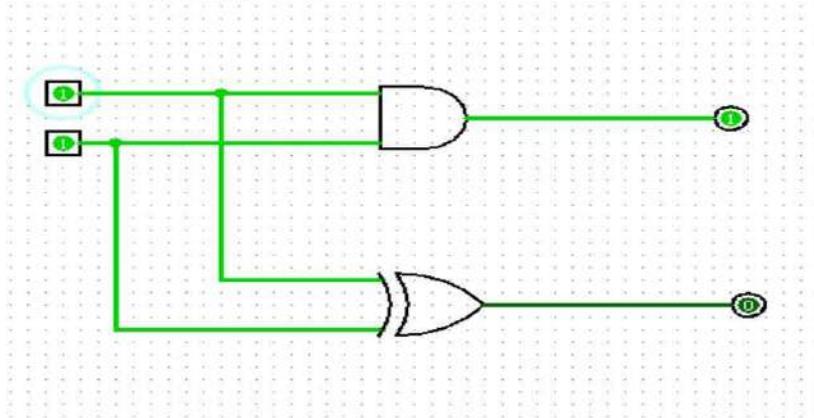
## HALF ADDER

- A half adder is a combinational circuit with two i/p & two o/p.
- It adds the inputs and produces the sum(s) and the carry(c) bits.
- The sum (s) is the X-OR therefore,  $S = AB' + BA' = A \text{ XOR } B$
- The carry (c) is the AND therefore,  $C = AB$

## Truth Table

<b>INPUT</b>		<b>OUTPUT</b>	
<b>A</b>	<b>B</b>	<b>SUM</b>	<b>CARRY</b>
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

## Circuit :



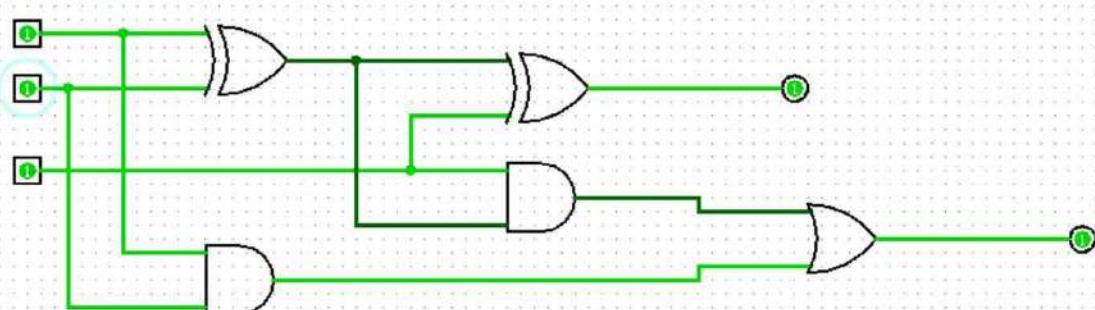
## FULL ADDER

- A full adder is a combinational circuit that adds two bits and a carry and outputs a sum bit and a carry it.
- The full adder adds the bits A and B and the carry from the previous column called the carry-in cin and output the sum bit s and the carry bit called the carry out cout.
- The variable S gives the value of the least significant bit of the sum.
- $SUM \quad S = A'B'Cin + A'BCin + AB'Cin + ABCin$   
A XOR B XOR Cin
- $Carry \quad Cout = A'BCin + AB'Cin + ABCin$   
AB + (A XOR B)Cin

## TRUTH TABLE

Input			Output	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

## Circuit :



# 16. Practical 3

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working.

## Module 2

**Aim:** Implement half and full Subtractors using logic gates.

### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

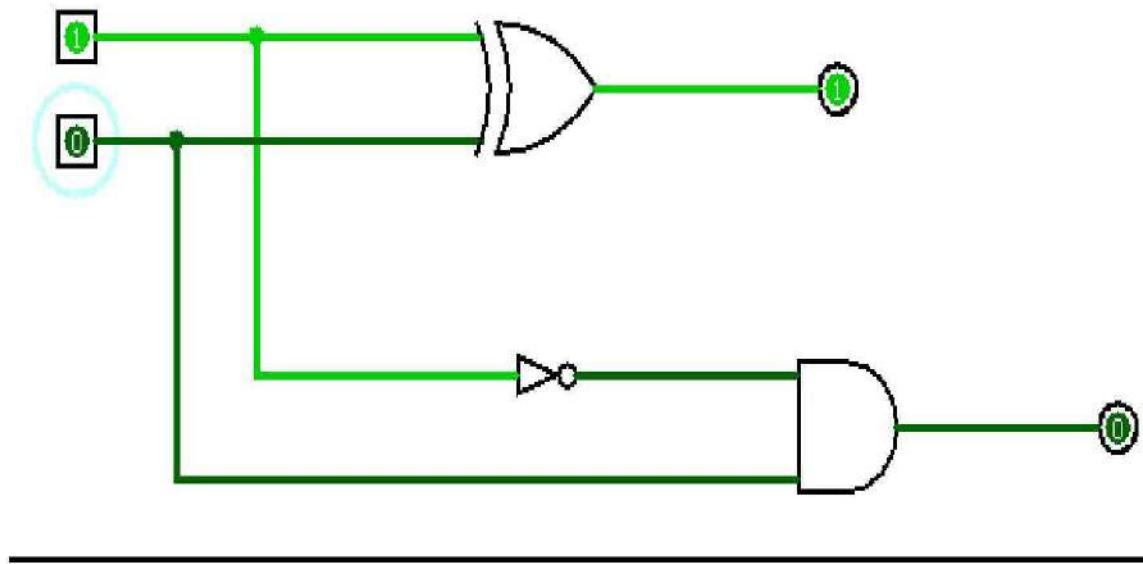
## HALF SUBTRACTOR

- a half subtractor is a combinational circuit that subtracts one bit from the other and produces the difference.
- It also has an output to specify if a 1 has been borrowed.
- Difference  $D = AB' + BA' = A \text{ XOR } B$
- Borrow  $B = A'B$

## Truth Table

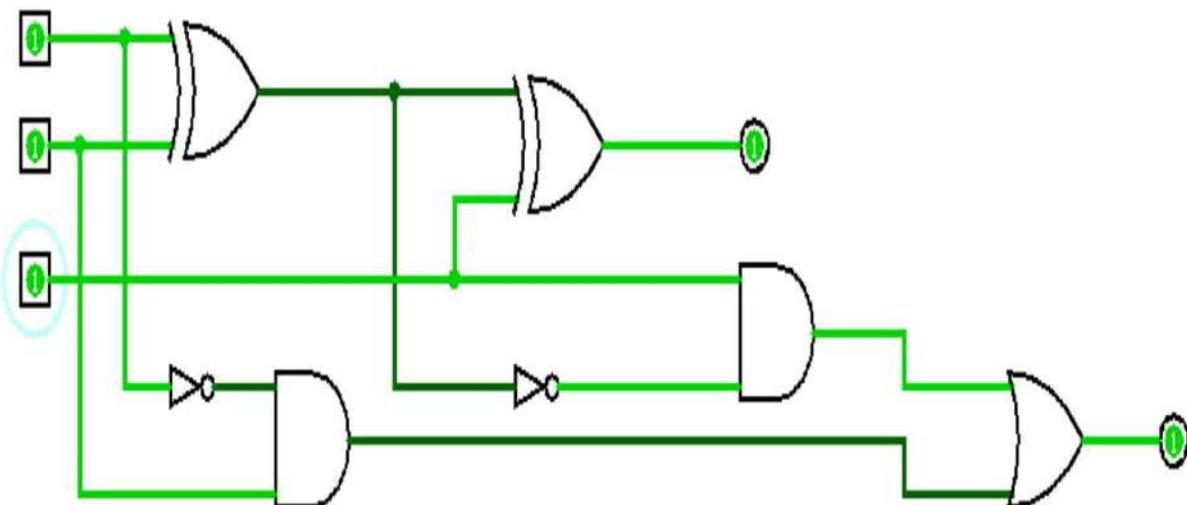
<b>INPUT</b>		<b>OUTPUT</b>	
<b>A</b>	<b>B</b>	<b>d</b>	<b>b</b>
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

## Circuit :



## FULL SUBTRACTOR

- The half subtractor can be used only for LSB subtraction.
- If there is a borrow during the subtraction of the LSBs, it affects the subtraction in the next higher column; the subtrahend bit is subtracted from the minuend bit, considering the borrow from that column used for the subtraction in the preceding column.
- Such a subtraction is performed by a full subtractor.
- Difference  $D = A'B'bin + A'Bbin + AB'bin' + ABbin$   
 $= A \text{ XOR } B \text{ XOR bin}$
- Borrow  $b = A'B'bin + A'Bbin' + A'Bbin + ABbin$   
 $= A'B + (A \text{ XOR } B)' \text{ bin}$



## Truth Table :

INPUT			OUTPUT	
A	B	bin	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

# 17. Practical 4

**CO3: Design and implement Combinational and Sequential logic circuits and verify its working.**

## Module 2

**Aim:** Perform Parity Checker.

**Code:**

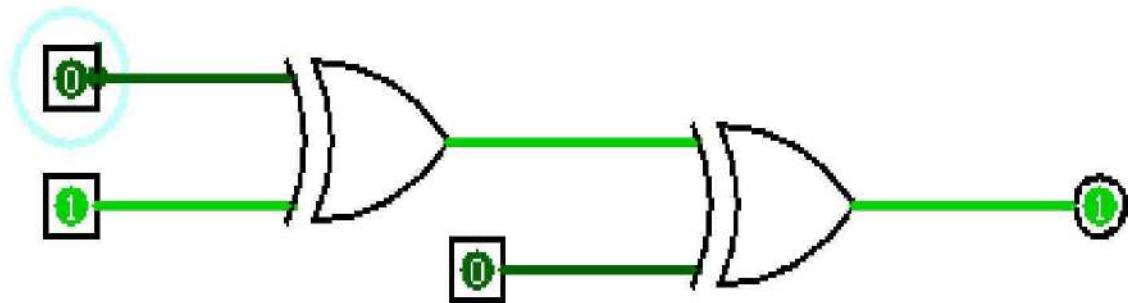
Output snapshot: (In output include practical details and execution date & time with your enrollment number)

## Parity checker

- the parity checker is needed to detect errors in communication and also in the memory storage devices parity checker is used for testing.
- $F = A'B'c + A'BC' + ABC + AB'C' = A \oplus B \oplus C$

**Truth table :**

<b>INPUT</b>			<b>OUTPUT Parity bit (f)</b>
<b>A</b>	<b>B</b>	<b>C</b>	
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

**CIRCUIT :**

# 18. Practical 5

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working.

## Module 2

**Aim:** Study and implement Multiplexer and Demultiplexer.

### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

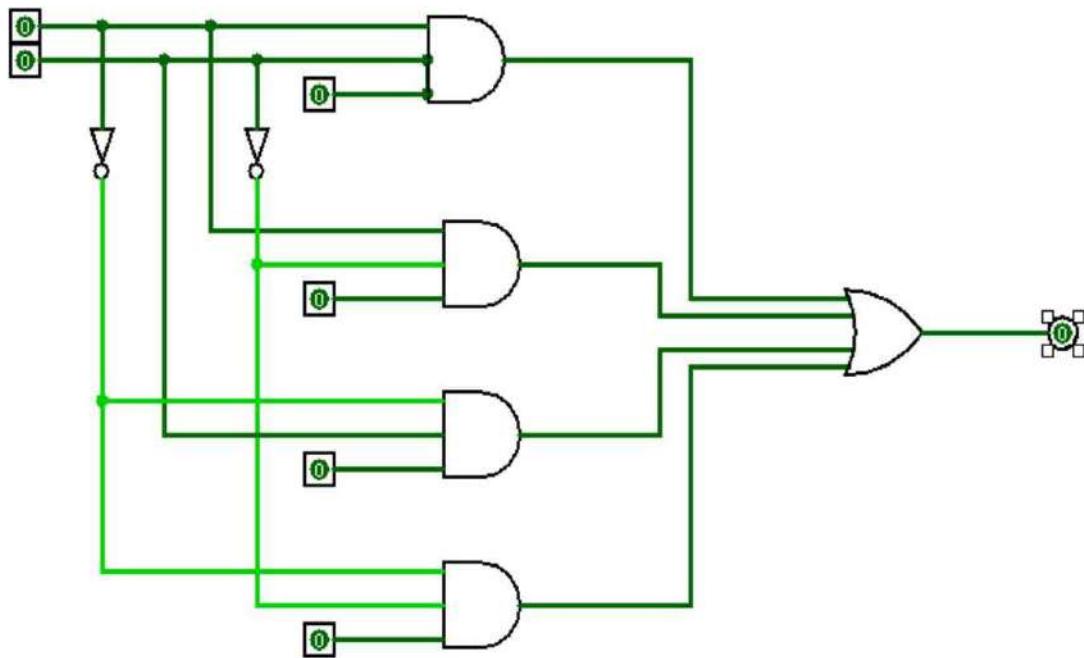
## Multiplexer

- it is a combinational circuit that has a maximum of  $2^n$  data inputs, ' $n$ ' selection lines, and a single output line. One of these data inputs will be connected to the output based on the values of the selection lines.

## Truth Table :

Input		output
S1	S0	Y
0	0	Y1
0	1	Y2
1	0	Y3
1	1	Y4

## CIRCUIT :

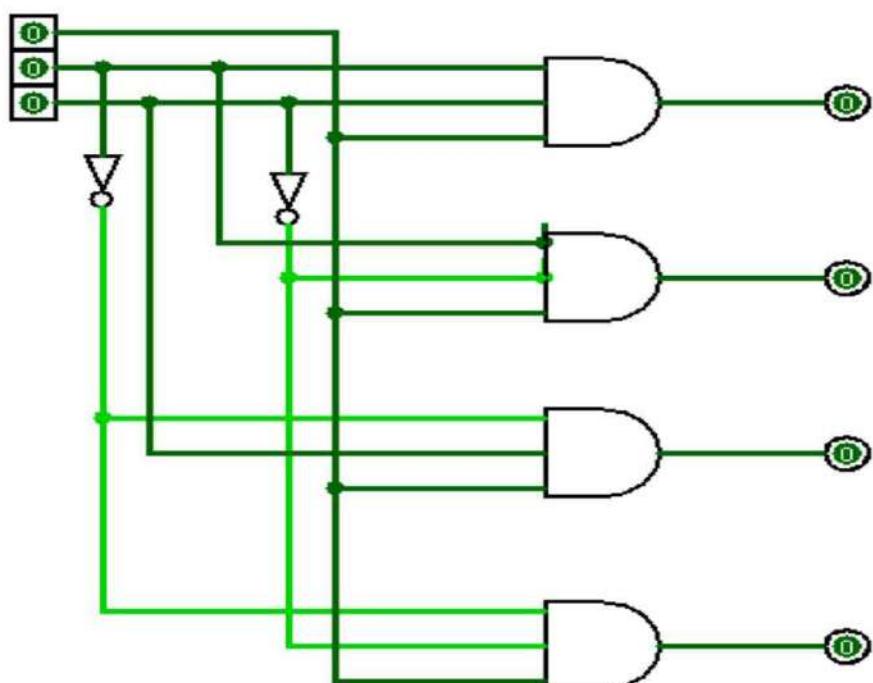


### Demultiplexer

- a demultiplexer performs the reverse operation of a multiplexer; it takes a single input and distributes it over several outputs.
- Demux is a 1 to N device.

**Truth table :**

input		output			
S1	S0	Y1	Y2	Y3	Y4
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

**Circuit :**

# 19. Practical 6

**CO4:** Examine the process of Analog to Digital conversion and Digital to Analog conversion

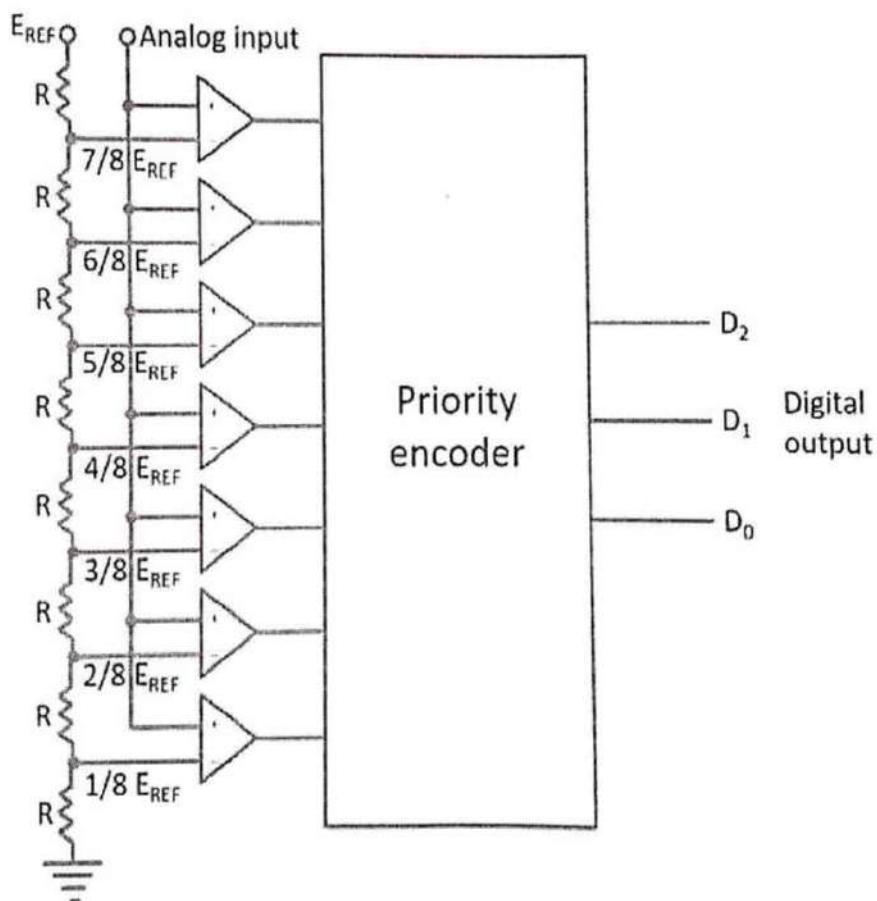
## Module 4

**Aim:** Study and configure A to D convertor and D to A convertor.

### Code:

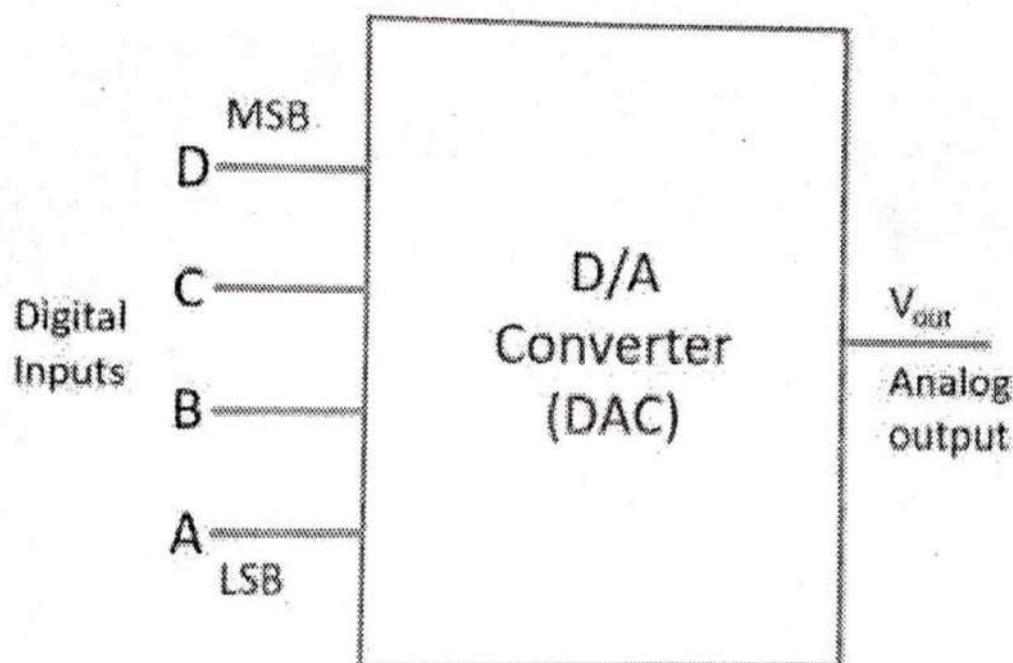
Output snapshot: (In output include practical details and execution date & time with your enrollment number)

## A to D converter :



## **D to A converter :**

### **2. D/A Converter :**



## 20. Practical 7

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working

**Module 3**

**Aim:** Study and implement a shifter.

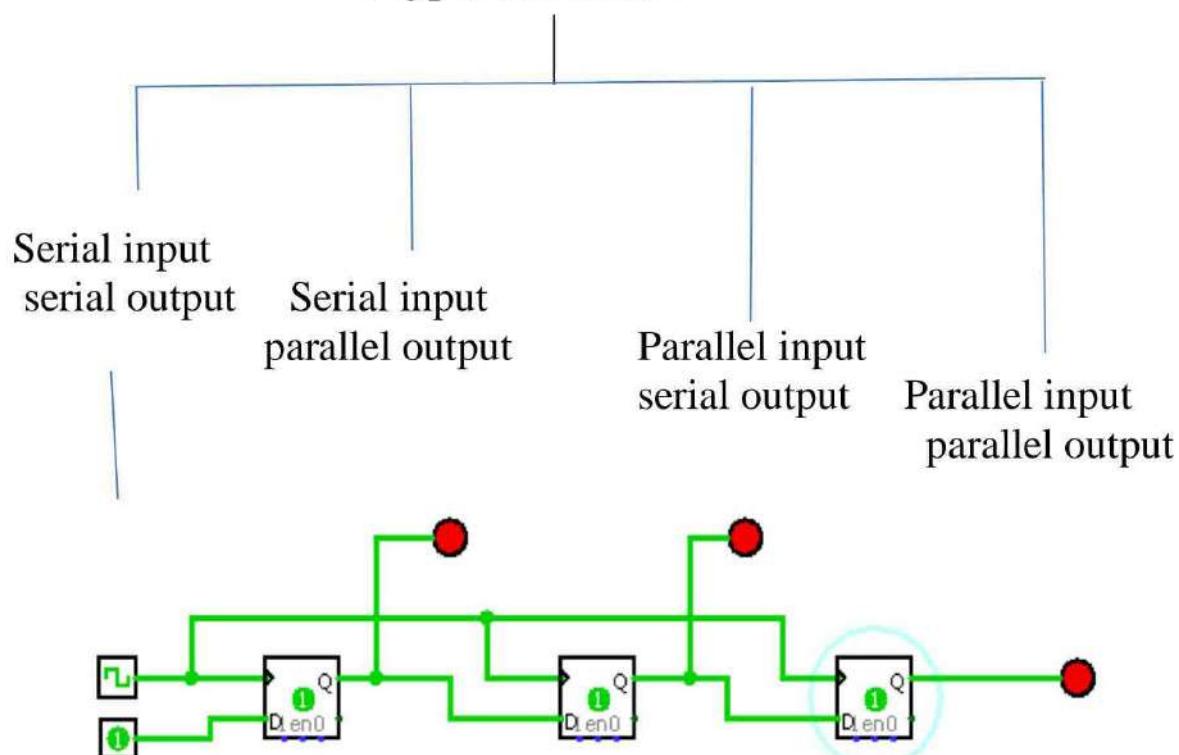
**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

### SHIFT REGISTER

- It is a group of flip flops connected in series used to store multiple bits of data. the information stored within these registers can be transferred with the help of shift registers. A shift register is a group of flip-flops used to store multiple bits of data.

**4 types are there :**



# 21. Practical 8

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working

**Module 3**

**Aim:** Study and implement Flip-flops.

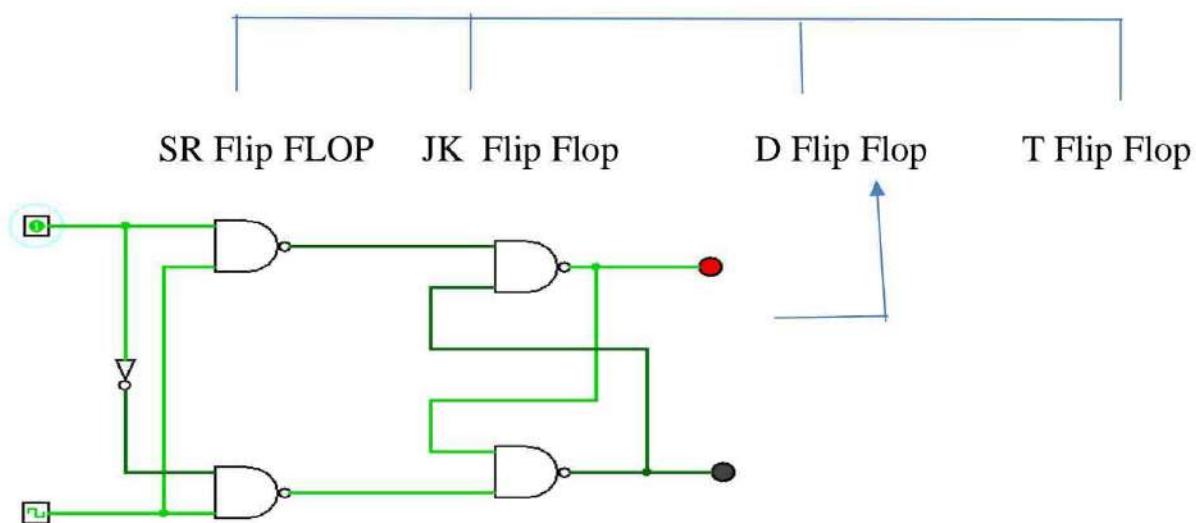
**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

## FLIPFLOP

- A circuit that has two stable states is treated as a **flip-flop**. These stable states are used to store binary data that can be changed by applying varying inputs. Flip-flops are the fundamental building blocks of the digital system. Flip flops and latches are examples of data storage elements. In the sequential logical circuit, the flip flop is the basic storage element.

**4 types are there :**



## 22. Practical 9

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working

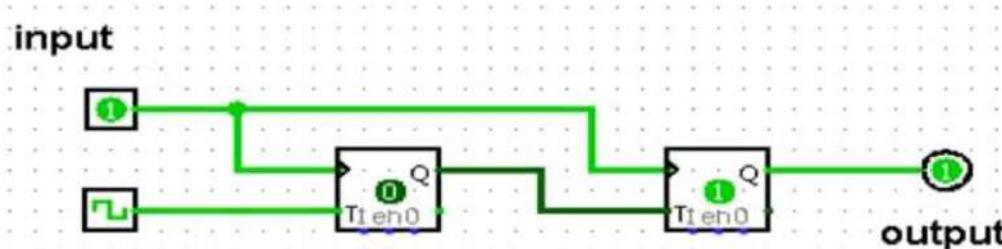
**Module 3**

**Aim:** Study and implement Counter.

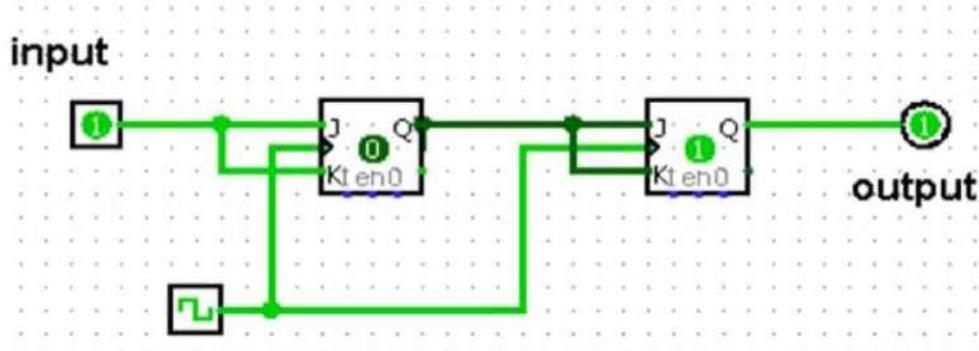
**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

### 1. Asynchronous counter :



### 2. Synchronous counter :



## 23. Practical 10

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working

### Module 3

**Aim:** Study and implement a shift register.

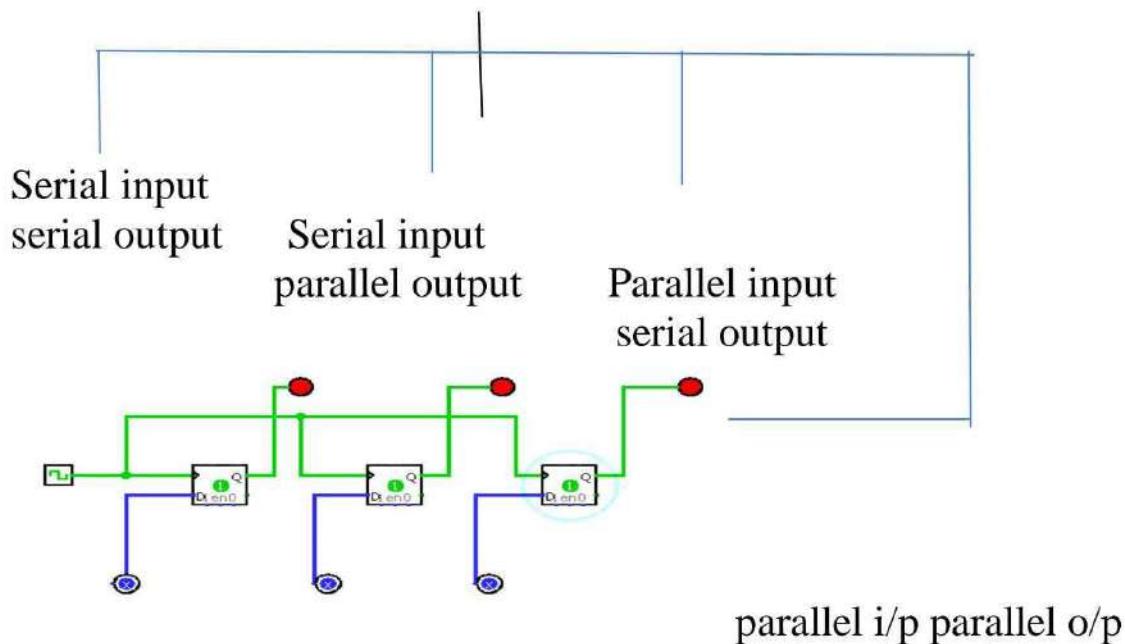
#### Code:

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

## SHIFT REGISTER

- It is a group of flip flops connected in series used to store multiple bits of data. the information stored within these registers can be transferred with the help of shift registers. A shift register is a group of flip-flops used to store multiple bits of data.

4 types are there :



## 24. Practical 11

**CO3:** Design and implement Combinational and Sequential logic circuits and verify its working

### Module 2

**Aim:** Study and implement K-Map for the given function:(SOP)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

**Code:**

Output snapshot: (In output include practical details and execution date & time with your enrollment number)

		$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$				
		CD \ AB	A'B'	A'B	AB	AB'
CD	AB	1				1
	A'B'			1		
	AB					
	AB'	1				1

**Answer :** SOP (F) =  $B'D' + ABC'D$