



Government Engineering College

Sec-28 Gandhinagar

Sem: - 3

Subject: - Digital Fundamental

Subject Code: - 3130704



Government Engineering College

Sec-28 Gandhinagar

Certificate

This is to certify that

Mr./Ms. Joshi Shubh Of class

.... 3rd Division ... A ..., Enrollment No. D2D06 Has

Satisfactorily completed his/her term work in

..... DF Subject for the term ending in

..... 6/1/2023

Date: -

Mehul

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department

Vision/Mission

Vision:

To be a Premier engineering institution, implying quality education of innovative solution relevant to society and environment

Mission:

- To develop human potential to its fullest extent so that intelligent and innovative engineers can emerge in wide range of professions
- To enhance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future
- To produce quality engineers, scientists and leaders to meet the present and future needs of society as well as environment

Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	Solve the given problem using fundamentals of Number system and Boolean algebra
CO-2	Analyze working of logic family and logic gate and design the suitable logic circuit for given function.
CO-3	Design and implement Combinational and sequential logic circuits and verify its working
CO-4	Examine the process of analog to digital conversion and Digital to Analog Conversion
CO-5	Implement PLDs for the given logical problem

7. Assignment Index

Sr. No	Assignment	Date	Page No.	Sign
1	Assignment 1	30/9/22		
2	Assignment 2	27/10/22		✓ 27/10/22
3	Assignment 3	30/11/22		✓ 30/11/22
4	Assignment 4	14/12/22		✓ 14/12/22
5	Assignment 5	30/12/22		✓ 30/12/22

8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1	13/9/22.		
2	Practical 2	24/9/22.		
3	Practical 3	4/10/22.		
4	Practical 4	11/10/22.		
5	Practical 5	18/10/22.		O
6	Practical 6	15/11/22		MWS
7	Practical 7	22/11/22.		
8	Practical 8	6/12/22		
9	Practical 9	7/12/22		
10	Practical 10	13/12/22.		
11	Practical 11	26/12/22.		



Government Engineering College, Gandhinagar

**Computer Engineering
B.E. Semester III
(AY 2021-22)**

SUBJECT: Digital Fundamental (3130704)

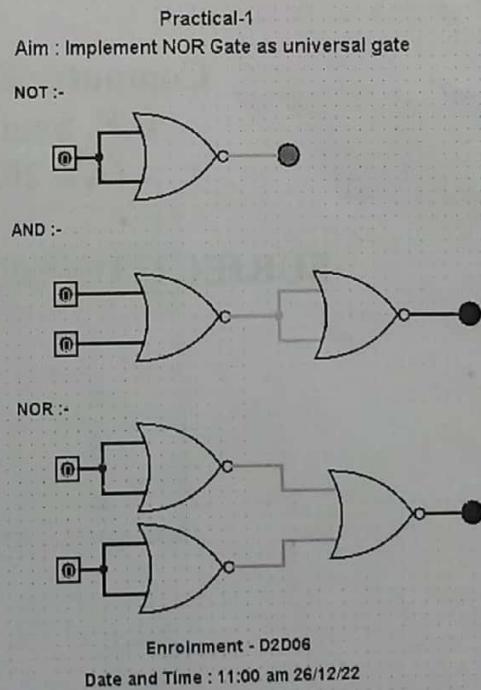
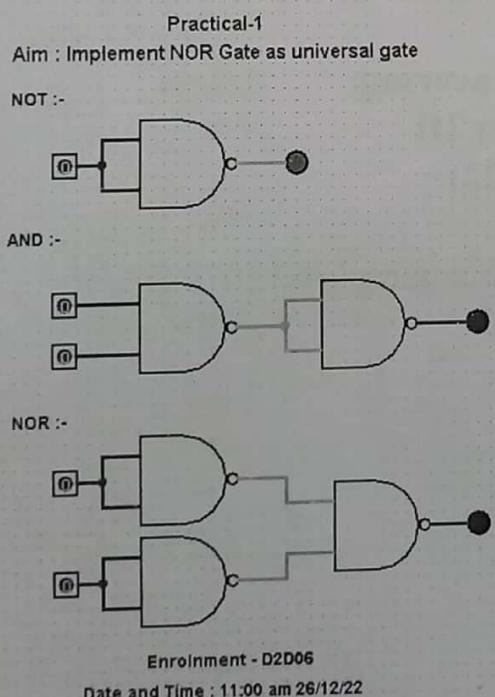
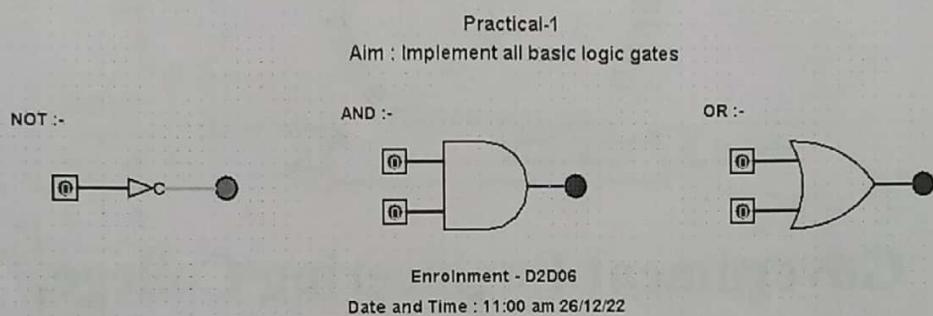
14.Practical 1

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

Module 1

Aim: Getting familiar with Logisim, Study and implement all basic logic gates.
Implement NAND and NOR logic gates as universal gates.

Code:

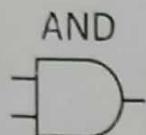


Brief Explanation & Truth Tables:

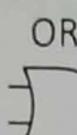
In an OR gate, the output of an OR gate attains state 1 if one or more inputs attain state 1.

In the AND gate, the output of an AND gate attains state 1 if and only if all the inputs are in state 1.

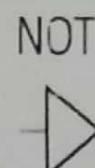
In a NOT gate, the output of a NOT gate attains state 1 if and only if the input does not attain state 1.



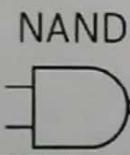
INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1



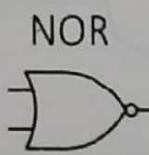
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1



INPUT		OUTPUT
A		
0		1
1		0



INPUT		OUTPUT
A	B	
0	0	1
1	0	1
0	1	1
1	1	0



INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

Mehdi

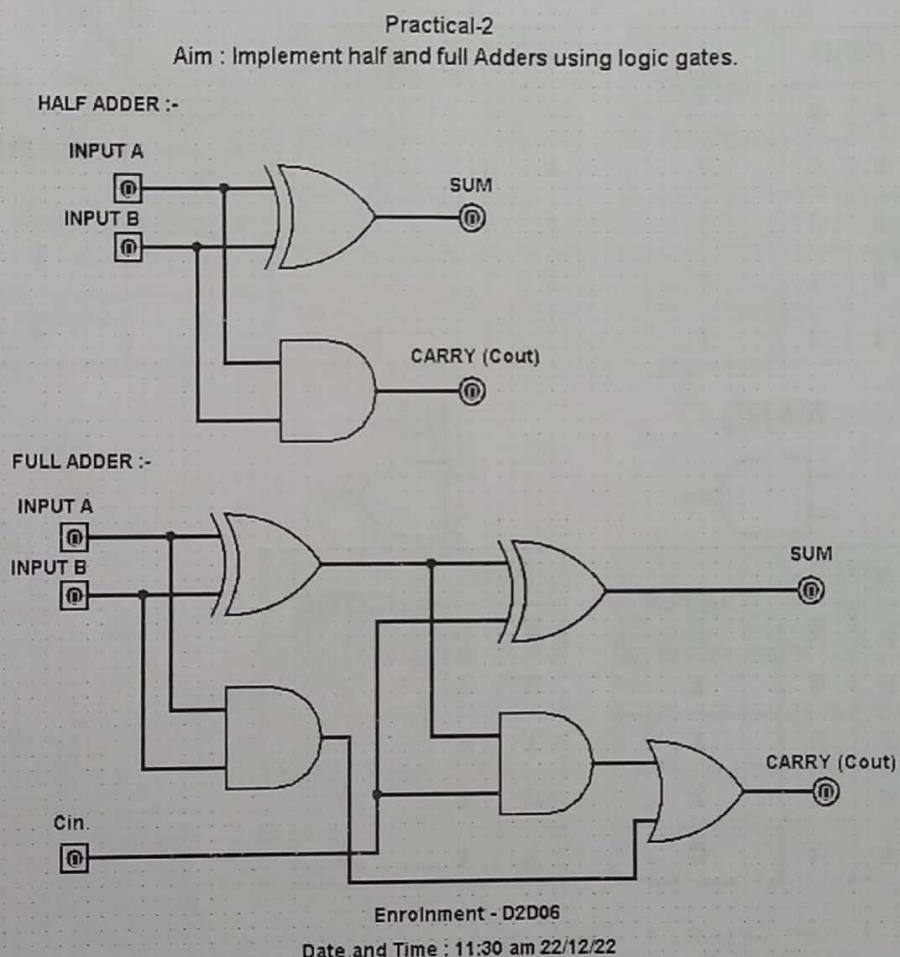
15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Adders using logic gates.

Code:



Brief Explanation & Truth Tables:

A half-adder circuit consists of two input terminals- namely A and B. Both of these add two input digits (one-bit numbers) and generate the output in the form of a carry and a sum.

Input		Output	
A	B	CARRY	SUM
0	0	0	0
1	1	1	0
0	1	0	1
1	0	0	1

The full adder adds three binary digits. Among all the three, one is the carry that we obtain from the previous addition as C-IN, and the two are inputs A and B. It designates the input carry as the C-OUT and the normal output as S

Input			Output	
A	B	C	SUM	CARRY OUT
0	0	0	0	0
1	1	1	1	1
0	1	1	0	1
1	0	1	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

Muzib

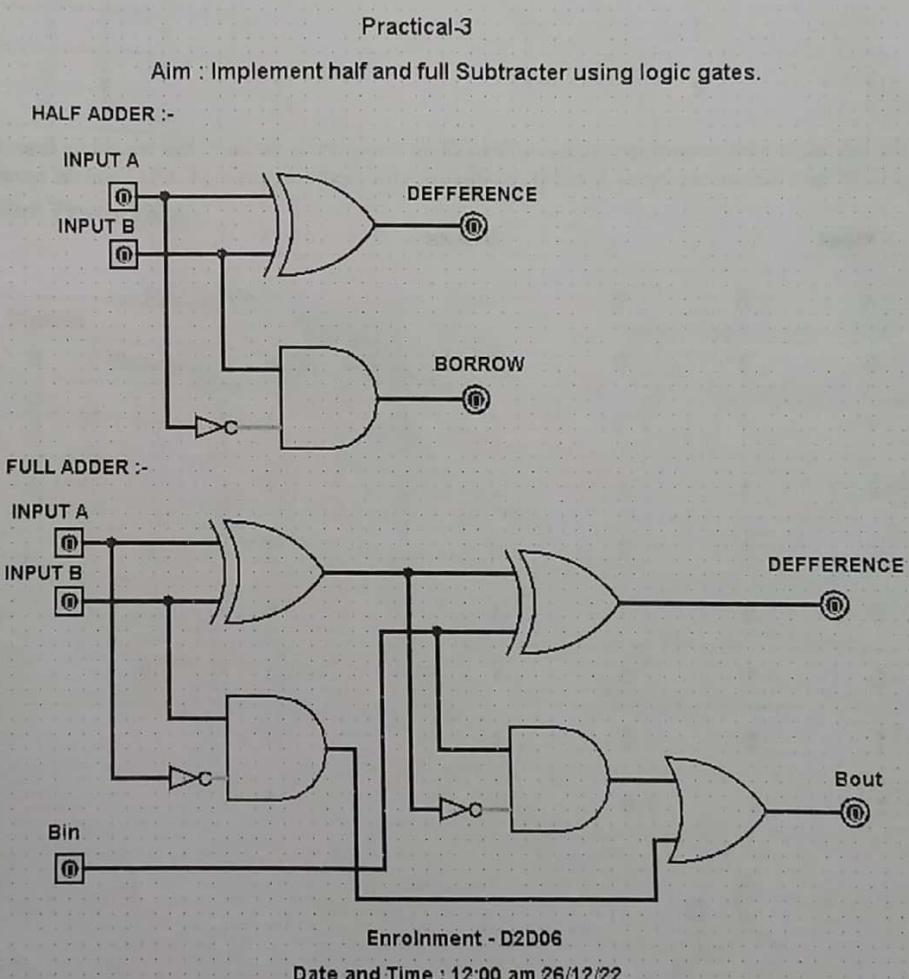
16. Practical 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Subtractors using logic gates.

Code:



Brief Explanation & Truth Tables:

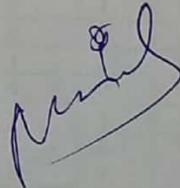
The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively.

Half Subtractor Truth Tables:

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor Truth Table:

Inputs			Outputs	
A	B	Borrow _{in}	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



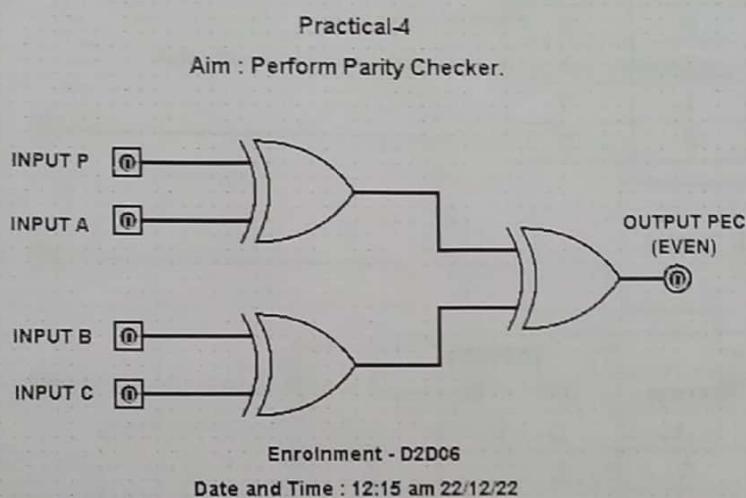
17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Perform Parity Checker

Code:



D ₃	D ₂	D ₁	D ₀	Even-parity P	Odd-parity P
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

18. Practical 5

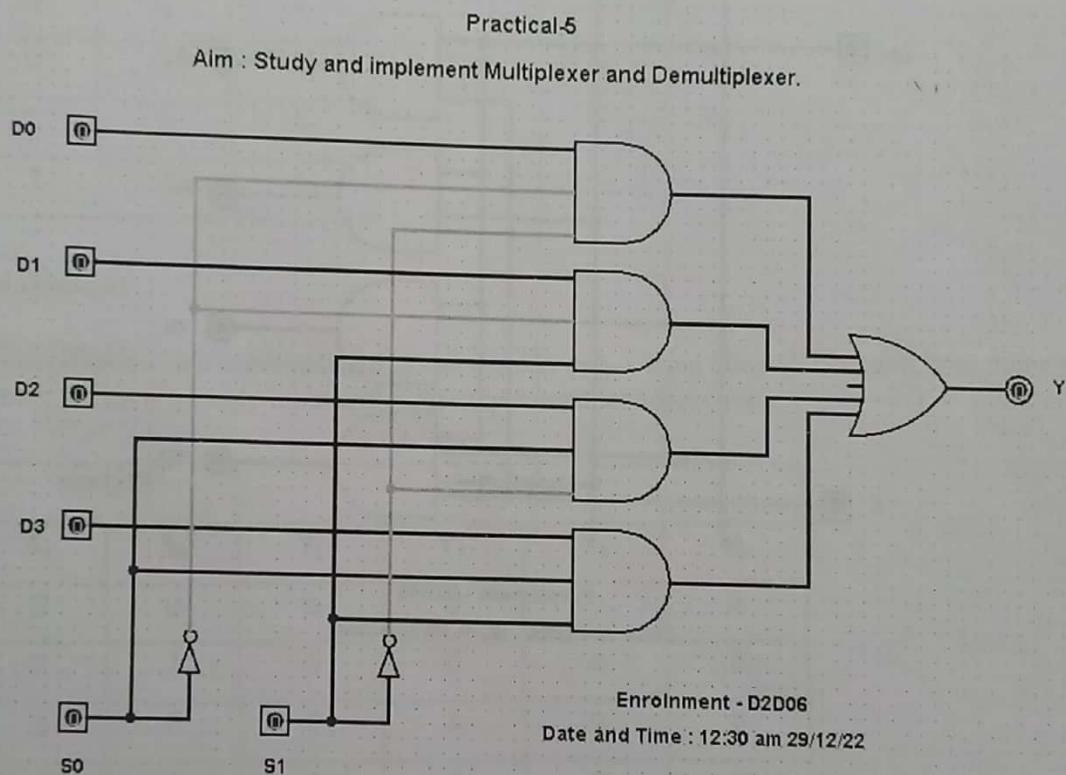
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement Multiplexer and Demultiplexer.

Code:

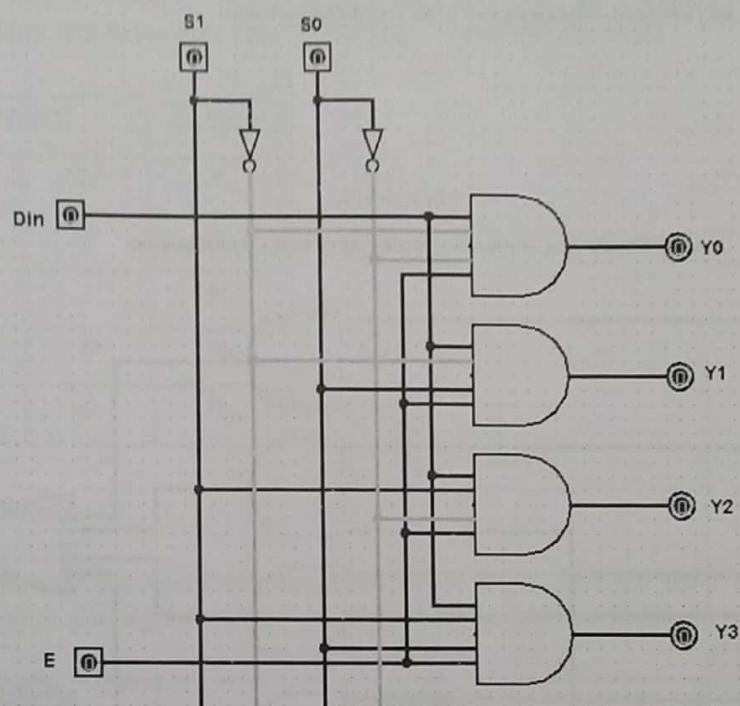
4:1 Multiplexer



1:4 Demultiplexer

Practical-5

Aim : Study and implement Multiplexer and Demultiplexer.



Enrolment - D2D05

Date and Time : 12:30 am 29/12/22

Brief Explanation & Truth Tables:

Multiplexer:

A multiplexer is a combinational circuit that has 2^n input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit.

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Demultiplexer:

A De-multiplexer is a combinational circuit that has only 1 input line and 2^N output lines. Simply, the multiplexer is a single-input and multi-output combinational circuit.

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

Manish

19. Practical 6

CO3: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

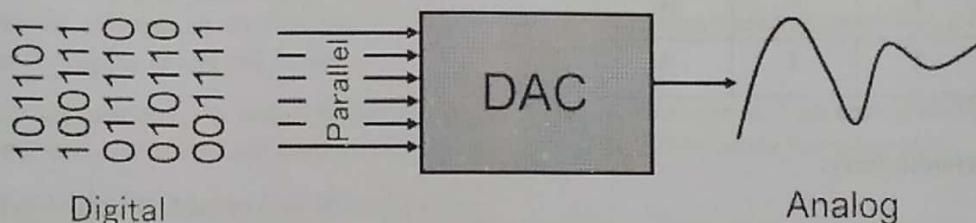
Module 2

Aim: Study and configure A to D convertor and D to A convertor.

What is Analog to Digital Converter?

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.

- Analog signals are directly measurable quantities.
- Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.



Application of Analog to Digital Converter:

ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.

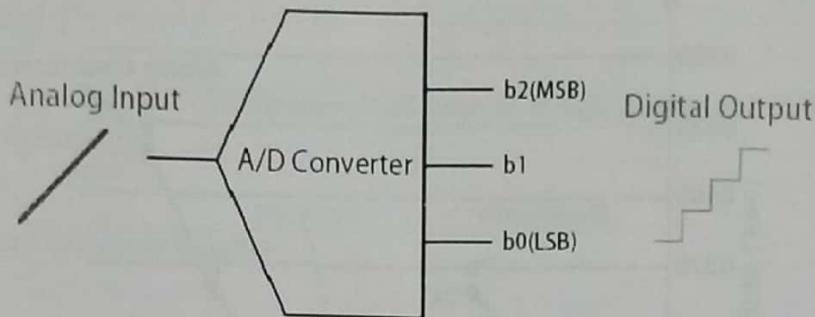
- Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.
- Microcontrollers commonly use 8, 10, 12, or 16-bit ADCs, our micro controller uses an 8 or 10-bit ADC

Types of Analog to Converters (ADC):

- Successive Approximation A/D Converter
- Flash A/D Converter
- Delta-Sigma A/D Converter

What is a Digital to Analog Converter?

Digital to analog converting is a process where digital signals that have a few (usually two) defined states are turned into analog signals, which have a theoretically infinite number of states. A Digital to Analog Converter, or DAC, is an electronic device that converts a digital code to an analog signal such as a voltage, current, or electric charge. Signals can easily be stored and transmitted in digital form; a DAC is used for the signal to be recognized by human senses or non-digital systems. Converting a signal from digital to analog can degrade the signal.



Applications for Digital to Analog Converters:

An example can be found in the processing of computer data by a modem into audio-frequency tones transmitted over a telephone line. The circuit that performs this is a digital to analog converter. In music players, digital to analog converters can be used for generation of audio signals from digital information. In TVs and cell phones, digital video signals are converted into analog in order to display colors and shades.

In VoIP applications, the source is first digitized for transmission through an analog to digital converter and is then reconstructed into an analog signal using a DAC at the receiving end.

Types of Digital to Analog Converter (DAC):

- Binary Weighted Resistor D/A Converter Circuit
- Binary ladder or R-2R ladder D/A Converter Circuit
- Segmented DAC
- Delta-Sigma DAC

Analog Signal to Digital Signal Conversion Methods:

1. Sampling:

Sampling is the process of taking amplitude values of the continuous analog signal at discrete time intervals (sampling period T_s).

[Sampling Period $T_s = 1/F_s$ (Sampling Frequency)]

Sampling is performed using a Sample and Hold (S&H) circuit.

2. Quantization:

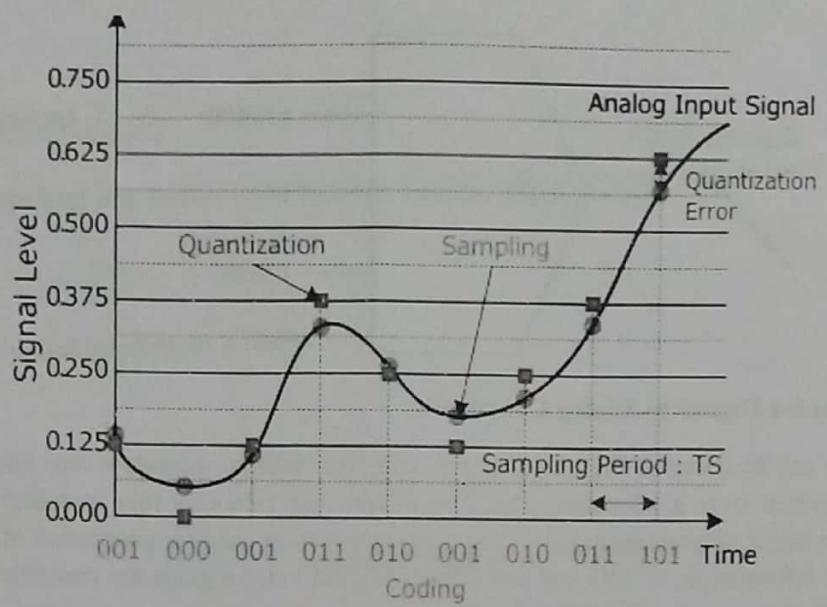
Quantization involves assigning a numerical value to each sampled amplitude value from a range of possible values covering the entire amplitude range (based on the number of bits).

[Quantization error: Sampled Value - Quantized Value]

3. Coding:

Once the amplitude values have been quantized they are encoded into binary using an Encoder.

Mohd



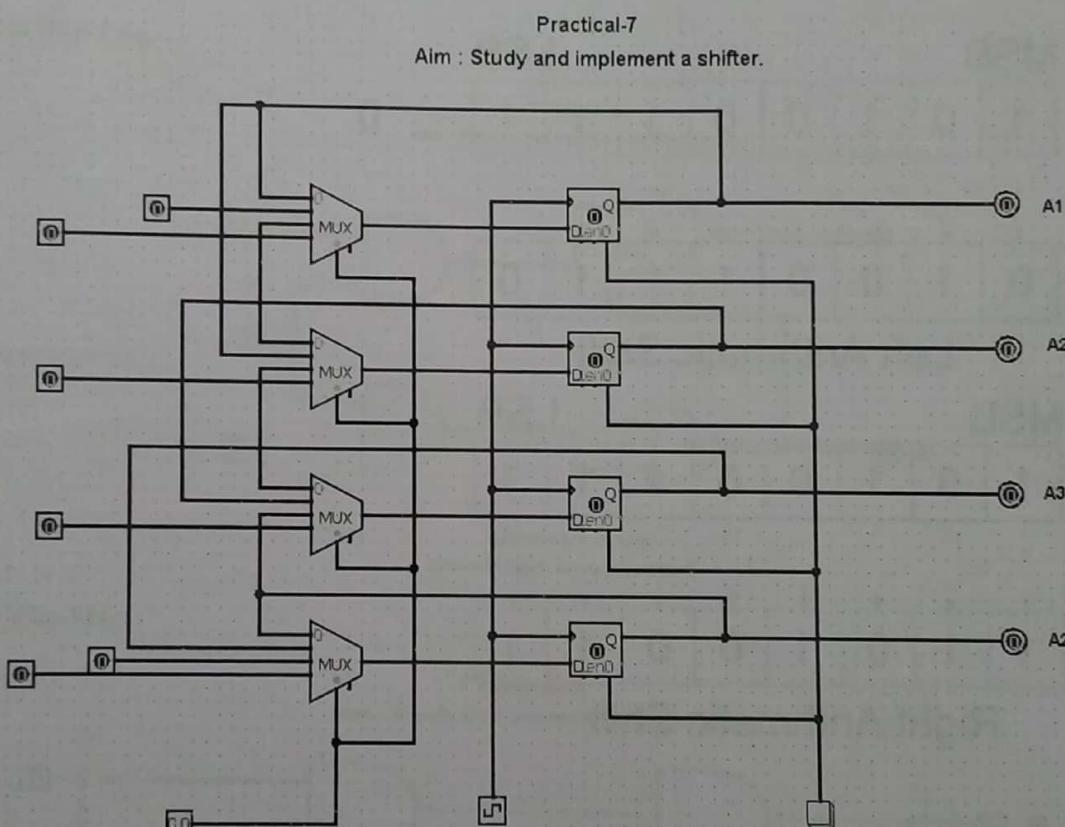
20. Practical 7

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement a shifter.

Code:



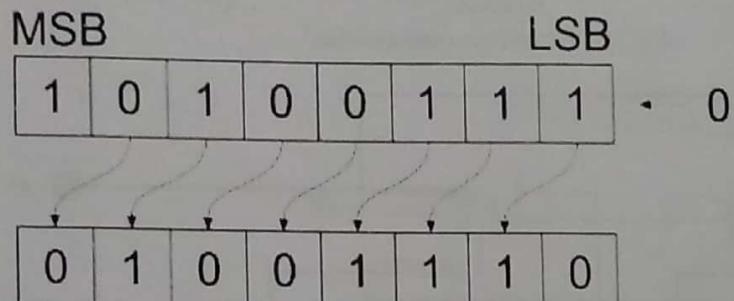
Enrolment - D2D06

Date and Time : 01:00 pm 21/12/22

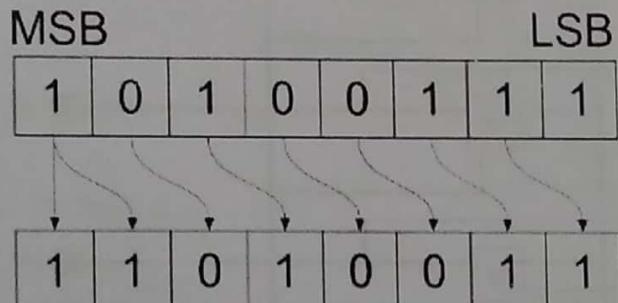
Brief Explanation & Truth Tables:

Arithmetic Shifter : is the same as a logical shifter, but on right shifts fills the most significant bits with a copy of the old most significant bit (MSB). This is useful for multiplying and dividing signed numbers Arithmetic shift left (ASL) is the same as logical shift left (LSL).

Truth Table:



Left Arithmetic Shift



Right Arithmetic Shift

21. Practical 8

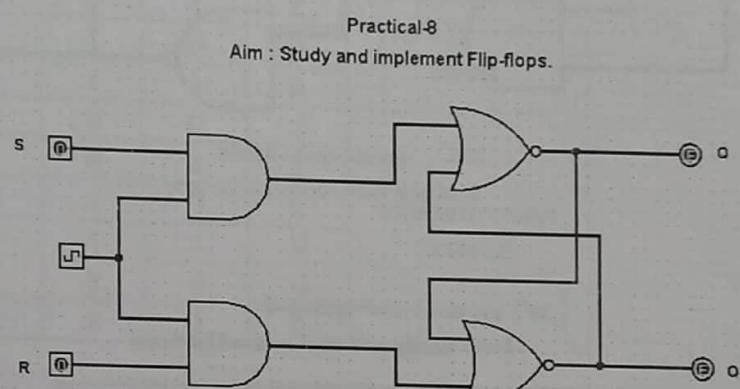
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

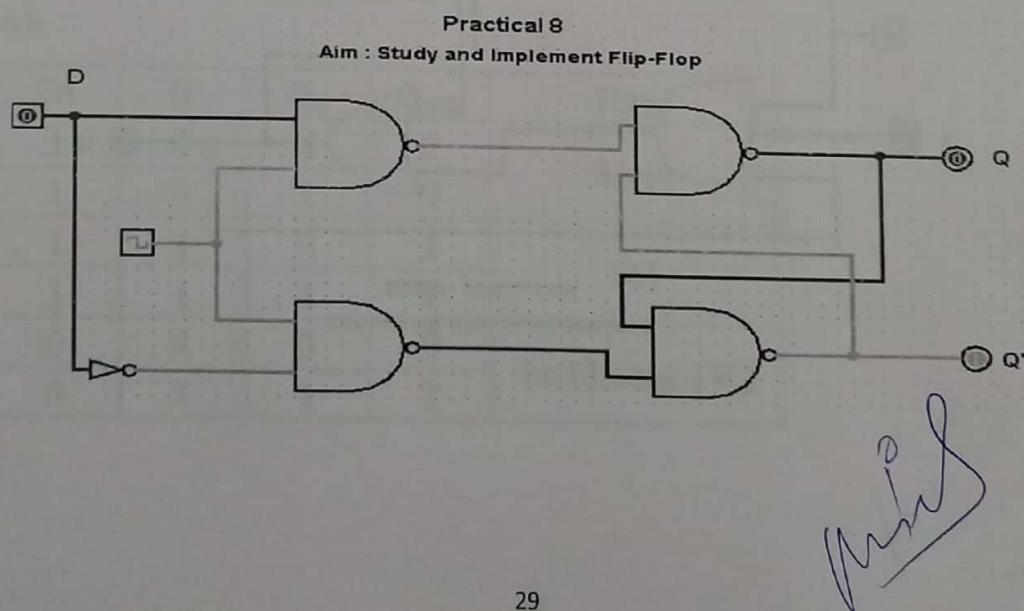
Aim: Study and implement Flip-flops.

Code:

SR Flip Flop



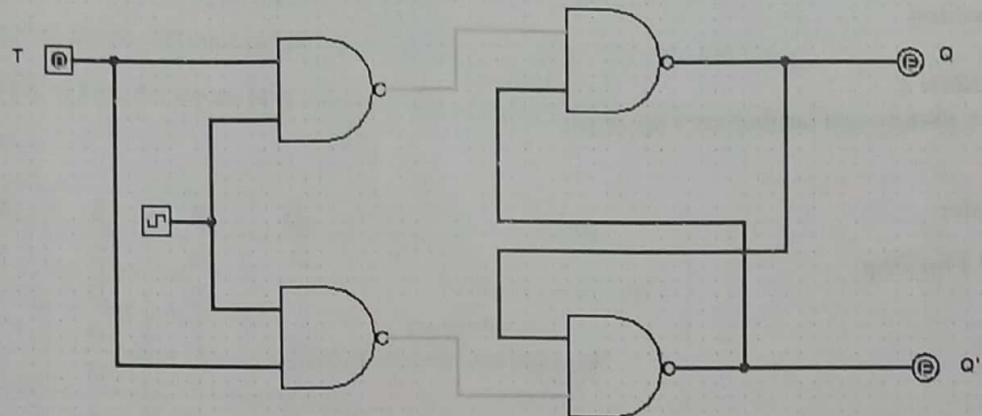
D Flip Flop



T Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



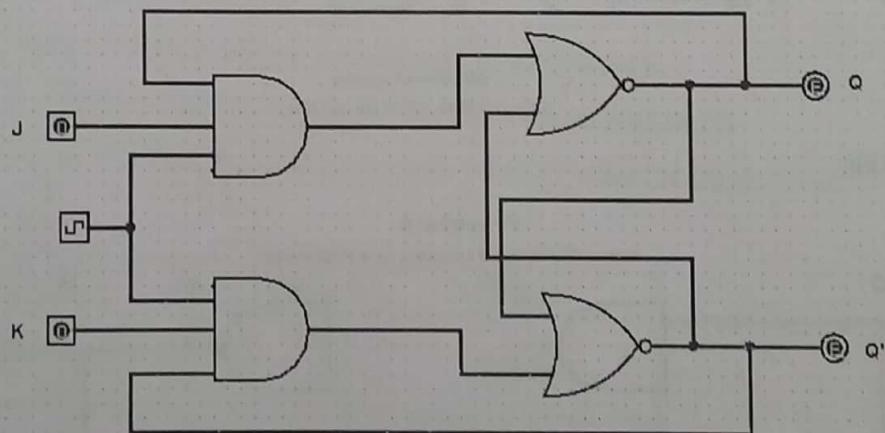
Enrolment - D2D06

Date and Time : 05:00 pm 22/12/22

JK Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



Enrolment - D2D06

Date and Time : 05:00 pm 29/12/22

Brief Explanation & Truth Tables:

SR Flip Flop

A gated SR latch requires an Enable (EN) input.

Its S and R inputs will control the state of the flip flop only when the EN is high.

When EN is low, the inputs become ineffective and no change of state can take place. Truth Table

En	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate (Invalid)
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

D Flip Flop

It differs from the S-R latch in that has only one input in addition to EN.

When D=1, we have S=1 and R=0, causing the latch to SET when ENABLED

When D=0, we have S=0 and R=1, causing the latch to RESET when ENABLED Truth

Table

En	D	Q_n	Q_{n+1}	State
1	0	0	0	
1	0	1	0	Reset
1	1	0	1	
1	1	1	1	Set
0	X	0	0	
0	X	1	1	No Change (NC)

JK Flip Flop

The JK flip flop is very versatile and also the most widely used.

The functioning of the JK flip flop is identical to that of the SR flip flop, except that it has no invalid state like that of SR flip flop.

Truth Table

En	J	K	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	
1	0	1	1	0	Reset
1	1	0	0	1	
1	1	0	1	1	Set
1	1	1	0	1	
1	1	1	1	0	Toggle
0	X	X	0	0	
0	X	X	1	1	No Change (NC)

T Flip Flop

A T flip flop has a single control input, labeled T for toggle.

When T is HIGH the flip flop toggles on every new clock pulse.

When T is LOW the flip flop remains in whatever state it was before.

Truth Table

En	T	Q_n	Q_{n+1}	State
1	0	0	0	No Change (NC)
1	0	1	1	
1	1	0	1	
1	1	1	0	Toggle
0	X	0	0	
0	X	1	1	No Change (NC)

22. Practical 9

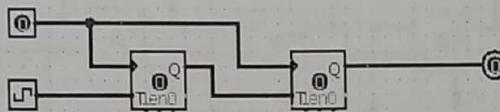
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

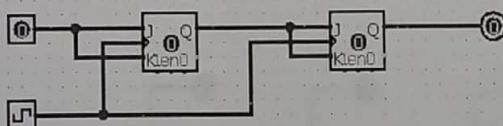
Aim: Study and Implement Counter

Code:

Practical 9
Aim : Study and implement Counter



Enrollment No : D2D06
Date and Time : 05:00am 28/12/2022



Brief Explanation & Truth Tables:

Asynchronous Counter

The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle(T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic

External clock is applied to the clock input of flip-flop A and Q A output is applied To the clock input of the next flip-flop.

10
mark

Synchronous Counter

If the "Clock" pulses are applied to all the flip flop in counter simultaneously, Then such a counters are called synchronous counter.

In this type of counter there is no connection between the output of first FF and clock input of next FF and so on.

23. Practical 10

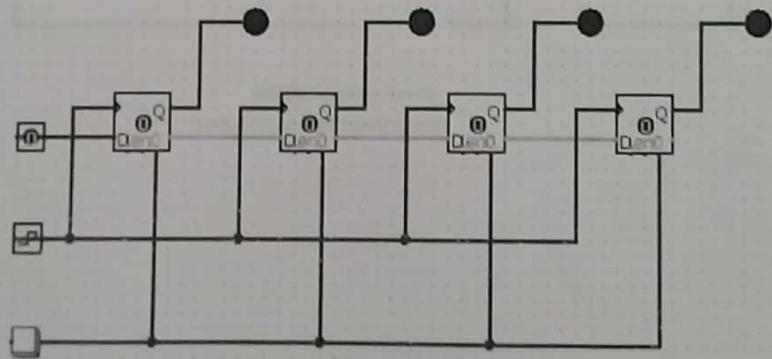
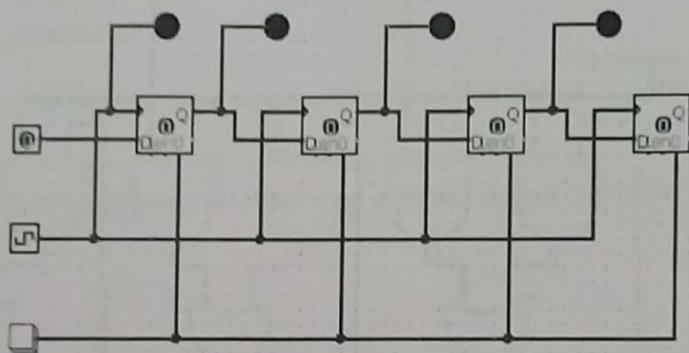
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

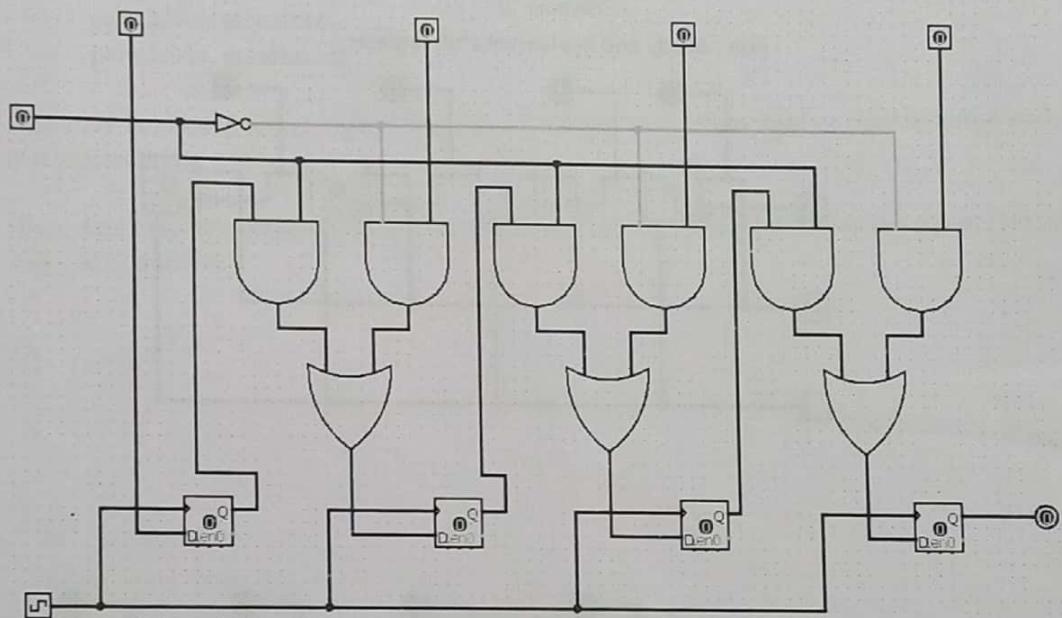
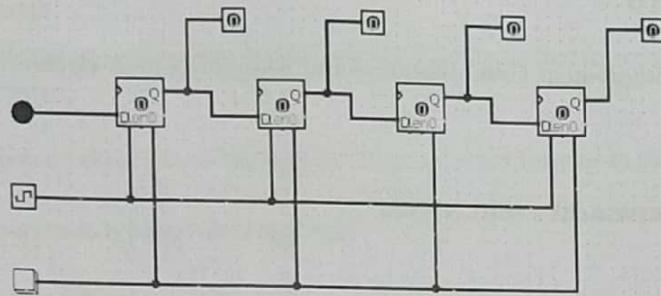
Module 3

Aim: Study and Implement a shift register

Code:

Practical 10
Aim : Study and implement shift register





Enroll number : D2D06

Date & time: 05:22am 28/12/2022

Brief Explanation:

A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.

Data may be shifted into or out of the register either in serial form or in parallel form.

So, there are four basic types of shift registers:

- serial-in, serial-out
- serial-in, parallel-out
- parallel-in, serial-out
- parallel-in, parallel-out

Data may be rotated left or right. Data may be shifted from left to right or right to left at will, i.e. in a bidirectional way.

Also, data may be shifted in serially (in either way) or in parallel and shifted out serially (in either way) or in parallel.

Muzahid

24. Practical 11

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and Implement K-Map for the given function:(SOP)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

Code:

Step 1: Finding the number of variables to build the K-map

$$\text{Number of variables} = 4(A,B,C,D)$$

So 4 variable K-map is to be used

Step 2: Filling cells of K-map for SOP with 1 respective to the min-terms for given equation

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	0	1	3	4	
	01	4	5	7	6	
	11	12	13	15	14	
	10	8	9	11	10	

Step 3: We create rectangular groups that contain total terms in the power of two like 2,4,8 and so on. Try to cover as many elements as we can cover in one group.

		CD	00	01	11	10
		AB	00	01	11	10
			1	0	1	3
			4	5	7	6
			12	13	15	14
			1	8	9	11
						1 10

Step 4: With the help of these groups, we find the product terms and sum of them for the SOP form

$$Y = ABC'D + B'D'$$

9. Assignment 1

CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra

Module 1

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function: $F = A'B'C + A'BC + AB'$.
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

Assignment - 2

Module - 2

(Q.2)

De Morgan suggested two theorems that form an important part of Boolean algebra

$$2. \bar{AB} = \bar{A} + \bar{B}$$

The complement of a product is equal to the sum of its complements

Truth Table:	A	B	\bar{AB}	$\bar{A} + \bar{B}$
	0	0	1	1
	0	1	1	1
	1	0	1	1
	1	1	0	0

2. $\bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$

The complement of a sum is equal to the product of its complements

Truth Table:	A	B	$\bar{A} + \bar{B}$	$\bar{A} \cdot \bar{B}$
	0	1	1	1
	0	0	0	0
	1	1	0	0
	1	0	0	0

Q.2 $f = \bar{ABC} + \bar{A}BC + AB\bar{C}$

$$= \bar{B}C(\bar{A} + B) + AB\bar{C}$$

$$= \bar{B}C + AB\bar{C}$$

$$\boxed{f = \bar{B}C + AB\bar{C}}$$

Q3 Logic families are divided in two parts

→ Bipolar

(a) Saturated

(i) Register Transfer logic (RTL)

(ii) Diode Register logic (DRL)

(iii) Direct coupled logic (DCL)

(iv) Integrated Injection logic (I²L)

(v) High Threshold logic (HTL)

(vi) Transistor Transfer logic (TTL)

(b) Unsaturated

(i) Schottky TTL

(ii) Emitter coupled logic (ECL)

(c) Unipolar

(i) P-channel MOSFET (PMOS)

(ii) n-channel MOSFET (NMOS)

(iii) Complementary MOSFET (CMOS)

→ It is a group of configurable ICs with the same logic level and supply voltage for performing various logic functions. They are fabricated using a specific circuit configuration called a field as a logic family. The circuit design of the basic gate of each logic family is the same.

Transistor-Transfer logic (TTL): It is a general term for its dependence on transistors alone to perform basic logic operations.

Q3

logic families are divided in two parts

(i) Bipolar

(a) Saturated

(i) Register Transfer logic (RTL)

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(2) Unipolar

(a) P-channel MOSFET (PMOS)

(b) n-channel MOSFET (NMOS)

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→ It is a group of compatible ICs with the same logic level and supply voltage for performing various logic functions. They are fabricated using a specific circuit configuration which is referred as a logic family. The circuit design of the basic gate of each logic family is the same.

Transistor-Transistor logic (TTL); It is a name for its dependence on transistors alone to perform basic logic operations

schottky TTL: A schottky transistor along with a combination of a diode and a schottky diode that prevents the transistor from saturating by diverting the excessive input current. It is also called schottky-transistor.

CMOS: Complementary metal oxide semi conductor is a type of metal oxide semi conductor. It uses ESD (Electrostatic Discharge) protection. It is a fabrication process that uses complementary and symmetrical layers of p-type and n-type MOSTET's for logic functions.

- Q4) Describe error detecting & correcting code
- To monitor the data integrity between transmitter & receiver, extra bits are added. These bits are called check bits. If the received data is correct, then no error is present in the data. If the data is wrong, then an error is present. Check bits form the codes. Codes which allow only error detection are called error detection codes and codes which can correct errors are called error correcting codes.

→ parity code

Even parity code: The value of even parity bit should be zero, if even number of ones present in the binary code. Otherwise, it should be one so that even number of ones present in even parity code.

Binary code Two parity bit Four parity code

000	0	0000
001	1	0011
010	1	0101
011	0	0110
100	1	1001
1000	0	
1001	0	1010
110	0	1100
111	1	1111

odd parity code

Binary code odd parity bit odd parity code

000	1	0001
001	0	0010
010	0	01100
011	1	10000111
100	0	1011000
101	1	1011
110	1	1101
111	0	1110

→ Hamming code

Hamming code is useful for both detection and correction of errors present in the received data. This code uses multiple parity bits and we have to place other parity bits in the register of fewer or 2

Bit designation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁
Bit location	7	6	5	4	3	2	1
Binary location number	111	110	101	100	011	010	001

- Parity P₃ checks bit locations 1, 3, 5, 7 and assigns P₃ accordingly to even or odd parity
- Parity P₂ checks bit locations 2, 3, 6, 7 and assigns P₂ accordingly to even or odd parity
- Parity P₁ checks bit locations 4, 5, 6, 7 and assigns P₁ accordingly to even or odd parity

Q5 Difference TTL, schottky-TTL and CMOS

Parameter	CMOS	TTL	Schottky
Device used	n-channel & p-channel	Bipolar JFET	Schottky diodes
V _H (min)	5V	2V	2V
V _L (max)	2.3V	0.8V	0.8V
V _{ON} (min)	2.95V	2.2V	2.2V
V _O (max)	0.05V	0.4V	0.3V
Power dissipation (max)	0.1 mW	10 mW	1 mW
Input current	0.50	2A	50
Applicable voltage range	and gate-to-emitter voltage	valleys clamping	cycle time to
	and gate-to-base voltage	emit-base to	emit-drain
	supply current	saturation	

10. Assignment 2

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem

Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
 - 2.1. $F(x,y,z) = \Sigma(2,3,6,7)$
 - 2.2. $F(A,B,C,D) = \Sigma(4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

Assignment-2

Module-2

Q1

Q1: The K-map method gives us a systematic approach for solving a Boolean expression.

The basis of this method is a graphical chart known as Karnaugh map (K-map).

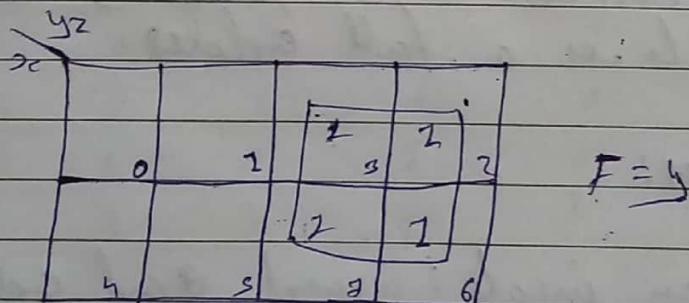
It contains four cells called cell.

A	B	00	01	11	10
0	0	0	1	1	0
1	1	1	0	0	1

C	D	000	001	111	110
0	0	0	1	1	0
1	1	1	0	0	1

E	F	0000	0001	0111	0110
0	0	0	1	1	0
1	1	1	0	0	1

Q2 $F(x, y, z) = \Sigma(2, 3, 6, 7)$



$$2.2 \quad F(A, B, C, D) = \Sigma(0, 6, 7, 15)$$

	00	02	12	10
00	0	2	3	2
02	1	7	2	6
12	12	13	13	12
10	8	9	11	10

$$F = \bar{A}B\bar{D} + BCD$$

a3

- **D adder:** The logic circuit which performs addition of two 1-bits is a full adder.

- The logic circuit which performs addition of three 1-bits is a full adder.

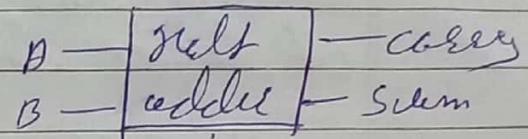
• **Half Adder:**

- Two binary inputs: carry-in and addend bits
- two binary outputs: sum and carry

Truth Table

block diagram

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



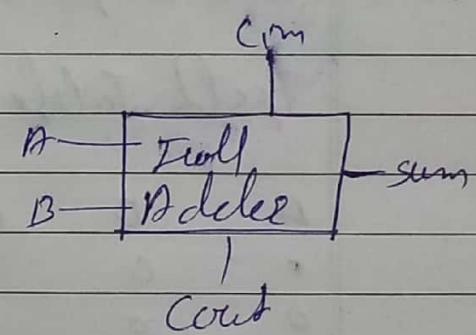
- Full Adder

- Three binary inputs (carry, addend and receiver)
- Two binary output : sum and carry

Truth Table

A	B	Cin	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

block diagram



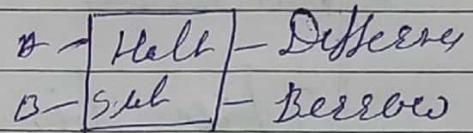
- Subtraction

A half subtractor is combined circuit that subtract two bits and produce their difference.

A full subtractor is called circuit that subtracts between two bits taking into account borrow at lower bit by

Truth Table

A	B	Diffall	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

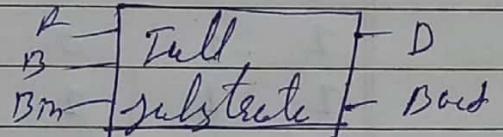


Full subtractor

- Three inputs: Minuend, subtrahend & borrow in
- Two outputs: difference & borrow out

Truth Table

A	B	B _n	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
1	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Q4

Ans

Multiplexer:

To select single data line from several data input lines, and the data is given. The selected data line should be available on the output. The digital circuit which does this task is a multiplexer.

21 Multiplexers

- D_0 is applied as an input to one DND gate & D_1 is applied as an input to another DND gate.
- Enable input is applied to both gates as one input.
- Selection line S is connected to second input to second DND gate. In unselected S is the second input to first DND gate.

Function Table

E	S	0	1	Data inputs	0	1	2	3	out
1	0	D_0		inputs	0				
1	1	D_1		Enable	1				
0	1	0		enable	E	S			

Select input

as

Q:- A parity bit is used for the purpose of detecting errors during transmission of binary information.

- > The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.
- parity checker Truth Table for even and odd parity

A	B	C	odd parity bit	Even parity bit
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

- parity checked

The other bits in the message symbols with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit.

* Truth Table for even parity checker

Decomposed P A B C parity checker
means check (PAC)

0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

fix

11. Assignment 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 3

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

Assignment - 3

Module - 3

Q 2

Combinational
Circuits

- In Combinational circuit, The output variables are at all times depended on the combination of input variables.

Easy to design

parallel adder is a
Combinational Circuit

Faster in speed

sequential
circuit

- In sequential circuits, if one gets variables depend not only on the present input result but they also depend upon the history of other input variables.

Harder to design

Serial adder is a
sequential circuit

slower than combinational
circuits

Q 2

- > Filet Slots are:
 - 1) J1c Flytter
 - 2) D Flytten
 - 3) T Flytbyg
 - 4) SR Flytflot

1) JK Flipflop

The data inputs are J & K which are ANDed with Q and \bar{Q} respectively, the outputs are Q and \bar{Q} inputs.

Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	\bar{Q}_n
1	0	\bar{Q}_n
1	1	\bar{Q}_n

2) D Flipflop:

Input contention can be avoided by making them complements of each other. The modified SR flipflop is known as D flipflop.

Truth Table

C	R	D	Q_{n+1}
1	0	0	0
1	1	1	1
0	1	Q _n	

3) T Flipflop

T flipflop is also known as "Toggle flipflop".

- modification of JK flip-flop

Truth Table

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

w) SR Edge flip-flop

The circuit is similar to SR latch except enable signal is replaced by the clock pulse followed by the positive edge detector circuit.

→ The edge detector circuit is a different kind Truth Table

CP	S	R	Ans
0	0	0	0n
↑	0	0	hold
↑	0	1	·0
↑	1	0	2
↑	1	1	invalid

C₃

- Q1:
- 1) D flip-flop
 - 2) Clocked D flip-flop
 - 3) Left register

1) D flip-flop

- Contains only four D flip-flops. Other registers are called latches
- Each D flip-flop is triggered with a common negative edge clock pulse
- N input bits set up the latches for clocking

3) Shift Registers

- The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulse.

The type of shift register or shifter is chosen for certain arithmetic and logic operations used in microprocessors. They may also be a group of registers called "shift register".

4) Ring Counter

- The Q output of each stage is connected to the D inputs of the next stage and the output of last stage feedback to the input of first stage.
- The CLR followed by PRE makes the outputs of first stage i.e. Q_1 and Q_2 having outputs all zero i.e. QA is 0 and QB, QC are zero.
- The first clock pulse produces $Q_3 = 1$ and remaining outputs are zero.
- The first clock pulse produces $Q_4 = 1$ and remaining outputs are zero.

Q5

Ans

steps involved in the design of asynchronous counter

- 1) Determine the number of flipflop needed
- 2) choose the type of flipflop to be used. T or J-K
If T flipflops are used. Connect J input of all flipflops to logic 1 if JK flipflops are used connect both J & K inputs of all J-K flipflops to logic 1 such connection toggles
- 3) write the state table for the counter
- 4) derive the next logic by K-map simplification
- 5) draw the logic diagram

Ans

12. Assignment 4

CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 4

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

Assignment - 4

Module - 4

A2.

Q1: Weighted Register Converter. A weighted DAC produces an analog output, which is almost equal to the digital (binary) input by using binary weighted resistors in the inverting adder circuits. In short, a binary weighted register converter DAC is called as weighted Register DAC.

→ For ON switch $I = \frac{V_R}{R}$ and

For OFF switch $I = 0$

→ Due to digit input selection of exp-amp summing current will flow through R_P . Hence the total current through n nodes can be given as

$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

when $R_f = R \cdot V_o$ is given as

$$V_{o2} = V_R (b_1 b_2^{-1} + b_2 b_3^{-1} + b_3 b_4^{-1} + \dots + b_n)$$

Q2

Q2: $n/2^n$ adder D/A converter used only two registers values. This avoids cascade spread drawback of binary weighted D/A converter.

- > easier to build accurately as only four precision op-amps
- > number of bits can be expanded by adding more series of same R/P ratios
- > In inverted R/P ladder, node voltage across capacitors will change except at every word
- > They avoid any slowdown effects by using comparators

Q3

- > Specification of D/A converter:
- > Resolution
- > Smallest change that occurs in an analog output as a result of a change in the digital output
- > 1. resolution = step size / full scale = 1/1000
- > Full scale = No. of steps × step size
- > Accuracy = specified in terms of full scale error and linearity error

3) Setting time

- The time required for the analog output to settle to within $\pm 1\%$ of its final value after a change in the digital input

4) Monotonicity

- This means that the analog output will have to change less as the binary input is converted from 0 to full scale.

5) Input-referred Sensitivity

- The \pm relay-output voltage for my first digital input varies with frequency

• Specifications of P/D converter:

1) Range of input voltage

2) Input impedance

3) Accuracy

4) Conversion Time

5) Format of digital output

A4

→ Quantizing / Encoding

The process of mapping the input analog voltage to discrete voltage levels, which are then represented by binary number (bits)

$$q = \frac{V_{max} - V_{min}}{2^n} = \frac{2 - 0}{8} = 0.25V$$

The value of q is more formally called the quantizer's resolution

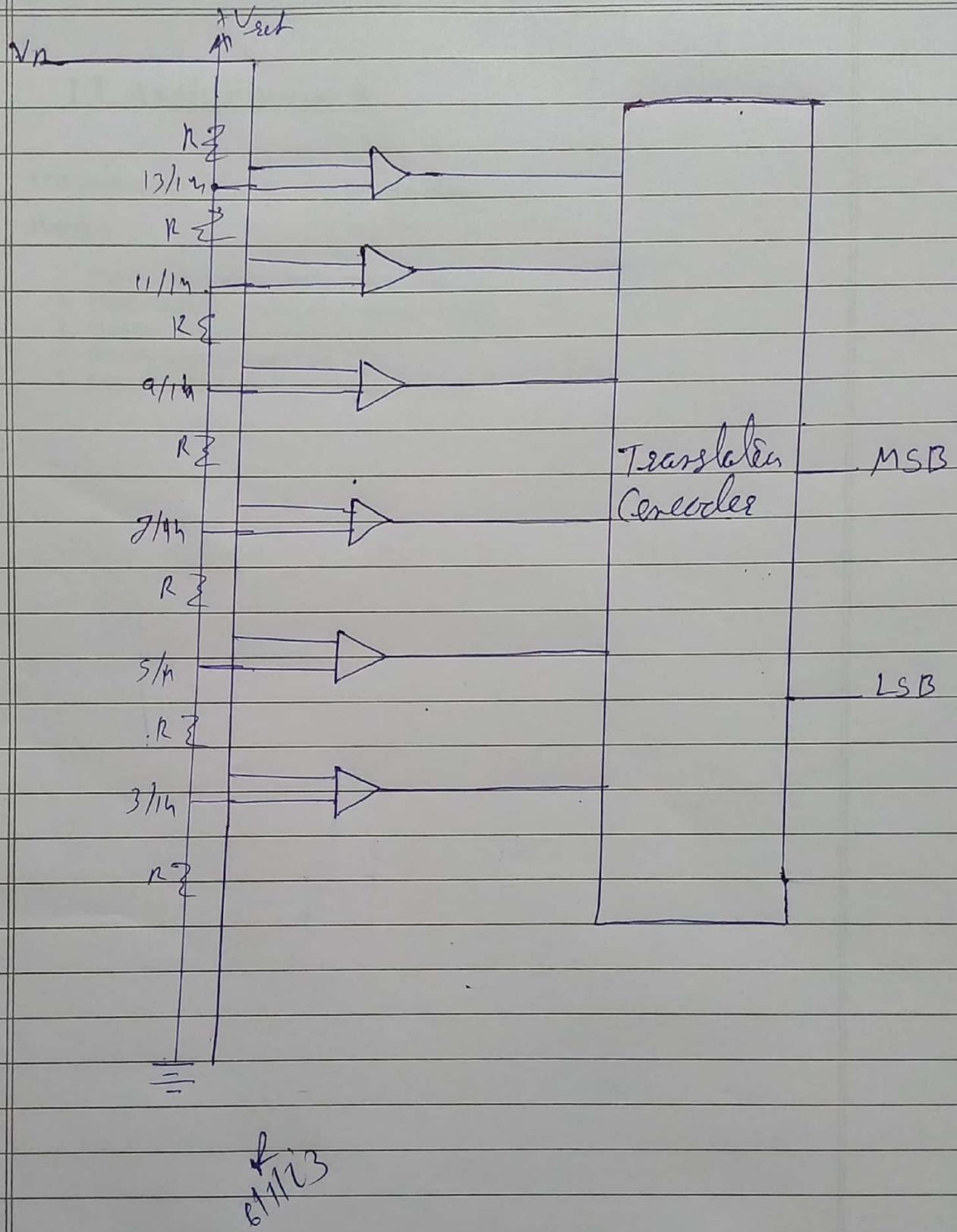
A5

→ The circuit is based of a series of comparators each one comparing the input signal to a unique reference voltage. The comparators output controls the output of a parallel encoder circuit which then produces binary output.

→ Based on the principle of comparing analog input voltage with a set of reference voltage

→ To convert the analog input voltage into a digital signal of n -bit output, ($\approx 2^n - 1$) comparators are required

→ Comparator as single end can be design



13. Assignment 5

CO5: Implement PLDs for the given logical problem.

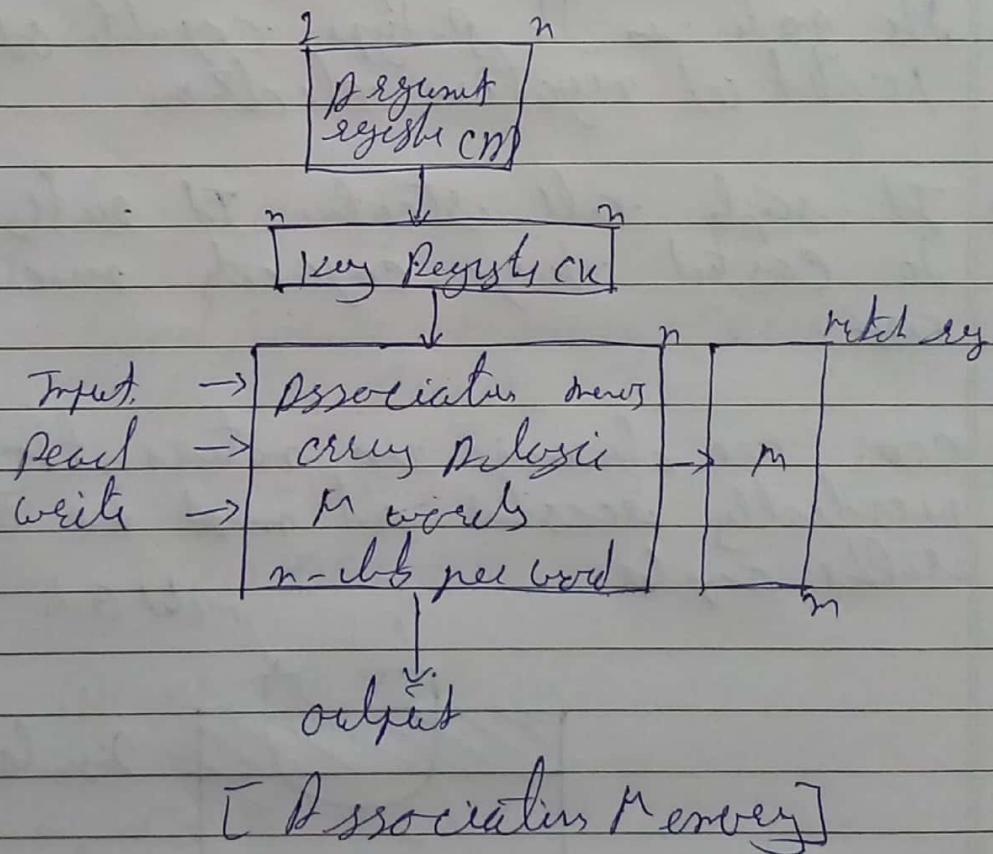
Module 5

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA)

Assignment-5

Module - 5

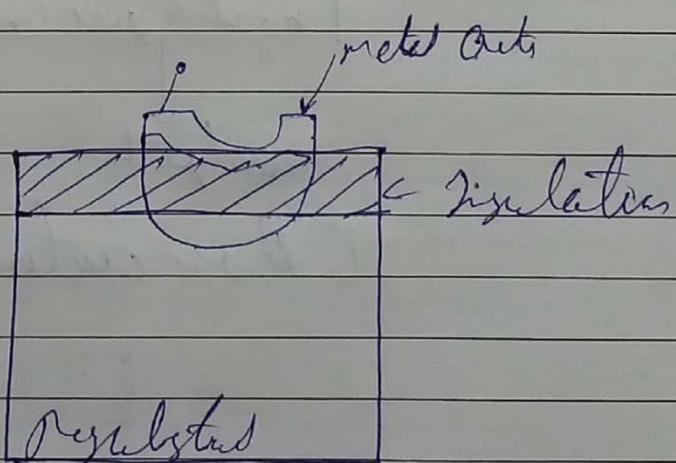
- Q2. The time required to find an object stored in memory can be reduced considerably if objects are selected based on their categories or their common address. Memory used access by the category is called an associative memory or a category Addressable memory (CAM).
- This type of memory is accessed simultaneously and is parallel on the basis of data content.



Q2

(a) charge coupled device (CCD) memory as a function of dynamic memory as which parts of CCD are functionally similar from one memory device to another.

- The structure of a mos charge coupled device as given below as shown in fig.
- When a high voltage is applied to the metal gate, poles are repelled from a drainable drain gate in the p-type material of acceptor &排斥 of negative electrons.
- It is only a structure. Is it really possible to construct a logic circuit since as far as I can see
- CCDs are dynamic in nature, they must be periodically cleared and must be driven by buffer amplifiers.



Q)

Non Volatile memory

i) Read Only Memory (ROM)

(i) Mask Programmable ROM

(ii) Programmable ROM

ii) Read/Write memory (NVRAM)

(i) EEPROM

(ii) EEPROM

(iii) ILDSN

Non volatile Memory

i) Read/Write Memory (RAM)

① Random Access

(i) SRAM

(ii) DRAM

② Non Random Access

(i) FIFO

(ii) LIFO

(iii) Shift Register

Q4

Ans.

A semiconductor is a substance that has specific electrical properties that enable it to serve as a insulation for computer and other electronic devices. It is typically a solid element made of copper that conducts electrically under certain conditions.

- > Semiconductors are materials which have a conductivity between conductors and non-conductivity between conductors and non-conductors or insulators
- > Semiconductors can be used as diodes

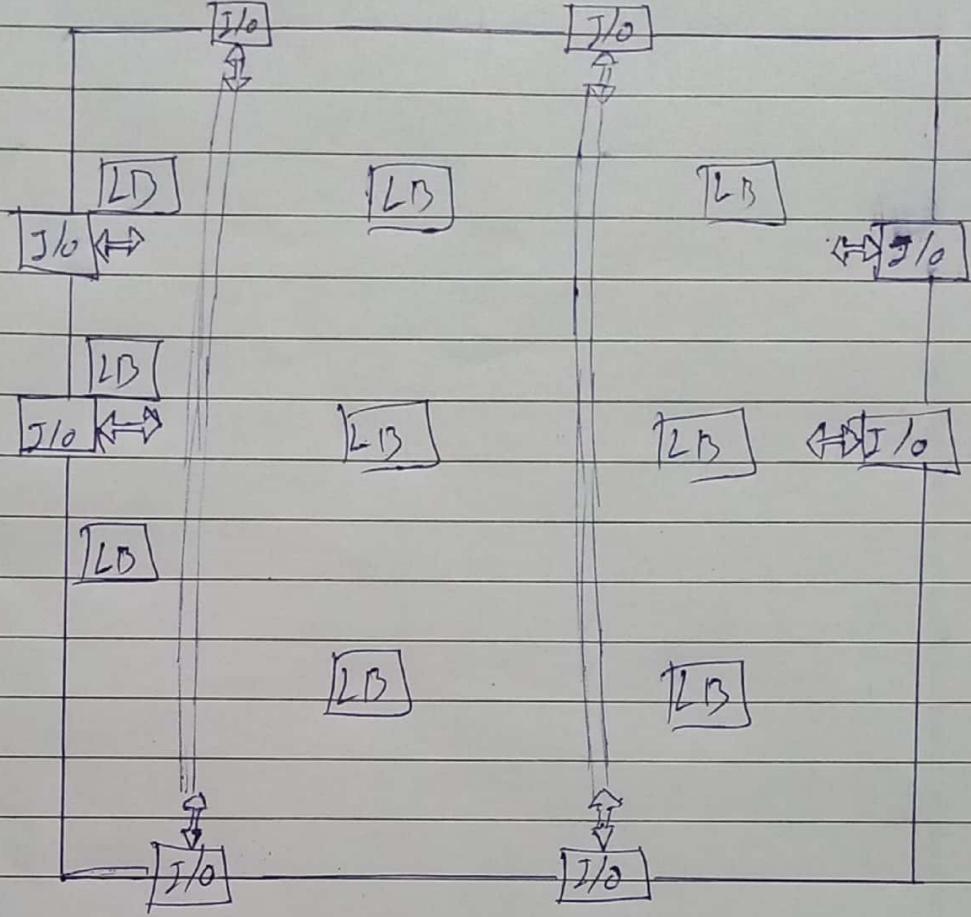
Q5

Ans.

Field programmable gate arrays provide the most generalities, the programmable logic devices

The word array is used to indicate a series of columns and rows of gates that can be programmed by the end user.

- > The programmable logic blocks of FPGA are called logic blocks or configurable logic blocks



6, 11, 22