

Assignment - 1

Q1 Solve the given problem using fundamental of Number Systems and Boolean algebra.

module 1

I) Explain de Morgan's theorem with truth table.

$$\textcircled{1} \text{ Law 1: } A + B + C = A \cdot B \cdot C$$

The complement of sum of variable equal to complement of product of variable

A	B	C	$A + B + C$	$\bar{A} + \bar{B} + \bar{C}$	\bar{A}	\bar{B}	\bar{C}	$\bar{A} \cdot \bar{B} \cdot \bar{C}$
0	0	0	0	1	1	1	1	1
0	0	1	1	0	1	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	1	0	1	0	0	0
1	0	0	1	0	0	1	1	0
1	0	1	1	0	0	1	0	0
1	1	0	1	0	0	0	1	0
1	1	1	1	0	0	0	0	0

$$\textcircled{2} \text{ Law 2: } \bar{A} \cdot \bar{B} \cdot \bar{C} = \bar{A} + \bar{B} + \bar{C}$$

the complement of product is equal to complement of sum of variable

A	B	C	ABC	\bar{ABC}	\bar{A}	\bar{B}	\bar{C}	$\bar{A} + \bar{B} + \bar{C}$
0	0	0	0	1	1	1	1	0
0	0	1	0	1	1	1	0	0
0	1	0	0	1	1	0	1	0
0	1	1	0	1	1	0	0	0
1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	0	1	0
1	1	1	1	0	0	0	0	1

Q. Simplify Boolean function $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$$

$$\bar{A}\bar{B}C + \bar{A}BC + \bar{A}B(C + \bar{C})$$

$$\bar{A}\bar{B}C + \bar{A}BC + \bar{A}BC + \bar{A}B\bar{C}$$

$$\bar{A}C(\bar{B} + B) + \bar{A}B(C + \bar{C})$$

$$\bar{A}C \cdot 1 + \bar{A}B \cdot 1$$

$$F = \bar{A}C + \bar{A}B \quad \underline{\underline{\text{Ans}}}$$

3. List and Explain logic family

Logic family Circuit are.

(i) TTL (ii) CMOS (iii) ECL.

Characteristic	TTL	CMOS	ECL
1 power input	moderate	low	moderate high
2 frequency limit	high	moderate	very high
3 circuit density	moderate	high very high	moderate
4. Circuit types	high	high	moderate
per family			

Transistor - Transistor Logic

- TTL family is so named because of its dependence on transistor alone to perform basic logic operations
- The basic TTL logic circuit is the NAND gate. good Speed, low manufacturing cost wide range of circuits and the availability in SSI and MSI are its merits
- TTL logic family consist of several Sub families

Standard TTL, high Speed TTL, low power TTL, Schottky TTL, low power Schottky TTL, advanced low power Schottky TTL

Schottky TTL:

- The Standard TTL, Low power TTL, and High Speed TTL Series operate using Saturated switches
- The Schottky TTL 74S Series reduces the delay by not allowing the transistor to go into full saturation
- Speed of the 74S Series is twice that of 74H Series

Tri-State TTL

- The third TTL Configuration is the tri-state configuration
- it is called the tri-state, both the transistors in the totem-pole arrangement are turned off, so that the output terminal is a high impedance to ground

4) describe error detecting & correction

when binary data is transmitted and processed it is susceptible to noise that can alter or distort it. Control

- the 1s may get changed to 0s and 0s to 1s.
- Several schemes have been devised to detect the occurrence of a single bit error in a binary word, so that whenever such an error occurs the concerned binary word can be corrected and retransmitted.

parity:

- The simplest technique for detecting errors is that of adding an extra bit, known as the parity bit, to each word being transmitted.
- There are two types of parity - odd parity and even parity.
- For even parity the parity bit is set to a 0 or a 1 at the transmitter such that the total no. number of 1 bits in the word excluding the parity bit is an odd number.
- When the digital data is received, a parity checking circuit generates an error signal if the total number of 1s is even in an odd-parity system or odd in an even-parity system.

- This parity check can always detect single-bit errors but can not detect two or more errors within the word.

Example if data is 1011010, then parity must be 0 and odd parity.

check Sum:

- Simple parity cannot detect two errors in the same word.
- One way of overcoming this difficulty is to use a sum of two elements.
- the receiver can check its sum with transmitted sum.
- if the two sums are the same, no errors were detected at the end.
- Block parity
- when several binary words are transmitted successively the collection of bits can be regrouped as blocks of data, having words.

- This technique also called word parity is widely used for data stored on magnetic tapes.
- These Single-bit errors detected can be corrected by complementing the error bit.
- Two errors as shown in figure 3 can only be detected but not corrected.

01011011	0	01011011	0	
10010101	1	10010101	1	
01101110	0	01100110	0	
11010011	0	11010011	0	+ parity error in
10001101	1	10001101	1	3rd row
01110111	1	01110111	1	
	0	01110110	0	
01110110	↑	↑		
	↑	parity column	↑	
		parity row		error 3rd column.

Error Correcting Code:

- A code is said to be an Error-Correcting Code, if the correct code word can always be deducted from an erroneous word.

The minimum distance of a code is
smallest number of bits by which
two code words must differ.

7-bit hamming code is one type of
correcting code.

The 7-bit hamming code.

To transmit four data bits, three parity bits located positions 2^0 , 2^1 and 2^2 may be added.

The word format would be as shown below

P_1	P_2	D_3	P_4	D_5	D_6	D_7
-------	-------	-------	-------	-------	-------	-------

P_1 is to be set a 0 or 1 so that it establishes even parity bits 1, 3, 5 and 7 (i.e. $P_1 D_3 D_5 D_7$)

P_2 is to be set a 0 or 1 so that it establishes even parity bits 2, 3, 6 and 7 (i.e. $P_2 D_3 D_6 D_7$)

The message 1001001 in the 7 bit hamming code is transmitted through a noisy channel. Decade the message assuming that at most a single error

allowed in each code word.

Bits 1, 3, 5, 7 (1001) \rightarrow no error $\rightarrow C_1 = 0$.

Bits 2, 3, 6, 7 (0001) \rightarrow error $\rightarrow C_2 = 1$

Bits 4, 5, 6, 7 (1001) \rightarrow no error $\rightarrow C_3 = 0$.

The error word is $C_3C_2C_1 = 010 = 2_{10}$ so

complement the 2nd bit from left.
therefore the correct code is 1101001

5. Differentiate TTL, Schottky TTL, CMOS.

CMOS	TTL	Schottky TTL
① more expensive less expensive than TTL but but not as are less costly economical at a System level also, they are smaller.	higher cost of the Schottky technique	
2 Between 20 and 50ns.	Arrangements propagation delay about 3 nanosecond	
③ longer rise shorter rise and fall times and fall times resulting in simpler less costly digital signals	Shottky rise and fall times	

Cmos

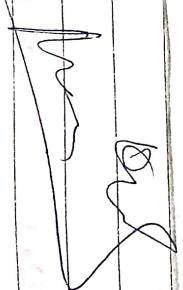
TTL

Schottky

point of being TTL chips have voltage more energy at high operating about 3.6V current voltage level which for excludes having typically the two low voltage ranging from falling in levels usually 4.75- V to 5.25V saturation between 0-1.0.

I₁₃ is held at a
low level.
and high level.

Cmos chip like voltage sequence.
require less. TTL chips require more current
limits power. current consumption





Q2 Analyze working of logic families and logic gates and design the simple circuit using various gates for a given problem.

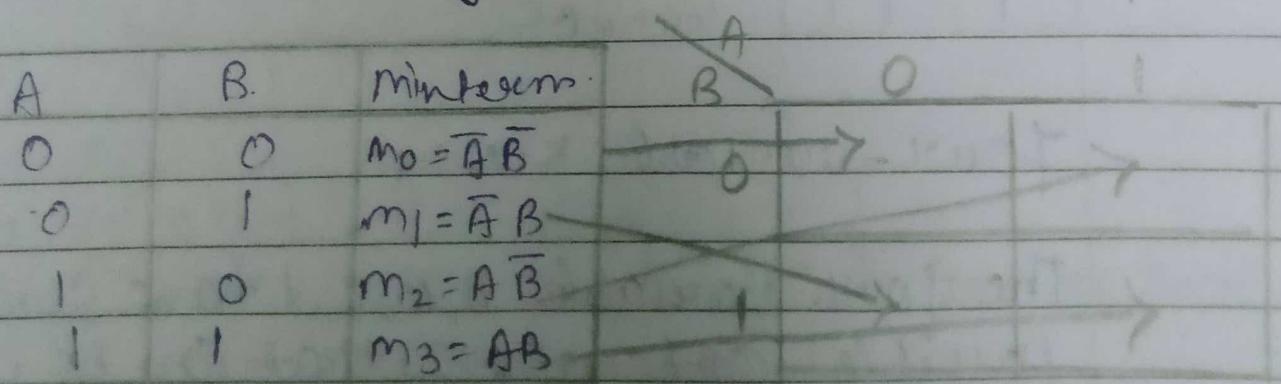
1. Explain K map.

- The Karnaugh map method is a systematic method of simplifying the boolean expression
- the K-map is a chart or a graph, composed of an arrangement of adjacent cells, each representing a particular combination of variables in sum of product form.

Two-variable K-map

- The two variable expression can have $2^2 = 4$ possible combinations of the input variables A and B
- each of these combinations $\bar{A}\bar{B}$, $\bar{A}B$, and $A\bar{B}$ (in SOP form) is called minterm
- These possible combinations can be represented in table and by the map as follows.

A	B	Minterm	\bar{A}	\bar{B}	0
0	0	$m_0 = \bar{A}\bar{B}$	1	1	0
0	1	$m_1 = \bar{A}B$	1	0	1
1	0	$m_2 = A\bar{B}$	0	1	1
1	1	$m_3 = AB$	0	0	0



by the map as follows -

A	B	C	D	minterm	A	B	C	D	minterm
0	0	0	0	$m_0 = \bar{A}\bar{B}\bar{C}\bar{D}$	1	0	0	0	$m_8 = A\bar{B}\bar{C}\bar{D}$
0	0	0	1	$m_1 = \bar{A}\bar{B}\bar{C}D$	1	0	0	1	$m_9 = A\bar{B}\bar{C}d$
0	0	1	0	$m_2 = \bar{A}\bar{B}C\bar{D}$	1	0	1	0	$m_{10} = A\bar{B}Cd$
0	0	1	1	$m_3 = \bar{A}\bar{B}Cd$	1	0	1	1	$m_{11} = A\bar{B}cd$
0	1	0	0	$m_4 = \bar{A}B\bar{C}\bar{D}$	1	1	0	0	$m_{12} = AB\bar{C}\bar{D}$
0	1	0	1	$m_5 = \bar{A}B\bar{C}d$	1	1	0	1	$m_{13} = AB\bar{C}d$
0	1	1	0	$m_6 = \bar{A}BC\bar{D}$	1	1	1	0	$m_{14} = A\bar{B}Cd$
0	1	1	1	$m_7 = \bar{A}BCd$	1	1	1	1	$m_5 = AB\bar{C}d$

AB		cd	00	01	11	10
cd		00	0	4	12	8
00	0	1	5	13	9	
01		1	5	13	9	
11		3	7	15	11	
10		2	6	14	10	

Example: 1 (A, B, C) = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC$

AB		cd	00	01	11	10	
cd		00	0	2	6	4	$\boxed{1} = C$
00	0	1	5	7			
0	0	1	5	7			
1	1	1	1	1	1	1	

2. Functions

2.1 $f(xyz) = \Sigma(2, 3, 6, 7)$

2.2 $f(A, B, C, D) = \Sigma(4, 6, 7, 15)$ Sum of products

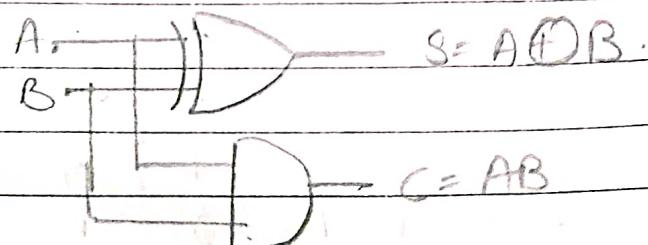
Half Adder:-

- half adder is a combinational circuit with two binary inputs and two binary outputs output
- it adds the two inputs and produces the sum and the carry bit
- the truth table of a half-adder are shown below.

Truth Table

A	B	Sum (Carry)
0	0	0
0	1	1
1	1	0
1	0	1

Figure.



$$S = A\bar{B} + B\bar{A} = A \oplus B$$

$$C = AB$$

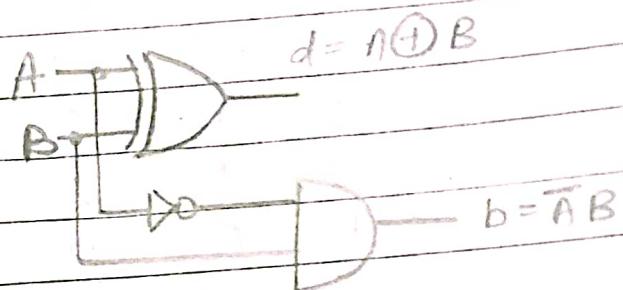
Full Adder:-

- Full adder is a combinational circuit that adds two bits and a carry and outputs a sum bit and a carry bit
- when we want to add two binary number each having two or more bits, the LSB's can be added by using a half adder
- The carry resulted from the addition of the LSBs is carried over to the next significant column and added to the two bits in the

Half Subtractor:

- Half Subtractor is a combinational circuit that subtract one bit from the other and produce the difference.
- it also has an output to specify if a 1 has been borrowed.
- it is used to Subtract LSB of the Subtrahend from the LSB of the minuend when one binary number is Subtracted from the other.

Input		Output	
A	B	d	b'
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

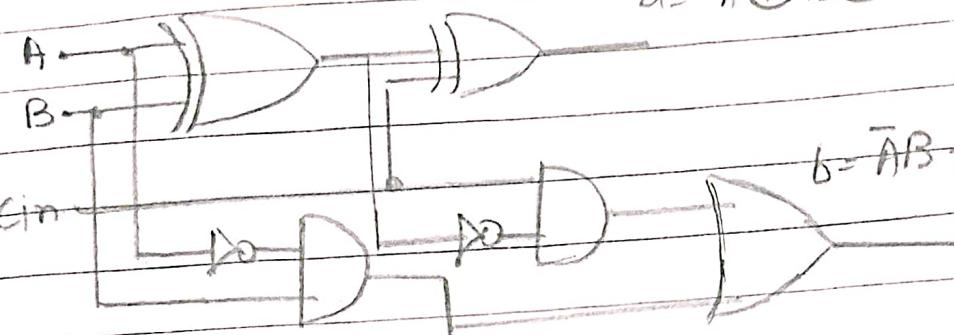


$$d = A\bar{B} + B\bar{A} = A \oplus B \text{ and } d = \bar{A}B$$

Full Subtractor:

- The half Subtractor can be used only for LSB Subtraction.
- if there is a borrow during the subtraction of the LSB, it affects the subtraction in the next higher column, the Subtrahend bit is Subtracted from the minuend bit, Considering the borrow from bit Column used for the subtraction in the preceding column.

Figure. 4) Full Subtractor



$$d = \bar{A} \oplus B \oplus b_1$$

$$b_2 = \bar{A}B + (\bar{A} \oplus B)b_1$$

Explain multiplexer & demultiplexer.

- A multiplexer is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.

- Consider an integer 'n' which is contained by the following integer

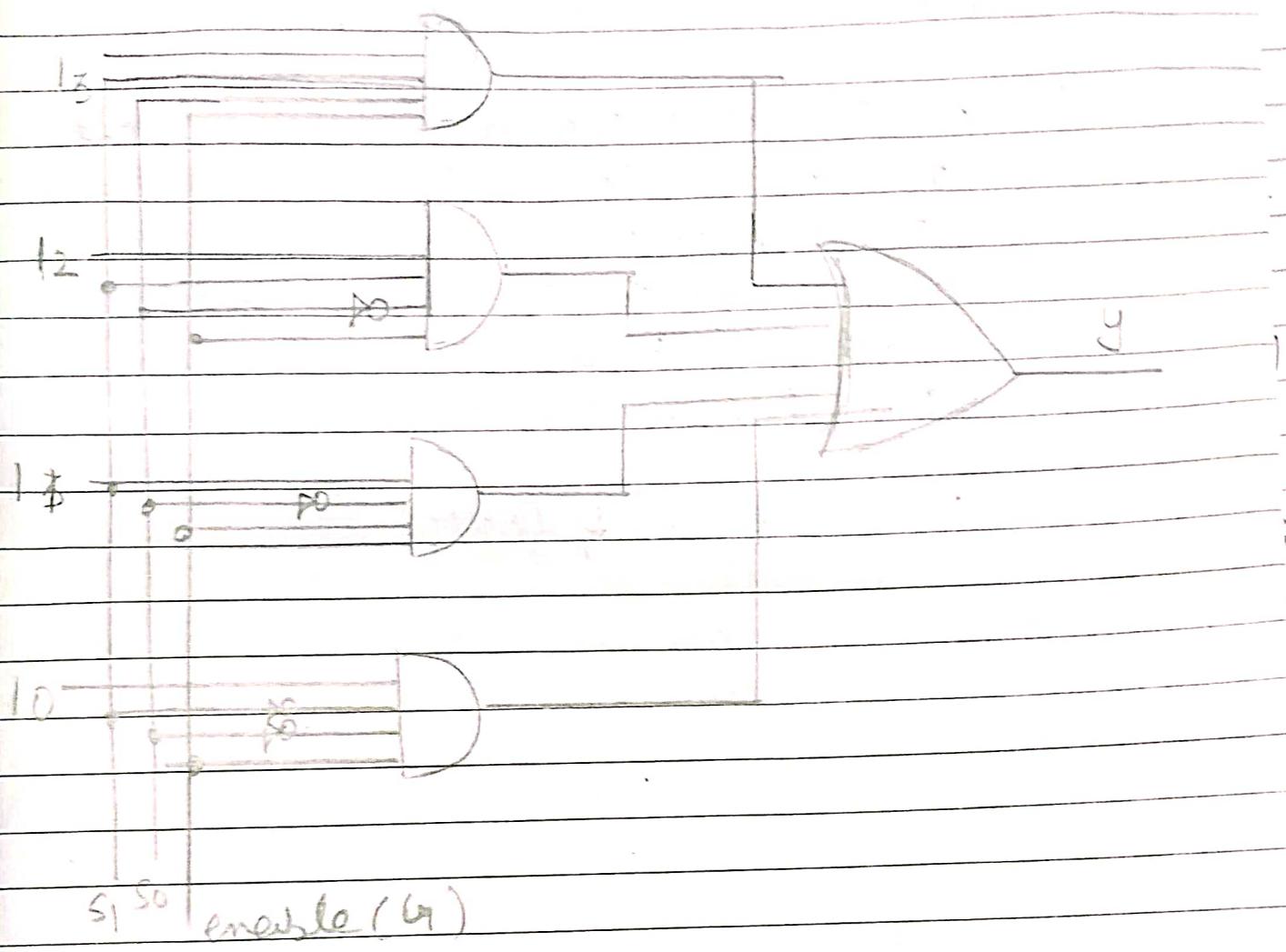
$n - 1$ multiplexer has

n input $I_0, I_1, I_2, \dots, I_{(n-1)}$

one output Y

n control inputs $S_0, S_1, S_2, \dots, S_{(n-1)}$

Majical circuit 4x1 multiplexer



Demultiplexers

A multiplexer takes several inputs and transmits one of them to the output

demultiplexer performs the reverse operation
it takes a single input and distribute it over several circuits

Describe parity checker & generator.

parity generator:

Inclusive-OR functions are very useful in systems requiring error detection and correction codes.

Binary data when transmitted and processed is susceptible to noise that can alter its 0s to 1s and 1s to 0s.

To detect such errors, an additional bit called the parity bit is added to the data bits and the word containing the data bits and the parity bits is transmitted.

At the receiving end the number of 1s in the word received are counted and the error, if any, is detected.

This parity check, however, detects only single bit errors.

The circuit that generates the parity bit is termed as called a parity generator.

The circuit that checks the parity in the receiver is called a parity checker.

The parity bit can be attached to the code group either at the beginning or the

accordance with some priority system among all those that may be simultaneously high

- The most common priority system is based on the relative magnitudes of the inputs whichever decimal input is the largest is the one that is enabled

Truth table.

Inputs				Output		
D ₀	D ₁	D ₂	D ₃	A	B	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

$$A = \text{Em}(1, 2, 3, 5, 6, 7, 9, 10, 11, 13, 14, 15)$$

$$B = \text{Em}(1, 3, 4, 5, 7, 9, 11, 12, 13, 15)$$

$$V = \text{Em}(1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$$

- In addition to the outputs A and B the circuit has a third output designated by V
- This is a valid bit indicator that is set to 1 when one or more inputs are equal to 1
- According to the truth table, the higher the subscript number, the higher the priority of the inputs

and implement Combinational and Sequential logic circuit and verify its working.

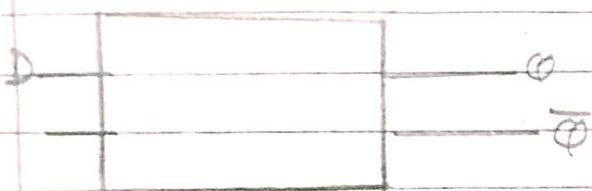
~~Digital~~ Differential Sequential & Combinational Circuits

Sequential Circuit	Combinational Circuit
A type of digital circuit whose the output is only a pure function of the present input	A type of digital circuit whose output depends not only on the present value of its input signals but also on the sequence of past inputs
Output depends on the present input and past present input outputs	
There is a memory unit to store immediate results	
There is a clock	There is no clock
Half adder, flip-flop and register	Half adder, full adder, multiplexer, encoder, decade.

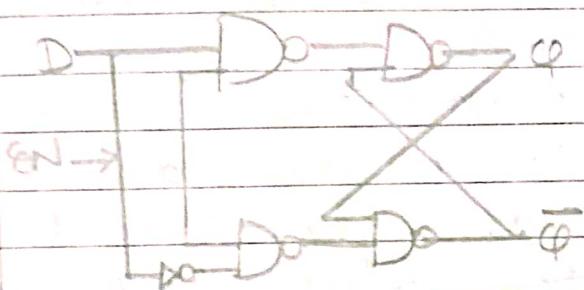
(2)

- A gated S-R latch requires enable input. its S and R inputs will control the state by the flip flop only when the EN is high. non EN output may be a clock, so a gated S-R latch is also called clocked SR latch.

D-flip flop:



Logical Symbol.



Logical diagram

- it differs from the SR latch in that it has only one input in addition EN
- when $D=1$, we have $S=1$ and $R=0$ causing the latch to set when enable.
- when $D=0$, we have $S=0$ and $R=1$ causing the latch to reset when enable.

bit and Extern Registers

- As a flip-flop can store only one bit of data a 0 or 1 its referred to as a Single-bit register
- A register is a set of FFs used to store binary data.
- the storage capacity of a register is the number of bits (1s and 0s) of digital data it can retain
- Loading a register means Setting all resetting the individual FFs
- In Serial loading data is transferred into the register in serial

Types of Registers

1. Buffer register
2. Shift register
3. Bidirectional Shift register
4. Universal Shift register

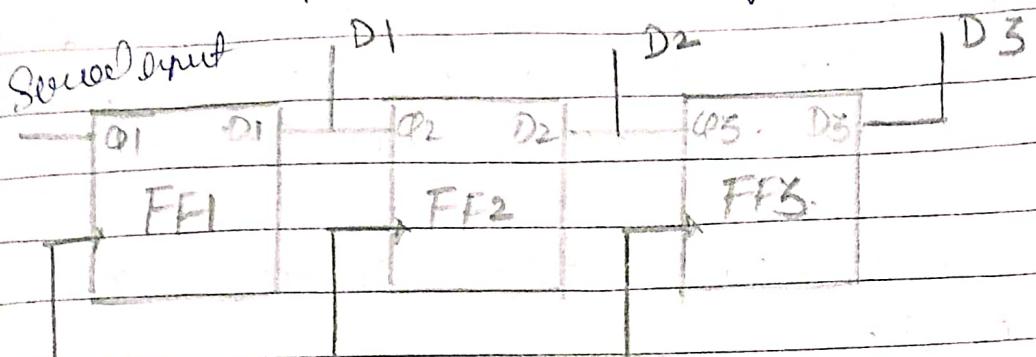
Shift Registers:

- no of flip-flops connected with each other and you can shift the bits from one shift register to another.

Types of Shift Registers

- Serial in, Serial out
- Serial in, Parallel out
- Parallel in, Serial out

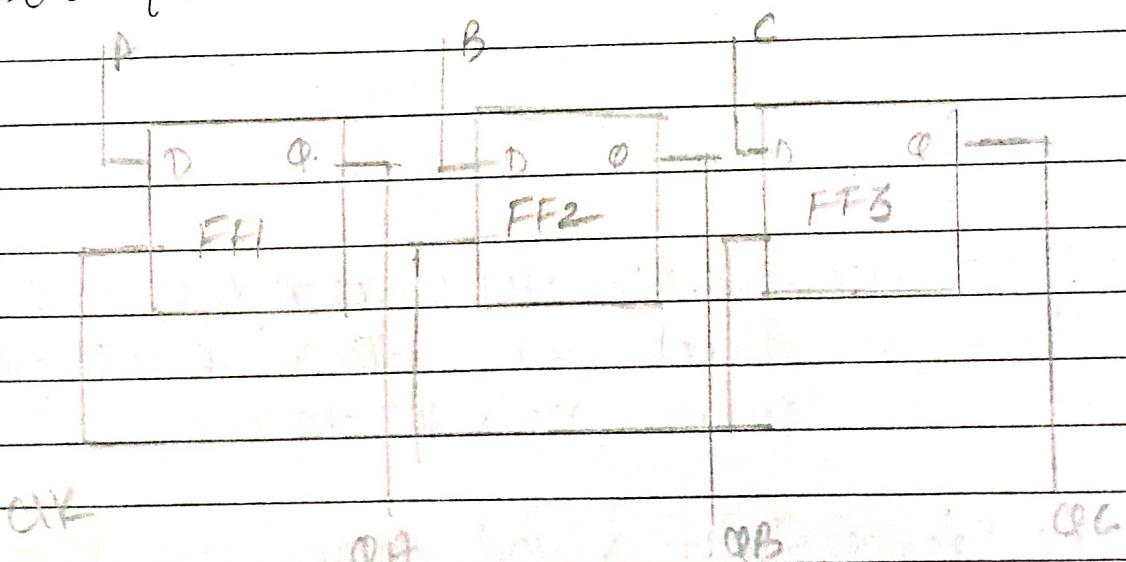
Serial-in Parallel-out Register



CLK

- This Register come as Serial in and Serial out
But little difference here we use very parallel output rather than Serial Output
- FF₁, FF₂, FF₃ Are Shift Registers.
- Serial output go through Q₁ and then collect
Collect by D₁ and that output point that
time and as well as pass to Q₂.
- here D₁, D₂, D₃ parallel output and
- Q₁, Q₂, Q₃ is inputs line

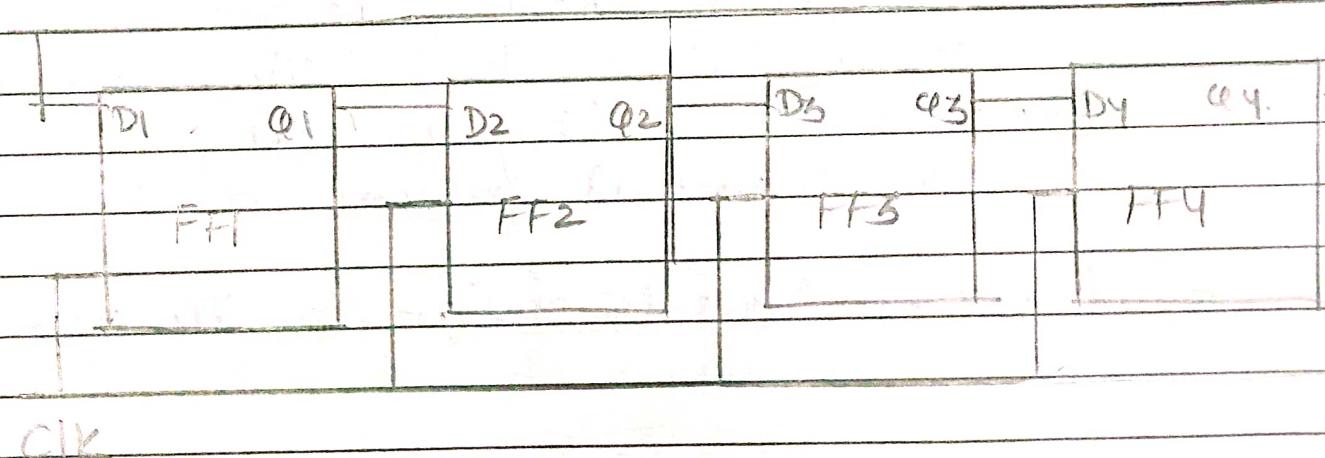
~~Serial parallel in Serial output parallel output~~



(5)

- entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q₄
- when Shift load line is high gates G₁₁, G₁₂ and disabled but gates G₁₄, G₁₅ and G₁₆ are enabled allowing the data bits to shift right from one stage to the next.
- when Shift load line is low gates G₁₄, G₁₅ and G₁₆ are disabled whereas gates G₁₁, G₁₂ and G₁₃ are enabled allowing the data input to appear at the D inputs of the respective FFs.
- The OR gate allows whether the normal shifting operations or parallel data entry depending on which AND gates are enabled by the level on the shift / load & input

4/ Describe ring counter using Up-Down.



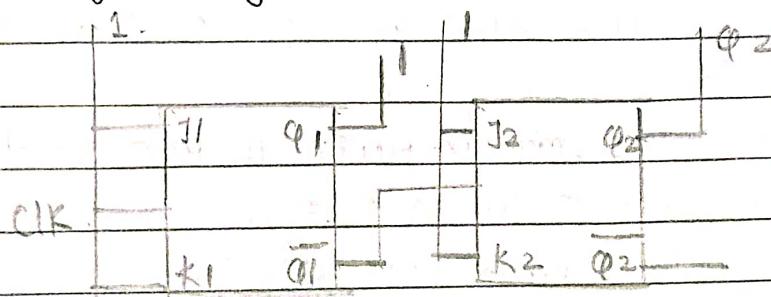
(6)

2 bit up-down counter using negative edge triggered FF

	J_1	Q_1	J_2	Q_2	CLK	Q_1	Q_0	Q_1	Q_0
	FF1		FF2		\downarrow	0	0	0	1
IK		\bar{Q}_1		\bar{Q}_2	\downarrow	0	1	1	0
					\downarrow	1	0	1	1
					\downarrow	1	1	0	0

- The 2 bit up counter in the states $0, 1, 2, 3, 0$
- The Counter is initially reset to 00
- When the first clock pulse is applied FF1 toggles at the negative edge of this pulse
it therefore, Q_1 goes from low to high

(2) 2 bit up-down - Counter using negative edge triggered FF



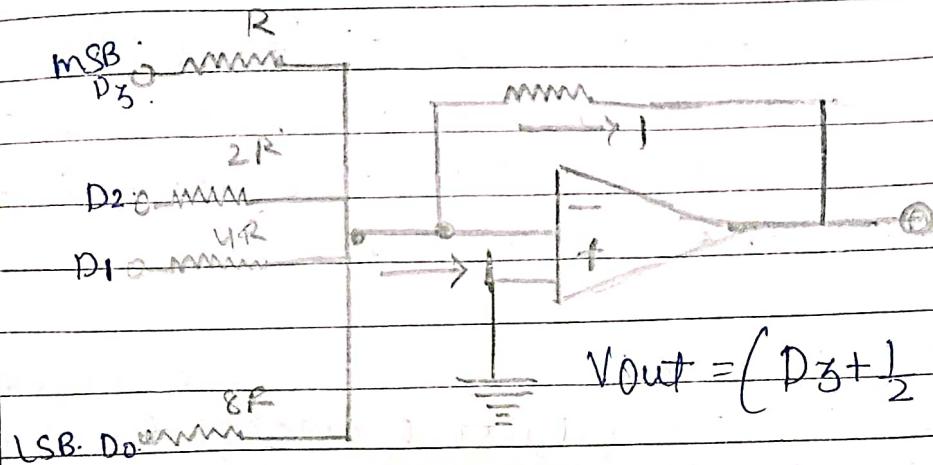
- At the negative edge of the first clock pulse FF1 toggle so Q_1 goes from 0 to 1 and Q_1 goes from 1 to 0

Note: this negative edge Q_1 applied to the clock input of FF2 toggle FF2 and therefore Q_2 goes from 0 to 1 so after one clock pulse $Q_2 = 1$ and $Q_1 = 1$ the state of the Counter is 11.

Assignment - 4

Examine the process of analog to digital conversion and digital to analog conversion.

Weighted resistor type DAC



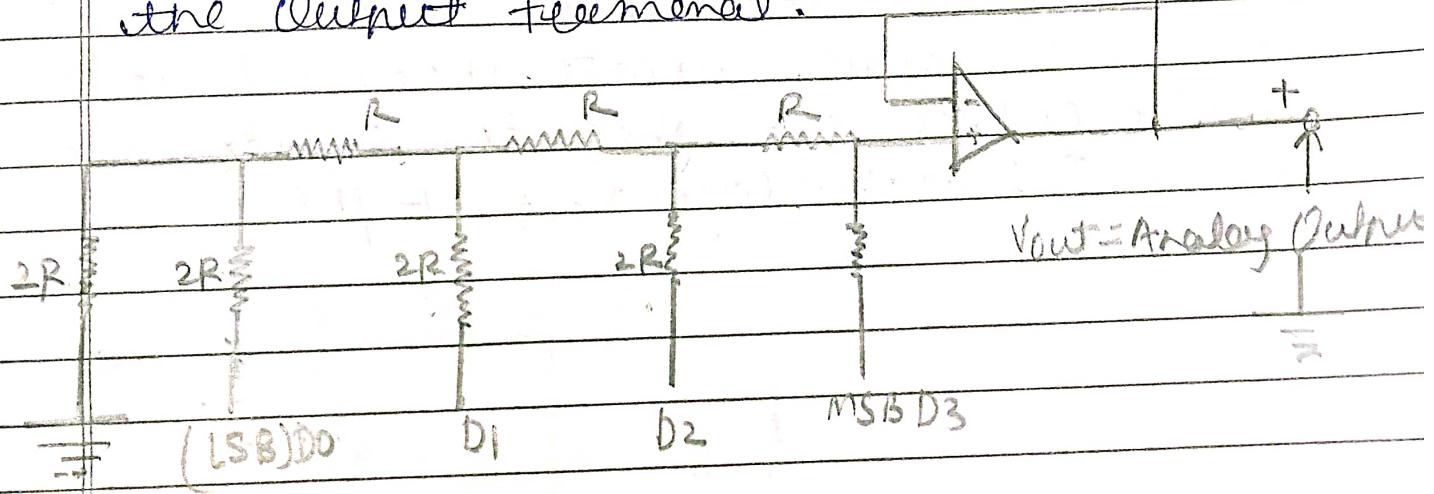
$$V_{out} = \left(D_3 + \frac{1}{2} D_2 + \frac{1}{4} D_1 + \frac{1}{8} D_0 \right) \frac{R_s}{R}$$

- The diagram of the weighted resistor DAC is shown in figure.
- The operational amplifier is used to produce a weighted sum of the digital value.
- ~~The figure shows the symbol.~~
- The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the bit position of inputs.
- The MSB D_3 is connected as an inverting amplifier each input is amplified by a factor equal to the ratio of the feedback resistance divided by the input resistance to which it is connected.

Assignment - 4.

2. Explain R-2R ladder D/A Converter

- The R-2R ladder type DAC is the most popular DAC. it uses a ladder network containing Series parallel Combinations of two resistors of values R and $2R$.
- The operational amplifier configured as voltage follower is used to prevent loading.
- Figure Shows the circuit diagram of a R-2R ladder type DAC having 4-bit digital input
- When a digital Sos Signal $D_3 D_2 D_1 D_0$ is applied at the input terminals of the DAC, an equivalent Analog Signal is produced at the Output terminal.



Case - 1 when the input is 1000

- Below figure illustrates the procedure Calculate V_{out} when the input is 1000
- Continuing in this manner we ultimately find that $R_{eq} = 2R$

(5)

5. describe Specification of A/d & D/A Converter

Specification for DAC:

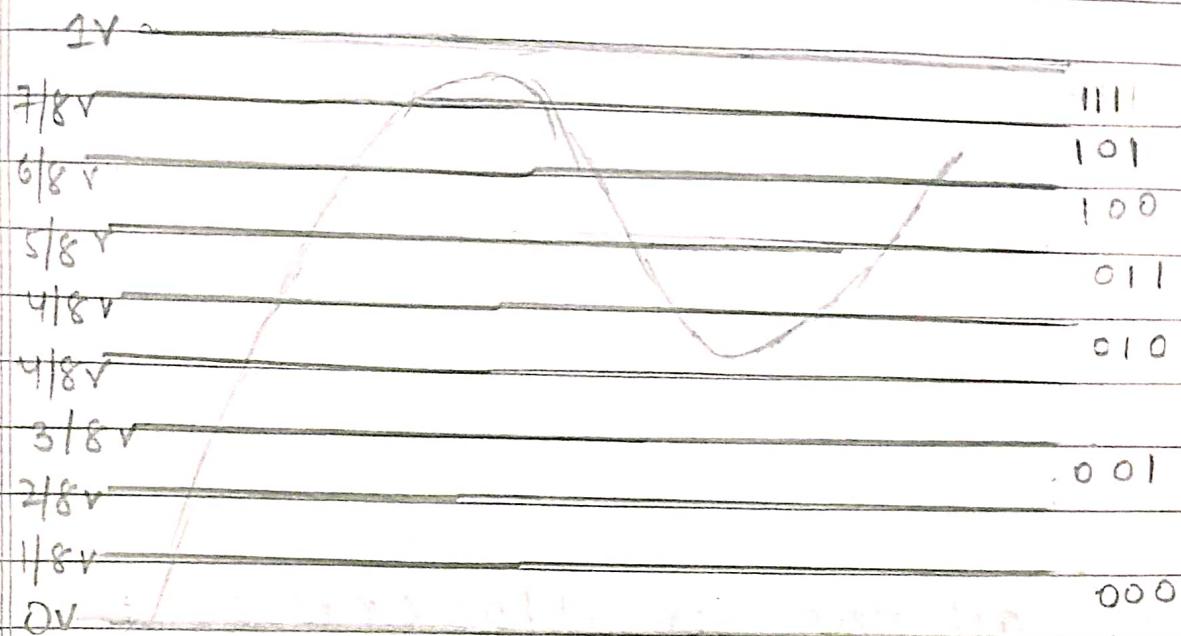
- The resolution of a DAC is defined as the smallest change that can occur in an analog output as a result of a change in the digital input
- The resolution of a DAC is also known as the reciprocal of the no of discrete steps in the full scale output of the DAC
- The Resolution of is always equal to the weight of the LSB and is also referred to as the Step Size
- The resolution or step size is the size of the jumps in the staircase waveform
- The Step Size of the DAC is the same as the proportionality factor in the DAC input output relationship

$$\% \text{ resolution} = \frac{\text{Step Size}}{\text{Full Scale}} \times 100\%$$

Since, Full Scale = number of steps \times Step size
 resolution Can be expressed as

$$\% \text{ resolution} = \frac{1}{\text{Total no of steps}} \times 100\%$$

In contrast in an analog to digital converter the input analog voltage can have any value in a range, but the digital output can have only 2^N discrete values for an N -bit A/D converter.



- Consider an analog voltage in the range of 0 to V and a 3-bit digital cluster to few. Any voltage in this
- Let us divide the whole range of analog voltage in 8 intervals of the size $S = V/8$
- Each interval is assigned a 3-bit binary word
- The intervals of the analog voltage and their corresponding digital values assigned are shown in above figure
Therefore there is an error referred to as quantization error or malence in this process of quantization

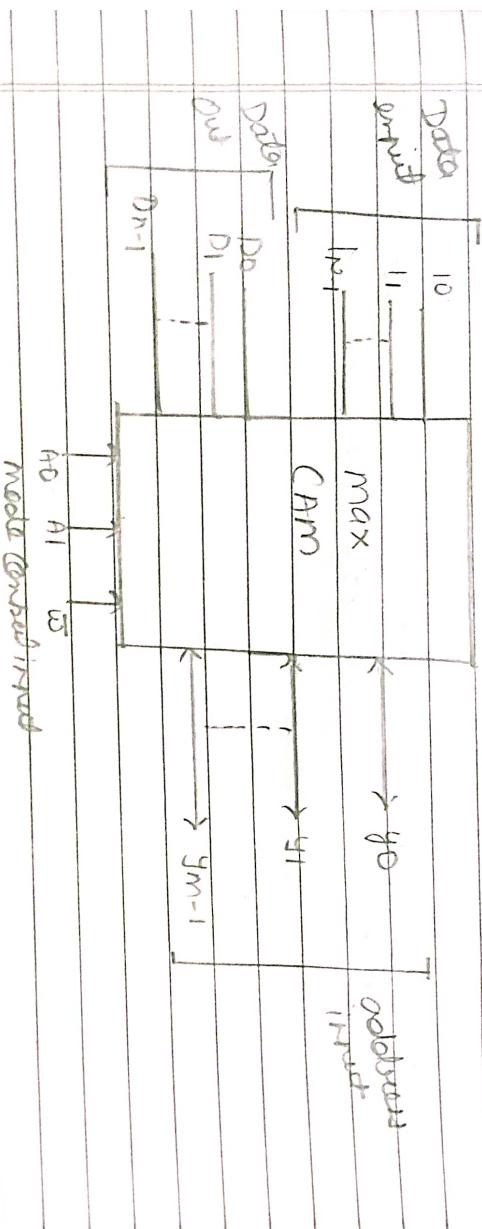
Assignment - 5

(1)

Q5 implement PUDs for the general logical problem

- 1 Explain Content addressable memory
- 2 Explain cache & Coupled device memory
- 3 Explain classification of memory
4. Discuss. Semiconductor
5. Explain level programming logic array

[Ans-1]

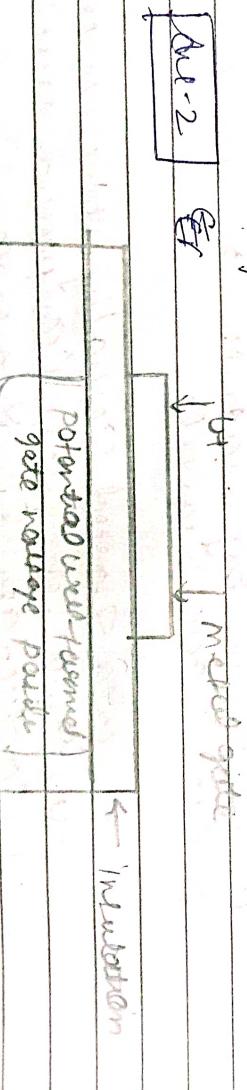


- A CAM can perform three basic operations
read, write, and associate
- Figure shows a block diagram of a CAM with its
Storage Capacity is $m \times n$ bits and is organised
as m words of n bit each
- it has N data input and N data output
lenses. The data input lenses so through In-1
are used to input data to be written

(2)

into the memory and pass key word in case of associate operation

- Data are read by the Cam at the data Clump lines P_{n-1} through P_{n+1}
- The Y lines are bidirectional. During a read or write operation three lines are used to select the storage location
- There is one address input line for each word in the Cam Y set. Example Y₀ is the address line for memory location 0, Y₁ has memory location 1 and so on.
- The Y lines select a group of clump lines. One line each memory section 3 and 8 clump Y₅ and Y₆ will become high to evaluate the match condition
- The main control inputs are used to select the required operation
- The reading up the data is non-destructive



3. ROM (Read Only Memory)

(3)

- It has become an important part of many digital systems such as implementation of combinational logic and sequential logic character generation look-up-table microprocessor program storage etc.
- The read-only memory and sequenced logic character generation, loose up task microprocessor program storage etc.
- ROM (Random access memory)
 - Many digital require memory which it should be possible to write into and read from any memory location with the same speed
 - In such memory the data stored at any location can be changed during the operation of the system
- This type of memory is known as a read/write memory and is usually referred to as RAM.
- The read write memory is RAM fabricated using bipolar devices or unipolar devices

(4)

Aur. 5

I/O \rightarrow

Q

Q

Q

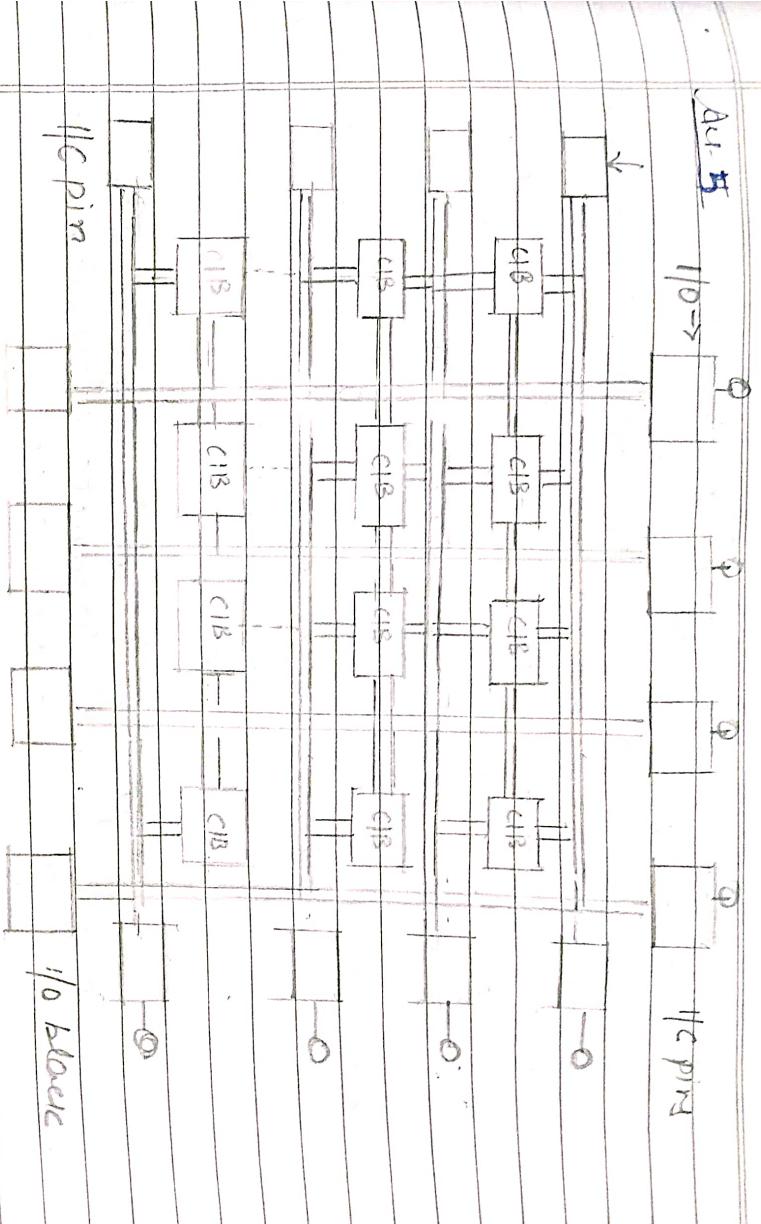
Q

Q

Q

Q

Q



- The programmable logic devices are based on Sram base architecture, the programmable array logic or the programmable logic array.
- The logic densities of FPLA are much higher than those of CPLD.
- They range in size from a few thousands to hundred of thousand equivalent gates.
- The basic FPLA architecture consists of an array of Configuration logic blocks.
- The various families of FPLA manufactured by different manufacturers differ primarily