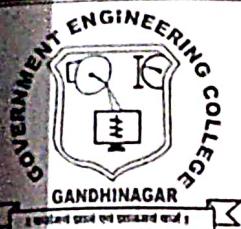




Government Engineering College, Gandhinagar

**Computer Engineering
B.E. Semester III
(AY 2021-22)**

SUBJECT: Digital Fundamental (3130704)



Government Engineering College

Sector-28 Gandhinagar

Certificate

This is to certify that

Mr./Ms Patel Jenil N Of class

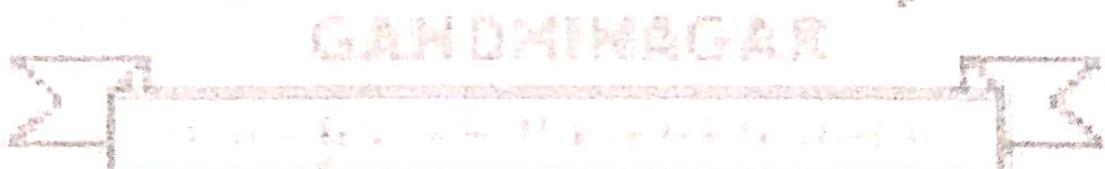
3rd Division A, Enrollment No....D2D22..... Has

satisfactorily completed his/her term work in

..... D.F Subject for the term

ending in ... Jan 2022-23.

Date:-



Signature of Teacher

Head of Department

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department

Vision/Mission

Vision:

To be a premier engineering institution impacting quality education for innovative solution relevant to society and environment.

Mission:

- To develop human potential to its fullest. extend so that intellectual and innovative engineers merge in a wide range of professions.
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Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communications skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	Solve the given problem using fundamentals of number system and boolean algebra
CO-2	Analyze working of logic families and logic gates and design simple circuits using logic gates
CO-3	Design and implement combinational circuits and sequential and verify its working
CO-4	Examine the process of Analog to digital conversion PCO's for given analog converter
CO-5	Implement PCO's for given logical problem

7. Assignment Index

Sr. No	Assignment	Date	Page No.	Sign
1	Assignment 1	30/09/22	1	✓ ✓ ✓
2	Assignment 2	17/10/22	7	✓ ✓ ✓
3	Assignment 3	30/11/22	15	✓ ✓ ✓
4	Assignment 4	14/12/22	21	✓ ✓ ✓
5	Assignment 5	30/12/20	27	✓ ✓ ✓

8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1	13/09/22	14	J
2	Practical 2	27/09/22	16	
3	Practical 3	04/10/22	18	P
4	Practical 4	11/10/22	20	
5	Practical 5	18/10/22	21	M
6	Practical 6	15/11/22	24	
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11	Practical 11	20/12/22	36	

9. Assignment 1

CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra

Module 1

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function: $F=A'B'C+A'BC+AB'$.
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

Parity code:-

- * Even parity code:- The value of even parity bit should be zero, if even number of ones are present in the binary code. Otherwise, it should be one. so that , even number of ones present in even parity code.

Binary Code	Even parity bit	Even parity code
000	0	0000
001	1	0011
010	0	0101
011	0	0110
100	1	1100
101	0	1010
110	0	1100
111	1	1111

- * odd parity code:- The value of odd parity bit should be zero, if odd numbers of ones present in the binary code. Otherwise, should be one. so . odd number of ones present in odd parity code.

Binary Code	Odd parity bit	Odd parity code
000	1	0001
001	0	0010
010	0	0100
011	1	0111
100	0	1000
101	1	1011
110	1	1101
111	0	1111

Assignment-1Module 1

Q-1.

- De Morgan suggested two theorems that form an important part of Boolean algebra:
- $\overline{AB} = \overline{A} + \overline{B}$: De Morgan's first theorem
 - The complement of product is equal to the sum of the complements.

Truth table:

A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	0

$$2. \overline{A+B} = \overline{A} \cdot \overline{B}$$

The complement of a ~~product~~ is equal to the ~~sum~~ of the complements.

Truth table:

A	B	$A+B$	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Q-2

$$\begin{aligned}
 F &= \overline{ABC} + \overline{ACB} + A\overline{B} \\
 &= \overline{A}C(C\overline{B} + B) + A\overline{B} \\
 &= \overline{A}C + A\overline{B} \quad [A + \overline{A} = 1] \\
 F &= \boxed{\overline{AC} + A\overline{B}}
 \end{aligned}$$

Q-3

my

Logic families are divided into two parts.

1) Bipolar.

2) Unipolar.

* Bipolar It has further two subparts.

(a) Saturated:

- Register Transistor logic (RTL)
- Diode Transistor logic (DTL)
- Direct coupled Transistor logic (DCTL)
- Integrated Injection logic (I²L)
- High threshold logic (HTL)
- Transistor Transistor Logic (TTL)

(b) Unsaturated:

- Schottky TTL
- Emitter coupled logic (ECL)

2) Unipolar:

- P-channel MOSFET (PMOS)
- N-channel MOSFET (NMOS)
- Complementary MOSFET (CMOS)

* It is a group of compatible ICs with the same logic level and supply voltages for performing various logic functions. They are fabricated using a specific circuit configuration which is referred as a logic family. The circuit design of basic gate of each logic family is same.

- Transistor Transistor logic (TTL):- It is named for its dependence on transistors alone to perform basic logic operations.
- Schottky TTL:- A schottky transistor is a combination of a transistor and a Schottky diode that prevents the transistor from saturating by diverting the excessive input current.
- CMOS:- Complementary metal-oxide-semiconductor is a type of metal oxide - semi-conductor effect transistor fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFET's for logic functions.

4. Describe error detecting & correcting code.

→ To maintain the data integrity between transmitter & receiver, extra bit or more than one bit are added in the data. These extra bits allow the detection & some time correction of errors in the data. The data along with the extra bits form the codes. Codes which allow only error detection are called error detecting code which allow error detection and correction are called error detecting & correcting code.

* Hamming Code: Hamming code is useful for both detection and correction of error present in the received data. This code uses multiple parity bits and we have to place these parity bits in the position of powers of 2.

Bit designation	D ₇	D ₆	D ₅	P ₄	D ₃	P ₂	P ₁
Bit location	7	6	5	4	3	2	1
Binary location number	110	101	100	011	010	001	

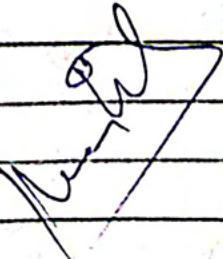
Parity P₁ checks bit locations 1, 3, 5, 7 and assigns P₁ according to even or odd parity.

- Parity P₂ checks bit locations 2, 3, 6, 7 and assigns P₂ according to even or odd parity.

- Parity P₄ checks bit locations 4, 5, 6, 7 and assigns P₄ according to even or odd parity.

Differentiate TTL, schotky TTL and cmos.

Parameter	CMOS	TTL	Schotky TTL
Device used	mosfet p-channel & n-channel	Bipolar junction transistor	Schotky diode
V _H (Vmin)	3.0 V	2 V	2 V
V _L (Vmax)	0.5 V	0.8 V	0.8 V
V _{OH} (Vmin)	1.015 V	2.7 V	2.7 V
V _{OL} (Vmax)	0.005 V	0.4 V	0.5 V
Power dissipation per gate	0.1 mW	10 mW	1 mW
Fan out	50	10	50
Applications	Portable instrument where Bailey is used	Laboratory instrument	Voltage clamping app" to prevent transistor saturation



10. Assignment 2

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem

Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
 - 2.1. $F(x,y,z) = \Sigma (2,3,6,7)$
 - 2.2. $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

Assignment :- 2.

Module - 2. The Karnaugh Map

Q1

- The map method gives us a systematic approach simplifying a Boolean expression.
- The basis of this method is a graphical chart known as Karnaugh map (Kmap)
 - It contains boxes called cells. Each of the cell represent one of the 2^n possible product that can be formed from n variables. Thus a 2-variable map contains $2^2 = 4$ cells, a 3 variable map contains $2^3 = 8$ cell and so forth.

A	B	00	01	10	11	m	C	00	01	11	10
0	0	0					00				
1	1	1	1				01				

(1 variable) (2 variable) (3 variable) (4 variable)
map map map map

Q-2

$$w) F(x, y, z) = \Sigma(2, 3, 6, 7)$$

x 4'00 01 11 10

0	0	1	1
1	0	1	1
1	1	1	1
0	1	1	0

$$F = y$$

$$F(A, B, C, D) = \Sigma(4, 6, 7, 15)$$

AB CD 00 00 01 11 10

00	0	1	0	1	0	1
01	1	0	1	0	1	1
11	0	1	1	1	0	1
10	1	1	0	1	1	0
00	0	0	0	0	0	0
01	0	0	0	1	0	1
11	0	0	1	0	1	0
10	0	1	0	0	1	1

$$F = \bar{A}B\bar{D} + BCD$$

Q-3

→ Adder:

- The logic circuit which performs addition of two bits is a half-adder.
- The logic circuit which performs addition of three bits is called a full adder.

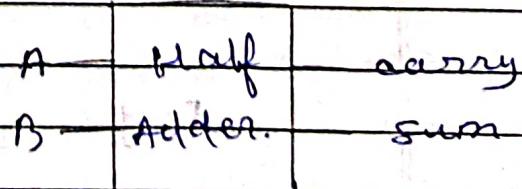
* Half adder:

- Two binary inputs : augend and added bit,
- Two binary output : sum and carry.

Truth table -

T	A	B	Carry	Sum
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	0	0

Block diagram:



* Full adder :

- Three binary inputs : augend, addend, carry
- Three binary outputs : sum and carry

Truth table:

* Block diagram

A	B	Cin	Carry	Sum			
0	0	0	0	0			
0	0	1	0	1			
0	1	0	0	1			
0	1	1	1	0			
1	0	0	0	1			
1	0	1	1	0			
1	1	0	1	0			
1	1	1	1	1			

* Subtractor :

- A half subtractor is a combinational circuit that subtracts two bits and produces their difference.
- A full subtractor is a combinational circuit that subtracts between two bits, taking into account borrow of lower stage.

* Half subtractor :

Two inputs and two output which is difference & borrow

Truth Table:

* Block diagram

A	B	Difference	Borrow			
0	0	0	0			
0	1	1	1			
1	0	1	0			
1	1	0	0			

* Full subtractor :-

- Three inputs : minuend, subtrahend and borrow in
- Two outputs difference and borrow out.

Tenth frame

A	B	Bin	D	Bout		Block diagram
0	0	0	0	0		
0	0	1	1	1	A	
0	1	0	1	1	B	
0	1	1	0	1	Bin	
1	0	0	1	0		
1	0	1	0	0		
1	1	0	0	0		
1	1	1	1	1		

Ques.



Multiplexer :-

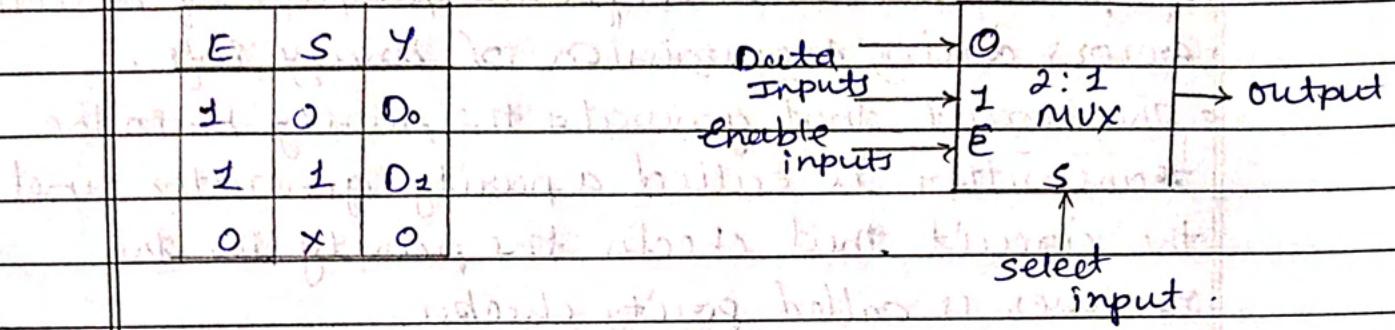
To select single data line from several data input lines, and to locate from the selected data line should be available on the output. The digital circuit which does this task is multiplexer.

2:1 Multiplexer

- Do D_1 is applied as an input to one AND gate and D_2 is applied as an input to another AND gate.
- Enable input is applied to both gates as one input.
- Selection line S is connected as second input to second AND gate. An inverted S is to second input to first AND gate.
- Output of both AND gate applied as inputs OR gate.

Function Table

Block diagram.



* Demultiplexer.

* demultiplexer is a circuit that receives info on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n select lines.

1:4 Demultiplexer.

- The single input variable Din has a path to all four output, but the input information is directed to only one of the output lines depending on the select inputs. Enable input should be high to enable demultiplexer.

Block diagram.

Function Table.

The block diagram shows a DEMUX component with an enable input (E), select inputs (S1, S0), and four outputs (Y0, Y1, Y2, Y3). The function table shows the relationship between E, S1, S0, and the four outputs Y0, Y1, Y2, Y3.

E	S ₁	S ₀	Din	Y ₀	Y ₁	Y ₂	Y ₃
0	x	x	x	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

Q-5.

Ans 1st parity bit is used for the purpose of detecting errors during transmission of binary info.

- The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called parity checker.

* Parity generator truth table for even and odd parity:

A	B	C	odd parity	even parity
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

* Parity Checker:

- These three bits in the message together with the parity bit are transmitted to their destination where they are applied to the parity checker circuit.
- The parity checker circuit checks for the possible errors in the transmitter.



* Truth table for even parity checker.

Decimal equivalent	P	N	B	C	Parity even checker
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

QJ
PK

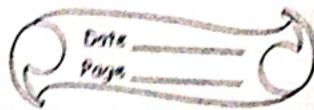
11. Assignment 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 3

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

Assignment on 3



Module :- 3

Q-1
→

Combinational circuits

Sequential circuits

- The output variables are not at all times dependent on the combination of input variables.
- The output variables depend not only on the present input but also depends on the past history of these inputs inevitable.
- Easy to design.
- Slower to design.
- Parallel adder is a combinational circuit.
- Serial adder is a sequential circuit.
- Faster in speed.
- Slower than combinational circuits.

Q2
→

—
Types of flip-flops are:

- JK flipflop
- D flipflop
- T flipflop
- SR flipflop

• J-K flip-flops:

- The data inputs are J and K which are ANDed with \bar{Q} and Q respectively to obtain S and R inputs

Truth table.

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

• D-flipflops.

- Input conditions can be avoided by making them complement of each other. This modified SR flip flop is known as D flip flop.

Truth table.

Cp	D	Q_{n+1}
1	0	0
1	1	1
0	x	\bar{Q}_n

• T flip-flop

- T-flip flop is also known as "Toggle flip-flop"
- It is modification of J-K flip flop

Truth table.

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

- S-R flipflop

- The circuit is similar to SR latch except enable signal is replaced by the clock pulse (C_p) followed by the positive edge detector circuit.
- The edge detector circuit is a differentiation.

Truth table:

	C_p	S	R	O_{n+1}
	0	X	X	O_n
↑	0	0	0	Hold
↑	0	1	0	1
↑	1	0	0	2
↑	1	1	1	Invalid

Q2-3

→ Types of registers:

- Buffer register.
- controlled Buffer register
- shift register

1) Buffer register:

- Constructed using four D-flipflops. This register is called a Buffer register.
- Each D flipflop is triggered with a common negative edge clock pulse.
- The Input bits set up the flipflop for loading.

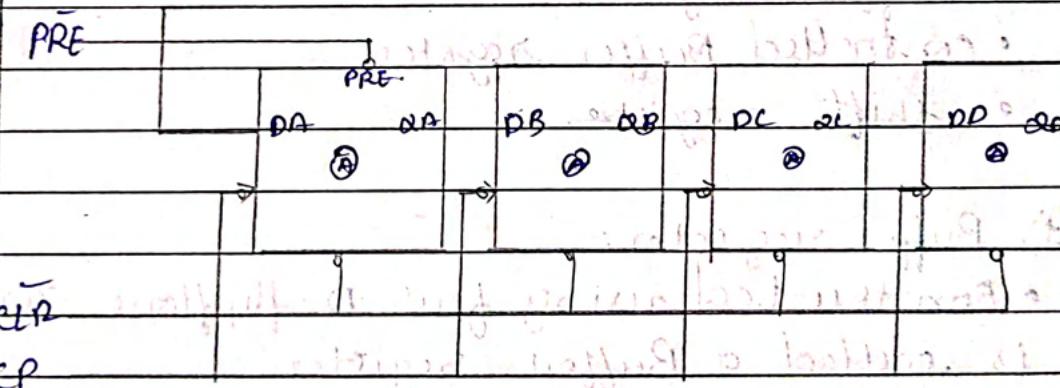
2) Controlled Buffer register:

- We can control Input and output of the register by connecting tri-state devices at the input and output sides so it is called Controlled Buffer register.

- Transistor switches are used to control the operation.
- (e) Shift register:
 • The binary information in a register can be moved from stage to stage within the register or into the or out of the register upon application of clock pulses.
- This type of bit movement or shifting is essential for certain arithmetic and logic operation used in microprocessor. This gives rise to a group of registers called shift registers.

Q4/
iii)

Ring Counter



- The output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage.
- The CLR followed by PRE makes the output of first stage '1' and remaining outputs are zero i.e. QA is one and QB, QC, QD are zero.

- The first clock pulse produces $Q_3=1$ and remaining outputs are zero.
- The first clock pulse produces $Q_2=1$ & remaining zeros.
- According to the clock pulses applied at the clock pulses applied at the clock input CP, a sequence of four states is produced.

Q5/1

→ Steps involved in the design of asynchronous counter.

- 1) Determine the number of flipflops needed.
- 2) Choose the type of flip-flops to be used: T or JK
 If T flipflops are used connect J input of all flipflops to logic 1. If JK flipflop are used connect both J and K inputs of all flip-flops to logic 1 - such connections toggle the flip-flop output on each clock transition.
- 3) Write the truth table for the counter.
- 4) Derive the reset logic by K-map simplified.
- 5) Draw the logic diagram.



12.Assignment 4

CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 4

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

Assignment - 4

Module - 4

Q-1

→ Weighted resistor converter: It weighted register DAC produces an analog output, which is almost equal to the digital input by using binary weighted resistor in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

E

- The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistor $2R, 4R, 8R, 2^{nd} R$
- For ON switch; $I = \frac{V_R}{R}$ and
- For OFF, $I = 0$.
- Due to high input impedance of op-amp summing current will flow through R_f hence the total current through R_f can be given as

$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

When $R_f = R$, V_o is given as

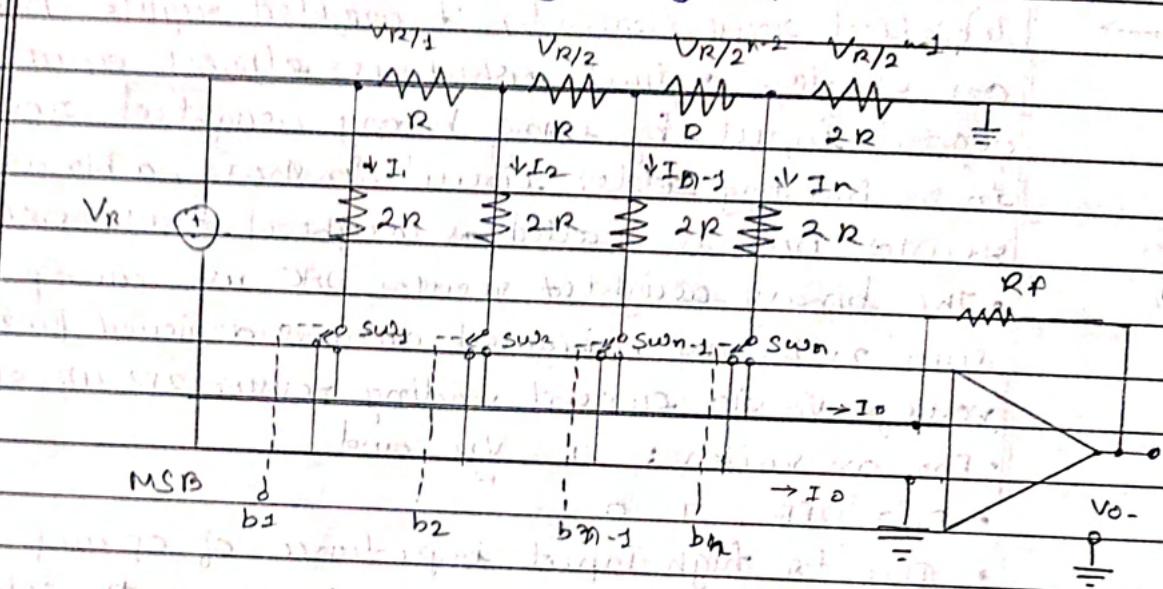
$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Q-2

→ R/2R ladder D/A converter uses only two resistor values. This matches resistance spread drawback of binary weighted D/A converter.

- Easier to build accurately as only two precision metal film resistors are required
- Number of bits can be expanded by adding more sections of same R/2R value

- In Inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any削減 effect by stray capacitance.



Q3

→ Specifications of DA converter

1) Resolution:

- The smallest change that occurs in an analog output as a result of a change in the digital input.

→ D/A resolution = step size / full scale $\times 100\%$.

• Full scale = No. of steps \times step size

$$\therefore \text{resolution} = 1/\text{No. of steps} \times 100\%.$$

2) Accuracy

- Specified in terms of full scale error and linearity error.

3) Setting time :

- The time required for the analog output to settle to within $\pm 1/2$ LSB of the final value after a change in the digital input.

4) Monotonicity:

- This means that the staircase output will have no downward steps as the binary input is incremental from 0 to full scale value.

5) Temperature sensitivity:

- The analog output voltage for any fixed digital input varies with temperature.

2. Specifications of A/D converter

1) Range of input voltage

2) Input impedance

3) Accuracy

4) Conversion time

5) Format of digital output

Q.11

→ Quantizing / Encoding → The process of mapping the sampled analog voltage values to discrete voltage levels, which are then represented by binary number (bits). This is needed because the analog sample values are real numbers that occur on a continuum.

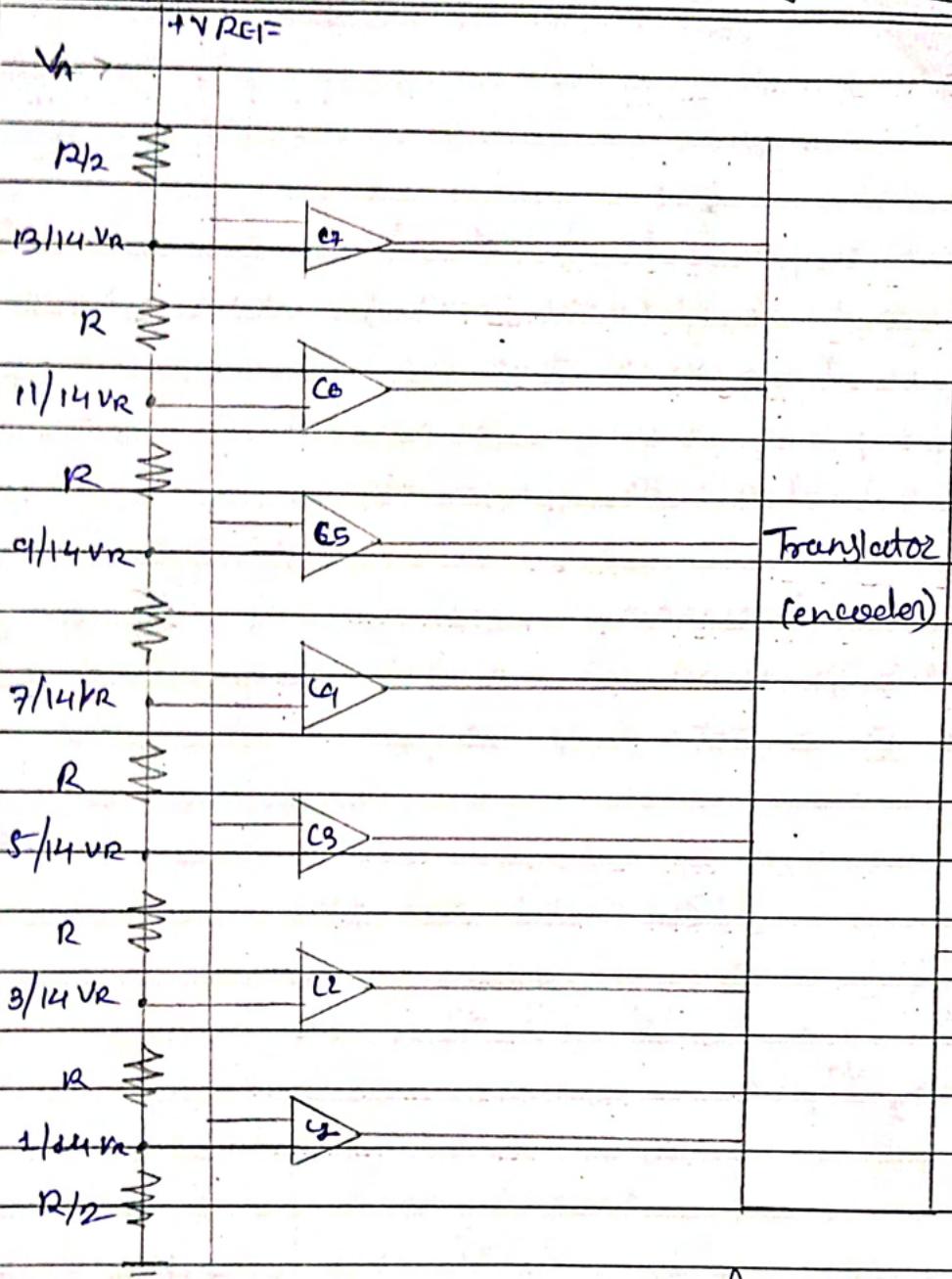
$$q = \frac{V_{max} - V_{min}}{2^n} = \frac{0.7 - (-1)}{8} = 0.25V$$

* The value of q is also formally called the quantization resolution.

Q.12

→ This circuit is formed of a series of comparators, each one comparing the input signals to a unique reference voltage. The comparator outputs connect to the input of a priority encoder circuit, which then produces binary output.

- Based on the principle of comparing analog input voltage with a set of reference voltage.
- To convert the analog input voltage into a digital voltage of n-bit output, (2^{n-1}) comparators are required.
- It is the fastest type of ADC because the conversion is performed simultaneously through a set of comparators hence referred as flash type ADC.
- Construction is simple and easier to design.



13. Assignment 5

CO5: Implement PLDs for the given logical

problem. Module 5

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA)

Assignment-5

Module-5

Q/

→ The time required to find an object stored in memory can be reduced considerably if objects are selected based on their contents, not on their location. A memory unit accessed by its content is called an associative memory or content addressable memory (CAM).

• This type of memory is accessed simultaneously and in parallel on the basis of data content rather than by specific address or location.

Segment register (A)

Key register (K)

Match register

Input → Associative memory

Read → array & logic

m-words

n-bits per word.

→ M

→ m

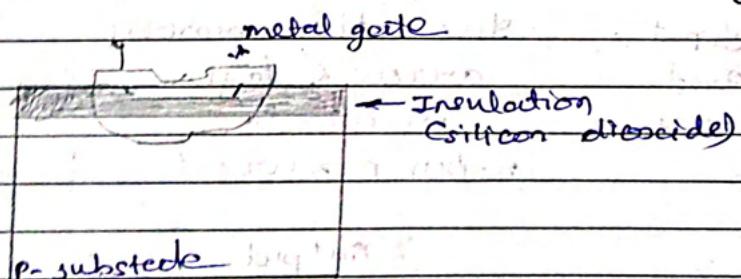
Output

(Block diagram of associative memory).

~~Q7~~ →

charge-coupled device (CCD) memory is a type of dynamic memory for which packets of charge are continuously transferred from one MOS device to another. The structure of MOS charge-coupled device is quite simple as shown in fig -

- When a high voltage is applied to the metal gate, holes are repelled from a region beneath the gate in the p-type substrate. This region, called a potential well, is then capable of accepting a packet of negative charges of electrons. Therefore, data is stored in a CCD as charge, and it is transferred from one device to an adjacent one by clocking their gates.
- It's simple cell structure. It makes it possible to construct large-capacity memories at low cost.
- CCDs are dynamic in nature, they must be periodically refreshed and must be driven by rather complex, multiphase clock signals.



2) \rightarrow Non-volatile memory

i) Read only Memory (ROM)

- Mask programmable ROM
- Programmable ROM

ii) Read/Write Memory (NVRAM)

- EEPROM
- EEROM
- Flash

Volatile memory

i) Read/Write memory (RAM)

- (a) Random access memory (RAM)
 - SRAM

- DRAM

(b) Non-random Access

- FIFO

- LIFO

- Shift register

- The volatile memory which can hold data as long as power is ON are called static RAMs (SRAMs)
- The dynamic RAM (DRAM) stores the data as a charge on the capacitor and they need refreshing of charge on the capacitor after every few milliseconds to hold the data even if power is OFF.
- EPROM or EEPROM are erasable memory in which the stored data can be erased and new data can be stored.

Q/1
→

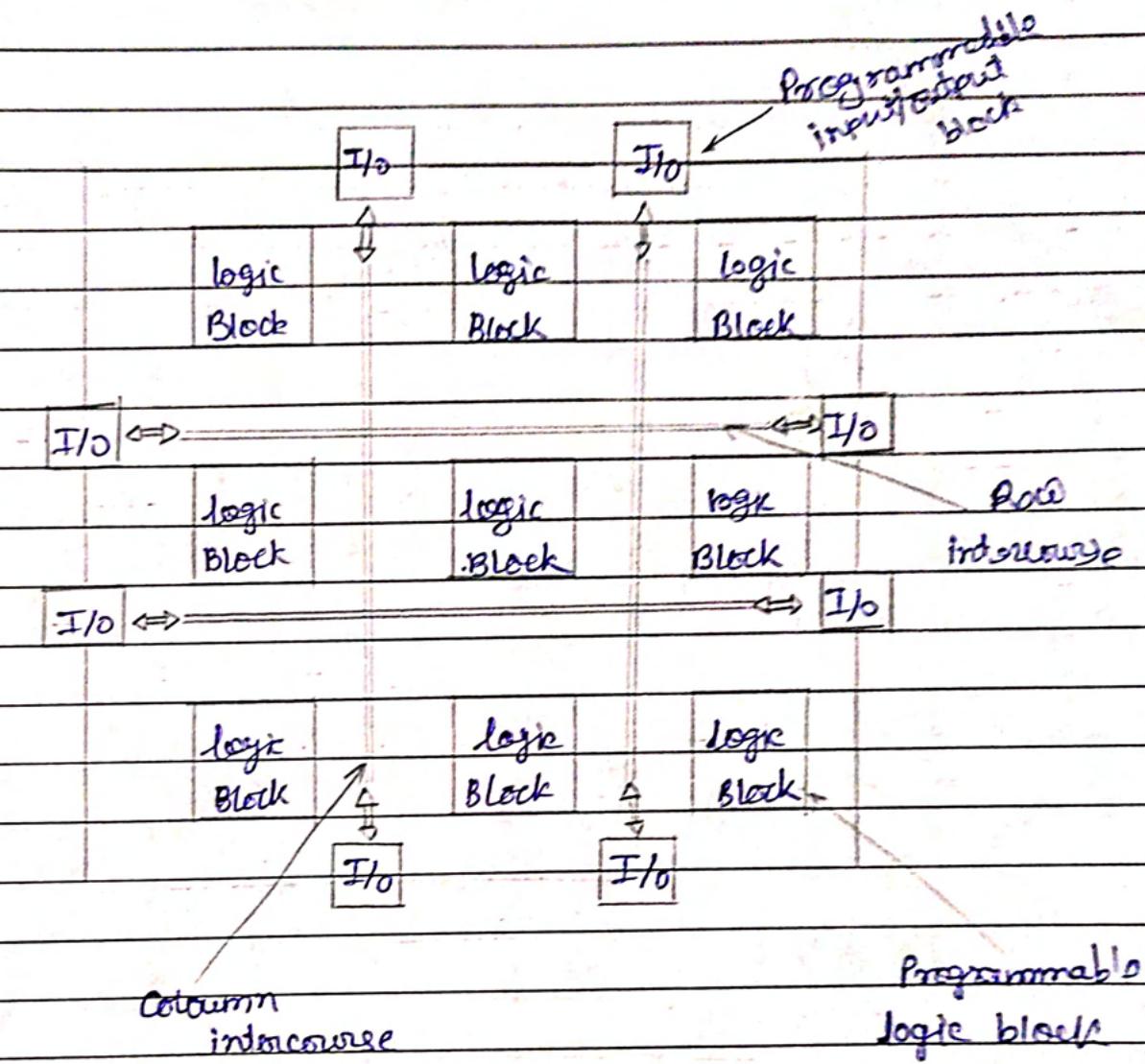
A semiconductor is a substance that has specific electrical properties that enable it to serve as a foundation for computers and other electronic devices. It is typically a solid chemical element or compound that conducts electricity under certain conditions but not others.

- Semiconductors are materials which have conductivity between conductors (generally metals) and insulators.
- Semiconductors can be pure elements such as silicon or germanium or compounds such as gallium arsenide or cadmium selenide.

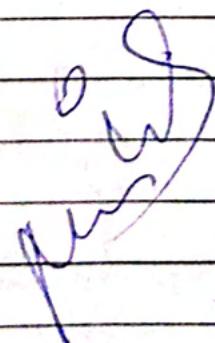
Q/2
→

Field programmable gate array (FPGA) provide the next generation in the programmable logic devices.

- The word field in the name refers to the ability of user arrays to be programmed for a specific function by the user instead of by the manufacturer of the device.
- The word array is used to indicate a series of columns and rows of gates that can be programmed by the end user.
- The programmable logic blocks of FPGA, are called logic blocks or configurable logic blocks (CLBs).



* Basic architecture of FPGA



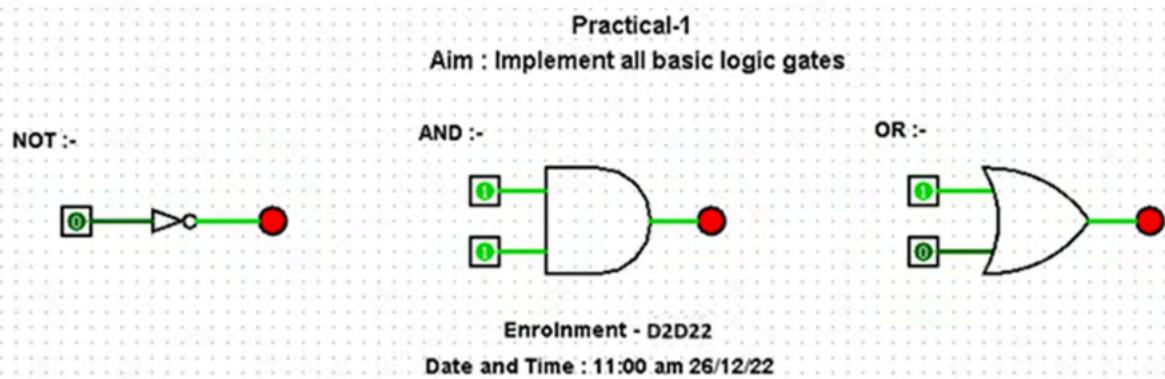
14. Practical 1

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

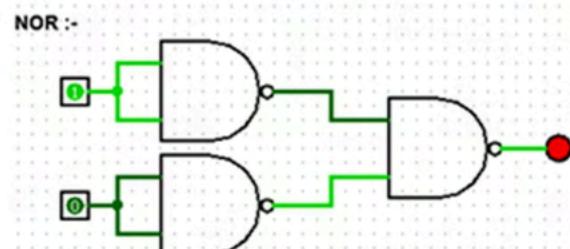
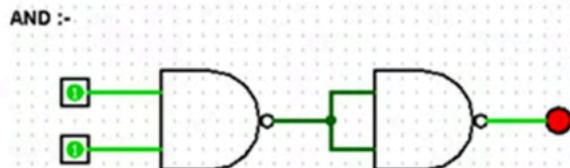
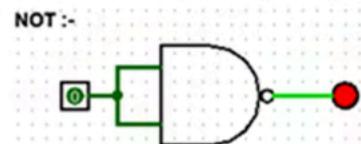
Module 1

Aim: Getting familiar with Logisim, Study and implement all basic logic gates.
Implement NAND and NOR logic gates as universal gates.

Code:

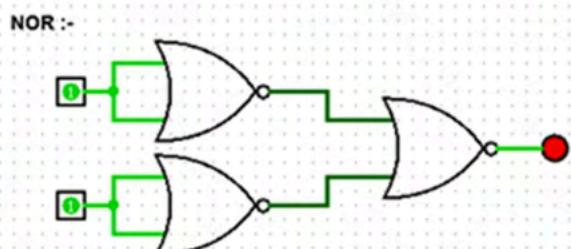
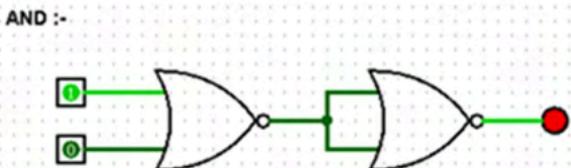
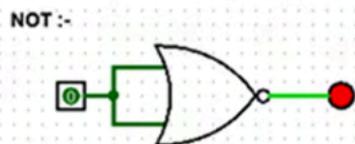


Practical-1
Aim : Implement NOR Gate as universal gate



Enrolment - D2D22
Date and Time : 11:00 am 26/12/22

Practical-1
Aim : Implement NOR Gate as universal gate



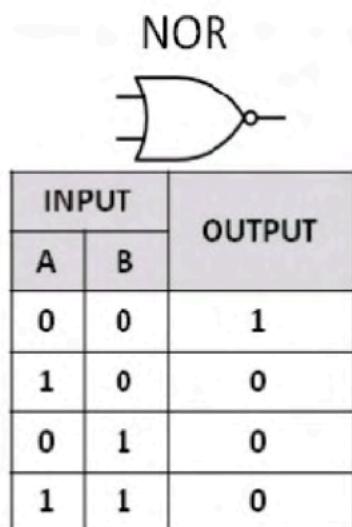
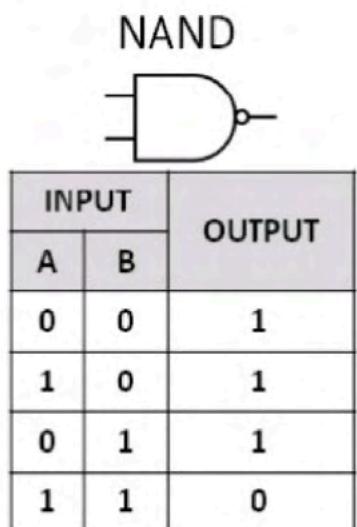
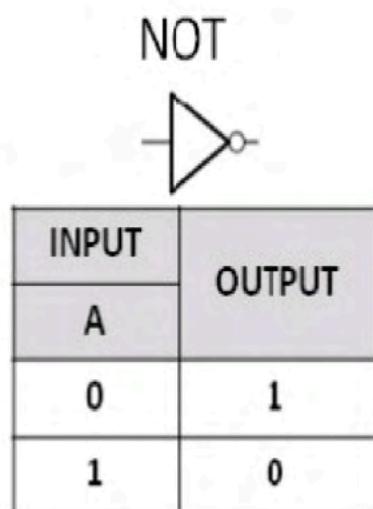
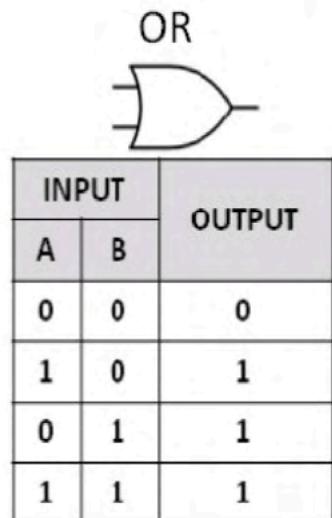
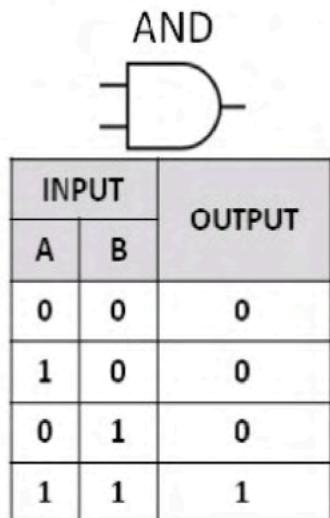
Enrolment - D2D22
Date and Time : 11:00 am 26/12/22

Brief Explanation & Truth Tables:

In an OR gate, the output of an OR gate attains state 1 if one or more inputs attain state 1.

In the AND gate, the output of an AND gate attains state 1 if and only if all the inputs are in state 1.

In a NOT gate, the output of a NOT gate attains state 1 if and only if the input does not attain state 1.



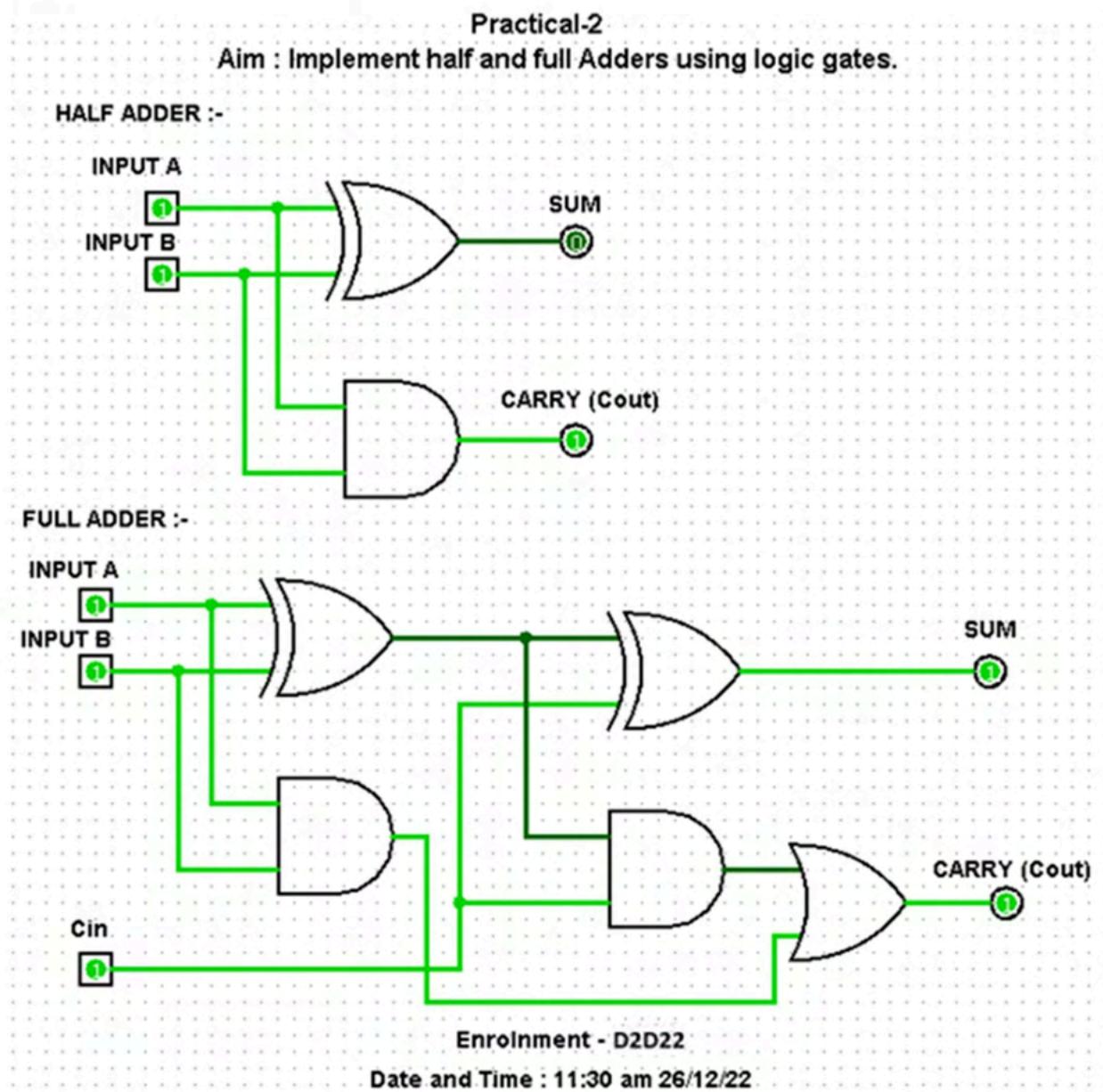
15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Adders using logic gates.

Code:



Brief Explanation & Truth Tables:

A half-adder circuit consists of two input terminals- namely A and B. Both of these add two input digits (one-bit numbers) and generate the output in the form of a carry and a sum.

Input		Output	
A	B	CARRY	SUM
0	0	0	0
1	1	1	0
0	1	0	1
1	0	0	1

The full adder adds three binary digits. Among all the three, one is the carry that we obtain from the previous addition as C-IN, and the two are inputs A and B. It designates the input carry as the C-OUT and the normal output as S

Input			Output	
A	B	C	SUM	CARRY OUT
0	0	0	0	0
1	1	1	1	1
0	1	1	0	1
1	0	1	0	1
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

16. Practical 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

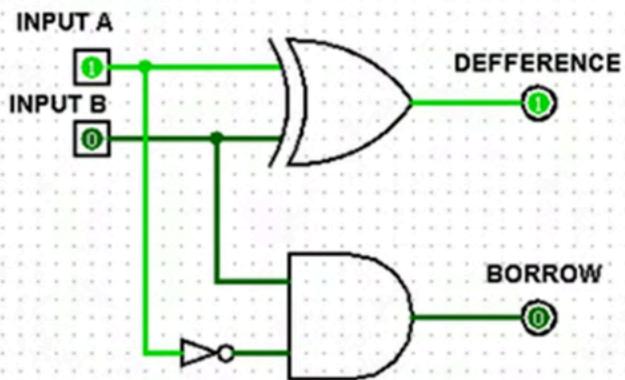
Aim: Implement half and full Subtractors using logic gates.

Code:

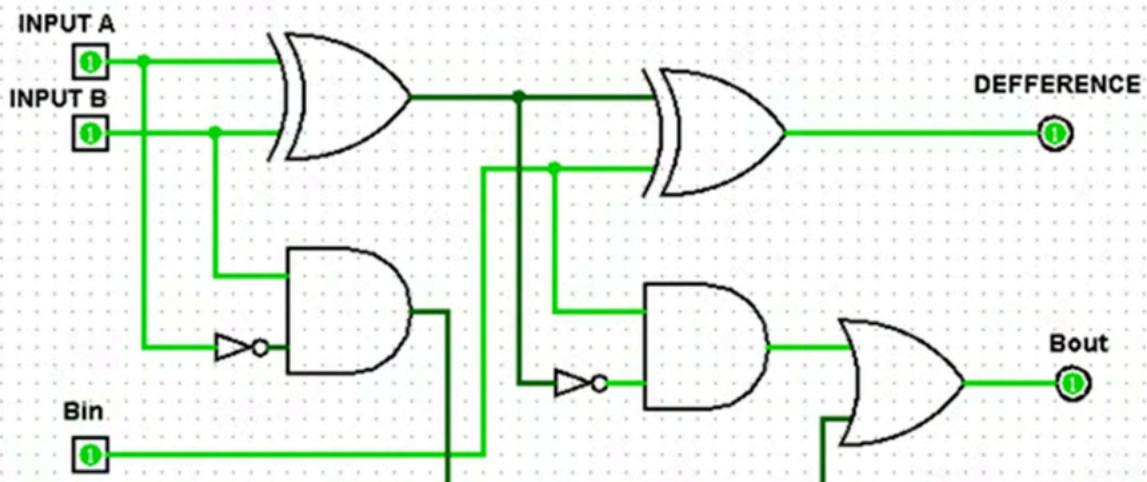
Practical-3

Aim : Implement half and full Subtractor using logic gates.

HALF ADDER :-



FULL ADDER :-



Enrolment - D2D22

Date and Time : 12:00 am 26/12/22

Brief Explanation & Truth Tables:

The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively.

Half Subtractor Truth Tables:

Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor Truth Table:

Inputs			Outputs	
A	B	Borrow _{in}	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

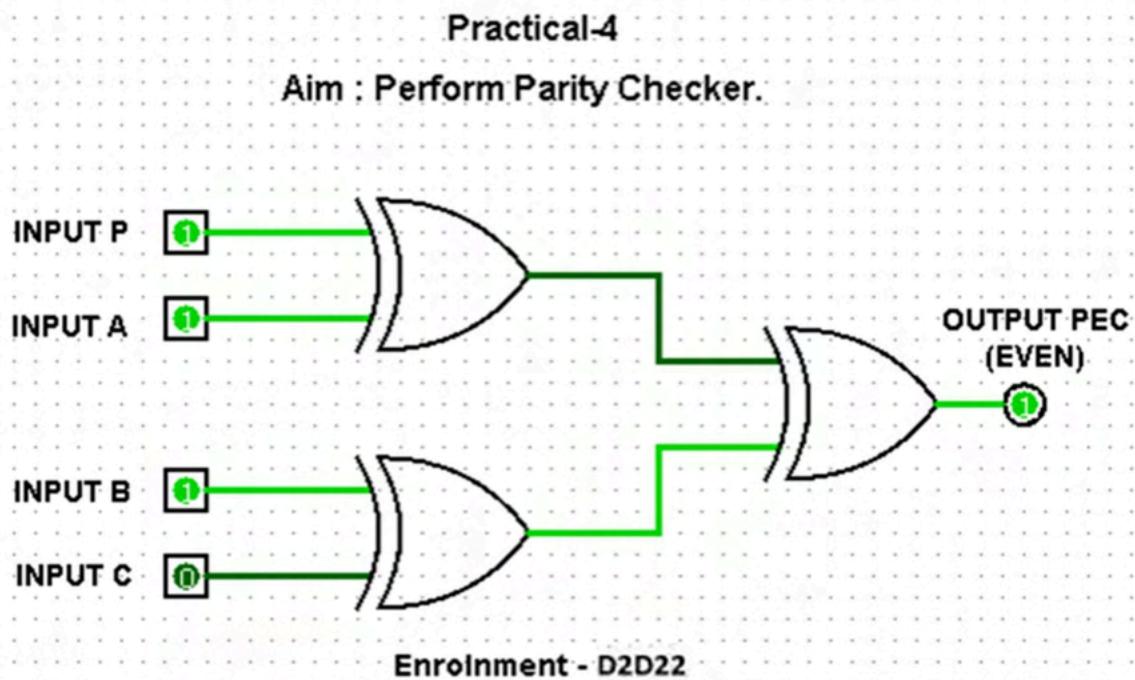
17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Perform Parity Checker

Code:



D_3	D_2	D_1	D_0	Even-parity P	Odd-parity P
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

18. Practical 5

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

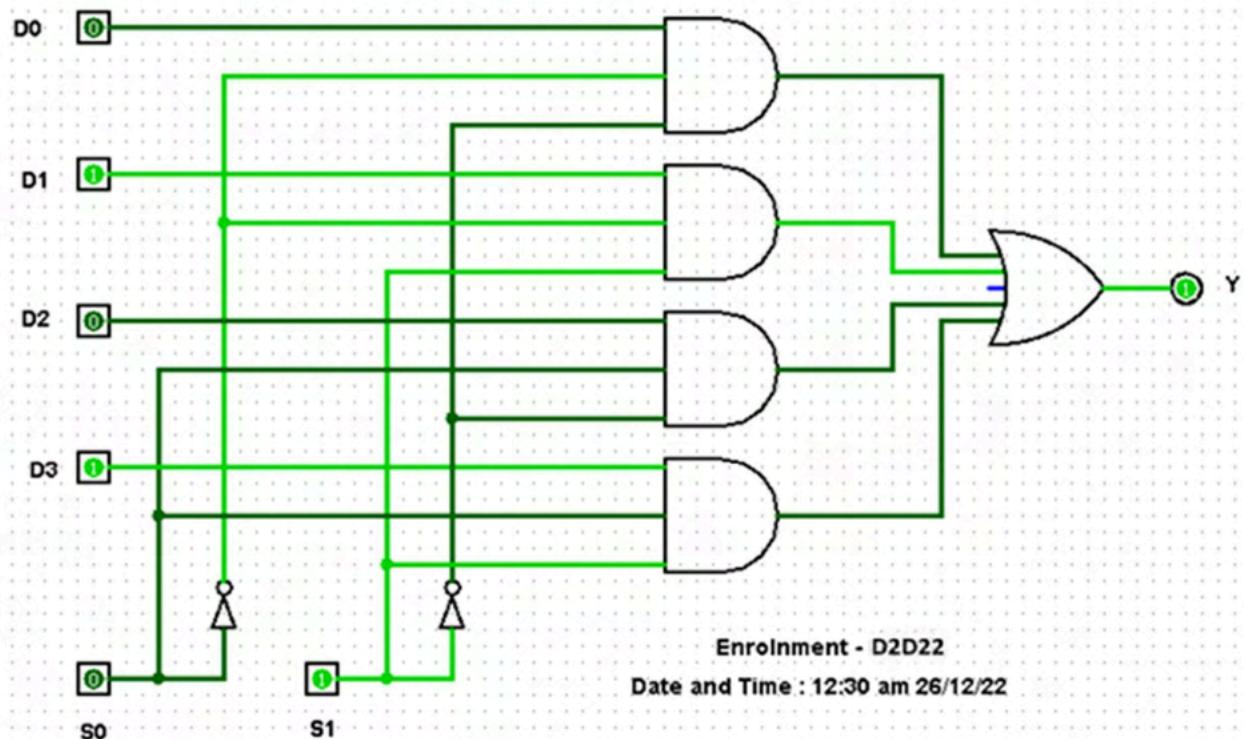
Aim: Study and implement Multiplexer and Demultiplexer.

Code:

4:1 Multiplexer

Practical-5

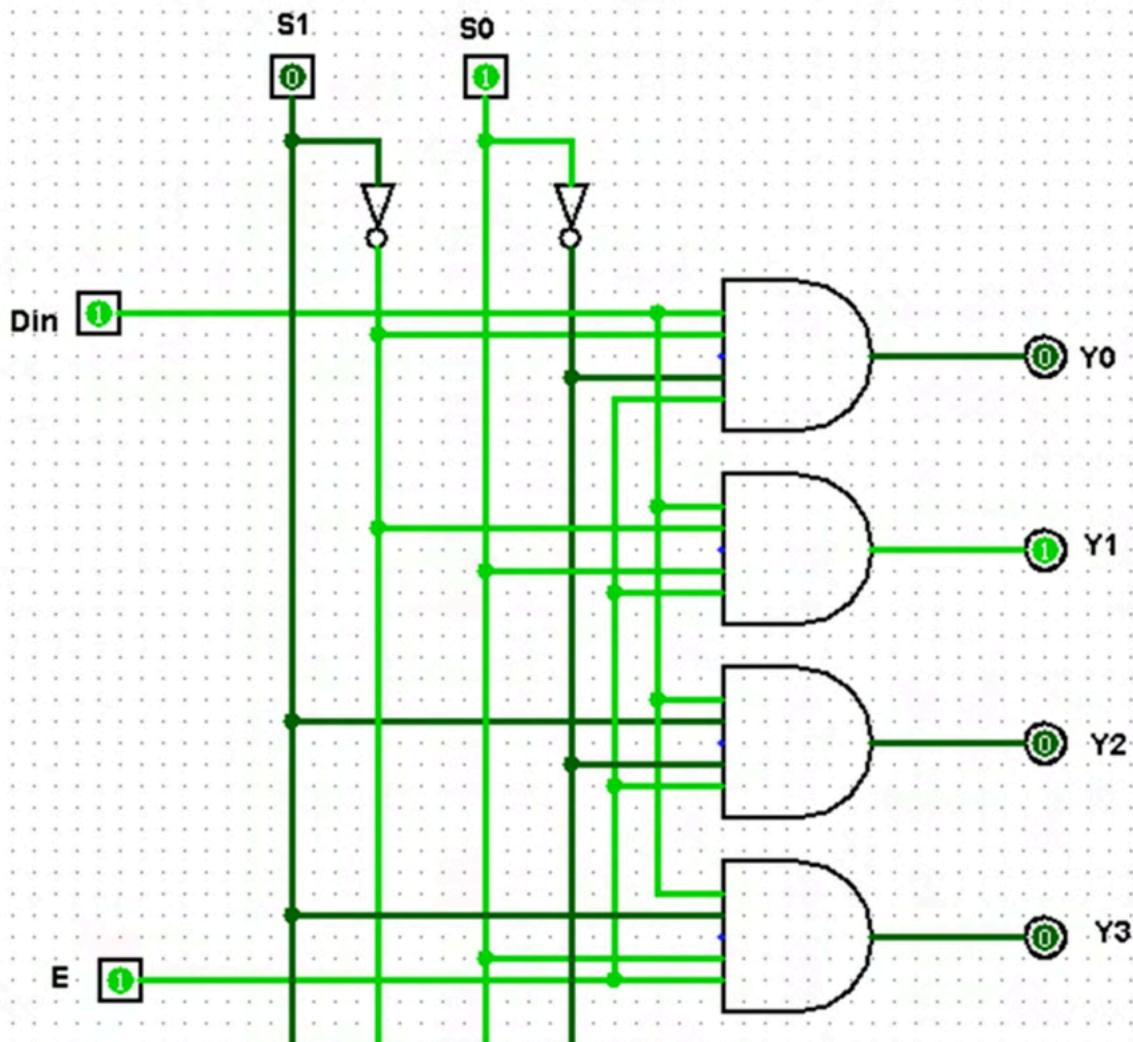
Aim : Study and implement Multiplexer and Demultiplexer.



1:4 Demultiplexer

Practical-5

Aim : Study and implement Multiplexer and Demultiplexer.



Enrolment - D2D22

Date and Time : 12:30 am 26/12/22

Brief Explanation & Truth Tables:

Multiplexer:

A multiplexer is a combinational circuit that has 2^n input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit.

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Demultiplexer:

A De-multiplexer is a combinational circuit that has only 1 input line and 2^N output lines. Simply, the multiplexer is a single-input and multi-output combinational circuit.

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

19. Practical 6

CO3: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 2

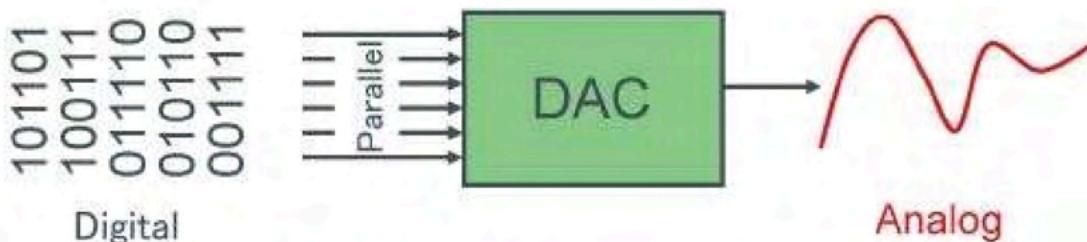
Aim: Study and configure A to D convertor and D to A convertor.

Code:

What is Analog to Digital Converter?

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.

- Analog signals are directly measurable quantities.
- Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.



Application of Analog to Digital Converter:

ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.

- Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.
- Microcontrollers commonly use 8, 10, 12, or 16-bit ADCs, our micro controller uses an 8 or 10-bit ADC

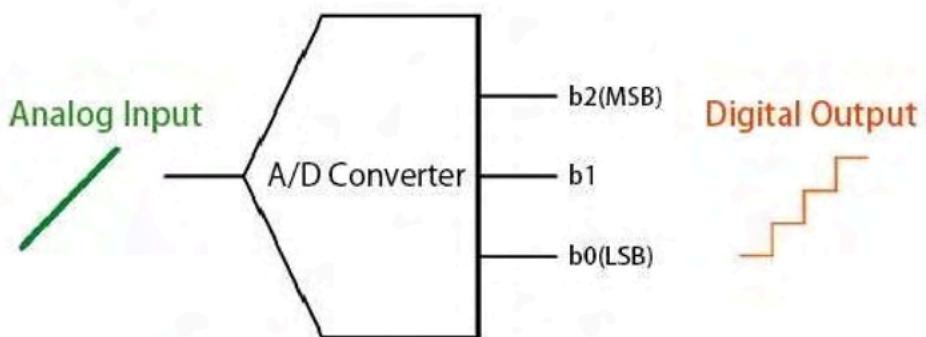
Types of Analog to Converters (ADC):

- Successive Approximation A/D Converter
- Flash A/D Converter
- Delta-Sigma A/D Converter

What is a Digital to Analog Converter?

Digital to analog converting is a process where digital signals that have a few (usually two) defined states are turned into analog signals, which have a theoretically infinite number of states. A Digital to Analog Converter, or DAC, is an electronic device that converts a digital code to an analog signal such as a voltage, current, or electric charge.

Signals can easily be stored and transmitted in digital form; a DAC is used for the signal to be recognized by human senses or non-digital systems. Converting a signal from digital to analog can degrade the signal.



Applications for Digital to Analog Converters:

An example can be found in the processing of computer data by a modem into audio-frequency tones transmitted over a telephone line. The circuit that performs this is a digital to analog converter. In music players, digital to analog converters can be used for generation of audio signals from digital information. In TVs and cell phones, digital video signals are converted into analog in order to display colors and shades.

In VoIP applications, the source is first digitized for transmission through an analog to digital converter and is then reconstructed into an analog signal using a DAC at the receiving end.

Types of Digital to Analog Converter (DAC):

- Binary Weighted Resistor D/A Converter Circuit
- Binary ladder or R-2R ladder D/A Converter Circuit
- Segmented DAC
- Delta-Sigma DAC

Analog Signal to Digital Signal Conversion Methods:

1. Sampling:

Sampling is the process of taking amplitude values of the continuous analog signal at discrete time intervals (sampling period T_s).

[Sampling Period $T_s = 1/F_s$ (Sampling Frequency)]

Sampling is performed using a Sample and Hold (S&H) circuit.

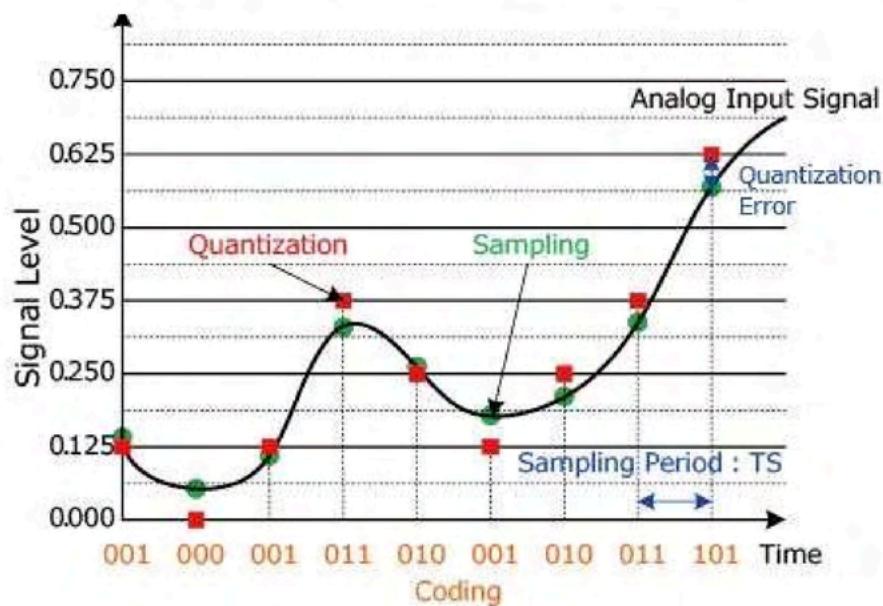
2. Quantization:

Quantization involves assigning a numerical value to each sampled amplitude value from a range of possible values covering the entire amplitude range (based on the number of bits).

[Quantization error: Sampled Value - Quantized Value]

3. Coding:

Once the amplitude values have been quantized they are encoded into binary using an Encoder.



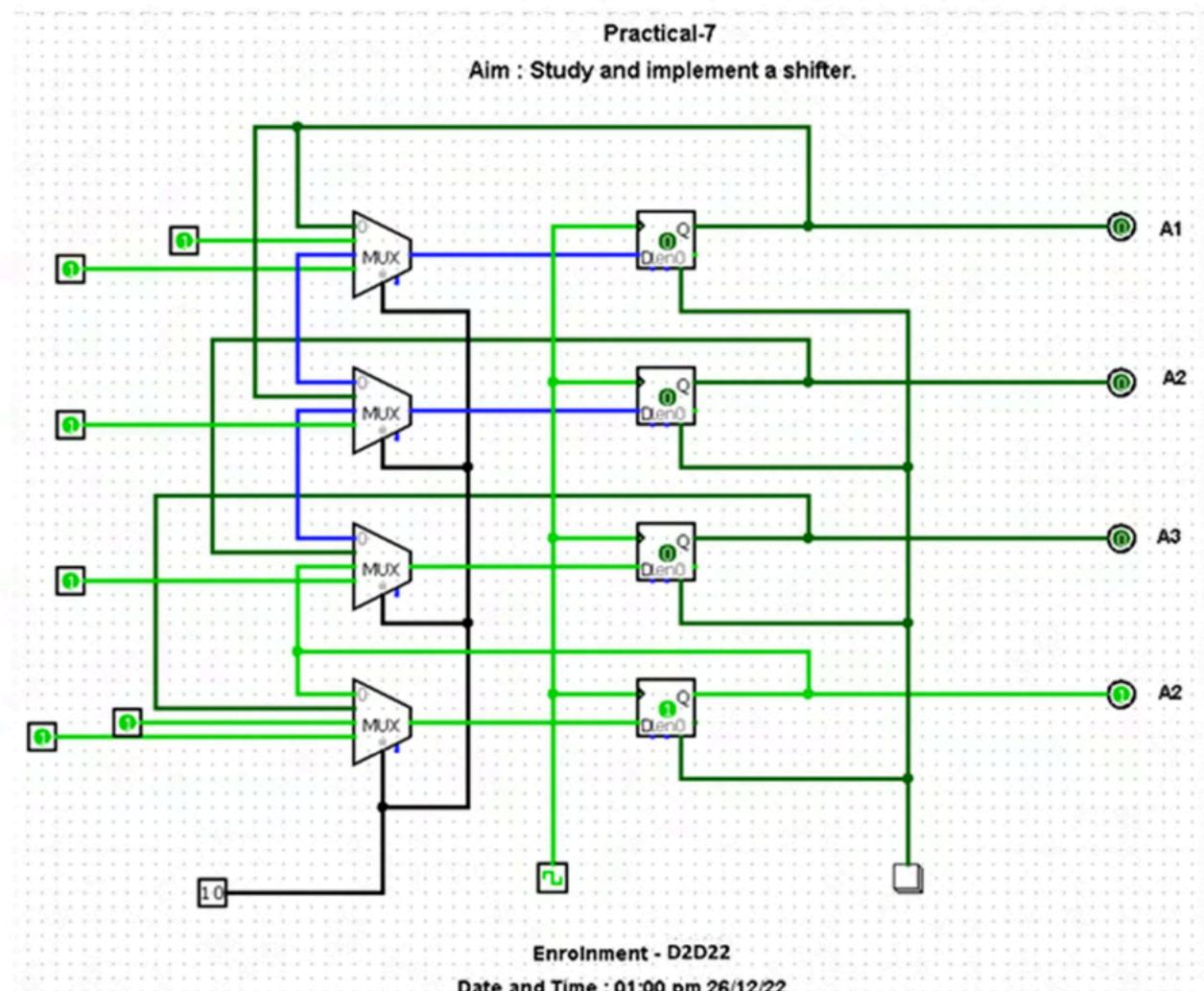
20. Practical 7

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Study and implement a shifter.

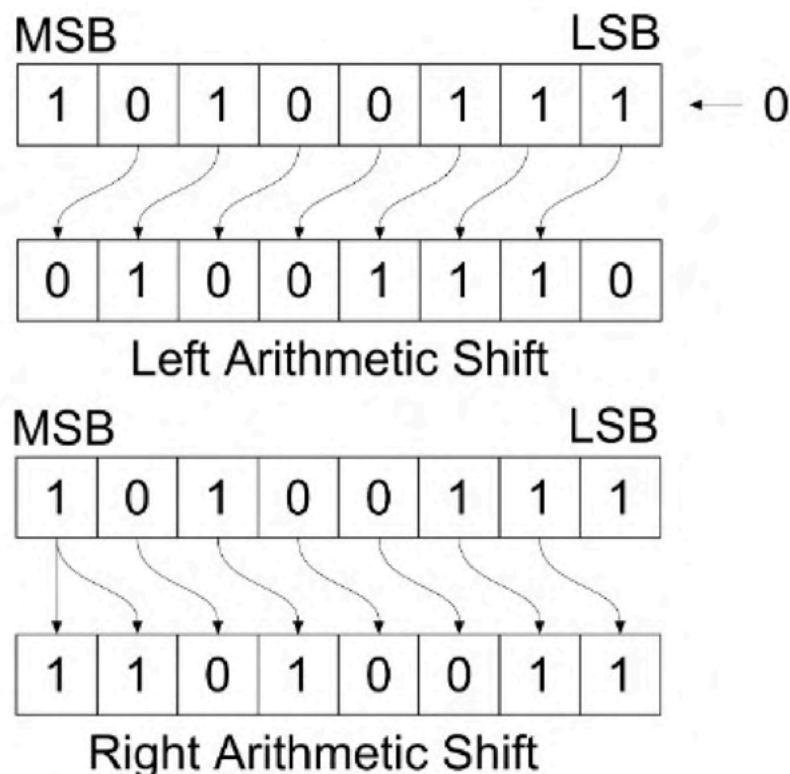
Code:



Brief Explanation & Truth Tables:

Arithmetic Shifter : is the same as a logical shifter, but on right shifts fills the most significant bits with a copy of the old most significant bit (MSB). This is useful for multiplying and dividing signed numbers Arithmetic shift left (ASL) is the same as logical shift left (LSL).

Truth Table:



21. Practical 8

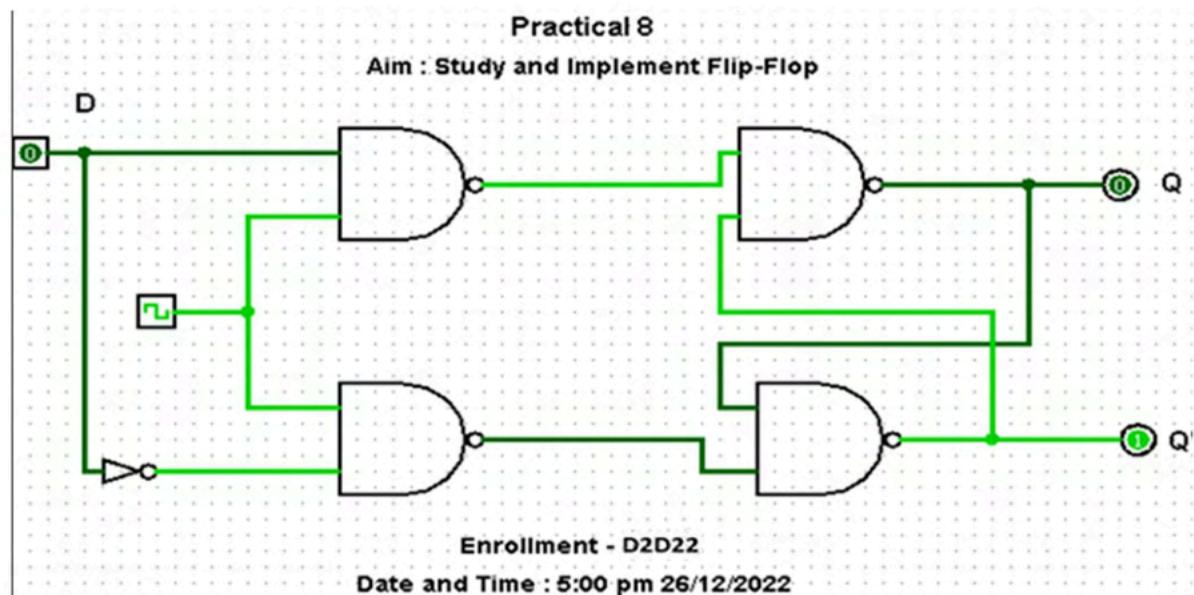
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

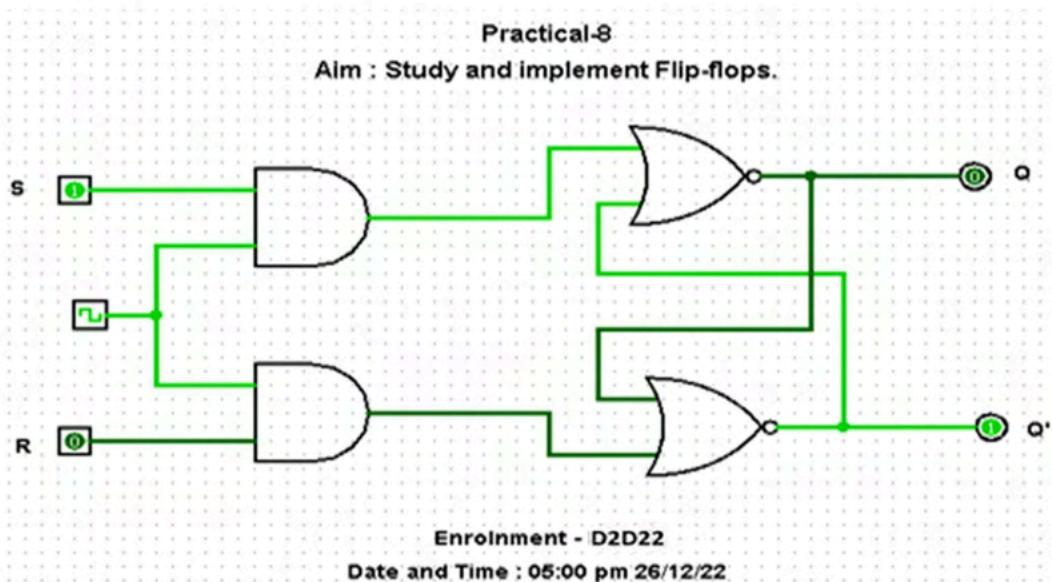
Aim: Study and implement Flip-flops.

Code:

SR Flip Flop



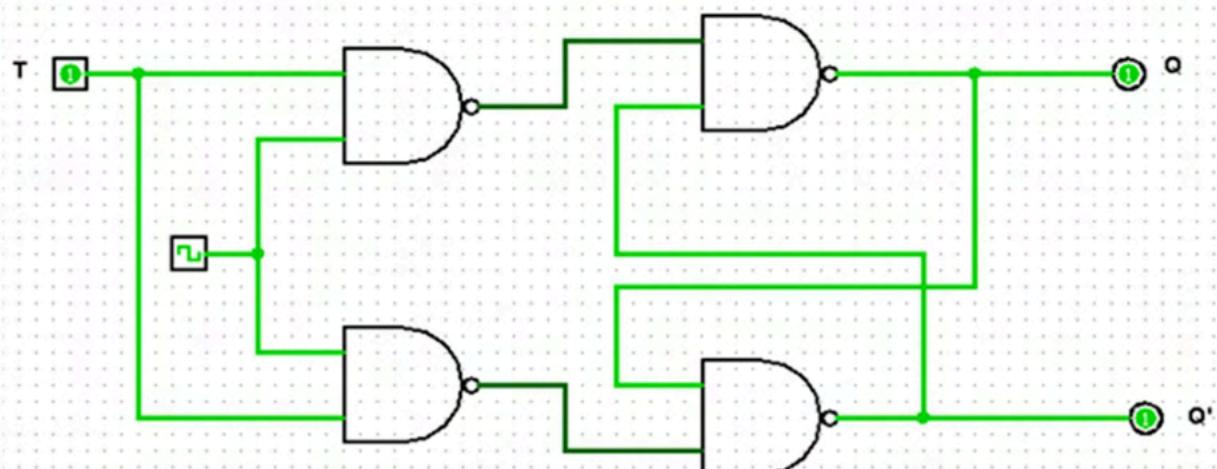
D Flip Flop



T Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



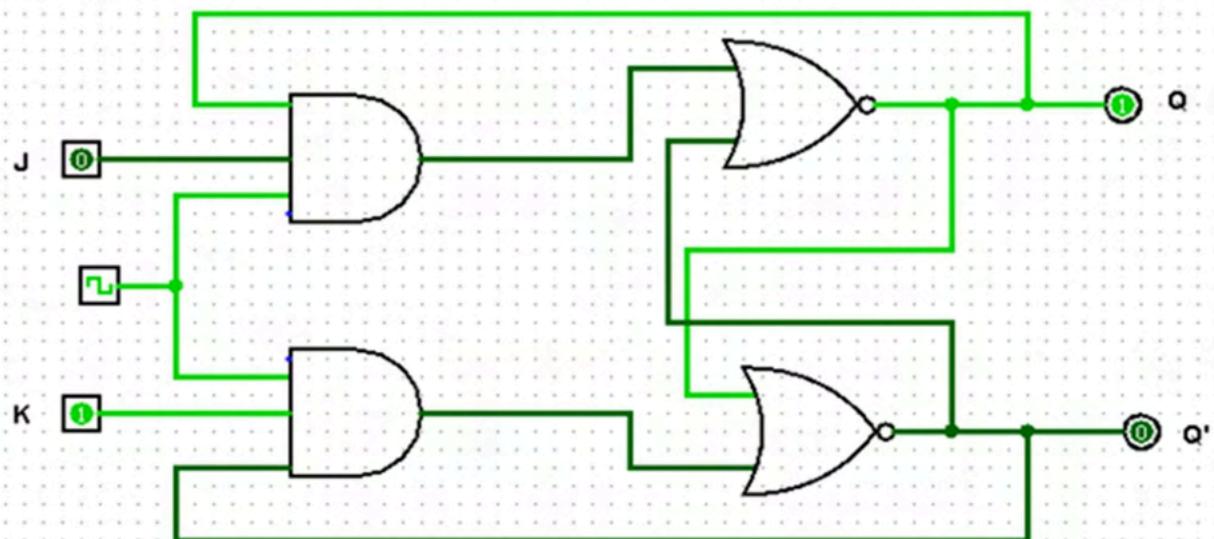
Enrolment - D2D22

Date and Time : 05:00 pm 26/12/22

JK Flip Flop

Practical-8

Aim : Study and implement Flip-flops.



Enrolment - D2D22

Date and Time : 05:00 pm 26/12/22

Brief Explanation & Truth Tables:

SR Flip Flop

A gated SR latch requires an Enable (EN) input.

Its S and R inputs will control the state of the flip flop only when the EN is high.

When EN is low, the inputs become ineffective and no change of state can take place.

Truth Table

En	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate (Invalid)
1	1	1	1	X	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

D Flip Flop

It differs from the S-R latch in that has only one input in addition to EN.

When D=1, we have S=1 and R=0, causing the latch to SET when ENABLED

When D=0, we have S=0 and R=1, causing the latch to RESET when ENABLED

Truth Table

En	D	Q_n	Q_{n+1}	State
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set
1	1	1	1	
0	X	0	0	No Change (NC)
0	X	1	1	

JK Flip Flop

The JK flip flop is very versatile and also the most widely used.

The functioning of the JK flip flop is identical to that of the SR flip flop, except that it has no invalid state like that of SR flip flop.

Truth Table

En	J	K	Q_n	Q_{n+1}	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	0	
0	X	X	0	0	No Change (NC)
0	X	X	1	1	

T Flip Flop

A T flip flop has a single control input, labeled T for toggle.

When T is HIGH the flip flop toggles on every new clock pulse.

When T is LOW the flip flop remains in whatever state it was before.

Truth Table

En	T	Q_n	Q_{n+1}	State
1	0	0	0	No Change (NC)
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	
0	X	0	0	No Change (NC)
0	X	1	1	

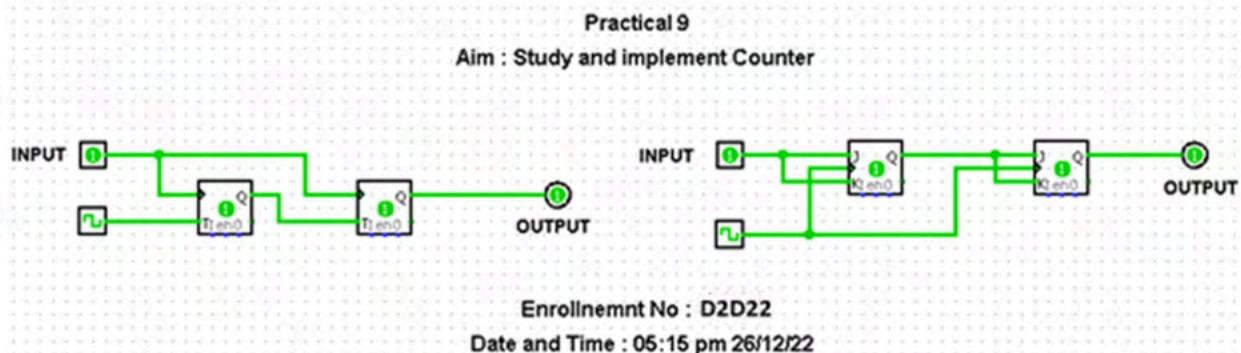
22. Practical 9

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and Implement Counter

Code:



Brief Explanation & Truth Tables:

Asynchronous Counter

The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle(T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic

External clock is applied to the clock input of flip-flop A and Q A output is applied To the clock input of the next flip-flop.

Synchronous Counter

If the "Clock" pulses are applied to all the flip flop in counter simultaneously, Then such a counters are called synchronous counter.

In this type of counter there is no connection between the output of first FF and clock input of next FF and so on.

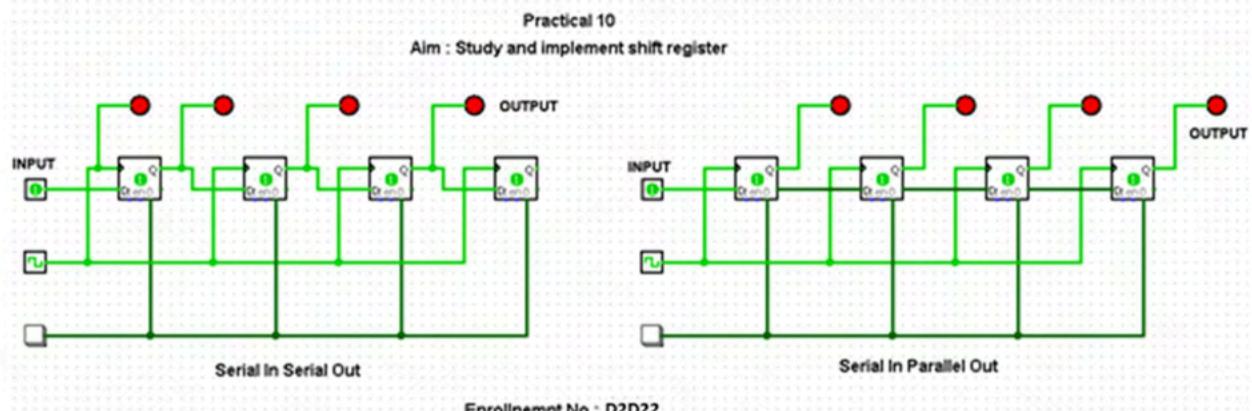
23. Practical 10

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

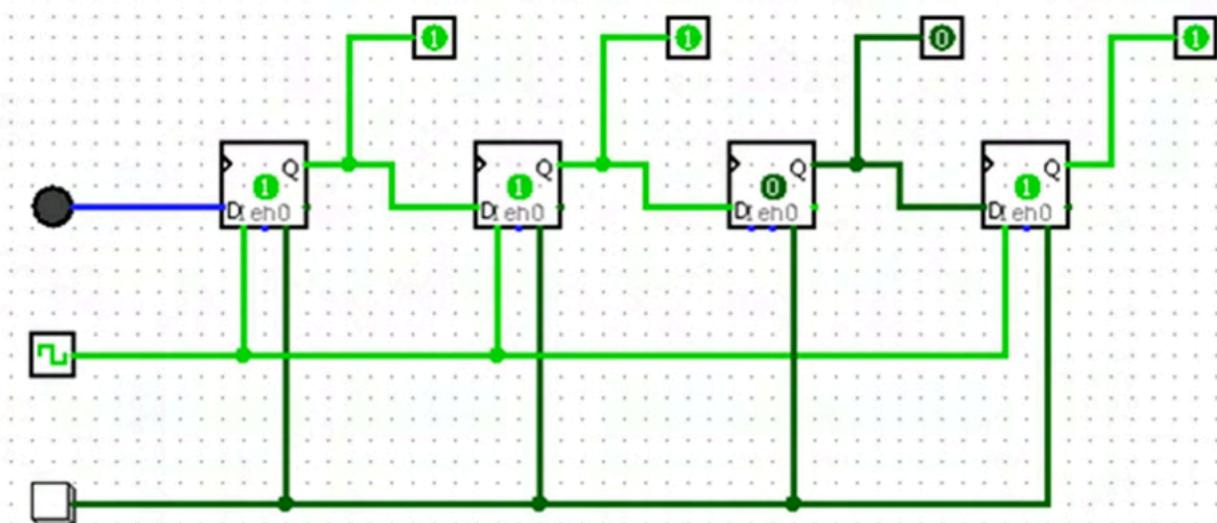
Module 3

Aim: Study and Implement a shift register

Code:

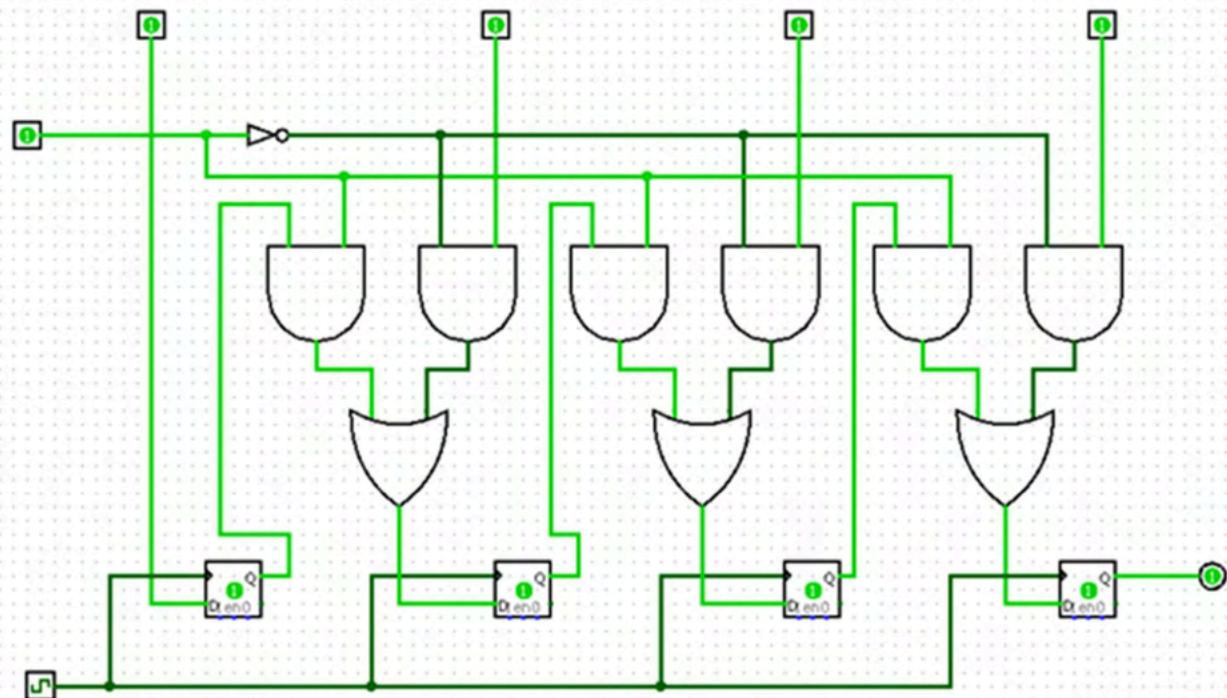


Practical 10
Aim : Study and implement shift register



Enrollment No : D2D22
Date and Time : 05:30 pm 26/12/22

Practical 10
Aim : Study and implement shift register



Enrollment No : D2D22
Date and Time : 05:30 pm 26/12/22

Brief Explanation:

A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.

Data may be shifted into or out of the register either in serial form or in parallel form.

So, there are four basic types of shift registers:

- serial-in, serial-out
- serial-in, parallel-out
- parallel-in, serial-out
- parallel-in, parallel-out

Data may be rotated left or right. Data may be shifted from left to right or right to left at will, i.e. in a bidirectional way.

Also, data may be shifted in serially (in either way) or in parallel and shifted out serially (in either way) or in parallel.

24. Practical 11

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and Implement K-Map for the given function:(SOP)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

Code:

Step 1: Finding the number of variables to build the K-map

$$\text{Number of variables} = 4(A, B, C, D)$$

So 4 variable K-map is to be used

Step 2: Filling cells of K-map for SOP with 1 respective to the min-terms for given equation

		CD	00	01	11	10		
AB	00	0		1		3		4
		4		5		7		6
AB	11	12		13		15		14
		8		9		11		10

Step 3: We create rectangular groups that contain total terms in the power of two like 2,4,8 and so on. Try to cover as many elements as we can cover in one group.

		CD	00	01	11	10		
AB	00	1	0		1	3	1	4
		4		5		7		6
AB	11	12	1	13		15		14
		8		9		11	1	10

Step 4: With the help of these groups, we find the product terms and sum of them for the SOP form $Y = ABC'D + B'D'$