Government Engineering College
Sec-28 Gandhinagar

Sem: - 3

Subject: - Digital Fundamental

Subject Code: - 3130704

Government Engineering College

Sec-28 Gandhinagar

Certificate

This is to certify that

Mr./~~Ms.~~ KALP M PATEL *Of class*

CE-B *Division* B4 *, Enrollment No.* 22D-46 *Has*

Satisfactorily completed his/her term work in

digital fundemental *Subject for the term ending in*

Jan/to 2022

Date: -

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department Vision/Mission

Vision:

- To achieve excellence for providing value based education in computer engineering through innovation, teamwork and ethical practices.

Mission:

- To produce computer science and engineering graduates according to the needs of industry, government, society and scientific community
- To develop partnership with industry government agencies and R&D organization.
- To motivate student/graduate to be entrepreneurs
- To motivate students to participate in reputed conferences workshops, symposiums seminars and related technical activities.

Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of

mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	Solve the given problem using fundamental of number system and boolean algebra.
CO-2	Analyze working of logic family and logic gates and design the simple circuit using various gates for a ~~design~~ given problem
CO-3	Design and implement combinational and sequential logic circuit and verify its working.
CO-4	Examine the process of analog to digital conversion and digital to analog conversion.
CO-5	Implement PLDs for the given logic problem

7. Assignment Index

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8. Practical Index

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Assignment-1

* Module-1

① State and explain De morgan's theorem with truth table

-) De morgan suggested two theorem that form an important part of Boolean algebra. In the eqn form, they are

1) $\overline{AB} = \bar{A} + \bar{B}$
2) $\overline{A+B} = \bar{A} \cdot \bar{B}$.

Theorem 1 ($\overline{AB} = \bar{A} + \bar{B}$) : The complement of a product is equal to the sum of the complements. This is illustrated by truth table below.

A	B	$\overline{AB}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Theorem 2 ($\overline{A+B} = \bar{A} \cdot \bar{B}$) :- The complement of a sum is equal to the product of the complements. This is illustrated by truth table below.

A	B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

(2) Simplify Boolean function : $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}$

$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}$

$F = \bar{A}C(\bar{B} + \bar{B}) + A\bar{B}$ (complementary property $A + \bar{A} = 1$)

$F = \bar{A}C \cdot 1 + A\bar{B}$

$\boxed{\therefore F = \bar{A}C + A\bar{B}}$

(3) list and explain logic Family.

→ A digital logic Family is a group of compatible devices with the same logic levels and supply voltages.

→ According to components used in the logic Family digital logic Family are classified.

- Advantages of digital integrated circuits (ICs)

1) ~~are~~ extremely small in size
2) low power consumption
3) Reliability
4) Reduced cost.
5) very small weight.
6) easy replacement.
7) operating speed is higher.

- Classification of logic Families:-

- Digital ICs
  - Bipolar
    - Saturated
      - Resistor Transistor logic (RTL)
      - Diode Transistor logic (DTL)
      - Direct coupled transistor logic (DCTL)
      - integrated injection logic (I^2L)
      - High Threshold logic (HTL)
      - Transistor Transistor logic (TTL)
    - unsaturated
      - Schottky TTL
      - Emitter coupled logic (ECL)
  - unipolar
    - P-MOS (P-channel MOSFET)
    - N-MOS (n channel MOSFET)
    - CMOS (complementary MOSFET)

- Characteristics of digital integrated circuits (ICs)

1) Fan out
2) Power dissipation
3) Propogation delay
4) Noise Margin
5) Fan in

6) operating temperature
7) power supply requirements
8) speed.

4) Describe error detecting & correcting code.

-) when the digital information in the binary Form is transmitted from one circuit or system to another circuit or system an error may occur. This means a signal corresponding to 0 may change to 1 or vice-versa due to presence of noise.

-) To maintain the data integrity between transmitter and receiver, extra bit or more than one bit are added in the data.

-) These extra bits allow the detection and some times correction of errors in data. The data along with the extra bit/bits forms the code.

-) Codes which allow only error detection are called error detection codes and codes which allow error detection and correction are called error detecting and correcting codes.

- Parity Bit: It is used for the purpose of detecting error during transmission of Binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message, including the parity bit is transmitted and then checked at the receiving end for errors.

- An error is detected if the checked parity does not correspond with the one transmitted.

- The circuit that generates parity bit is called parity generator and the circuit that checks the parity in the receiver is called parity checker.

-) In even parity the added parity bit will make the total number of 1s an even amount. In odd parity the added parity bit will make the total number of 1s an odd amount.

-) Hamming code :- Hamming code not only provides the detection of a bit error, but also identifies which bit is in error so that it can be corrected. Thus Hamming code is called error detecting and correcting code. The code uses a ~~no~~ number of parity bit (dependent on the no. of information bits) located at certain positions in the code group.

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(5) Differentiate TTL, Schottky TTL, CMOS

SR NO.	Parameter	CMOS	TTL	Schottky TTL
1.	Device used	n-channel and P-channel MOSFET	Bipolar junction transistor	unsaturated bipolar junction transistor
2.	V_{IH} (min)	3.5V	2V	2V
3.	V_{IL} (max)	1.5V	0.8V	0.8V
4.	V_{OH} (min)	4.95V	2.7V	2.7V
5.	V_{OL} (max)	0.005V	0.4V	0.5V
6.	Speed Power Product	0.7pJ	100pJ	57pJ
7.	Fan out	50	10	10
8.	Power Supply voltage	3-15V	Fixed 5V	Fixed 5V.
9.	Application	Portable instrument where battery supply is used.	laboratory instruments.	It is used to speed up the time of operation.

Assignment-2

* module :- 2

① Explain K-map

→ During the process of simplification of Boolean expression we have to predict each successive step.

→ we can never be absolutely certain that an expression simplified by Boolean algebra alone is the simplest possible expression.

→ on the other hand, the map method gives us a systematic approach for simplifying a Boolean expression.

→ The map method, first proposed by veitch and modified by Karnaugh, hence it is known as the veitch diagram or the Karnaugh map.

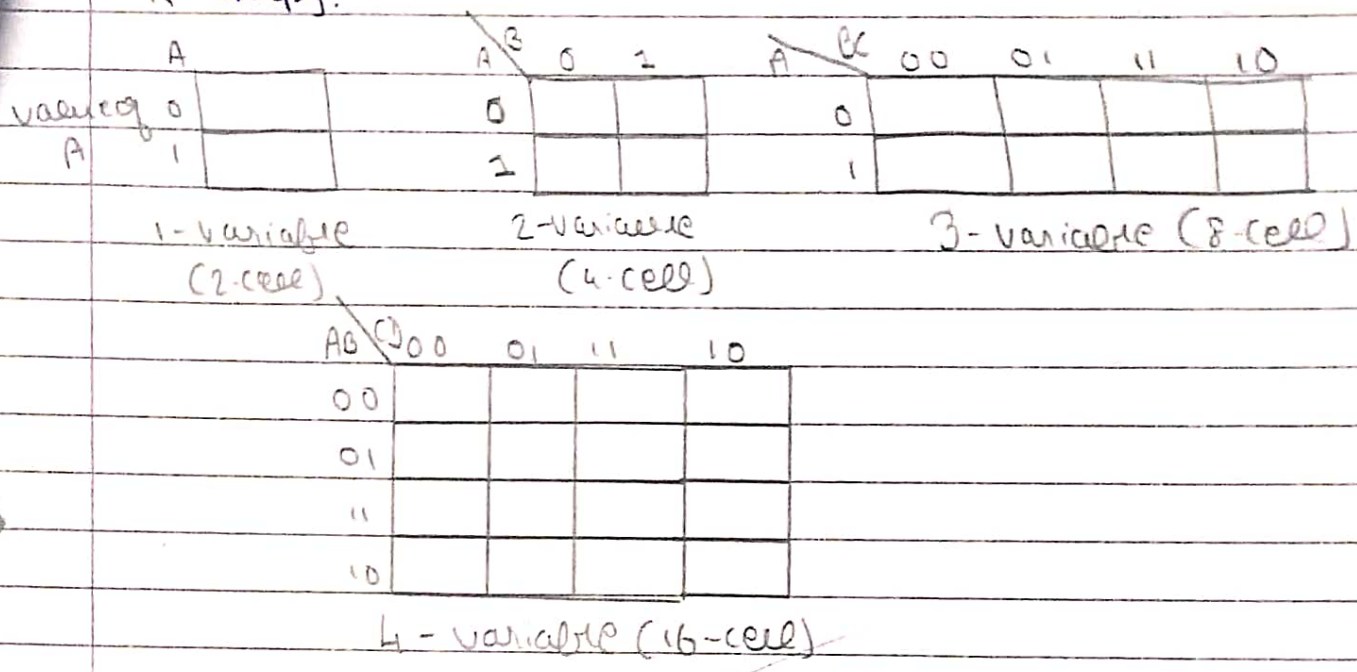
* One-variable, Two-variable, Three-variable and Four-variable K-maps.

* The basis of this method is a graphical chart known as Karnaugh map (K-map)

* It contains boxes called cells.

• Each of the cell represents one of the 2^n possible product that can be formed from n variable. Thus a 2-variable map contains $2^2 = 4$ cells, 3-variable map contains $2^3 = 8$ cells and so forth.

- Fig below shows outlines of 1, 2, 3 and 4 variable K-maps.



- Product terms are assigned to the cells of a K-map by labelling each row and each column of the map with a variable, with its complement, or with a combination of variable and complement.

- The product term corresponding to a given cell is then the product of all variable in the row and column where the cell is located.

② Obtain the simplified expression in sum of product for the following Boolean functions:-

i) $F(x,y,z) = \Sigma(2,3,6,7)$

$F = m_2 + m_3 + m_6 + m_7$

$F = \bar{x}y\bar{z} + \bar{x}yz + xy\bar{z} + xyz$

$F = \bar{x}y(\bar{z}+z) + xy(\bar{z}+z)$

$\because$ (complement property $A+\bar{A} = 1$)

$F = \bar{x}y \cdot 1 + xy \cdot 1.$

$F = \bar{x}y + xy.$

$\therefore F(x,y,z) = \bar{x}y + xy$ -- Ans

ii) $F(A,B,C,D) = \Sigma(4,6,7,15)$

$F = m_4 + m_6 + m_7 + m_{15}.$

$F = \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + \bar{A}BCD + ABCD$

$F = \bar{A}B\bar{D}(\bar{C}+C) + BCD(\bar{A}+A)$

$\because$ (Complement property $\bar{A}+A = 1$)

$F = \bar{A}B\bar{D} \cdot 1 + BCD \cdot 1$

$F = \bar{A}B\bar{D} + BCD$

$\therefore F(A,B,C,D) = \bar{A}B\bar{D} + BCD.$

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(1) Describe adder & substractor.

→ Adders

Digital computers perform various arithmetic operations. The most basic operation, no doubt, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely,

$0+0=0$

$0+1=1$

$1+0=1$

$1+1=10_2$.

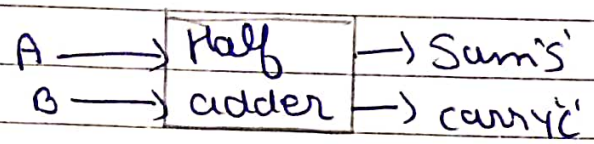
→ The first three operations produce a sum whose length is one digit, but when the last op^n is performed sum is two digit. The higher significant bit of this result is called a carry, and lower significant bit is called sum. The logic circuit which performs this operation is called half-adder. The circuit which performs addition of three bits is a full-adder.

. Half-adder :-

Half adder is a combinational logic circuit with two inputs and two outputs.

. The half adder circuit is designed to add two single bit binary no A and B

-) This circuit has two output sums and carry.



Block diagram of Half-adder

K-map simplification for carry and sum.

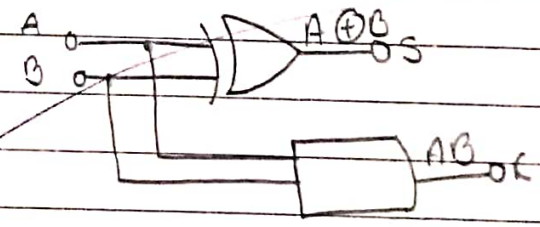
Sum

A \ B	0	1
0	0	1
1	1	0

carry

A \ B	0	1
0	0	0
1	0	1

logic Diagram :-



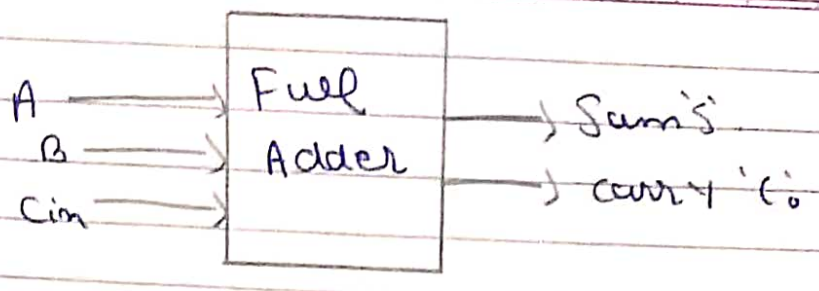
Truth table for half-adder.

A	B	Sum 'S'	Carry 'C'
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder

The full adder is a three input and two output combinational circuit.

-) This circuit has two output sum and carry.



Block diagram of full-adder

-) Truth-table For full-adder

A	B	Cin	Sum 'S'	carry 'Co'
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map simplification for Sum and carry

carry

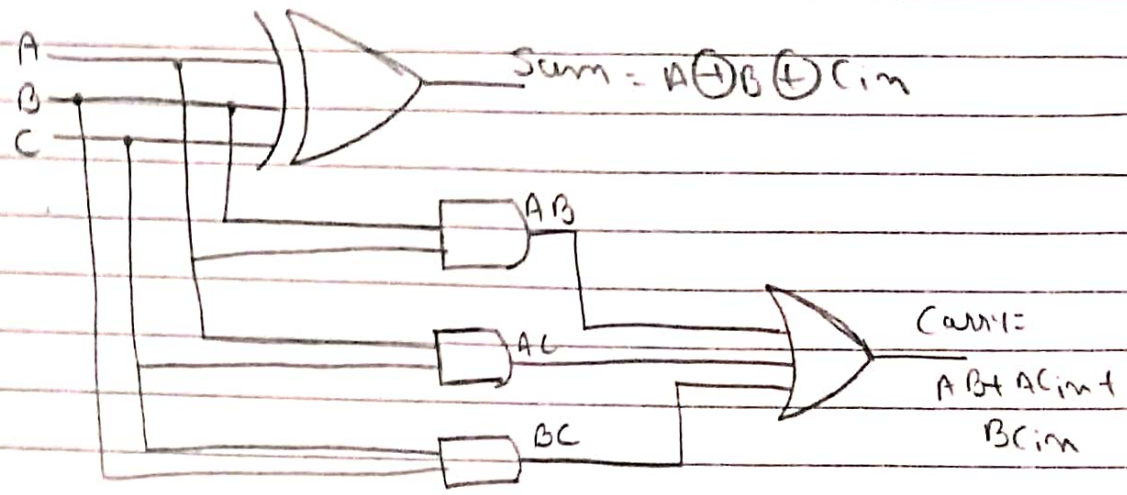
A \ BCi	00	01	11	10
0	0	0	1	0
1	0	1	1	1

A \ BCi	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$C = BC_i + AC_i + AB$

$S = A \oplus B \oplus C$

logic diagram of full adder:-



* Substractors:-

- The substraction consists of four possible elementary operations namely.

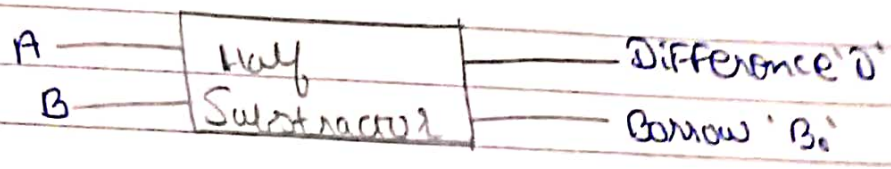
  0 - 0 = 0
  0 - 1 = 1 with 1 Borrow
  1 - 0 = 1
  1 - 1 = 0

→ In all operation each substracted bit is substracted from the minuend bit. In case of second operation the minuend bit is smaller than the substrahend bit, hence 1 is borrowed. Just as there are half and full-adders, there are half and full-substractors.

Half substractor

- Half substractor is a combination circuit with two inputs and two output

- It Produces the difference Between the two Binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed.



Block diagram of Half-substractor

K-map simplification for half-substractor.

Difference

A \ B	0	1
0	0	1
1	1	0

$D = A \oplus B$

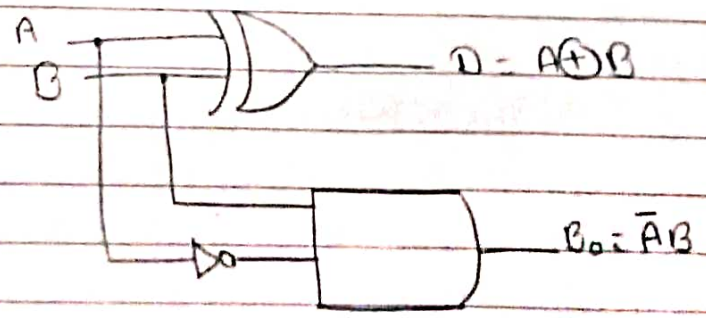
A \ B	0	1
0	0	1
1	0	0

$B_0 = \bar{A}B$

Truth table for half-substractor

A	B	difference 'D'	Borrow 'B_0'
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

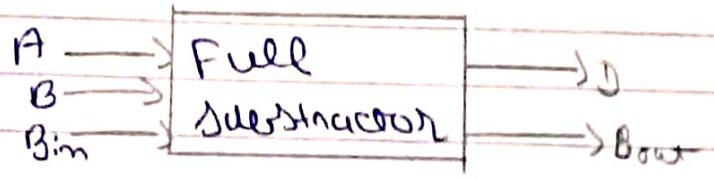
logic diagram for half-adder



Full Substractor :-

→ The full substractor is a combinational circuit with three input A, B, B_i and two output D and B_o.

→ A is the 'minuend' B is 'subtrahend' B_i is the borrow in produced by the previous stage D is the difference 'output' and B_o is the borrow output.



Block diagram of full substractor.

K-map simplification for full-substractor

A \ B_iB	00	01	11	10
0	0	1	0	1
1	1		1	0

$D = A \oplus B \oplus B_i$

Borrow

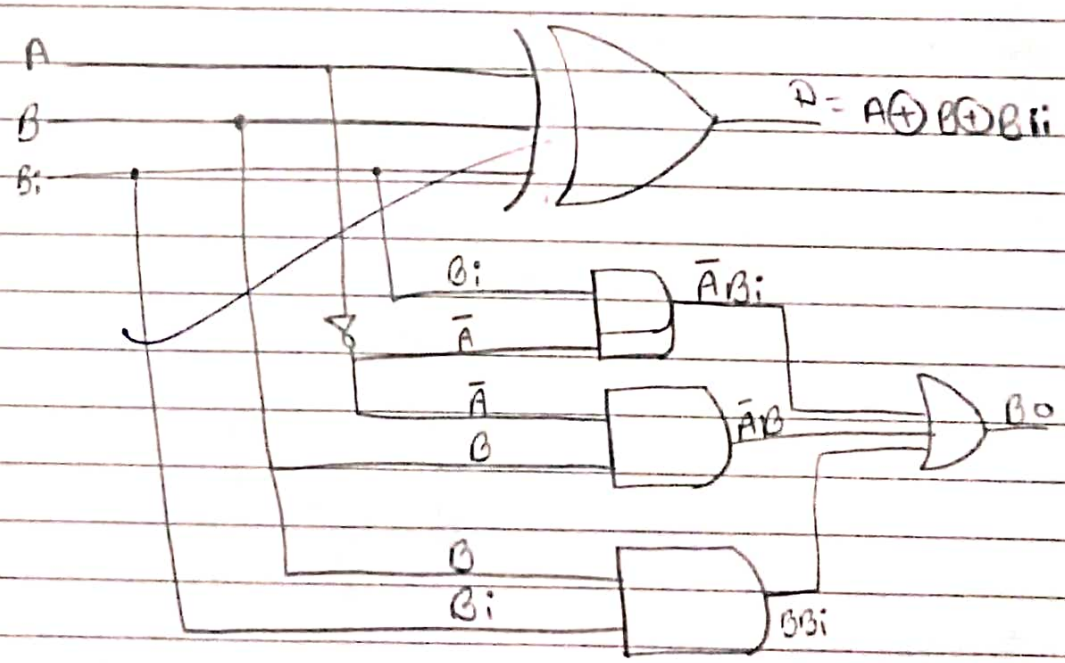
A \ BB_i	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$B_o = \bar{A}B_i + \bar{A}B + BB_i$

Truth table for full subtractor

A	B	Borrow In (B_i)	Difference 'D'	Borrow Out (B_o)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

logic diagram for full subtractor



(4) Explain Multiplexer & Demultiplexer.

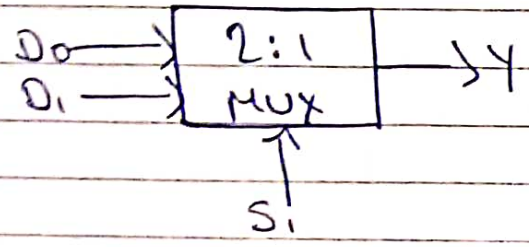
→ Multiplexer:-

Multiplexer means many to one. Multiplexer is a circuit having many number of input lines and only one output line. The input line is selected by selection line.

Types of Multiplexer are:

1) 2:1 Multiplexer
2) 4:1 Multiplexer
3) 8:1 Multiplexer
4) Quadruple 2 to 1 Multiplexer
5) The 74151 Multiplexer
6) The 74xx153 Dual 4 to 1 Multiplexer
7) expanding Multiplexer.

1) 2:1 Multiplexer : It is a 2 input and 1 output multiplexer combinational circuit. It has 1 select input line.

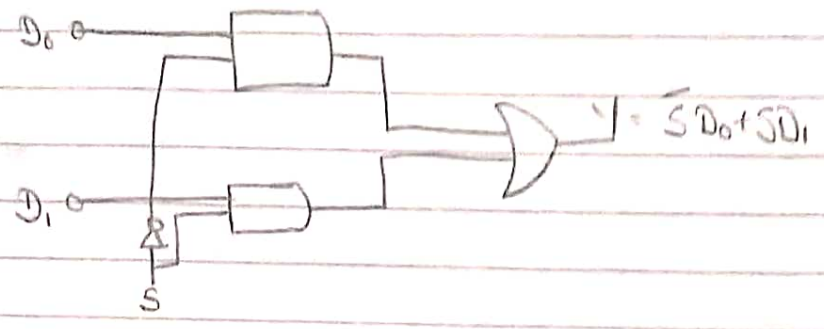


Block diagram of 2:1 MUX

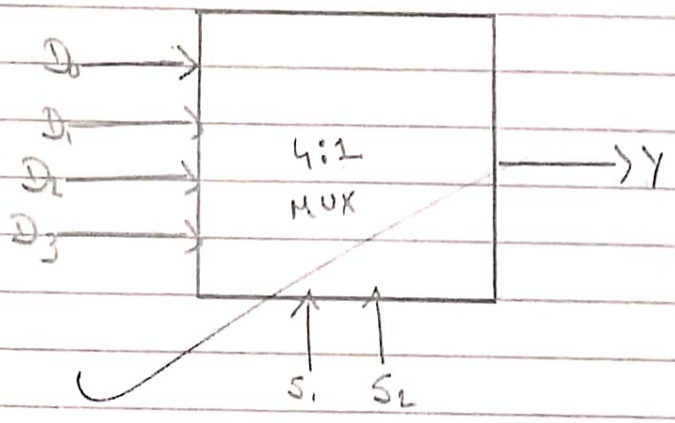
Truth Table / Function Table of 2:1 MUX:-

S	Y
0	D_0
1	D_1

logic diagram of 2:1 MUX:-



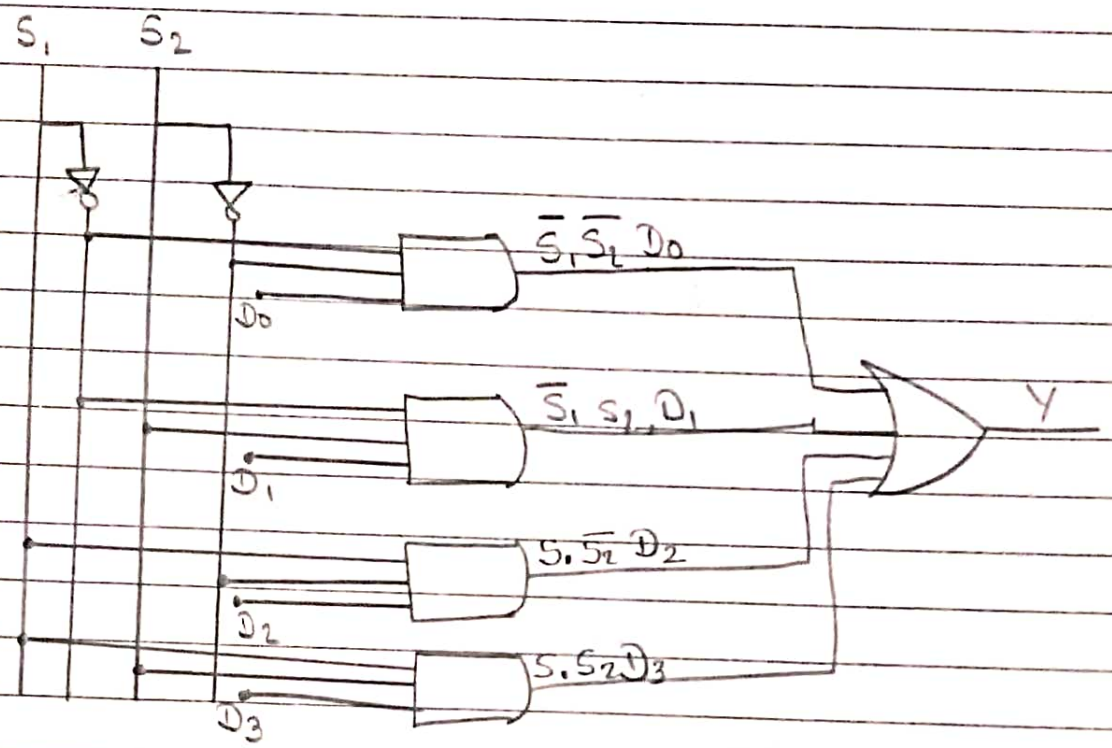
2) 4:1 Multiplexer: It is a 4 input and 1 output multiplexer combinational circuit. It has 2 select lines.



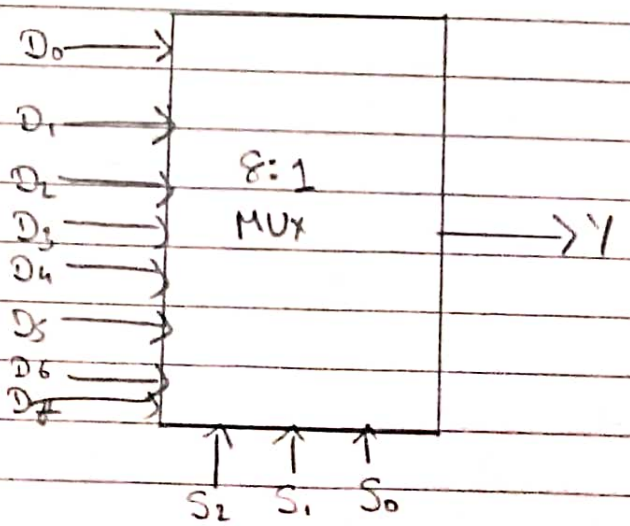
Truth table / Function table of 4:1 MUX:-

S_1	S_2	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

logic diagram of 4:1 Mux :-



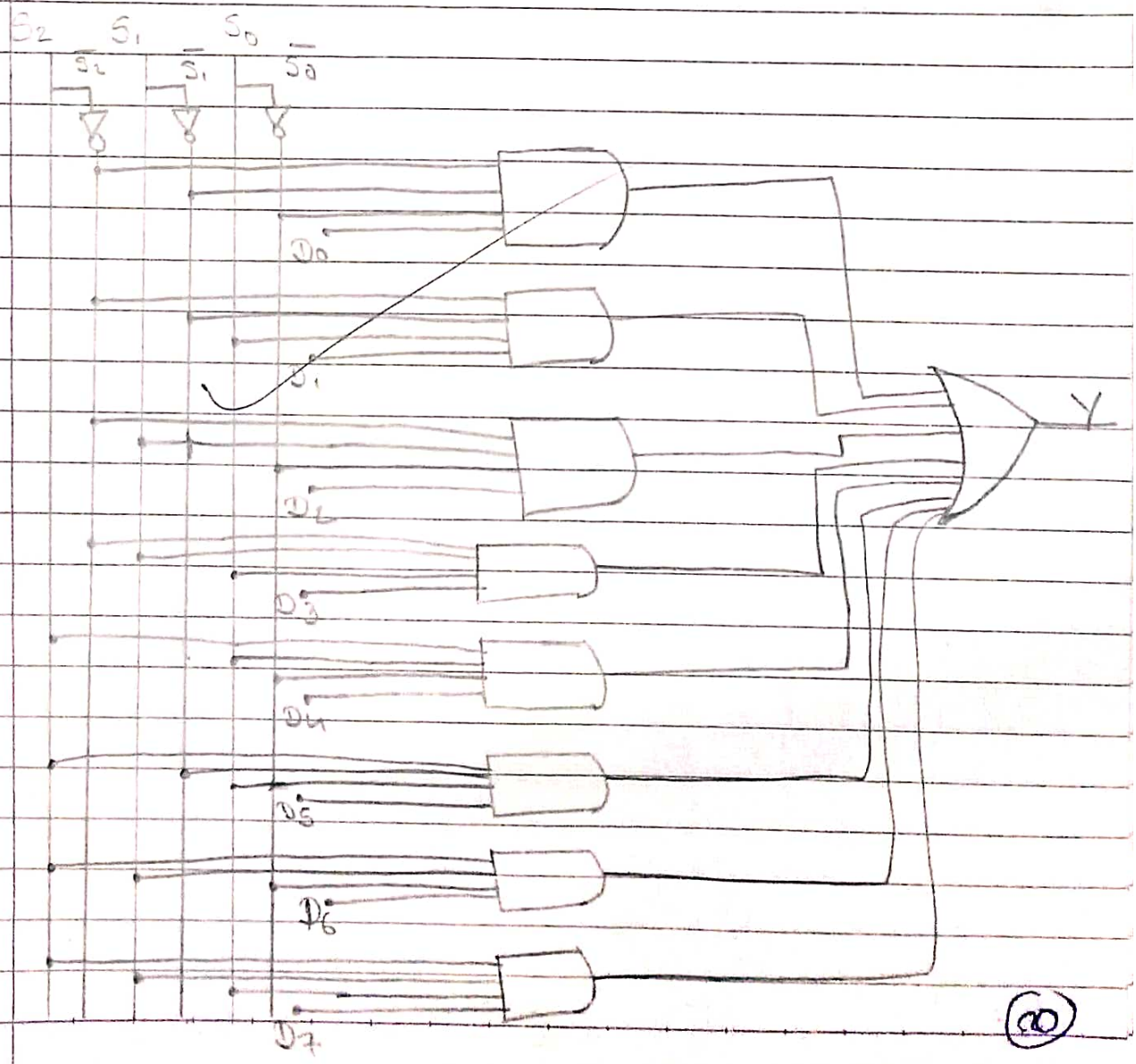
iii) 8:1 Multiplexer :- It is 8 input and 1 output multiplexer combinational circuit. It has 3 service inputs.



Truth table / Function table for 8:1 MUX:-

S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

logic diagram of 8:1 MUX:-



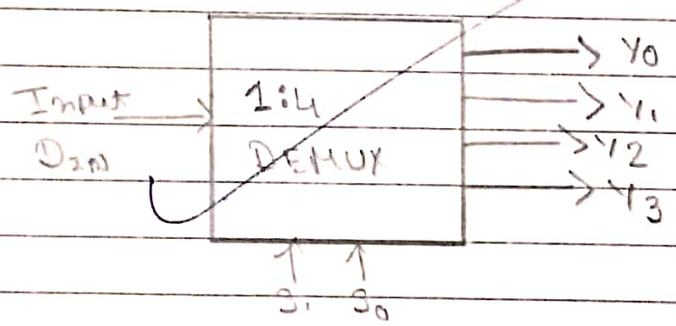
Demultiplexer -

De Multiplexer means one to many. De Multiplexer is a circuit having one input line and many number of output lines. The output line is selected by selection line (control line).

Types of Demultiplexer:

1) 1:4 Demultiplexer
2) 1:8 Demultiplexer
3) expanding De Multiplexer

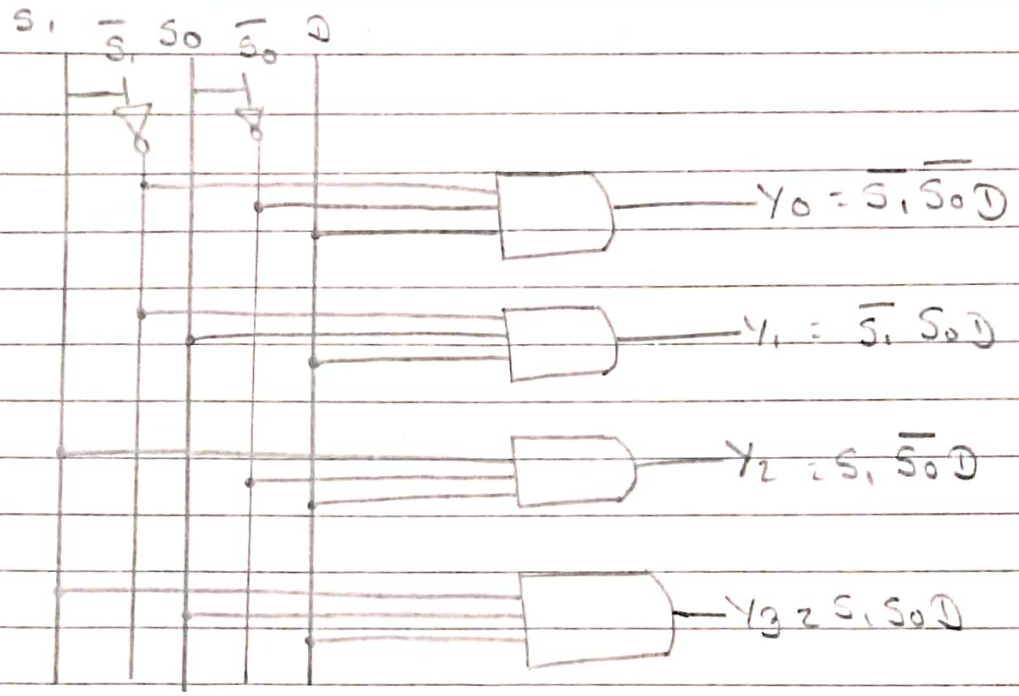
1) 1:4 Demultiplexer:- It has one input line and four output lines. It has two select input lines.



Truth table / Function table for 1:4 DEMUX:-

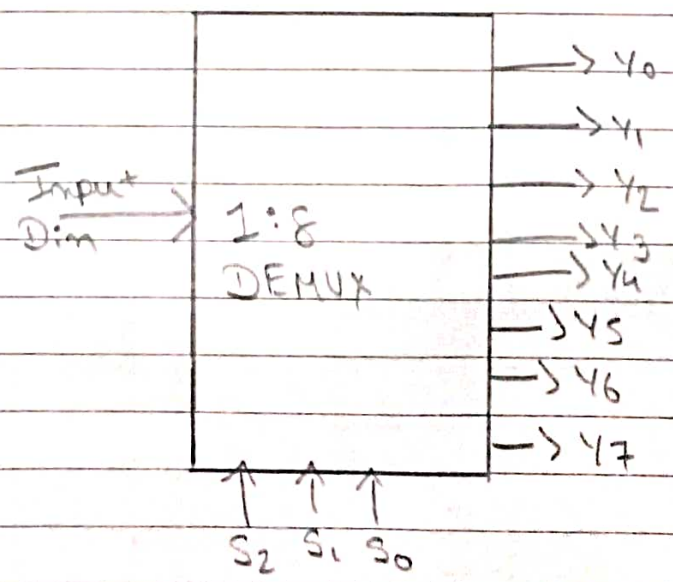
Input	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

logic diagram of 1:4 DEMUX :-



$Y_0 = \overline{S_1}\,\overline{S_0}D$, $Y_1 = \overline{S_1}S_0D$, $Y_2 = S_1\overline{S_0}D$, $Y_3 = S_1S_0D$

2) 1:8 Demultiplexer :- It has one input line and eight output lines. It has three select inputs lines.

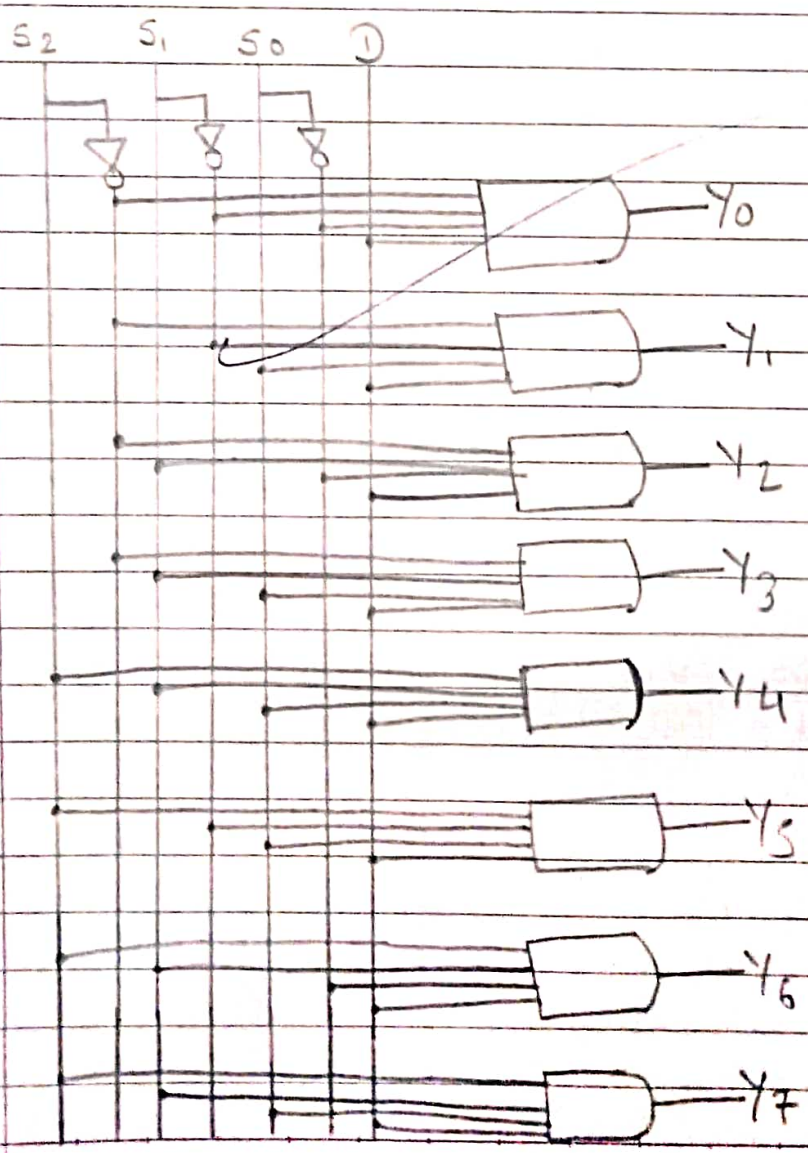


Block diagram of 1:8 DEMUX.

Truth table / Function table of 1:8 DEMUX:-

Input	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

Logic Diagram of 1:8 DEMUX:-



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(5) Describe Parity checker & generator.

→ * Parity Generator: It is a combinational circuit that accept an 'n' bit data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is called as a Parity bit.

- In even Parity, the Parity bit is '0' if there are even number of 1s in the data stream and the Parity bit is '1' if there are odd no. of 1s in the data.

- In odd Parity bit the bit is '1' if there are even number of 1s and the parity is '0' if there are odd no. of 1s in the data stream.

- Even Parity Generator: let us assume that a 3 bit message is to be transmitted with an even parity bit. let the three input 'A', 'B' and 'C' are applied to the circuit and output Bit is the Parity bit P. The total no. of 1s must be even.

Truth table of even Parity Generator

3-bit message			even Parity Generator 'P'
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1

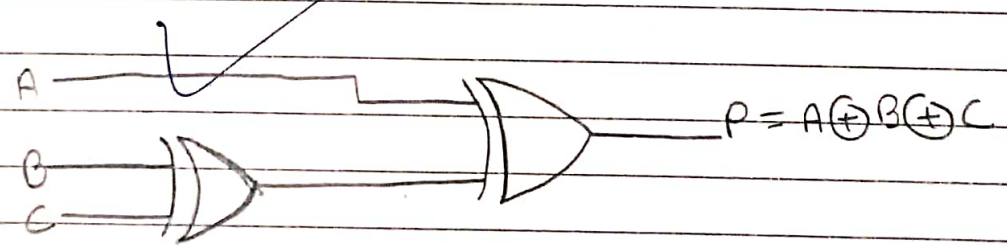
A	B	C	even Parity Gen 'P'
1	0	1	0
1	1	0	0
1	1	1	1

K-map Simplification for 3-bit even parity Generator.

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$P = \bar{A}\cdot(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$P = A \oplus B \oplus C$$

logic diagram for 3-bit even Parity generator:-



- Odd Parity Generator:- let us consider that 3-bit data is to be transmitted with an Odd parity bit. The three input are 'A', 'B' and 'C' and 'P' is the odd parity generated as the output bit. The no. of 1s is placed in the parity bit in order to make the total no. of bits odd when the total no. of 1s in the truth table is even.

→ Truth table of 3-bit even parity generator

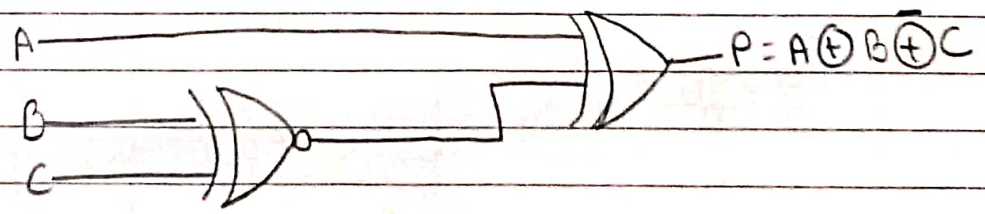
3-bit message			Odd parity bit generator 'P'
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

K-map Simplification for 3-bit odd Parity generator

A \ BC	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$P = A \oplus B \overline{\oplus} C$

logic diagram for 3-bit odd parity generator.



* Parity Checker:- It is a logic circuit that checks for possible error in the transmission. This circuit can be even parity or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker the no. of input bits must always be even.

- Even Parity checker:- Consider three input message along with even parity bit is generated at the transmitted end. These 4 bits are inputs to the even parity bit checker. Since, the data is transmitted with even parity, Four bits received at circuit must have even no. of 1s.

Truth table for even parity checker

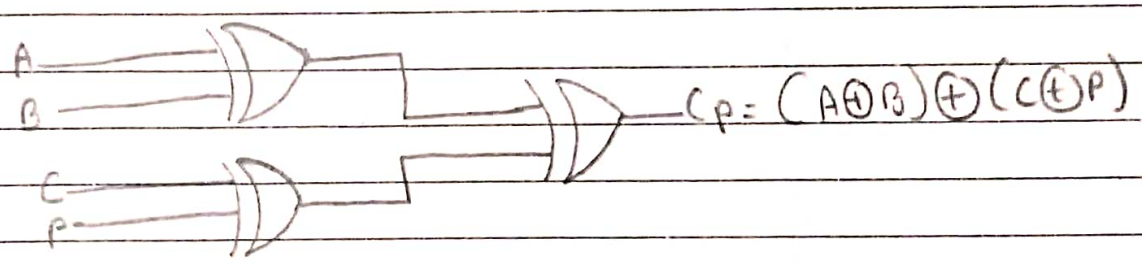
4 Bit message received				Parity error check 'Cp'
A	B	C	D	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-map Simplification for even-Parity Checker

AB \ CP	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$C.P = (A \oplus B) \oplus (C \oplus P)$

logic Diagram for even-Parity Checker



Odd Parity Checker :- Consider a three bit message along with odd Parity is transmitted at the transmitting end. Odd Parity Checker circuit receives these 4 bits and checks whether any error are present in the data. If the total no. of 1s in the data is odd, then it indicates no error, whereas if the total no. of 1s is even then it indicates error.

Truth table for odd parity checker.

4-bit Message Received				Parity error check 'CP'
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

K-map simplification for 3-bit odd parity checker

AB \ CP	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

$CP = (A \odot B) \odot (C \odot P)$

Logic diagram for 3-bit odd parity checker

Assignment-3

(1) Differentiate sequential and combinational circuits

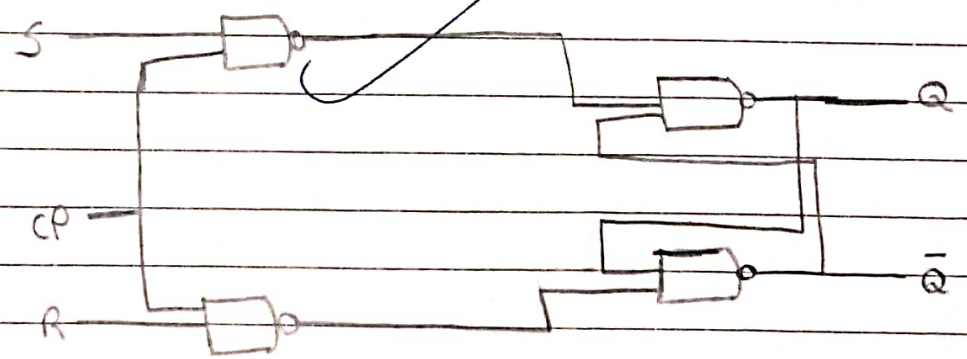
Sequential circuits	Combinational Circuits
In Sequential circuits, the output variables depend not only on the present input variable but they also depend upon the past history of these input variable	In combinational circuits the output variable are at all times dependent on the combination of input variables.
Memory unit is required to store the past history of input variable in the sequential circuit	Memory unit is not required in combinational circuit.
Sequential circuit are slower than the combination circuit	Combinational circuit are faster in speed because the delay between input and output is due to propagation delay of gates
Sequential circuit are comparatively hard to design.	Combinational circuit are easy to design.
Serial adder is a sequential circuit.	Parallel adder is a combinational circuit.

(2) List & explain flip flops.

→ A flip flop is a sequential digital electronic circuit having two stable states that can be used to store one bit of binary data. Flip flop are the fundamental building blocks of all memory devices.

Types of Flip-flop
1) S-R flip flop
2) J-K flip flop
3) D flip-flop
4) T flip-flop.

1) S-R flip flop :- This is the simplest flip-flop circuit it has set input (S) and a reset input (R). When in this circuit when S is set as active, the output Q would be high and Q will be low. If R is set to active then the output Q is low and $\bar{Q}$ is is high.



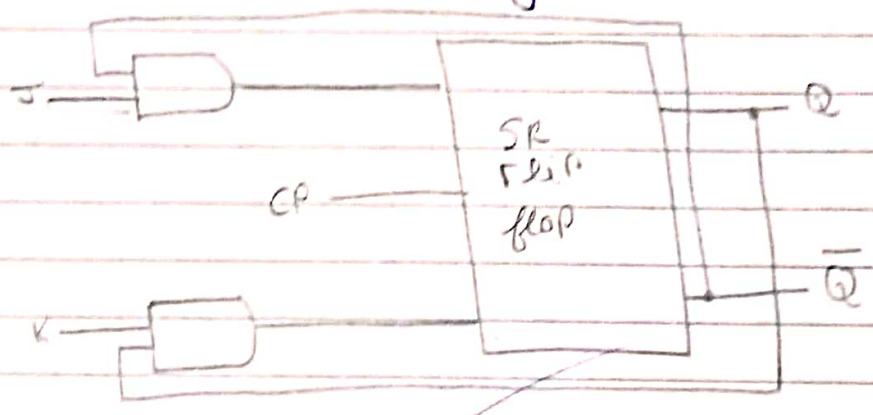
Truth table of S-R flip flop.

S	R	Q	State	S	R	Q	State
0	0	0	No Change	1	0	1	set
0	1	0	Reset	1	1	X	

Characteristic eqn for S-R flip flop:-

$$Q(t+1) = S + R' Q(t)$$

ii) J-K flip-flop :- Because of the invalid state corresponding to S=R=1 in the SR flip flop, there is a need of another flip flop. The J K flip flop operates with only positive or negative clock transitions. The data inputs are J and K which are ANDed with Q and $\bar{Q}$ respectively as shown below:



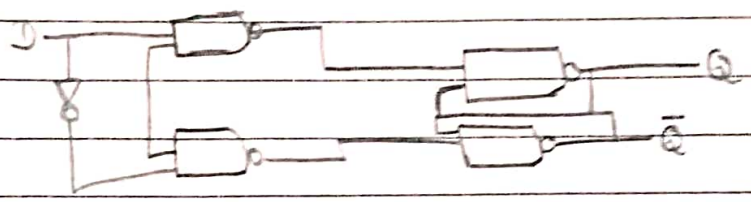
Truth table

J	K	Q	State
0	0	0	No change
0	1	0	Reset
1	0	1	Set
1	1	Toggle	Toggle

Characteristic eqn of JK Flip flop -

$$Q(t+1) = JK(Q(t))' + K' Q(t)$$

3) D flip flop:- In a D flip-flop, the output can only be changed at positive or negative clock transitions and when the inputs changed at other times, the output will remain unaffected. The D flip-flops are generally used for shift registers and counters.

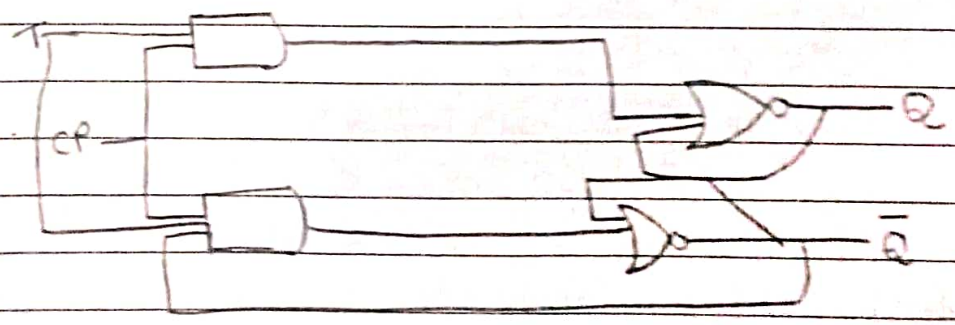


Truth table

D	Q
0	0
1	1

Characteristic eqn of D flip-flop : $Q(t+1) = D$.

4) T Flip-flop - A T Flip-flop is a simplified version of JK flip-flop. The T flop is obtained by connecting J and K inputs together. This flip-flops has one input terminal and clock pulse input. T flip-flops are mostly used in counters.



Truth table of T Flip flop:-

T	Q(t)	Q(t+1)
0	0	0
0	1	1

T	Q(t)	Q(t+1)
1	0	1
1	1	0

Characteristics eqn of T flip flop:-

$$Q(t+1) = \bar{T}Q(t) + T\bar{Q}(t) = T \oplus Q(t)$$

(2) list & explain Registers.

-) Flip flops can be used to store a single bit of binary data (1 or 0). However in order to store multiple bit of data, we need multiple flip-flops. N flip-flops are connected in an order to store n bits of data. A register is a device which is used to store such information. It is a group of flip-flops connected in series used to store multiple bits of data.

-) The informations stored within these register can be transferred with the help of shift registers. Shift register is a group of flip flops used to store multiple bits of a data.

Shift Registers are basically of 4 types.

1) Serial In Serial Out shift register
2) Serial In parallel out shift register.
3) Parallel In Serial out shift register
4) Parallel In Parallel out shift register

1) Serial-In Serial out shift Register (SISO):-

-) The shift register, which allows serial input and produces a serial output is known as Serial-In Serial-Out shift register.

2) Serial-In Parallel out shift Register (SIPO):-

-) The Shift register, which allows serial input and produces a parallel output is known as Serial-In parallel out shift register.

3) Parallel-In Serial out shift Register (PISO):-

-) The shift register, which allows parallel input and produces a serial output is known as parallel In serial out shift register.

4) Parallel In parallel out shift Register (PIPO):-

-) The Shift register, which allows parallel input and produces a parallel output is known as parallel In parallel out shift Registers.

(4) Describe Ring counter

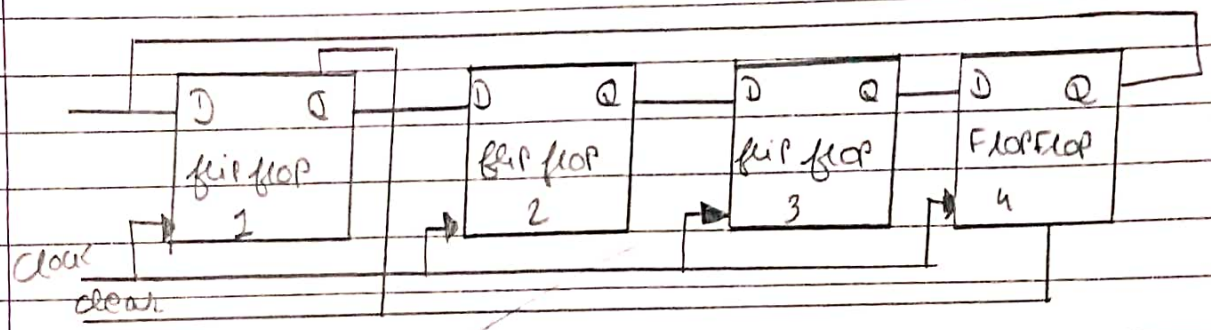
-) A ring counter is basically a shift register counter in which the output of the first flip is connected to the next flip flop and so on and the output of the last flip flop is again fed back to the input of the ~~last flip-flop~~ first flip-flop, thus the name ring counter. The data pattern within the shift register will circulate as long as clock pulses are applied.

-) A ring counter is generally used because it is self-decoding. No extra decoding circuit is needed.

Truth Table of Ring counter:-

Clock pulse	Q_1	Q_2	Q_3	Q_4
0	1	0	0	1
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1

logic circuit / Diagram of Ring counter:-



5) Describe how to design counter using flip flops.

-) The Synchronous counters or counters count the number of clock pulses received at its inputs. The synchronous counter uses the same sources and at exactly the same time. Generally it is constructed using either JK flip flop or T flip-flop. Synchronous counter use edge-triggered flip-flops. These flip-flop change the state during the next clock pulse.

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Design Steps of Synchronous counter.

→ The design steps are somewhat similar for both synchronous count and asynchronous counter but differ slightly. Follow the below given steps to design the synchronous counter.

1) Find the number of flip flops using $2^n \geq N$, where N is the number of states and n is the number of flip flops.

2) Choose the type of flip-flop.

3) Draw the state diagram of the counter

4) Draw the excitation table of the selected flip flop and determine the excitation table for the counter.

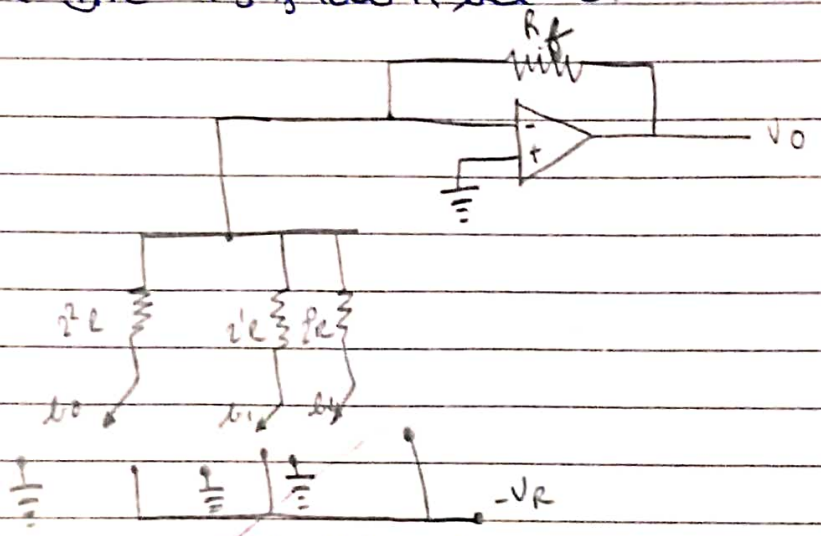
5) use K-map to derive the flip-flop input functions

Assignment-4

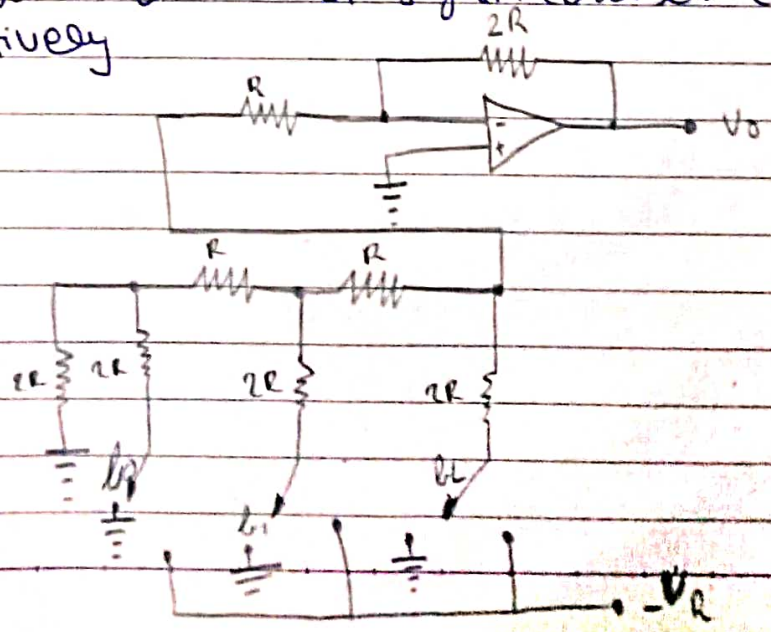
(1) Explain weighted resistor/ converter.

→ A weighted resistor DAC produces an analog output, which is almost equal to the digital input by using binary weighted resistors in the inverting adder circuit. In short a binary weighted resistor DAC is called as weighted resistor DAC.

→ The circuit diagram of a 3-bit binary weighted resistor DAC is shown below.



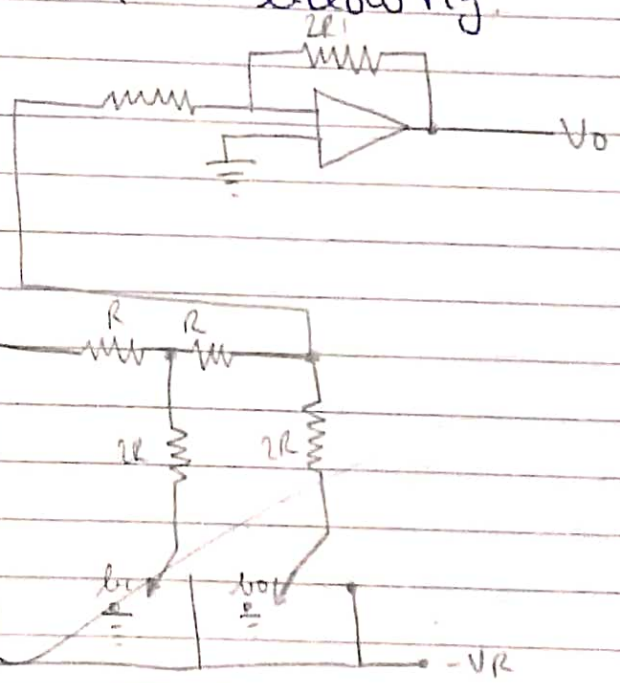
→ Recall that the bits of a binary number can have only one of the two values ie either 0 or 1. Let the 3-bit binary input is $b_2 b_1 b_0$. Here, the bits b_2 and b_0 denotes the most significant bit (MSB) and least significant bit (LSB) respectively



② Explain R-2R Ladder D/A converter.

→ The R-2R ladder DAC overcomes the disadvantages of a binary resistor DAC. As the name suggests, R-2R ladder DAC produces an analog output, which is almost equal to the digital (Binary) input by using a R-2R ladder network in the inverting adder circuit.

→ The circuit diagram of a 3-bit R-2R Ladder DAC is shown in below fig.



Recall that the bits of a binary number can have only one of the two values ie either 0 or 1. Let the 3-bit binary input is $b_2 b_1 b_0$. Here the bits b_2 and b_0 denote the Most Significant Bit (MSB) and least Significant Bit (LSB) respectively

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(3) Describe specification of A/D & D/A converter.

→ A/D converter specifications.

1) Resolution:- The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with the respect to no. of bits. It is given as 1/2n, where n is the no. of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the no. of bits or the number of representing the given analog input voltage.

2) Quantization error:- If the binary output bit combination is such that for all the values of input voltage Vi between any two voltage levels there is a unavoidable uncertainity about the exact of Vi when the output is a particular binary combination. This uncertainity is termed as quantization error. Its value is ± (1/2) LSB

3) linearity error:- It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

4) DNL (Differential Non-linearity) error:- The analog input levels that trigger any two successive output codes should differ by 1LSB. Any deviation from this 1LSB value is called DNL error

5) input Voltage Range:- It is the Range of voltage that an A/D converter can accept as its input without causing any overflow in its digital output.

• D/A converter Specifications:-

1) Resolution: Resolution is defined as the no. of different analog output voltage levels that can be provided by a DAC. Or alternative resolution is defined as the ratio of a change in output voltage resulting for a change of 1LSB at the digital input. Simply resolution is the value of LSB.

2) linearity :- linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001 % of full scale. The linearity of D/A converter is defined as the precision or exactness with which the digital input is converted into analog output.

3) Monotonicity: A D/A converter is said to be monotonic if the analog output increase for an increase in the digital input. A monotonic characteristics is essential in control application. Otherwise it would lead to oscillations.

4) Conversion time: It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the amplifier.

(4) Explain Quantization and Encoding.

Quantization:-

-> It is the process of taking a continuous voltage signal and mapping it to a discrete no. of voltage levels. The no. of voltage levels affects the quantization noise that occurs. Since digital computers are binary in nature, the no. of quantization levels is usually a power of 2 ie $N = 2^n$,
where n is the number of quantization bits

-> The signal may be amplified before going into the ADC, so that the maximum and minimum voltage levels give the best compromise between resolution of the signal levels and minimization of clipping

Encoding:-

-> It is the process of converting the quantized signals into a digital representing. This encoding is performed by giving each quantization level a unique label. For instance, if four bits are used, the lowest level may be (in binary) 0000, and the next higher level 0001, etc.

(2) Explain parallel comparator A/D converter.

→ When system designs calls for the highest speed available, flash type ADCs are likely to be the right choice. They get their names from their ability to do the conversion very rapidly. Flash A/D converters, also known as a simultaneous or parallel comparator ADC, bcoz the fast conversion speed is accomplished by providing $2^n - 1$ comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

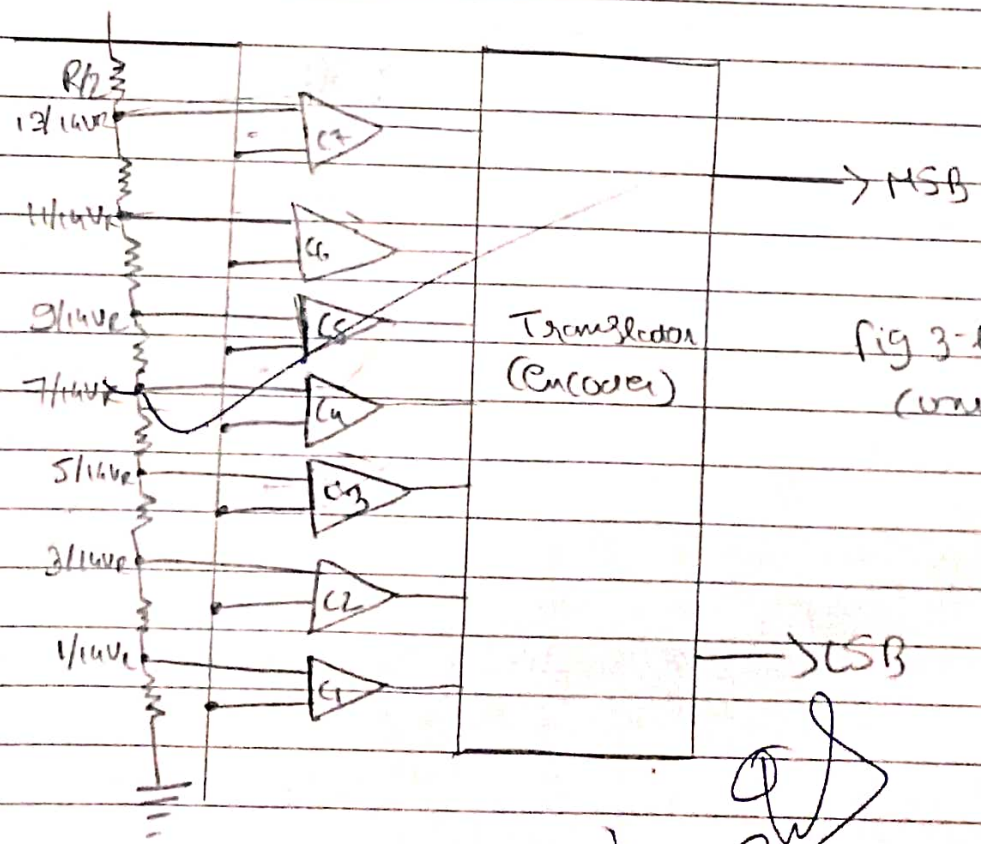

fig 3-bit flash converter

Assignments

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(1) Explain content addressable memory (CAM)

-) Many data processing application require the search of items in a table stored in memory. They use object names or numbers to identify the location of the named or numbered object within a memory space.

-) The time required to find an object stored in memory can be reduced considerably if object are selected based on their contents, not on their locations. A memory unit accessed by the content is called an associative memory or CAM.

-) CAM is a data storage device, that stores memory in cells. When any aspects of the memory is entered the CAM compares the input with all the stored data. It is a high speed technology.

- Features of CAM:-
1) it is used in DBMS
2) CAM is expensive than Ram
3) CAM is suitable for parallel search.
4) It return the list of data word address that was located.

There are two basic forms of CAM and TCAM

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(2) Explain Charge de coupled device memory (CCD)

→ A Charge-coupled (CCD) is a semiconductor device capable of both photo-detection and memory, which converts light to electronic impulses

→ One and two-dimensional CD arrays are used in scanners to perform the first stage in converting an image into digital data.

→ They are particularly attractive because they can step the signals from each detector across the array in response to a clock signal, permitting each scan line to be read through a single electrical connection.

→ For many year CDs were the sensors of choice in a wide range of devices, but they're steadily being replaced by image sensor based on complementary metal oxide semiconductor (CMOS) technology.

→ In the past CCs could deliver much better quality images than other types of sensors including those based on CMOS technology.

→ As a result, they were used in a wide range of devices, including ~~sca~~ scanners, bar code readers, microscopes medical equipment and astronomical telescope.

③ Explain classification of memory.

Classification of memory

Non-volatile Memory		Volatile Memory	
Read only memory (ROM)	Read/write memory (NVRAM)	Read/write memory (RWM)	
• Mask-programmable ROM	• EPROM	Random access	Non-random access
• Programmable ROM	• EEROM	• SRAM	• FIFO
	• FLASH	• DRAM	• LIFO
			• Shift Register

Note:

ROM - Read only memory
PROM - Programmable ROM.
EPROM - Erasable PROM
EEPROM - Electrically erasable PROM.
SRAM - Static Random Access Memory
DRAM - Dynamic Random Access Memory
FIFO - First-In First-out.
LIFO - Last-in-First-out

④ Describe Semiconductors.

A-4 A semiconductor is a substance that has specific electrical properties that enable it to serve as a foundation for computer and other electronic devices.

It is typically a solid chemical element or compound that conducts electricity under certain conditions but not others.

-) This makes it an ideal medium to control electrical current and everyday electrical appliances. It is a popular components of electronic chip made for computing components and a variety of electronic devices, including solid-state storage

-) Semiconductors have properties sit between the conductor and insulator. Most semiconductors are composed of crystal made of several materials

(5) Explain Field programmable gate Array (FPGA)

A-5 -) Field Programmable gate array are semiconductor devices that are based around a matrix of configurable logic block (CLBS) connected via programmable interconnects.

-) FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing.

-) A field programmable gate array consists of logic blocks which are programmable, reconfigurable interconnects and input/output pads. The logic blocks used in a field-programmable gate array could consist of memory elements such as flip-flops or memory blocks. The logic blocks are capable of performing simple to complex computational function

-) Field-programmable gate array are used in a wide range of application and in markets such as aerospace, defense, data centers, automotive, medical and wireless communications.

DF PRACTICALS

NAME: - KALP M. PATEL

ENROLLMENT NUMBER: - D2D46

SUBJECT: - DIGITAL FUNDAMENTALS

SUBJECT CODE: - 3130704

CLASS: - CE-B

BATCH: - B4

DEPARTMENT: - COMPUTER ENGINEERING

PRACTICAL 1

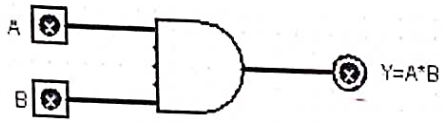
AIM: - Getting familiar with Logisim, Study and implement all basic logic gates. Implement NAND and NOR logic gates as universal gates.

Basic Gates:-

1). **AND Gate: -** AND Gate has an output which is normally at logic level "0" and only goes "HIGH" to a logic level "1" when ALL of its inputs are at logic level "1"

Boolean Function Y = A*B.

Logical Symbol:



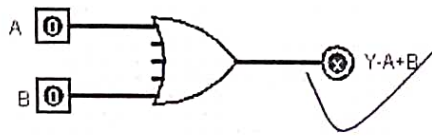
Truth Table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2). **OR Gate: -** OR Gate or Inclusive-OR gate has an output which is normally at logic level "0" and only goes "HIGH" to a logic level "1" when one or more of its inputs are at logic level "1".

Boolean Function = A+B.

Logical Symbol:



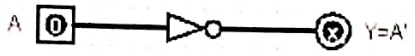
Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3). **NOT Gate:** NOT gate has an output which is always opposite to input level.

Boolean Expression: - Y=A'.

Logical Symbol: -



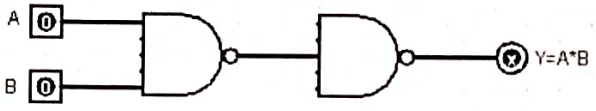
Truth Table: -

A	Y
0	1
1	0

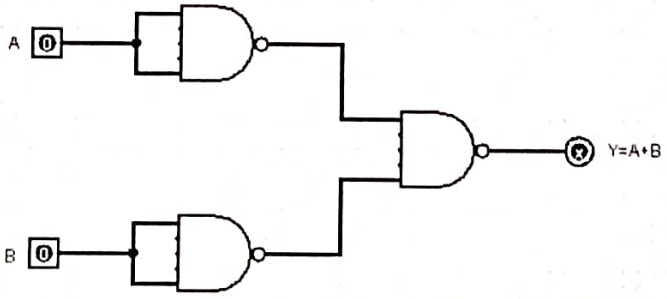
Universal Gates: -

1). NAND Gate:

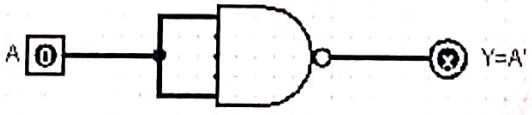
a). AND using NAND Gate:



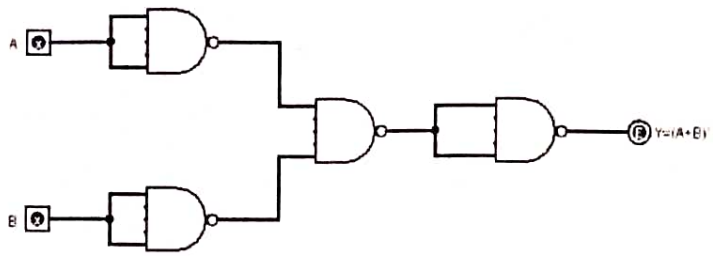
b). OR using NAND Gate:



c). NOT using NAND Gate:

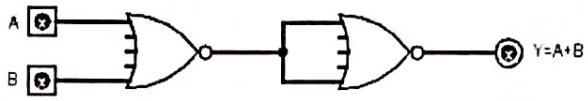


d). NOR using NAND Gate:

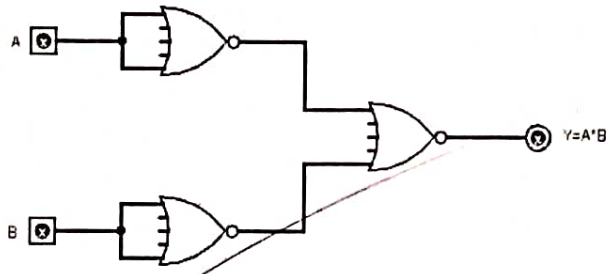


2). NOR Gate:

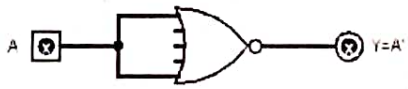
a). OR using NOR Gate:



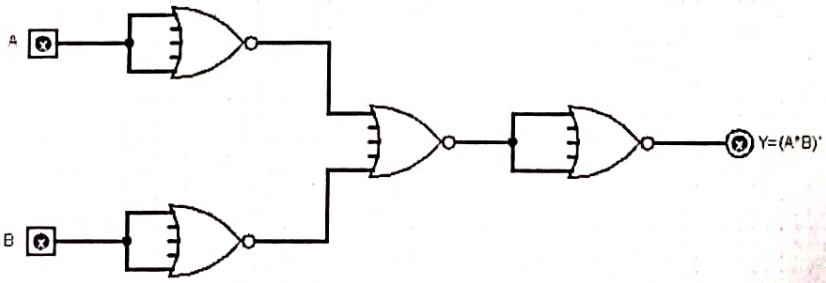
b). AND using NOR Gate:



c). NOT using NOR Gate:



d). NAND using NOR Gate:



PRACTICAL 2

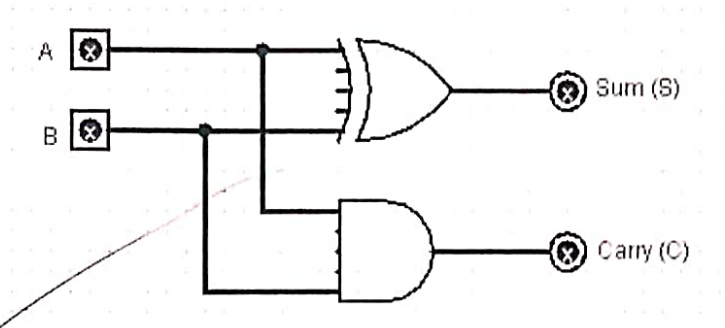
AIM: - Implement Half Adder and Full Adder using Logic Gates.

a). Half Adder: - A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value.

Truth Table:

Input		Output	
A	**B**	**Sum(s)**	**Carry(c)**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Circuit:



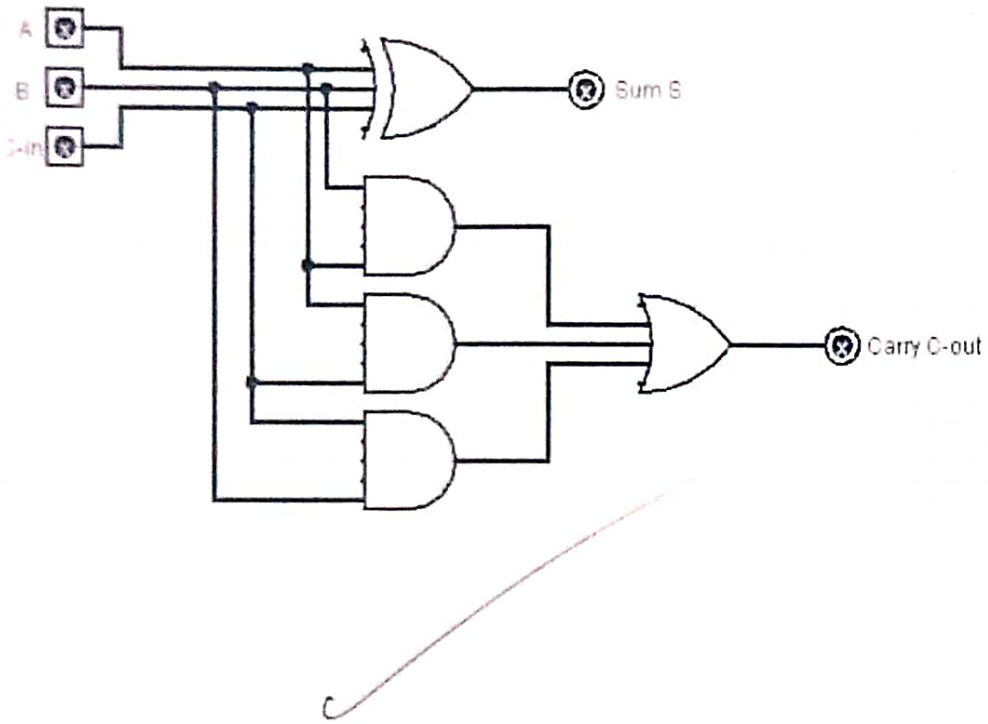
b). Full Adder: - A full adder circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit.1 It therefore has three inputs and two outputs.

Truth Table:

Input			Output	
A	**B**	**C-in**	**Sum(s)**	**C-out**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0

1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Circuit:



PRACTICAL 3

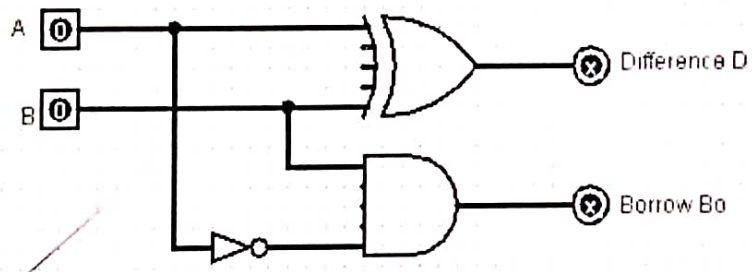
AIM: - Implement Half Subtractor and Full Subtractor using Logic Gates.

a). Half Subtractor: - Half Subtractor is a Combinational circuit with two inputs A and B, and two outputs Difference and Borrow. It produces the difference between two binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed.

Truth Table:

Input		Output	
A	**B**	**Difference(d)**	**Borrow(b)**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic Circuit:



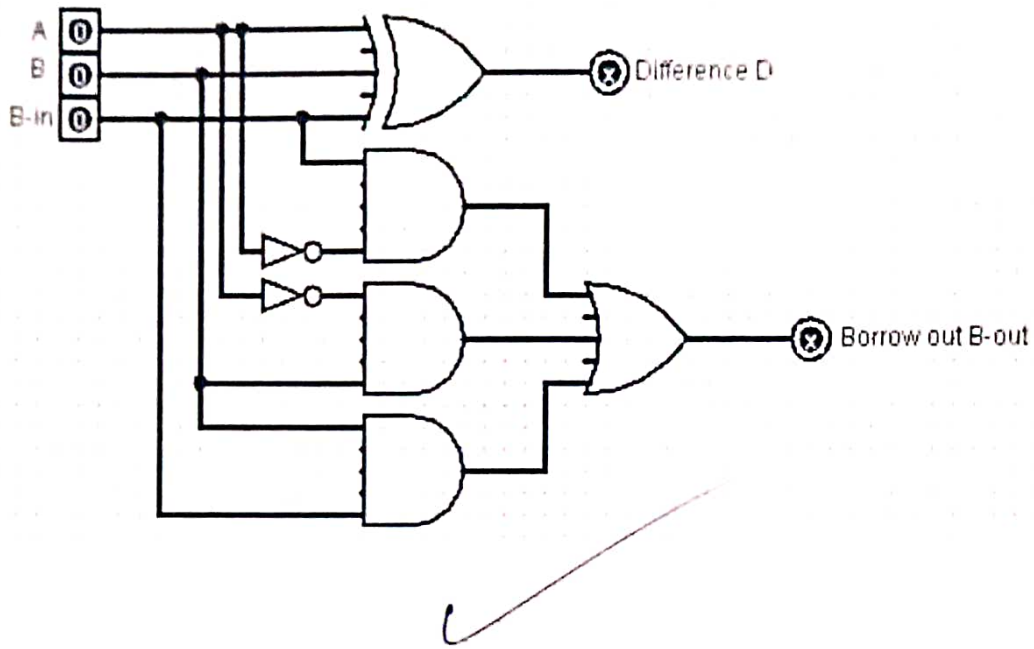
b). Full Subtractor: - Full Subtractor is a Combinational circuit with three inputs A, B, B-in and two outputs D and Bo. A is 'minuend', B is 'subtrahead', Bin is 'borrow in' produced by the previous stage, D is the 'difference' output and Bout is 'borrow out'.

Truth Table:

Input			Output	
A	**B**	**B-in**	**Difference(d)**	**B-out**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0

1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Circuit:



PRACTICAL 4

AIM: - Perform Parity Checker.

The Combinational circuit that checks the parity in the receiver is called Parity Checker. This checker takes the received message including the parity bit as input. It gives output '1' if there is some error found and gives output '0' if no error is found in the message including the parity bit.

There are two types of parity checker: a). Even parity checker, b). Odd parity checker.

a). Even parity checker: - In even parity checker if the error bit (E) is equal to '1', then we have an error. If error bit E is 0 then it indicates no error.

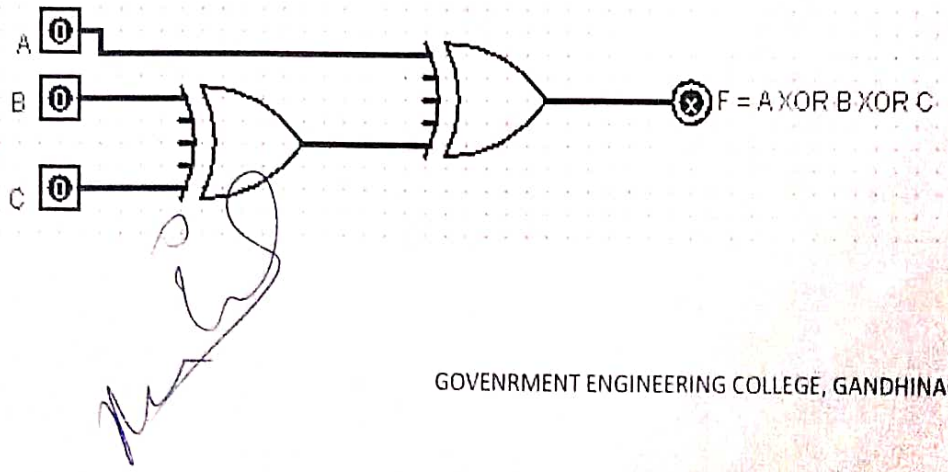
b). Odd parity checker: - In odd parity checker if the error bit (E) is equal to '1' then it indicates no error. If error bit E is 1 then it indicates an error.

Boolean Function: F = A'B'C+A'BC'+AB'C'+ABC = A XOR B XOR C.

Truth Table:

Input			Output
A	**B**	**C**	**parity bit (p)**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Logic Circuit:



PRACTICAL 5

AIM: - State and implement Multiplexer and Demultiplexer.

a).Multiplexer: - Multiplexer means many to one . Multiplexer is a circuit having many number of input lines and only one output line. The input line is selected by selection line (control line).

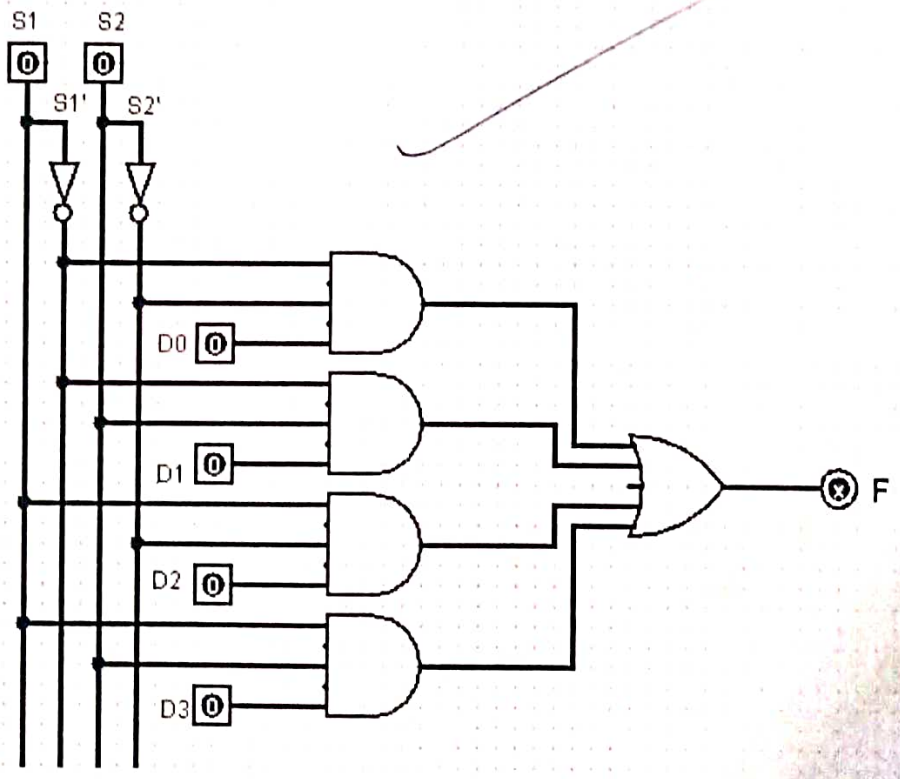
Examples: - 2 to 1 Multiplexer, 4 to 1 Multiplexer, 8 to 1 Multiplexer etc.

Truth Table:

Input		Output
S0	**S1**	**Y**
0	0	A0
0	1	A1
1	0	A2
1	1	A3

Boolean Function F = S1'S2'D0+S1'S2D1+S1S2'D2+S1S2D3.

Logic Circuit:



b) Demultiplexer: - Demultiplexer means one to many. Dempultiplexer is circuit having one input lines and many number output of output lines. The output line is selected by selection line (control line).

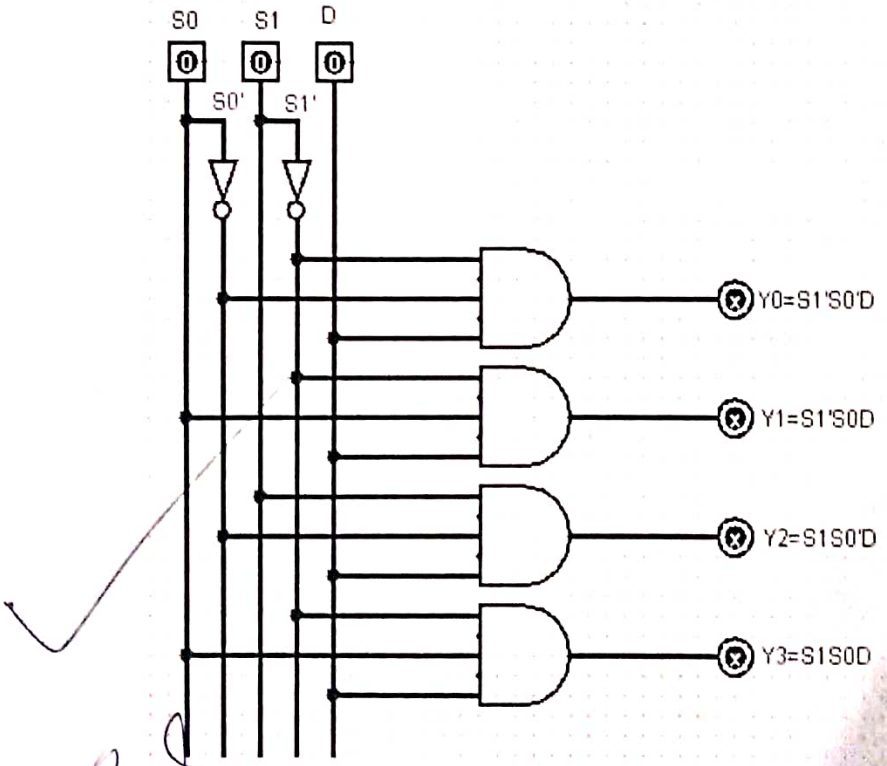
Examples: - 1 to 4 Demultiplexer, 1 to 8 Demultiplexer etc.

Truth Table:

Input		Output			
S1	**S0**	**Y3**	**Y2**	**Y1**	**Y0**
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

Boolean Function Y0 = S1'S0'D, Y1=S1'S0D, Y2=S1S0'D, Y3=S1S0D.

Logic Circuit:

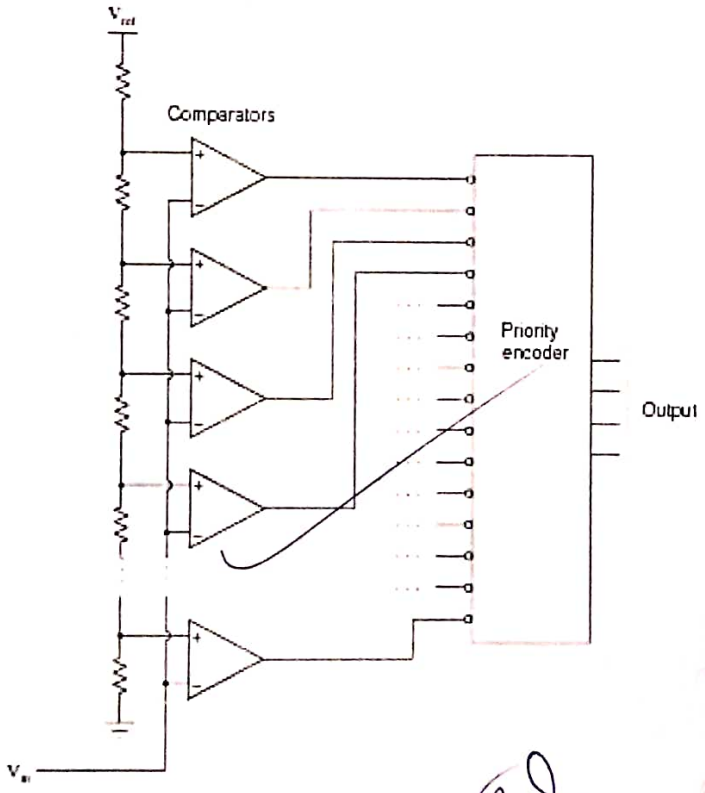


PRACTICAL 6

AIM: - Study and configure A to D converter and D to A converter.

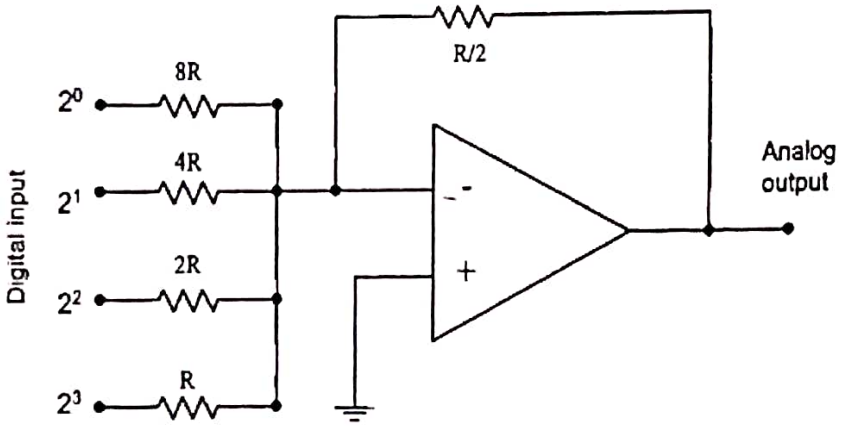
a). A to D converter: - A converter that is used to change the analog signal to digital is known as an analog to digital converter or ADC converter. This converter is one kind of integrated circuit or IC that converts the signal directly from continuous form to discrete form. This converter can be expressed in A/D, ADC, A to D. The inverse function of DAC is nothing but ADC.

Logic Circuit:



b). D to A converter: -A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the number of binary inputs of a DAC will be a power of two.

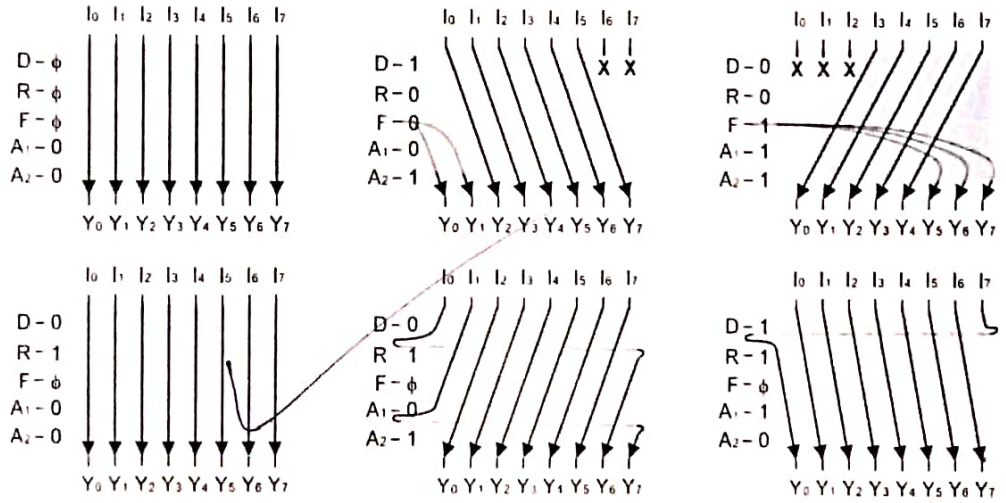
Logic Circuit:



PRACTICAL 7

AIM: - Study and implement a shifter.

A shifter is a circuit that produces an N-bit output based on an N-bit data input and an M-bit control input, where the N output bits are place-shifted copies of the input bits, shifted some number of bits to the left or right as determined by the control inputs.



PRACTICAL 8

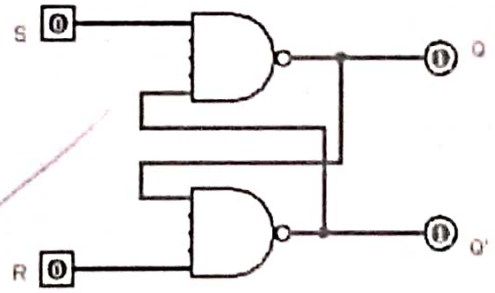
AIM: - Study and implement flip flops

Flip Flop is a sequential circuit which generally samples its inputs and changes its outputs only at particular instants of time and not continuously. Flip flops and latches are used as data storage elements. A flip flop is a device which stores a single bit (binary digit) of data. One of its two states represents a "one" and the other represents a "zero". A basic flip flop can be constructed using four NAND or NOR gates.

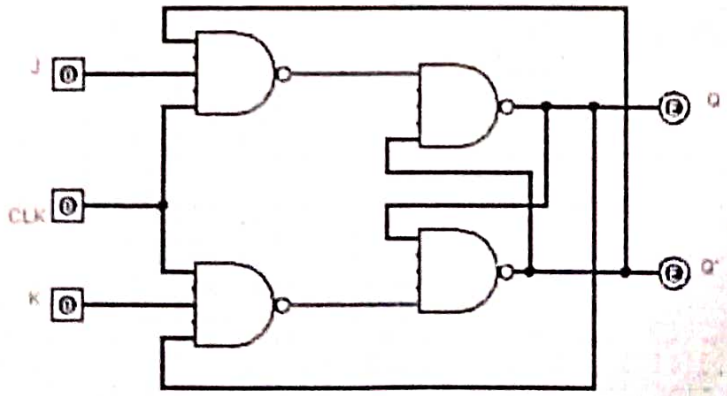
Types of Flip flops: -

- SR Flip flop
- JK Flip flop
- D Flip flop
- T Flip flop

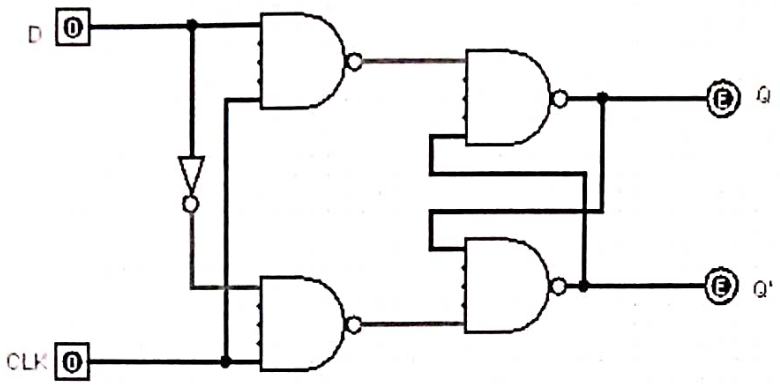
a). SR Flip flop logic diagram:



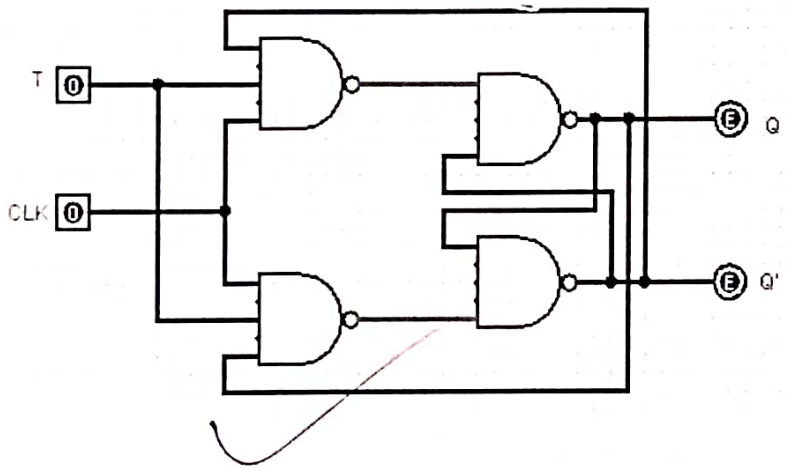
b). JK Flip flop logic diagram:



c). D Flip flop logic diagram:



d). T Flip flop logic diagram:



PRACTICAL 9

AIM: - Study and Implement Counter.

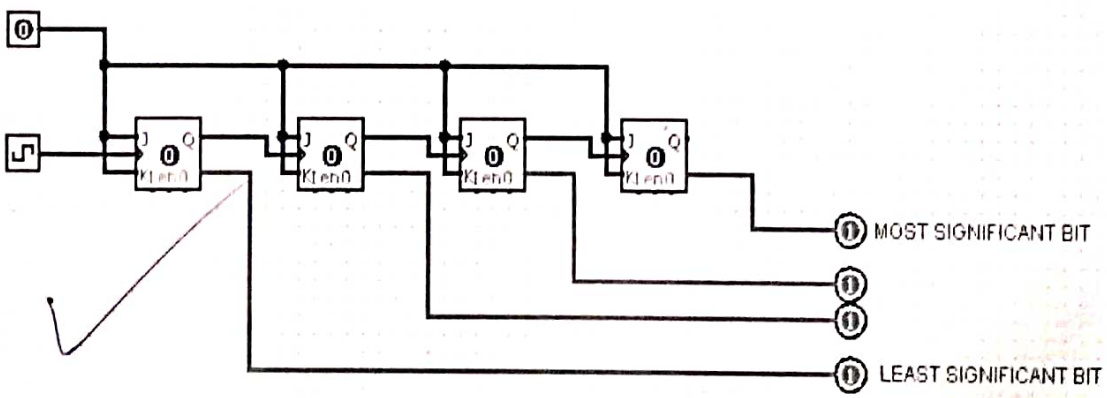
A Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit.

The counter is one of the widest applications of the flip flop. Based on the clock pulse, the output of the counter contains a predefined state. The number of the pulse can be counted using the output of the counter.

Counters are broadly classified in two categories: -

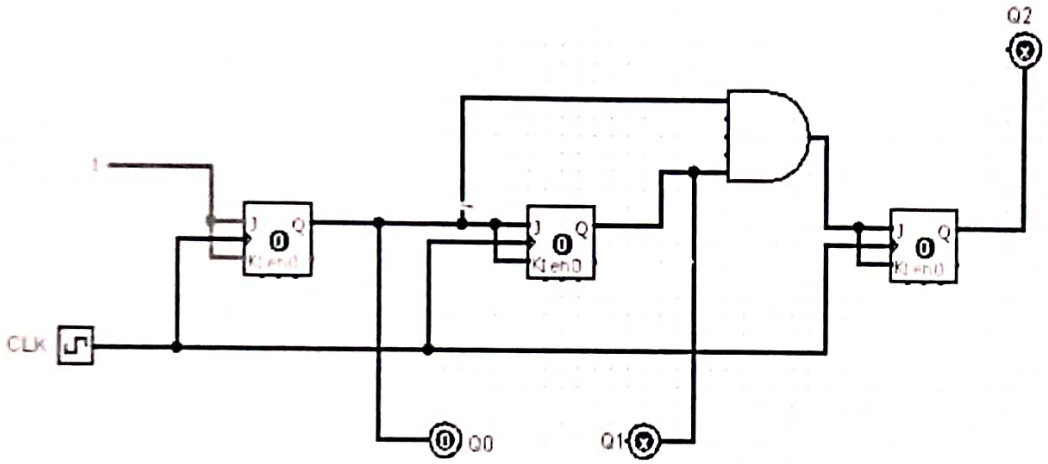
a). Asynchronous Counter: -

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. It is also known as Ripple Counter.



b). Synchronous Counter: -

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.



PRACTICAL 10

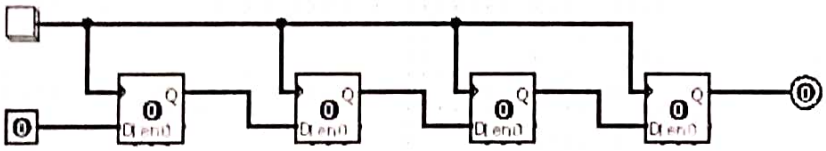
AIM: - Study and implement shift registers.

A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another is known as Shift Register. A Shift Register can shift the bits either to the left or to the right. A Shift Register, which shifts the bit to the left, is known as "Shift left register", and it shifts the bit to the right, known as "Right left register".

The shift register is classified into the following types:

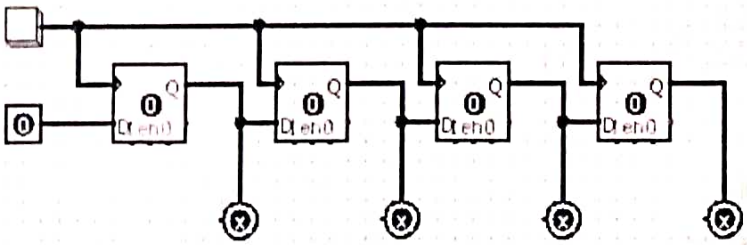
- Serial In Serial Out
- Serial In Parallel Out
- Parallel In Serial Out
- Parallel In Parallel Out

a).Serial In Serial Out:



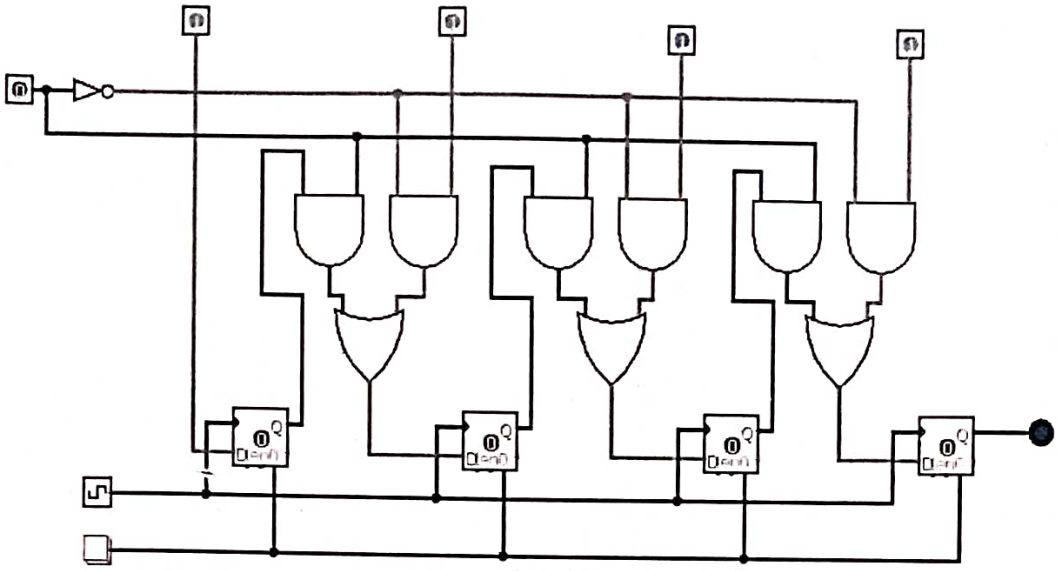
Serial In Serial Out (SISO)

b). Serial In Parallel Out:

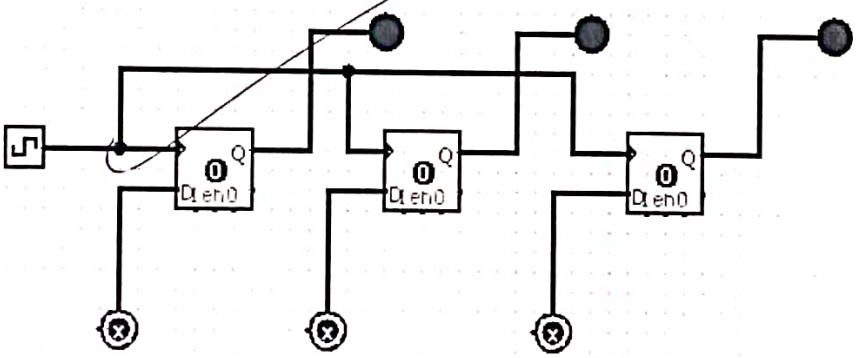


Serial In Parallel Out (SIPO)

c). Parallel In Serial Out:



d). Parallel In Parallel Out:



PRACTICAL 11

AIM: - Study and implement K-Map for the given function: (SOP)

F = ABC`D + AB`C`D` + AB`CD` + A`B`CD` + A`B`C`D`

AB \ CD	C'D'	C'D	CD	CD'
A'B'	1			1
A'B				
AB		1		
AB'	1			1

SOP(F) = B'D' + ABC'D.