



Government Engineering College

Sec-28 Gandhinagar

Sem: - 3

Subject: - Digital Fundamental

Subject Code: - 3130704



Government Engineering College

Sec-28 Gandhinagar

Certificate

This is to certify that

Mr./Ms. Patel Sunny kantibhai Of class

CE B3 Division Enrollment No. 210130107111 Has

Satisfactorily completed his/her term work in

Digital fundamentals Subject for the term ending in

10/1/2023 2022.

Date: -

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Institute Vision/Mission

Vision:

- To be a premier engineering institution, imparting quality education for innovative solutions relevant to society and environment.

Mission:

- To develop human potential to its fullest extent so that intellectual and innovative engineers can emerge in a wide range of professions.
- To advance knowledge and educate students in engineering and other areas of scholarship that will best serve the nation and the world in future.
- To produce quality engineers, entrepreneurs and leaders to meet the present and future needs of society as well as environment.

Computer Engineering Department

Vision/Mission

Vision:

Mission:

Program Educational Outcome (PEO)

- To provide students with a strong foundation in the mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze engineering problems and to prepare them for graduate studies, R&D, consultancy and higher learning.
- To develop an ability to analyze the requirements of the software, understand the technical specifications, design and provide novel engineering solutions and efficient product designs.
- To provide exposure to emerging cutting edge technologies, adequate training & opportunities to work as teams on multidisciplinary projects with effective communication skills and leadership qualities.
- To prepare the students for a successful career and work with values & social concern bridging the digital divide and meeting the requirements of Indian and multinational companies.
- To promote student awareness on the life-long learning and to introduce them to professional ethics and codes of professional practice

PSO

By the completion of Computer Engineering program the student will have following Program specific outcomes.

- Design, develop, test and evaluate computer-based systems by applying standard software engineering practices and strategies in the area of algorithms, web design, data structure, and computer network
- Apply knowledge of ethical principles required to work in a team as well as to lead a team

POs

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

- 2. Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- 6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- 11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12. Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Digital Fundamental (3130704)

Course Outcomes (COs)

CO-1	
CO-2	
CO-3	
CO-4	
CO-5	

7. Assignment Index

Sr. No	Assignment	Date	Page No.	Sign
1	Assignment 1			
2	Assignment 2			
3	Assignment 3			
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8. Practical Index

Sr. No	Assignment	Date	Page No.	Sign
1	Practical 1			
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8	Practical 8			
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9. Assignment 1

CO1: Solve the given problem using fundamentals of Number systems and Boolean algebra

Module 1

1. State and explain De Morgan's theorems with truth tables.
2. Simplify Boolean Function: $F=A'B'C+A'BC+AB'$.
3. List & explain logic family.
4. Describe error detecting & correcting code.
5. Differentiate TTL, Schottky TTL, CMOS

10. Assignment 2

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem

Module 2

1. Explain K map.
2. Obtain the simplified expressions in sum of products for the following Boolean Functions:
 - 2.1. $F(x,y,z) = \Sigma (2,3,6,7)$
 - 2.2. $F(A,B,C,D) = \Sigma (4,6,7,15)$
3. Describe adder & subtractor.
4. Explain multiplexer & demultiplexer.
5. Describe parity checker & generator

11. Assignment 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 3

1. Differentiate sequential & combination circuits.
2. List & explain flip flops.
3. List & explain registers.
4. Describe ring counter.
5. Describe how to design counters using flip flops.

12. Assignment 4

CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion.

Module 4

1. Explain weighted resistor/converter.
2. Explain R-2R Ladder D/A converter.
3. Describe specification of A/D & D/A converter.
4. Explain quantization and encoding.
5. Explain parallel comparator A/D converter.

13. Assignment 5

CO5: Implement PLDs for the given logical problem.

Module 5

1. Explain content addressable memory (CAM).
2. Explain charge de coupled device memory (CCD).
3. Explain classification of memory.
4. Describe semiconductors.
5. Explain Field Programmable Gate Array (FPGA).

14. Practical 1

CO2: Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem.

Module 1

Aim: Getting familiar with Logisim, Study and implement all basic logic gates. Implement NAND and NOR logic gates as universal gates.

Code: THE LOGIC AND FUNCTION: • The AND gate is an electronic circuit that gives a true output (1) only if all its inputs are true. A dot (·) is used to show the AND operation i.e. $A \cdot B$. • Note that the dot is sometimes omitted i.e. AB



Switch A	Switch B	Output	Description
0	0	0	A and B are both open, lamp OFF
0	1	0	A is open and B is closed, lamp OFF
1	0	0	A is closed and B is open, lamp OFF
1	1	1	A is closed and B is closed, lamp ON
Boolean Expression (A AND B)		A . B	

OR GATE: THE LOGIC OR FUNCTION: • The OR gate is an electronic circuit that gives a true output (1) if one or more of its inputs are true. A plus (+) is used to show the OR operation. Switch A Switch B Output Description.

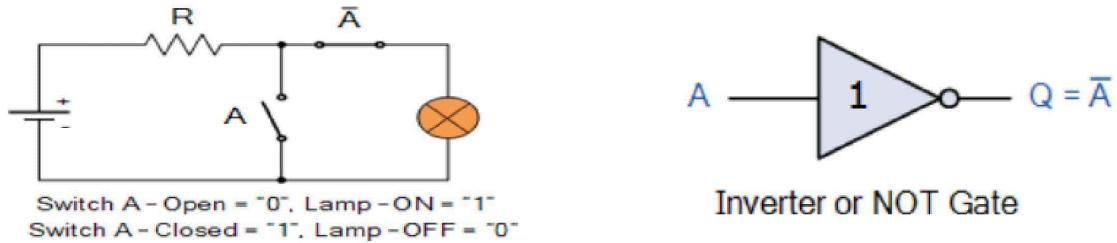
Switch A	Switch B	Output	Description
0	0	0	A and B are both open, lamp OFF
0	1	1	A is open and B is closed, lamp ON
1	0	1	A is closed and B is open, lamp ON
1	1	1	A is closed and B is closed, lamp ON
Boolean Expression (A OR B)		$A + B$	



NOT GATE:

THE LOGIC NOTFUNCTION:

- The Logic NOT Function is simply a single input inverter that changes the input of a logic level “1” to an output of logic level “0” and vice versa.

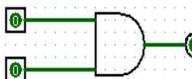


Switch	Output
1	0
0	1
Boolean Expression	not-A or A

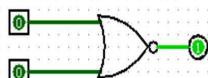
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AND GATE



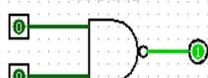
NOR GATE



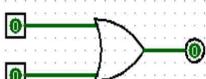
NOT GATE



NAND GATE



OR GATE



NAND GATE AS UNIVERSAL GATE

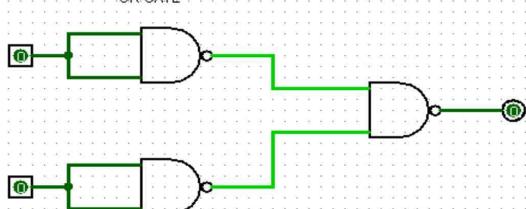
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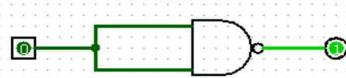
AND GATE



OR GATE



NOT GATE



15. Practical 2

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Implement half and full Adders using logic gates.

Code:

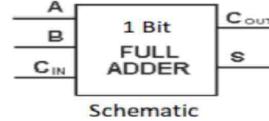
Full Adder:

The full adder is a little more difficult to implement than a half adder. The main difference between a half adder and a full adder is that the full adder has three inputs and two outputs. The two inputs are A and B, and the third input is a carry input C_{IN} . The output carry is designated as C_{OUT} , and the normal output is designated as S. The output S is an EX – OR between the input A and the half adder SUM output B. The C_{OUT} will be true only if any of the two inputs out of the three are HIGH or at logic 1.

Input A	Input B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

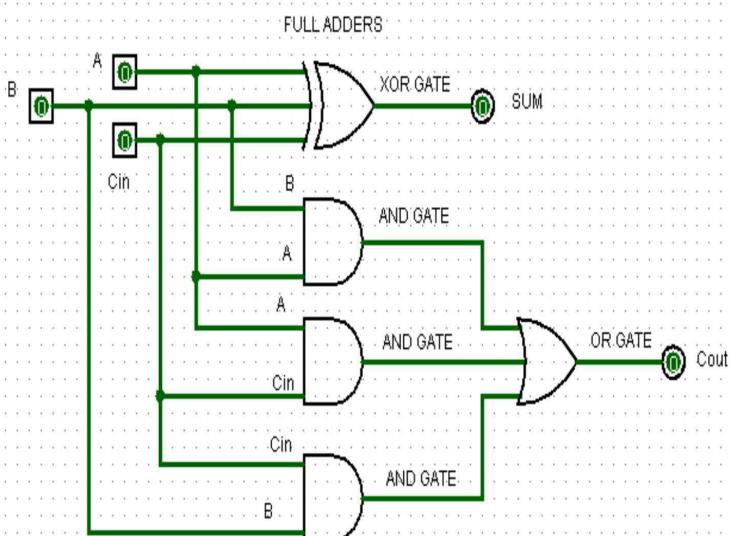
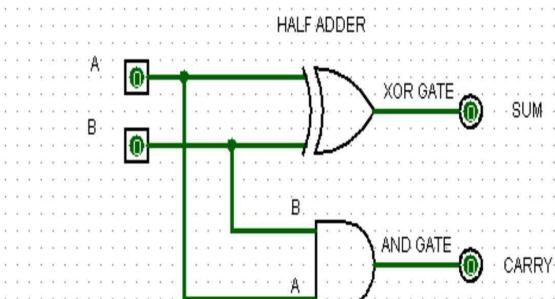


X	Y	Z(C_{in})	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



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16. Practical 3

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

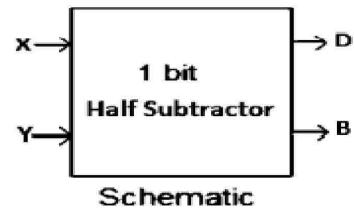
Module 2

Aim: Implement half and full Subtractors using logic gates.

Half Subtractor is a combinational arithmetic circuit that subtracts two numbers and produces a difference bit (D) and borrow bit (B) as the output. If X and Y are the input bits, then Difference bit (D) is the X-OR of X and Y and the Borrow bit (B) will be the AND of X' and Y. From this it is clear that a half Subtractor circuit can be easily constructed using one X-OR gate, one NOT gate and one AND gate.

Truth Table:

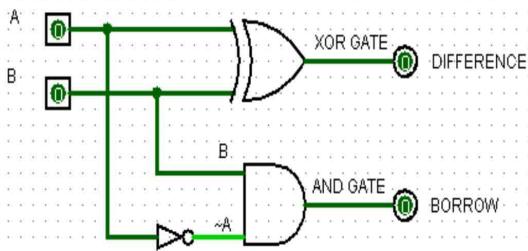
Input X	Input Y	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



Full Subtractor:

- Full Subtractor is little more difficult than a half- Subtractor circuit. The main difference in both Subtractor is that the full- Subtractor has three inputs and half- Subtractor has only two inputs.

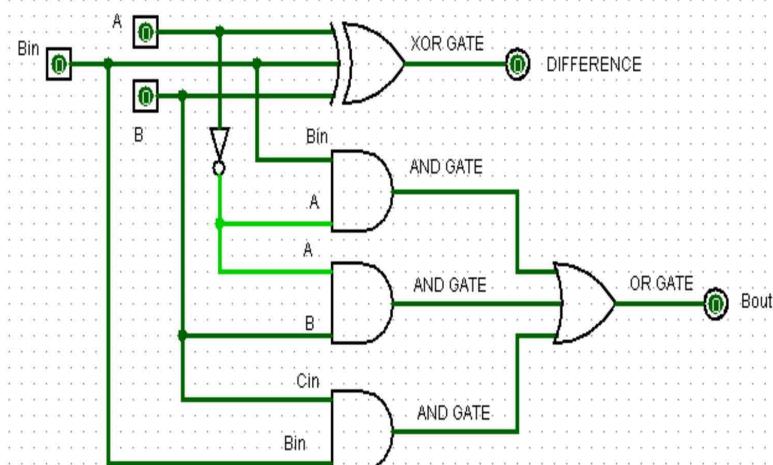
HALF SUBTRACTOR



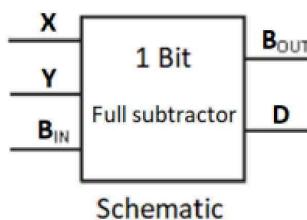
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FULL SUBTRACTOR



X	Y	Z(B_{in})	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
1	0	0	1	0
0	1	1	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Schematic

17. Practical 4

CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

Module 2

Aim: Perform Parity Checker.

Parity Generator:

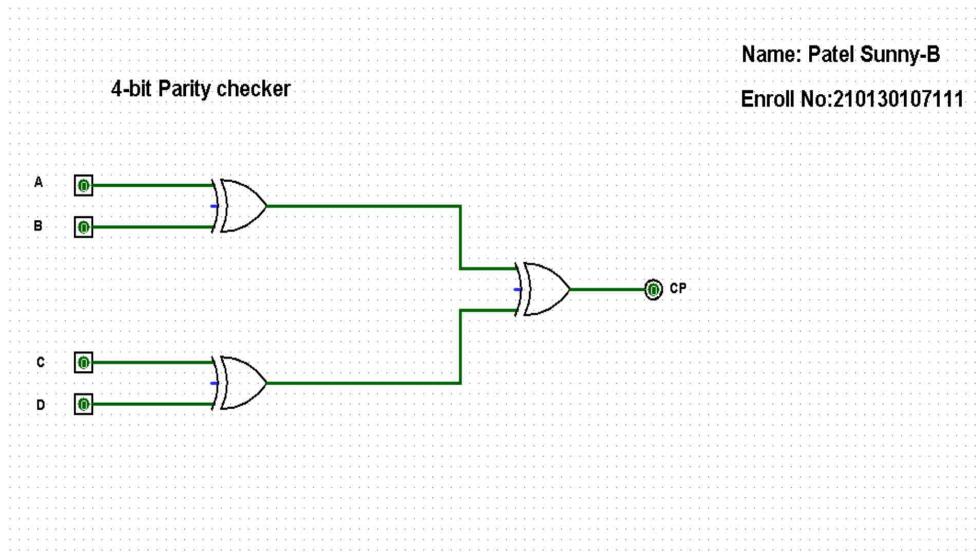
The parity generator is a combination circuit at the transmitter, it takes an original message as input and generates the parity bit for that message and the transmitter in this generator transmits messages along with its parity bit. There are two types of Parity Generator Even parity generator and Odd parity generator.

Even Parity Generator:

The even parity generator maintains the binary data in even number of 1's, for example, the data taken is in odd number of 1's, this even parity generator is going to maintain the data as even number of 1's by adding the extra 1 to the odd number of 1's. This is also a combinational circuit whose output is dependent upon the given input data, which means the input data is binary data or binary code given for parity generator.

Odd Parity Generator:

The odd parity generator maintains the binary data in an odd number of 1's, for example, the data taken is in even number of 1's, this odd parity generator is going to maintain the data as an odd number of 1's by adding the extra 1 to the even number of 1's. This is the combinational circuit whose output is always dependent upon the given input data. If there is an even number of 1's then only parity bit is added to make the binary code into an odd number of 1's.

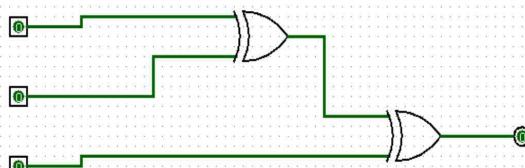


4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

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3 Bit even parity generator



18. Practical 5

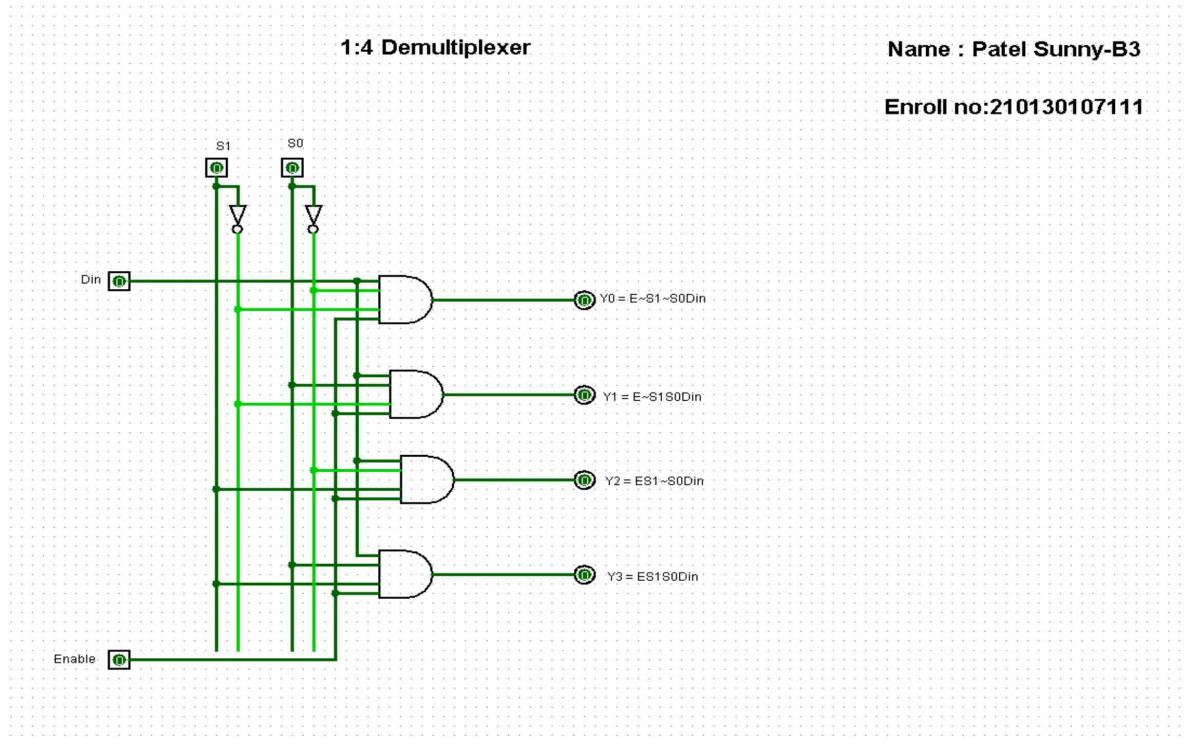
CO3: Design and implement Combinational and Sequential logic circuits and verify its working.

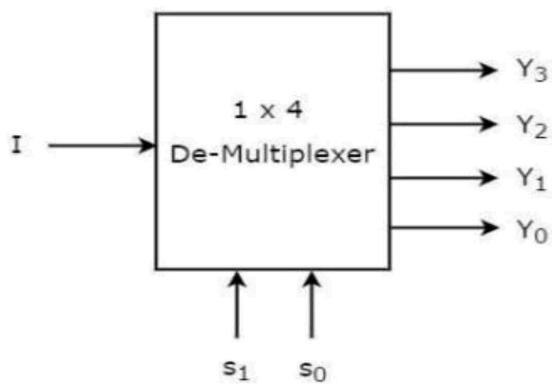
Module 2

Aim: Study and implement Multiplexer and Demultiplexer.

De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination can select only one output. De-Multiplexer is also called as De-Mux.

Selection Inputs		Outputs			
S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

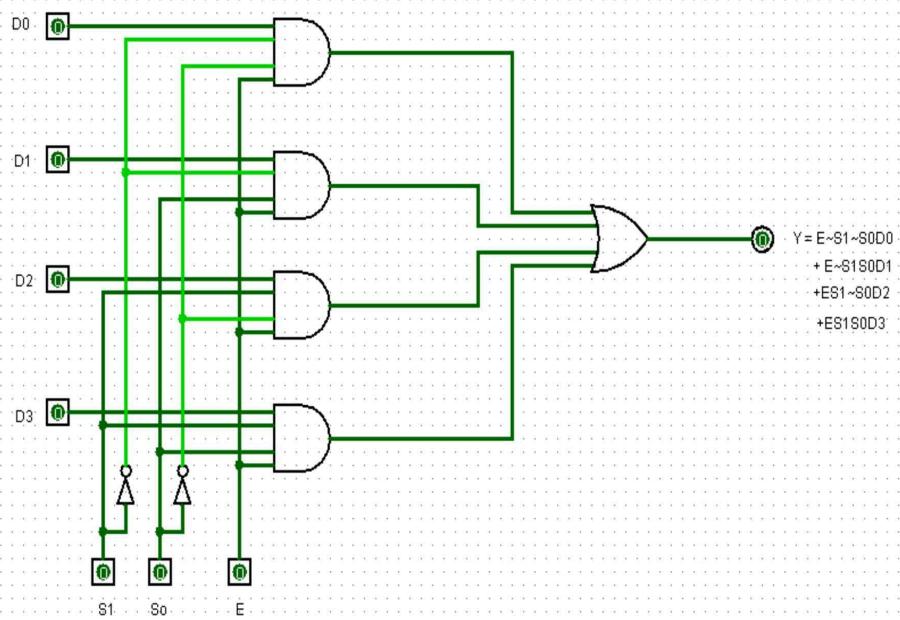




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4:1 Multiplexer



19. Practical 6

CO4: Examine the process of Analog to Digital conversion and Digital to Analog conversion

Module 4

Aim: Study and configure A to D convertor and D to A convertor.

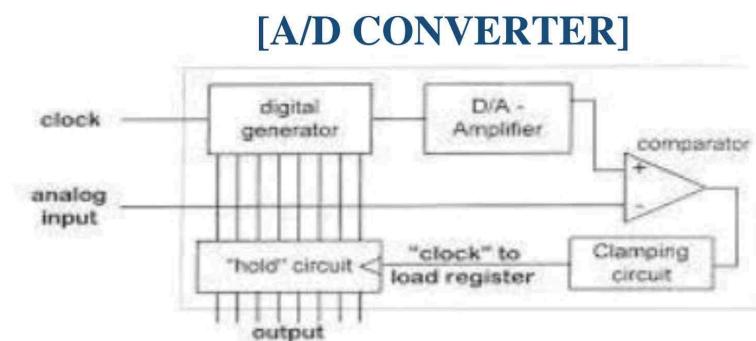
Code:

Analog-to-Digital Converter (ADC):

The transducer's electrical analog output serves as the analog input to the ADC. The ADC converts this analog input to a digital output. This digital output consists of a number of bits that represent the value of the analog input. For example, the ADC might convert the transducer's 800- to 1500-mV analog values to binary values ranging from 01010000 (80) to 10010110 (150). Note that the binary output from the ADC is proportional to the analog input voltages so that each unit of the digital output represents 10mV. The digital representation of the analog values is transmitted from the ADC to the digital computer, which stores the digital value and processes it according to a program of instructions that it is executing.

Analog-to-Digital Conversion:

An analog-to-digital converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input. The A/D conversion process is generally more complex and time-consuming than the D/A process. The techniques that are used provide insight into what factors determine an ADC's performance. Several important types of ADC utilize a DAC as part of their circuitry.

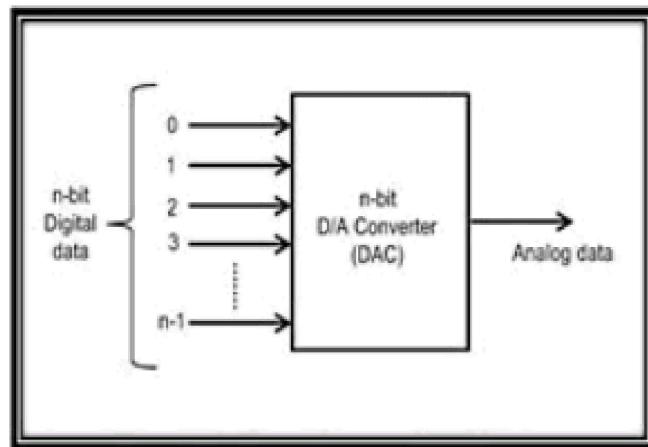


Digital-to-Analog Converter (DAC):

This digital output from the computer is connected to a DAC, which converts it to a proportional analog voltage or current. For example, the computer might produce a digital output ranging from 0000000 to 1111111, which the DAC converts to a voltage ranging from 0 to 10V.

Digital to Analog (D to A) Conversion:

Digital to Analog (D to A) Conversion: Basically, D/A conversion is the process of taking a value represented in digital code (such as straight binary or BCD) and converting it to a voltage or current which is proportional to the digital value. Fig. 7.2 shows the symbol for a typical 4-bit D/A converter. Now, we will examine the various input/output relationships



D	C	B	A	V(out)
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

20. Practical 7

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and implement a shifter.

Code: Shifters :- Shifters move bits and multiply or divide by powers of 2. As the name implies, a shifter shifts a binary number left or right by a specified number of positions.

1)Logical Shifter: shifts the number to the left (LSL) or right (LSR) and fills empty spots with 0's. Ex: 11001 LSR 2=00110; 11001 LSL 2=00100

2)Arithmetic shifter: is the same as a logical shifter, but on right shifts fills the most significant bits with a copy of the old most significant bit (msb). This is useful for multiplying and dividing signed numbers Arithmetic shift left (ASL) is the same as logical shift left (LSL). Ex: 11001 ASR 2=11110; 11001 ASL 2=00100

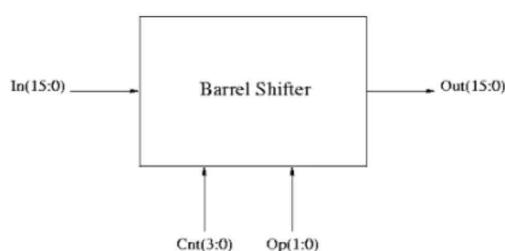
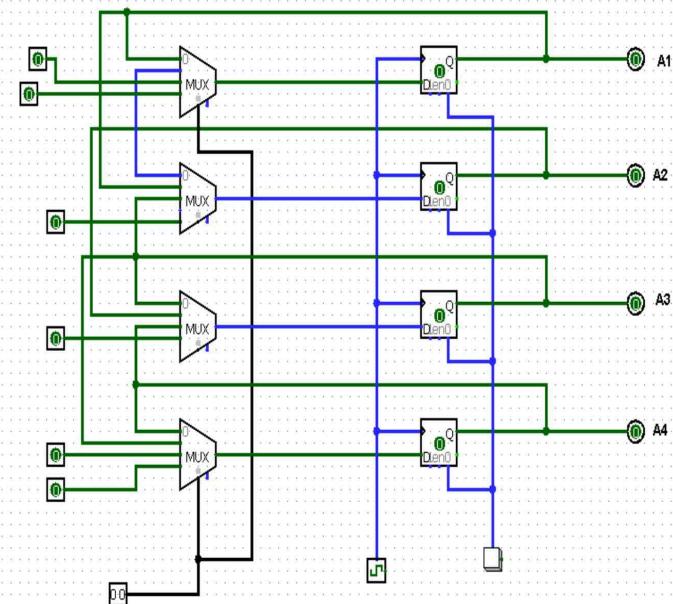
3) Barrel Shifters: The people most affected by change on a personal level seem in many cases to be blamshifters. The usual laments include, "The boss had it in for me. The company deceived me. Lady Luck was against me." They are self-doubters who end up failing because they fear success. They tend to undervalue their talents and destroy their chances of getting ahead. The losers in change are sometimes people who are so locked into their own identity they cannot tolerate working differently. Change to the job is unacceptable because the job and the person are one and the same. "They wanted me to be the fleet manager when I was already the head of security. They can't do that to me." But they did.

4)Frequency Shifter As demonstrated in Figure the conversion from LP01 to LP11 occurs with a frequency shift equal to the acoustic frequency. Thus, the setup in Figure acts as an optical frequency shifter

SHIFTER

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Row	Variable			Output
	S2	S1	S0	Y
0	0	0	0	?
1	0	0	1	No Shift
2	0	1	0	Shift Left
3	0	1	1	Rotate Right
4	1	0	0	?
5	1	0	1	?
6	1	1	0	?
7	1	1	1	?

21. Practical 8

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

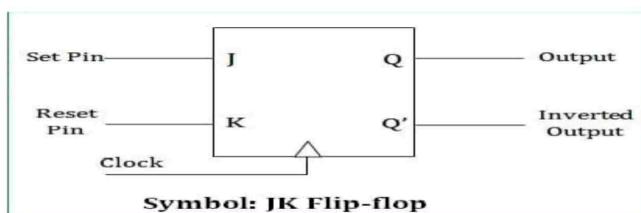
Aim: Study and implement Flip-flops.

SR flip flop:

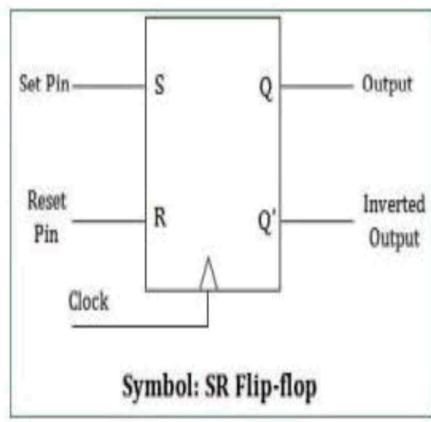
The SR flip-flop, also known as a SR Latch, can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled S and one which will “RESET” the device (meaning the output = “0”), labelled R.

JK flip flop:

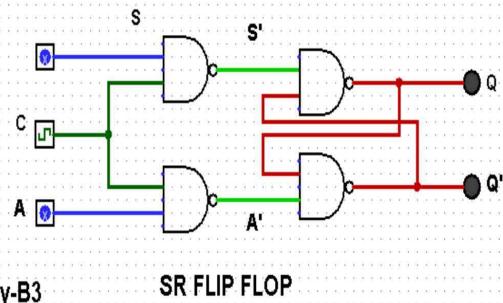
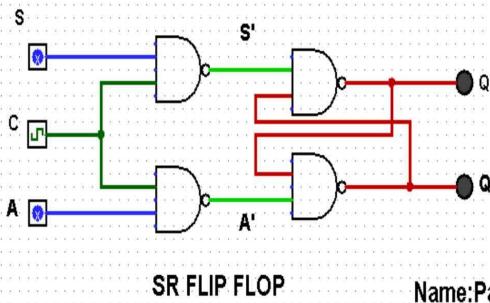
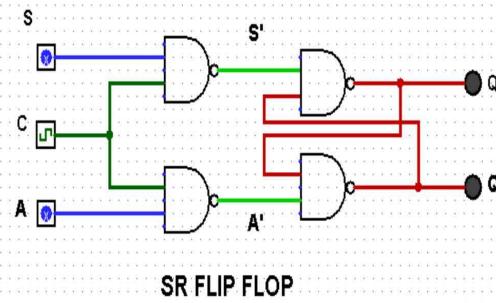
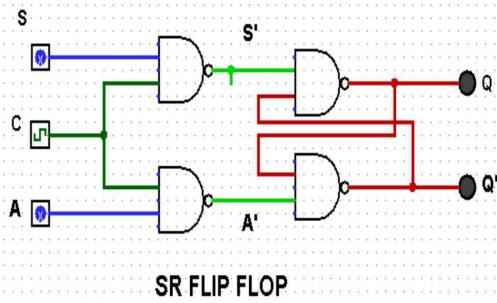
JK flip flop: The J-K flip-flop is the most versatile of the basic flip-flops. It has the input following character of the clocked D flip-flop but has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.



J	K	Q _n	Q _{n+1}	state
0	0	0	0	Q _n
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	1
1	0	1	1	
1	1	0	1	Q _{n'}
1	1	1	0	

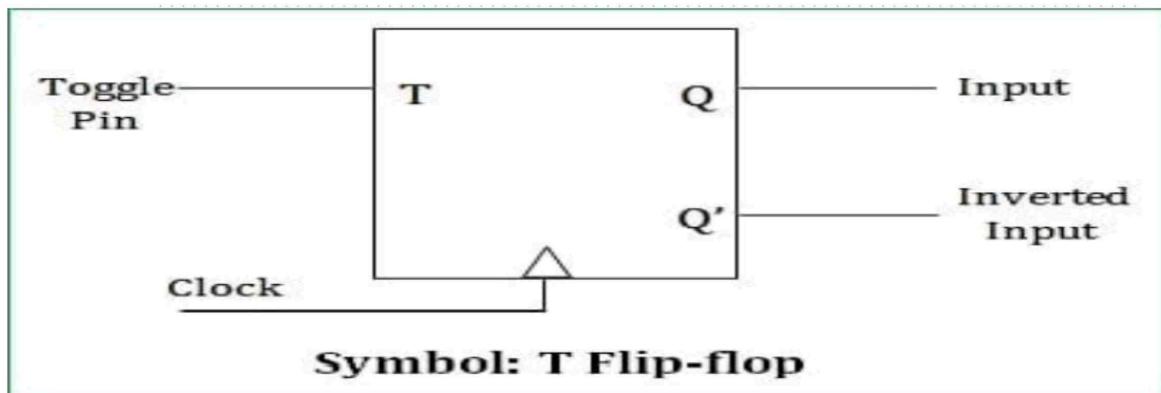


S	R	Q _n	Q _{n+1}	state
0	0	0	0	Q _n
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	1
1	0	1	1	
1	1	0	invalid	Don't care
1	1	1	invalid	

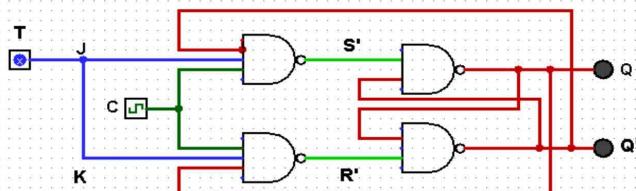
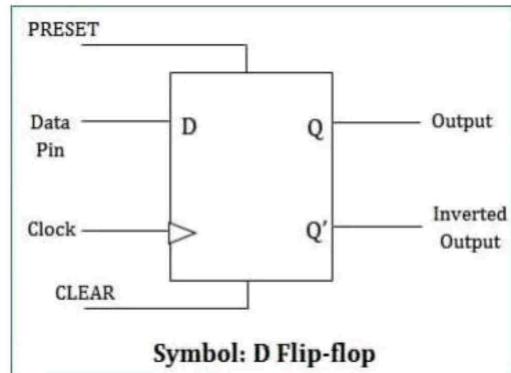


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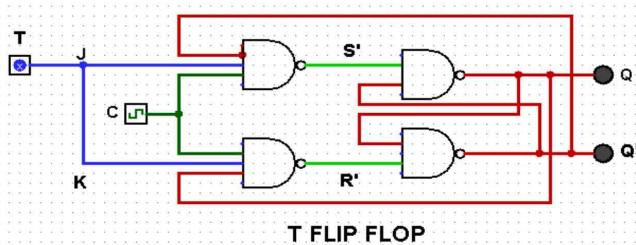


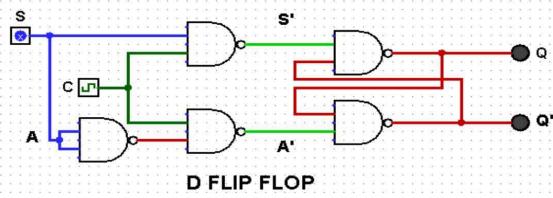
D	Q_{n+1}
0	0
1	1



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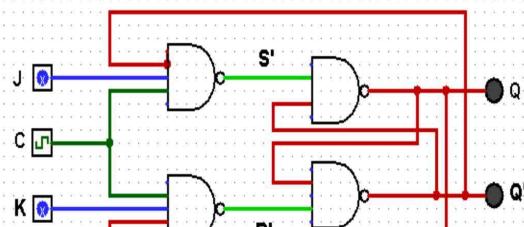
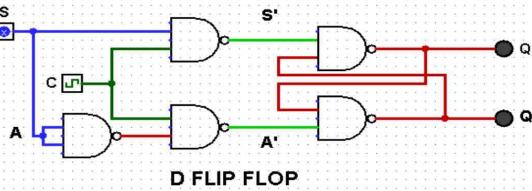
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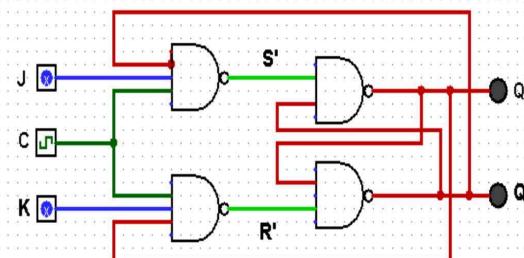


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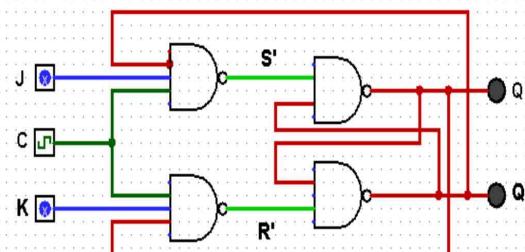
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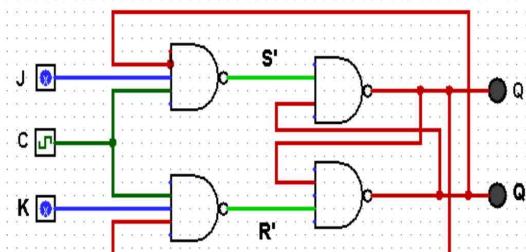
JK FLIP FLOP



JK FLIP FLOP



JK FLIP FLOP



JK FLIP FLOP

Name: Patel Sunny-B3

Enroll No: 210130107111

22. Practical 9

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 3

Aim: Study and implement Counter.

Counters:

Counters An 'N' bit binary counter consists of 'N' T flip-flops. If the counter counts from 0 to 2^N-1 , then it is called as binary up counter. Similarly, if the counter counts down from 2^N-1 to 0, then it is called as binary down counter

Asynchronous counters: The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle(T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1. External clock is applied to the clock input of flip-flop A and Q A output is applied To the clock input of the next flip-flop.

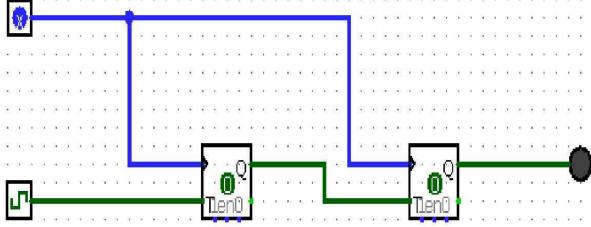
Synchronous counters:

Synchronous counters If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, Then such a counters called asynchronous counter

Synchronous up counters:

2-bit Synchronous up counter: The JA and KA inputs of FF-A are tied to logic1. So FF-A will work as a toggle flip-flop. The JB and KB inputs are connected to QA.

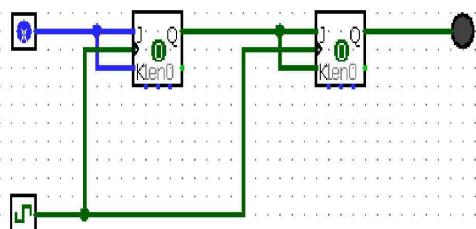
clock	Counter output		State number	Decimal counter output
	Qs	Qa		
Initially	0	0	-	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0



Asynchronous Counter

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Enroll no:210130107111



Synchronous Counter

23. Practical 10

CO3: Design and implement Combinational and Sequential logic circuits and verify its working

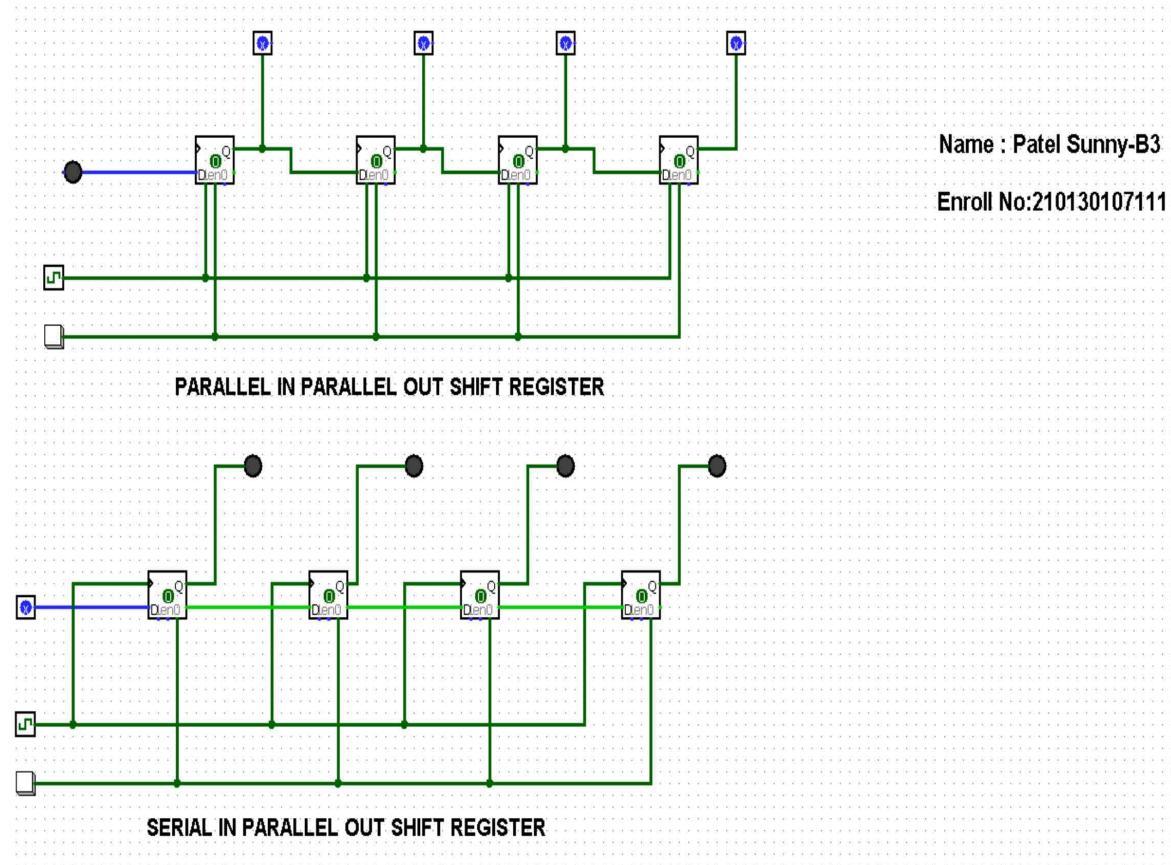
Module 3

Aim: Study and implement a shift register.

Code: Shift Register: Flip flops can be used to store a single bit of binary data (1 or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A Register is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data. The information stored within these registers can be transferred with the help of shift registers.

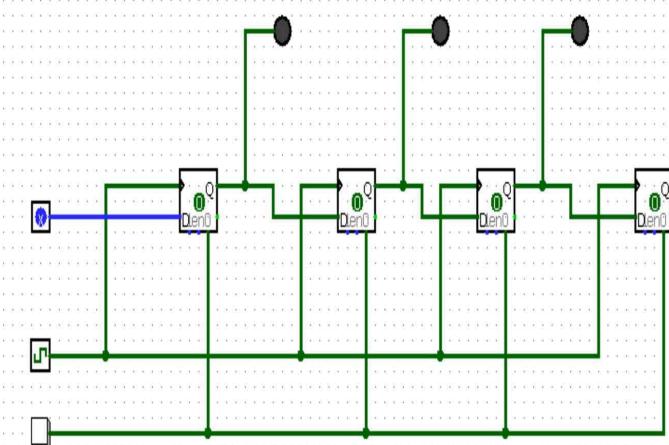
Shift registers are basically of 4 types. These are:

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register.

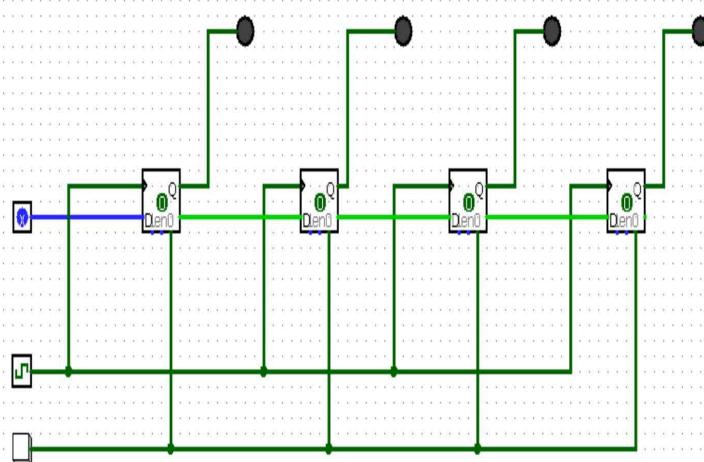


Name : Patel Sunny-B3

Enroll No : 210130107111



SERIAL IN SERIAL OUT SHIFT REGISTER



SERIAL IN PARALLEL OUT SHIFT REGISTER

24. Practical 11

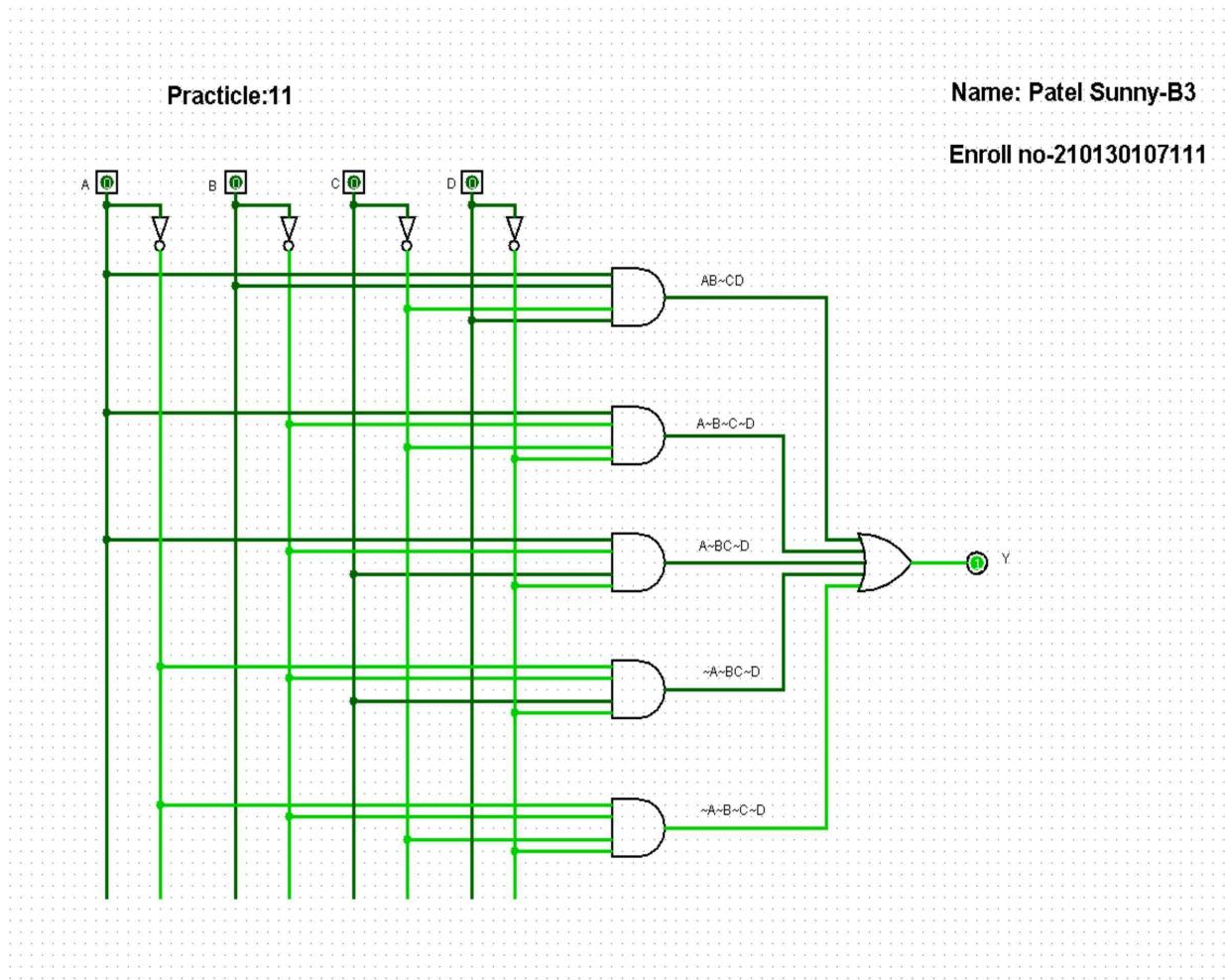
CO3: Design and implement Combinational and Sequential logic circuits and verify its working

Module 2

Aim: Study and implement K-Map for the given function:(SOP)

$$F = ABC'D + AB'C'D' + AB'CD' + A'B'CD' + A'B'C'D'$$

Code: K-Map (Karnaugh Map) In many digital circuits and practical problems we need to find expression with minimum variables. We can minimize Boolean expressions of 3, 4 variables very easily using K-map without using any Boolean algebra theorems. K-map can take two forms Sum of Product (SOP) and Product of Sum (POS) according to the need of problem. K-map is table like representation but it gives more information than TRUTH TABLE. We fill grid of K-map with 0's and 1's then solve it by making groups.



(1)

Assignment :-

C01: Solve the given problem using fundamentals of number system.

1. Explain De Morgan's theorem with truth tables.

⇒ DeMorgan suggested two theorems that form an important part of Boolean algebra. In the equation form, they are : 1. $\overline{AB} = \overline{A} + \overline{B}$

2. $\overline{A+B} = \overline{A} \cdot \overline{B}$

	A	B	\overline{AB}	$\overline{A} + \overline{B}$
Truth Table	0	0	1	1
	0	1	1	1
	1	0	1	1
	1	1	0	0

1. $\overline{AB} = \overline{A} + \overline{B}$: The complement of a product is equal to the sum of the complements.
2. $\overline{A+B} = \overline{A} \cdot \overline{B}$: The complement of a sum is equal to the product of the complements.

	A	B	$\overline{A+B}$	$\overline{A} \cdot \overline{B}$
Truth Table	0	0	1	1
	0	1	0	0
	1	0	0	0
	1	1	0	0

2. Simplify Boolean functions:-

$$\text{Given } F = \overline{A} \overline{B} C + \overline{A} B C + A \overline{B} C$$

$$\text{Simplification} = \overline{A} C (\overline{B} + B) + A \overline{B} C$$

$$\text{Final simplification} = \overline{A} C + A \overline{B} C$$

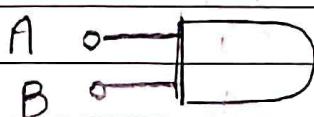
3. List & explain logic family.

(i) NOT gate: The output is a complement of input.



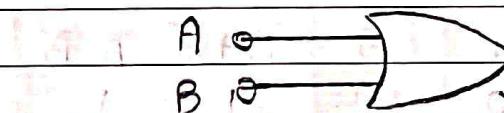
Input	Output
A	Y
0	1
1	0

2. AND gate:- The output is high only when all inputs are high.



Input	Output
A B	Y
0 0	0
0 1	0
1 0	0
1 1	1

3. OR gate: The output is high when at least one of the input is high.



Input	Output
A B	Y
0 0	0
0 1	1
1 0	1
1 1	1

Logic families:-

- (i) RTL: Registered Transistor logic
- (ii) DTL: Diode Transistor logic
- (iii) I²L: Integrated Injection logic
- (iv) TTL: Transistor Transistor logic

(2).

A-1

1. TTL: Propagation delay : ns
 Power dissipation per gate : 10mA
 Noise margin = 0.4V
 Fan-in = 8, Fan-out = 10,

2. CMOS: propagation delay = < 50
 power dissipation = 0.01
 noise margin = 5V
 Fan-in = 10
 Fan-out = 50

3. ECL: propagation delay = 1
 power dissipation = 50
 noise margin = 0.25V
 Fan-in = 5
 Fan-out = 10

Q-4 Describe error detecting & correcting code:

* Error - detecting codes:-

- Noise can alter or the data in transmission.
- The 1s may get changed to 0s and 0s to 1s. Because digital system must be accurate to digit, errors can pose a serious problem.
- Single bit errors should be detect & correct by different schemes.
- Parity, checks sums and Block parity are the examples of error detecting code.

- => Parity : parity bit is simplest technique
- There are two types of parity - odd parity and even parity.
 - For even parity, the parity is set to a 0 or a 1 at the transmitter such that the total no. of 1 bits in word including the parity bit is an even number.
 - For exp, 110 binary no. has "1" as odd parity and "0" as even parity.

* check sums:-

- Simple parity can't detect two errors within the word.
- Added to the sum of previously transmitted words.
- At the transmission, check sum up to that time is sent to received.
- If there is an error, the receiving location can ask for retransmission of entire data.

* Error Correcting Codes:-

- 7 bit Hamming Code is widely used error correcting code, containing 4 bits of data and 3 bits of even
- Pattern : $P_1, P_2, D_3, P_4, D_5, D_6, D_7$
- Group 1 : P_1, D_3, D_5, D_7
 Group 2 : P_2, D_3, D_6, D_7
 Group 3 : P_4, D_5, D_6, D_7

(3) A-1

* How to detect errors?

Exp: Received data: 1001001

$$P_1 P_2 \oplus D_3 P_4 D_5 D_6 D_7 = 1001001$$

$$P_1 D_3 D_5 D_7 = 1001 \text{ (No error)}$$

$$P_2 D_3 D_5 D_7 = 0001 \text{ (Error)}$$

$$P_4 D_5 D_6 D_7 = 1001 \text{ (No error)}$$

- The error word is $010 = 2_{10}$
- Complement the 2nd bit (from left)
- Correct code is 1101001

Q-5. Diff. TTL, Schottky TTL and CMOS

SE. NO.	PARAMETERS	CMOS	TTL
1.	Device used	n-channel & p-channel MOSFET Transistor	Bipolar junction Transistor
2.	V_{IH} (min)	3.5V	2V
3.	V_{IL} (max)	1.5V	0.8V
4.	V_{OH} (min)	4.95V	2.7V
5.	V_{OL} (max)	0.005V	0.4V
6.	High level noise margin	$V_{NH} = 1.45V$	0.4V
7.	Noise immunity	Better than TTL	Less than CMOS
8.	Switching Speed	Less than TTL	Better than CMOS
9.	Fan-out	50	10
10.	Power Supply Voltage	3-15V	Fixed 5V

Assignment - 2

CO 2: Analysis working of logic families and logic gates and design the simple circuit using various gates for a given problem.

Q-1. Explain K-map.

- K-map means Karnaugh map which is a systematic method of simplifying the Boolean expression.
- The K-map is a chart, composed of adjacent of adjacent cells, each representing a particular combination of variables.
- The output values placed in each cell are derived from the minterm of Boolean fun.
- A minterm is product term that contains all of the function's variable exactly one either complemented or not complemented.

* two-variable K-maps:-

- The two-variable expression A can have $2^2 = 4$ possible combinations of input Variables A and B .

	0	1
0	0	1
1	0	1
	2	3

- Each of these combination $\bar{A}\bar{B}$, $\bar{A}B$, $A\bar{B}$ and AB is called minterm.

(2). A - 2

* three-variable K-maps:-

- A function in three variable expressed in SOP form can have eight possible combination: $\bar{A}\bar{B}C$, $\bar{A}B\bar{C}$, $A\bar{B}C$, $A\bar{B}\bar{C}$, AB , $\bar{A}\bar{B}\bar{C}$, ABC .
- In POS form the eight possible combination are $A+BC$, $A+B+\bar{C}$, $A+\bar{B}+C$, $A+\bar{B}+\bar{C}$, $\bar{A}+B+C$, $\bar{A}+B+\bar{C}$, $A+\bar{B}+C$, $\bar{A}+\bar{B}+\bar{C}$

		AB	00	01	11	10	
		C	0	1	2	6	4
		0					
		1					
		0					
		1					

* four-variable K-maps:-

- The four variable A, B, C & D have sixteen possible combination that can be represented by map as follows.

		AB		00	01	11	10	
		CD		00	01	11	10	
		00	0	4	12	8		
		01	1	5	13	9		
		11	3	7	15	11		
		10	2	6	14	10		

Q-2) obtain expression

(a) $F(x, y, z) = \Sigma(2, 3, 6, 7)$

$$F = x$$

$$\text{Ans. } \rightarrow F = x$$

(b) $F(A, B, C, D) = \Sigma(4, 6, 7, 15)$

	A	B	C	D	F
	0	1	0	1	
0	0	0	0	0	0
1	1	0	0	0	1
2	0	1	0	0	0
3	1	1	0	0	1
4	0	0	1	0	0
5	1	0	1	0	1
6	0	1	1	0	1
7	1	1	1	0	1
8	0	0	0	1	0
9	1	0	0	1	1
10	0	1	0	1	1
11	1	1	0	1	1
12	0	0	1	1	0
13	1	0	1	1	1
14	0	1	1	1	1
15	1	1	1	1	1

$$F = \bar{A}B + BCD$$

Q.1 A-1

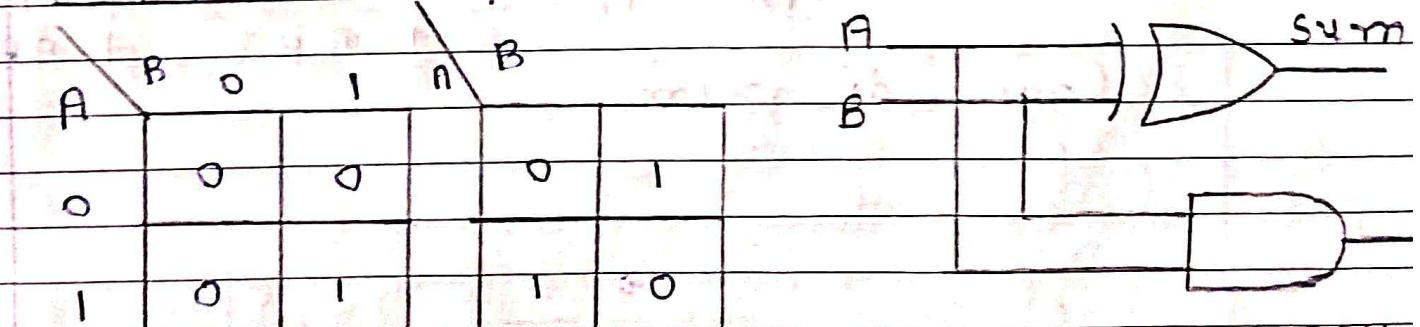
Q.3 Describe adder & subtractor.

Adder:- The first three operations produce a sum whose length is one digit, but when the last operation is performed sum is two digits. The higher significant bit of this result is called a carry, and lower significant bit is called sum. The logic circuit which performs this operation is called a half-adder. The circuit which performs addition of three bits is a full-adder.

Half Adder:- The half-adder operation needs two binary inputs: augend and addend bits; and two binary outputs: sum and carry.

Inputs		Outputs		A	B	Half adder	carry
A	B	carry	sum				
0	0	0	0				
0	1	0	1				
1	0	0	1				
1	1	1	0				

logic diagram:



$$\text{carry} = AB$$

$$\text{sum} = A\bar{B} + \bar{A}B$$

$$= A \oplus B$$

* Full Adder :- is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by A and B, represent the two significant bits to be added.

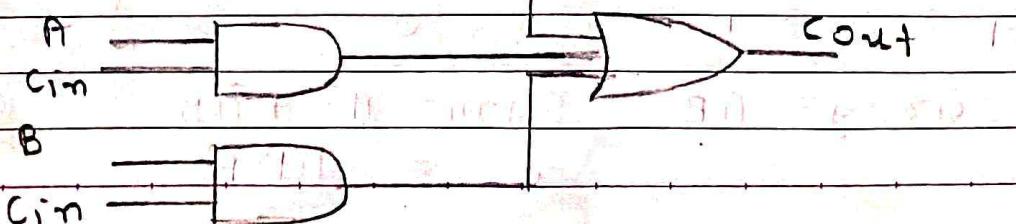
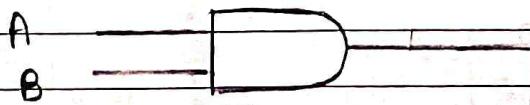
Inputs			Outputs		Cin
A	B	Cin	Carry sum		
0	0	0	0	0	
0	0	1	0	1	A
0	1	0	0	1	
0	1	1	1	0	
1	0	0	0	1	B
1	0	1	1	0	
1	1	0	1	1	
1	1	1	0	0	

↓ Cout

A	B	Cin	0	1	10	A	B	Cin	0	1	0	1	0
0	0	0	1	0		0	0	1	0	1		0	1
1	0	1	1	1		1	1	0	1	1		1	0

$$\text{Cout} = AB + AC_{\text{int}} + BC_{\text{int}} \quad \text{Sum} = \bar{A}\bar{B}C_{\text{in}} + \bar{A}B\bar{C}_{\text{in}} + A\bar{B}\bar{C}_{\text{in}} + ABC_{\text{in}}$$

logic diagram



(3) A-2

Subtractors:- (i) Half subtractor
(iii) Full subtractor

(i) Half Subtractor:- is a combinational circuit that subtract two-bits and produced their difference. It also has an output to specify if a 1 has been borrowed.

For difference Inputs Outputs

	A	B	A	B	Difference	Borrow
	0	1	0	0	0	0
	0	1	0	1	1	1
	1	0	1	0	1	0
	1	0	1	1	0	0
	1	1	0	0	1	1
	1	1	0	1	0	0
	1	1	1	0	1	0
	1	1	1	1	0	1

$$\text{Difference: } A\bar{B} + \bar{A}B \\ = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

(ii) Full-Subtractor:- is a combinational circuit that performs a subtraction b/w two bits, taking into account borrow of the lower Significant stage.

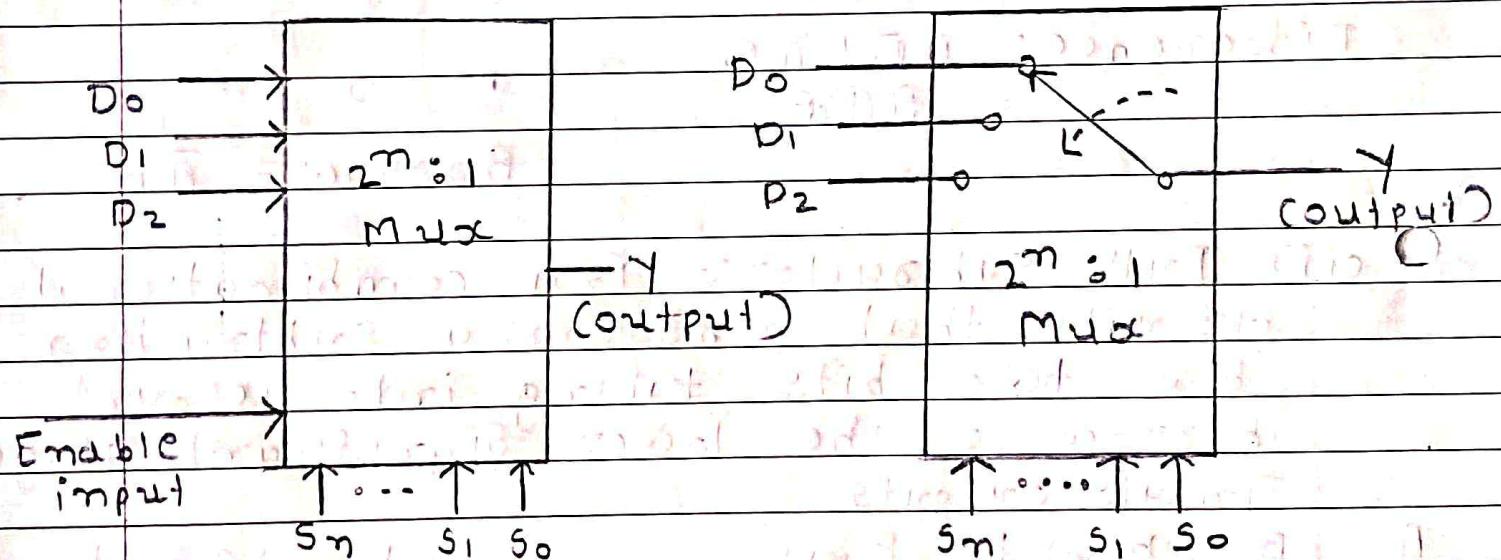
Inputs Outputs A B_{Bin}

A	B	B _{Bin}	D	B _{out}	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	1	
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	1	1	

$$D = \bar{A}\bar{B}B_{bin} + \bar{A}B\bar{B}_{bin} + A\bar{B}B_{bin} + AB\bar{B}_{bin}$$

Q.4. Explain Multiplexers:-

- => In digital System, many times it is necessary to select single data line from several data-input lines, and the data from the selected data line should be available on the output. The digital circuit which does this task is a multiplexer. It is a digital switch.
- The selection of a particular input line is controlled by a set of selection lines. Since multiplexer selects one of the input and routes it to output, it is also known as data selector.
- There are 2^n input lines and n selection lines whose bit combinations determine which input is selected.



Q-4)

A-2

* Demultiplexers:-

- A demultiplexer is a device that allows digital information from one source to be routed onto a multiplexer for transmission over diff. destinations.
- Consider an integer m , which is constrained by following relation:-
- $m = 2^n$, where $m \neq n$ are both integers

Data input	Din	y_0	—	—
		y_1	—	—
		y_2	—	—
Enable	E	y_n	—	—
		y_{2-1}	—	—

Types of demultiplexers:-

- (i) 1:4 demultiplexers
- (ii) 1:8 demultiplexers.

Q-5. Describe parity checker & generator.

- A parity bit is used for the purpose of detecting errors during transmission of binary info.
- A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even.
- The message, including the parity bit is transmitted and then checked.

at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted.

- * IC 74180 : Parity generator/checked
- The 74180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval system. Both even and odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bit.

I6	1		8	I ₀
I7	2	15	9	I ₁
PE	3		10	I ₂
P0	4		11	I ₃
ZE	5		12	I ₄
CO	6		13	I ₅
GND	7		14	14 V _{CC}

C13. Assignment :- 3

CO3: Design and implement combinational and sequential logic circuits and verify its working.

Sequential circuits

combinational circuits

- | | |
|--|---|
| 1. Sequential circuits use computatively harder to design. | 1. Combinational circuits are easy to design. |
| 2. Parallel adder is a combinational circuit. | 2. So serial adder is sequential circuit. |
| 3. Memory unit is not required in combinational circuits. | 3. Memory unit is required to store the past history. |
| 4. Sequential circuits are slower than a combinational circuits. | 4. Combinational circuits are faster in speed. |

2. List and explain flip-flops :-

- The flip-flops are basically the circuit that maintain a certain state unless and until directed by input for changing data.
- Types of flip-flops:-

1. S-R flip flop
2. J-K flip flop
3. T flip flop
4. D flip flop

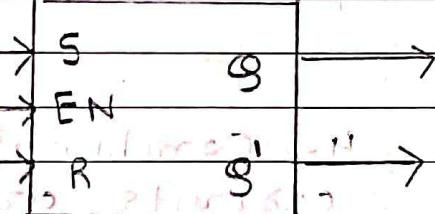
7. S-R Flip-flop:-

EN	S	R	G _n	G _{nti}	state
1	0	0	0	0	No change
1	0	0	1	1	

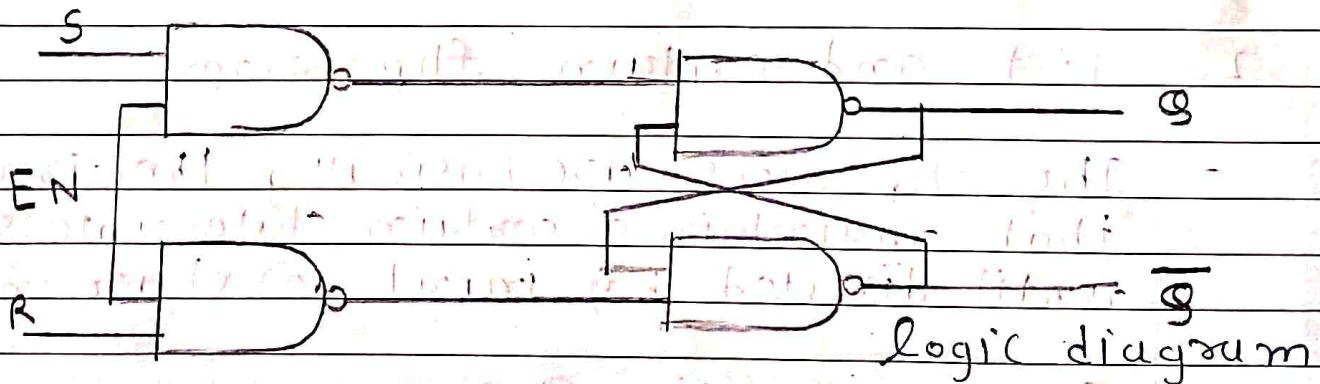
EN	S	R	G _n	G _{nti}	Reset
1	0	1	0	0	
1	0	1	1	0	
1	1	0	0	0	Set or
1	1	0	1	1	

EN	S	R	G _n	G _{nti}	Indeterminate
1	1	1	1	1	X
0	X	X	0	0	No change

EN	S	R	G _n	G _{nti}	Set or Reset
0	X	X	0	0	
0	X	X	1	1	



logic symbol of SR flip-flop



logic diagram

Q2) A - 3

→ D Flip-flop

EN	D	Q_n	Q_{n+1}	state
1	0	0	0	Reset
1	0	1	0	

1	1	0	1	set
1	1	1	1	

0	X	0	0	No-change
0	X	1	1	

* J-K Flip-flop :-

EN	J	K	Q_n	Q_{n+1}	state
1	0	0	0	0	No change
1	0	0	1	1	

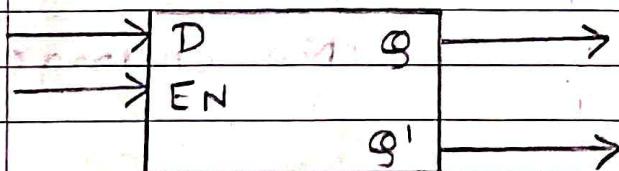
1	0	1	0	0	Reset
1	0	1	1	0	

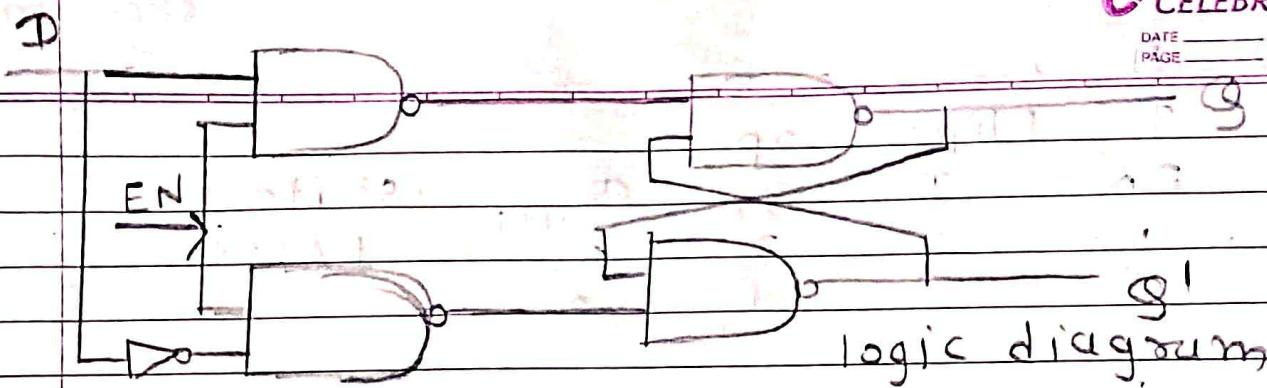
1	1	0	0	1	set
1	1	0	1	1	

1	1	1	0	1	Toggle
1	1	1	1	0	

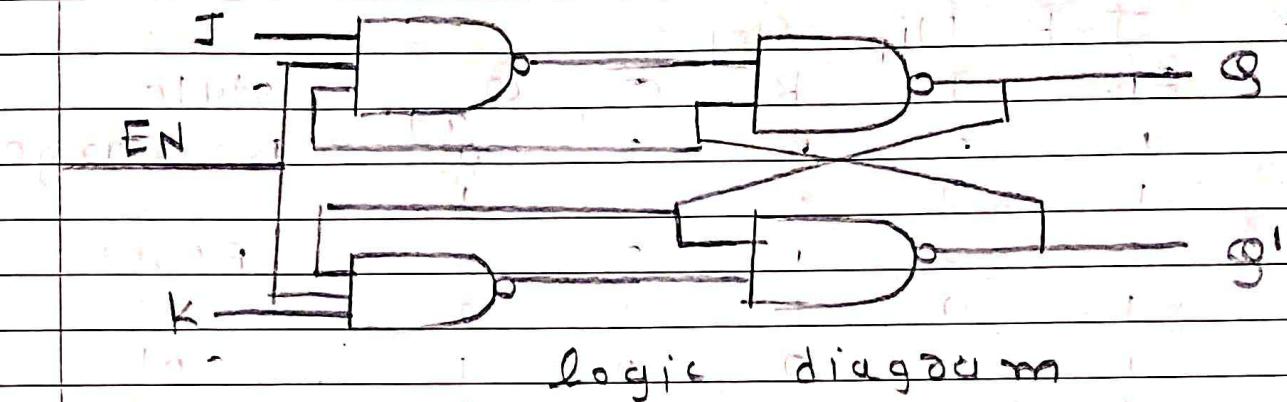
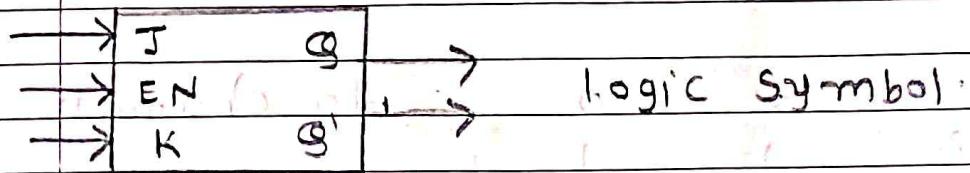
0	X	X	0	0	No change
0	X	X	1	1	

Logic Symbol :- D Flip-flop





J-K flip-flop



→ T flip-flop:-

EN T Qn Qn+1 state
1 0 0 0 No change

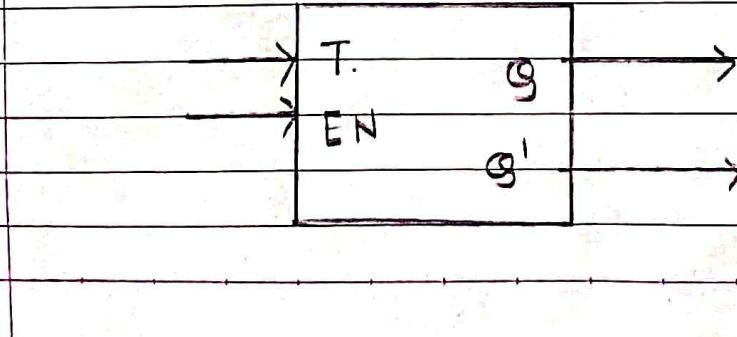
1 0 1 1

1 1 0 1 Toggle

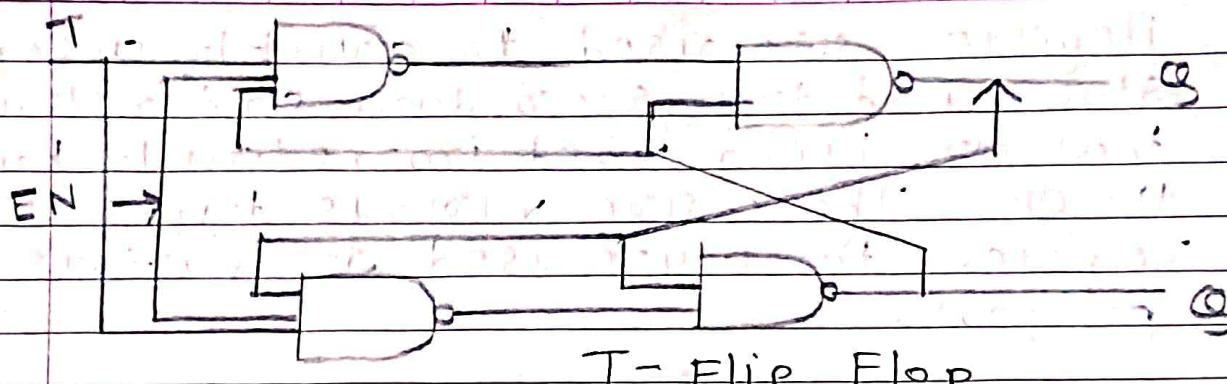
1 1 1 0

0 X 0 0 No change

0 X 1 1



(3) A-3



Q-3 list and explain registers:-

- ⇒ i) Buffer register
- ii) Shift register
- iii) Bidirectional shift register
- iv) Universal shift register

- As a flip-flop can store only one bit of data at a time, it is referred to as a single bit register.

- A register is a set of FFS used to store binary data; The storage capacity of a register is the number of bits of digital data it can retain.

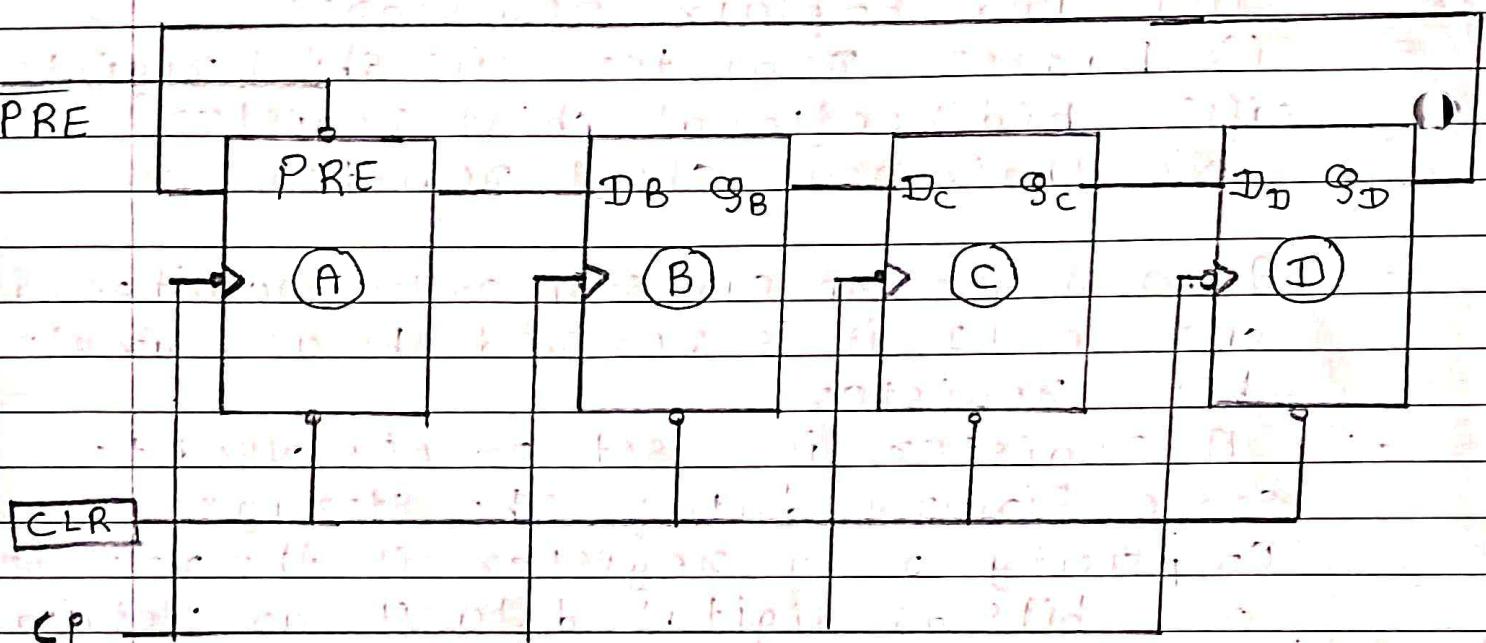
- Loading a register means setting or re-setting the individual FFS in putting data into the register so that their states correspond to the bits of data to be stored. Loading may be serial or parallel.

- In serial loading, data is transferred into the register in serial form one bit at a time.

- In parallel loading, the data is transferred into the register in parallel form meaning that all the FFS change triggered into their new states at the same time.

- Registers are used to quickly accept, store and transfer data and instruction that are being used immediately by the CPU. There are various types of registers those are used for various purpose.

Q.4 Describe Ring Counter:-



- Figure shows the logic diagram for four-bit ring counter. In all stages which
- The Q output of each stage is connected to the Q inputs of the next stage and the output of last stage feedback to the input of first stage
- The CLR followed by PRE make the output of first stage to 1 and remaining outputs are zero.
- The first clock pulse produces $Q_B = 1$ and remaining outputs are zero. According to the clock pulses applied at the

(4) A-3

Clock input C_P , a sequence of four step states is produced. These states are listed in table.

Figure gives the timing sequence for a four bit ring counter.

clock Pulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

- the ring counter can be used for counting the number of pulses.

- The number of pulses counted is ready by nothing which flip-flop is in state 1 or it will:

- No decoding circuitry is required.

- Ring counter can be constructed for any desired MOD number, that is $MOD = N$ ring counter requires N flip-flop.

Q-5. Describe how to design counters using flip-flops.

→ Step 1: Number of flip-flops.

- Based on the description of the problem determine the required number of the FFS - the smallest value of n 's which that the number of states $N \leq 2^n$ and the desired counting sequence.

Step 2: State diagram:

- Draw the state diagram showing all the possible states.

Step 3: choice of flip-flops and excitation table:

- Select the type of flip-flops to be used and write the excitation table.

An excitation table is a table that lists the present state, the next state and the required excitations.

Step 4: Minimal expressions for excitations:

- obtain the minimal expressions for the excitations of the FFS using K-maps for excitation of flip-flops in terms of the present states and inputs.

Step 5: logic diagram:

- Draw the logic diagram based on the minimal expressions.

(1) Assignment :- 4

Q 4: Examine the process of Analog digital conversion.

Q-1 Explain weighted resistor converter.

$$\rightarrow V_{out} = - \left(D_3 + \frac{1}{2} D_2 + \frac{1}{4} D_1 + \frac{1}{8} D_0 \right) \frac{R_f}{R}$$

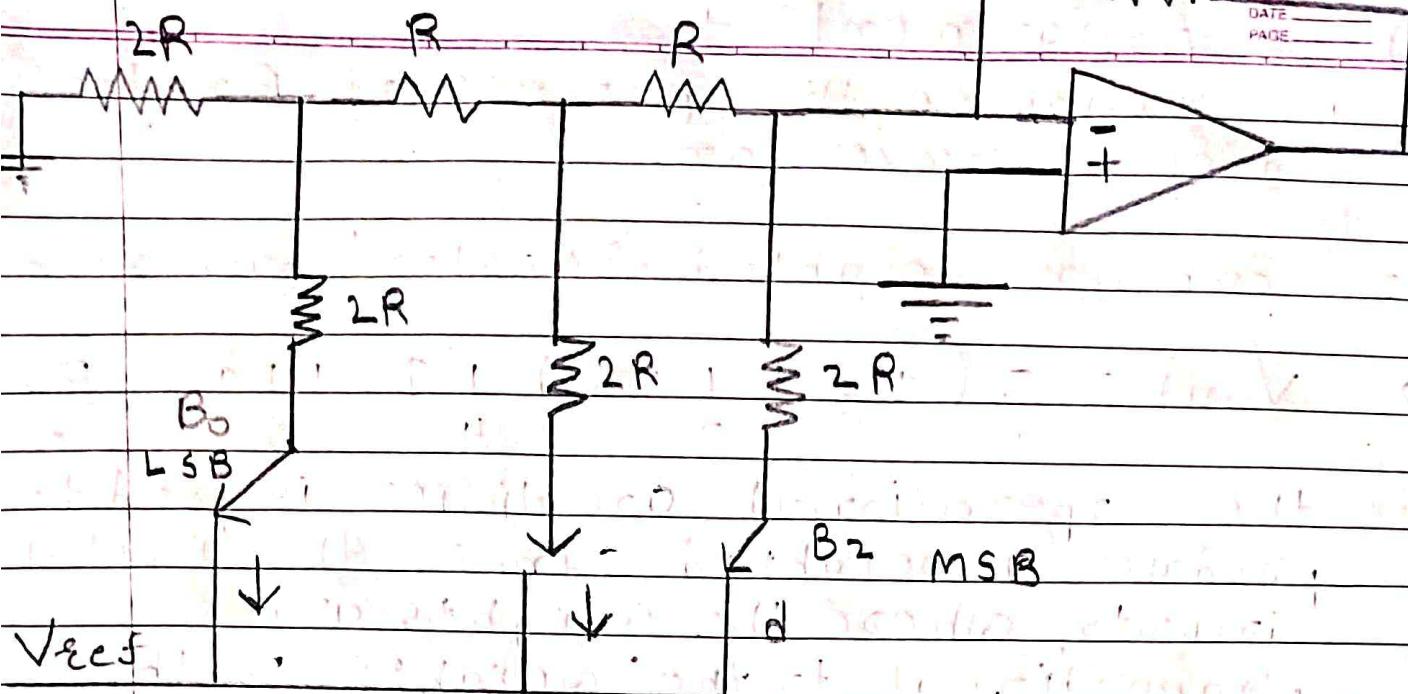
- the operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit position of inputs.

- Since the amplifier is connected as an inverting amplifier, each input is amplified by a factor equal to ratio of the feedback resistance devived by the input resistance to which it is connected.

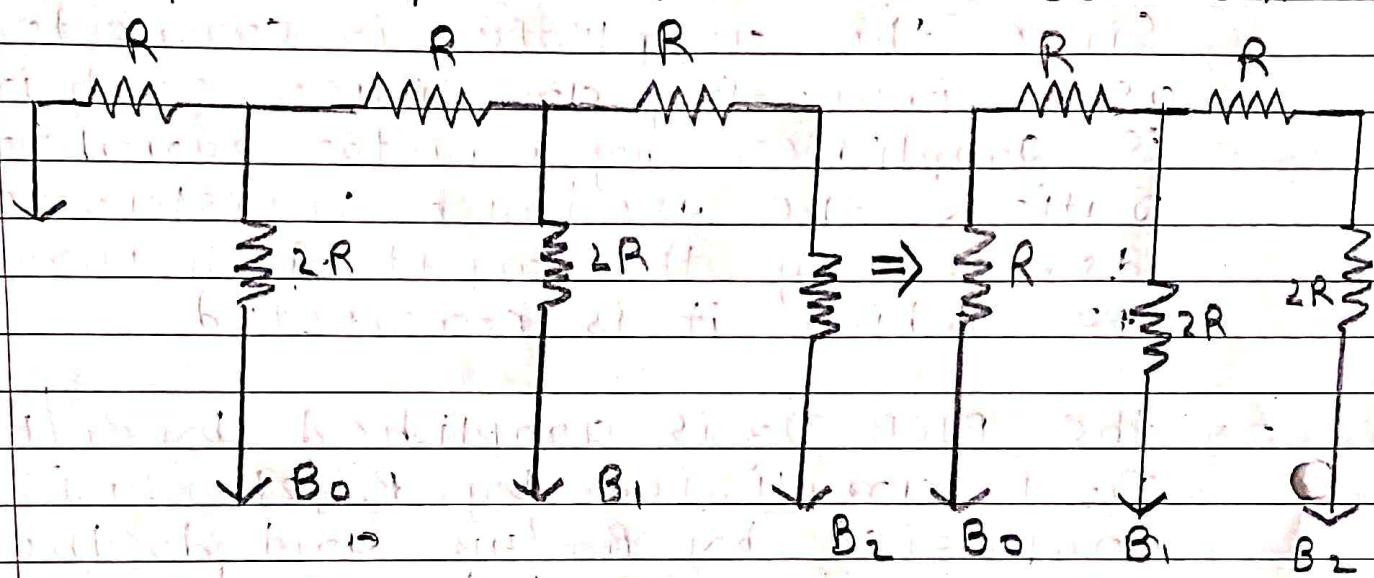
- the MCB D_3 is amplified by R_f/R , D_2 is amplified by $R_f/2R$, D_1 is amplified by $R_f/4R$ and do the LSB is amplified by $R_f/8R$

Q-2. Explain R₂R ladder D/A converter.

\rightarrow R₂R digital to analog converter or DAC is a data converter which use two resistors to convert digital binary number into an analog output signal proportional to value of digital numbers.



→ Output impedance of R-2R ladder DAC:



Q.3. Describe Specification of A/D & D/A converters:-

- **① Resolution:** - smallest change in digital state that can occur in a bit.
- Smallest change that can occur in an analog output as a result of change in digital input.
- Equals to weight of 'LSB' and also referred to as digital input value.

(2). A-4

• resolution = $\frac{1}{\text{No of steps}} \times 100\%$

2. Accuracy:-

- Specified in terms of full scale error and linearity error.
- Full scale is max deviation of DAC's output from its expected value.
- Linearity error is maximum deviation of analog output from ideal output.

(3)

Setting time:-

- The time required for analog output to settle within $\pm \frac{1}{2}$ LSB of final value after a change in digital output.
- It is because of presence of switches, active devices and inductance.

(4). Offset Voltage:-

- Ideally output of DAC should be zero when binary input is zero.
- However, in practice there is a very small voltage under this condition called offset voltage.

(5). Monotonicity:-

- This means that the staircase output will have no downward steps as binary inputs is incremented to its full scale value.

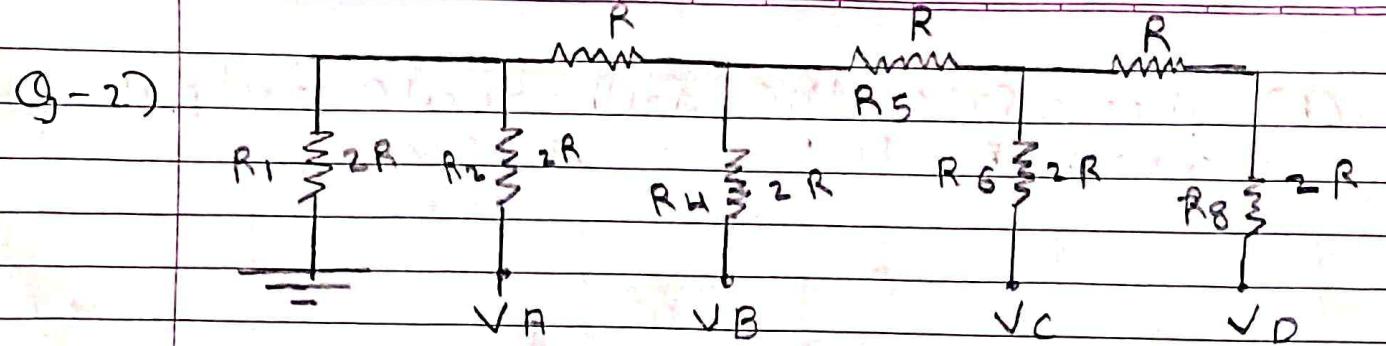
(6). Temperature insensitivity:

- The change of voltage for any fixed digital input varies with temperature.

Q-4. Explain quantization and encoding:

- ⇒ In a digital to analog converter, the possible number of digital inputs is fixed.
- for example, in a 3-bit D/A converter there are 8 possible inputs.
 - In contrast, in an analog to digital converter the input analog voltage can have any value in a range but digital output can have any value discrete values for an A/D converter.
 - Therefore, the presented suitably in 2^n intervals. So whole range of analog voltage is required to be presented.
 - This process is known as quantization.
 - Each interval is then assigned a unique n-bit binary code, which is replaced to is encoding.
 - Each interval is assigned a 3-bit binary value.
 - Each the intervals of analog voltage and their corresponding digital values assigned are shown in fig.

C2) A-4

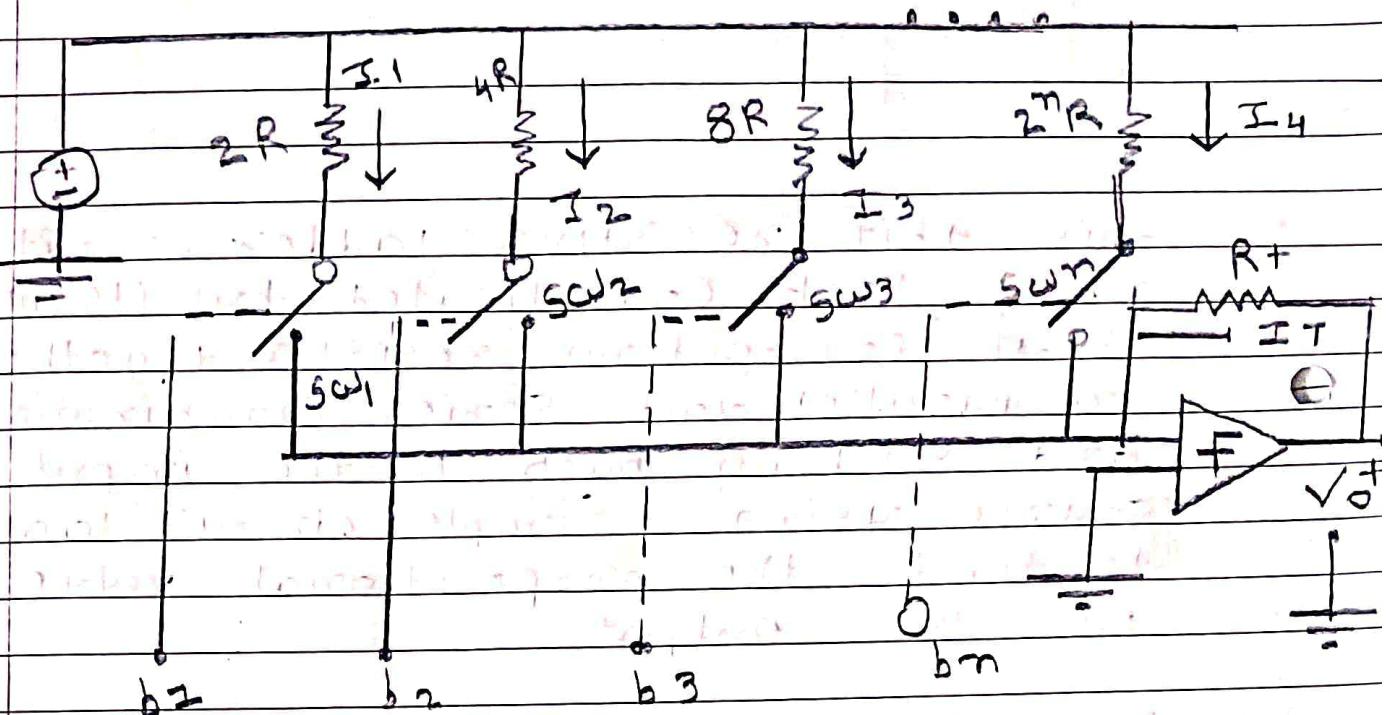


- this 4 bit resistive ladder circuit may look complicated, but it's all about connecting resistors together in parallel and series combinations and working back to the input source using simple circuit laws to find the proportional value of the output.
- less Assume all binary inputs are grounded at 0 volts, that is $V_A = V_B = V_C = V_D = 0 \text{ V (} 10^0 \text{)}.$ The binary code corresponding to these four inputs will therefore be 1000.
- Starting from the left hand side and using the simplified eqn for two parallel resistors and series resistor we can find the equivalent resistance of the ladder network as resistor R_1 & R_2 are in 'parallel' with each other but in "series" with resistor R_3 .

$$R_A = R_3 + \frac{R_1 \times R_2}{R_1 + R_2} = R + \frac{2R \times 2R}{2R + 2R} = R + R = 2R$$

$$R_B = R_5 + \frac{R_A \times R_4}{R_A + R_4} = R + \frac{2R \times 2R}{2R + 2R} = 2R$$

Q-1 (b) Therefore, the full-scale output when $R = 1\text{k}\Omega = -9.375\text{V}$



→ The operational amplifier is used as a summing amplifier. Due to high input impedance of, summing current will flow through it. Hence the total current through R_f can be given as

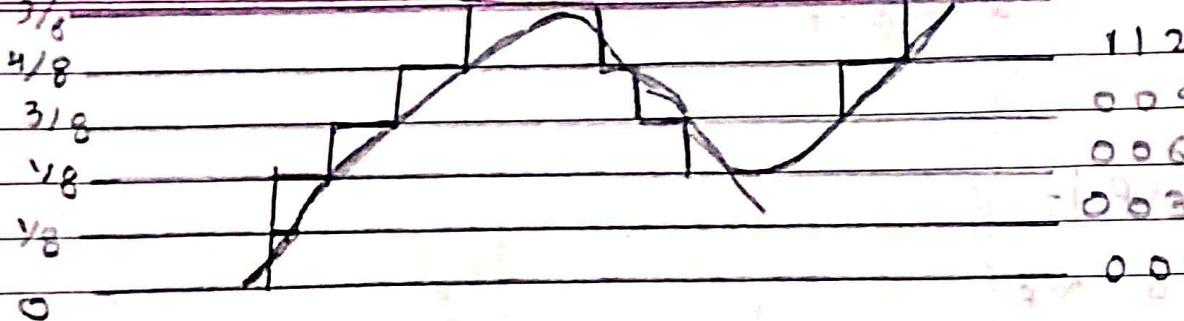
$$\begin{aligned}
 V_o &= -I_f(R_f) = -(I_{in} + \dots + I_n)/R_f \\
 &= -\left(\frac{b_1 V_R}{2R} + \frac{b_2 V_R}{4R} + \dots + \frac{b_n V_R}{2^n R}\right) R_f \\
 &= -\frac{V_R}{R} \left(b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n} \right)
 \end{aligned}$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})$$

compute is connected to the encoder.

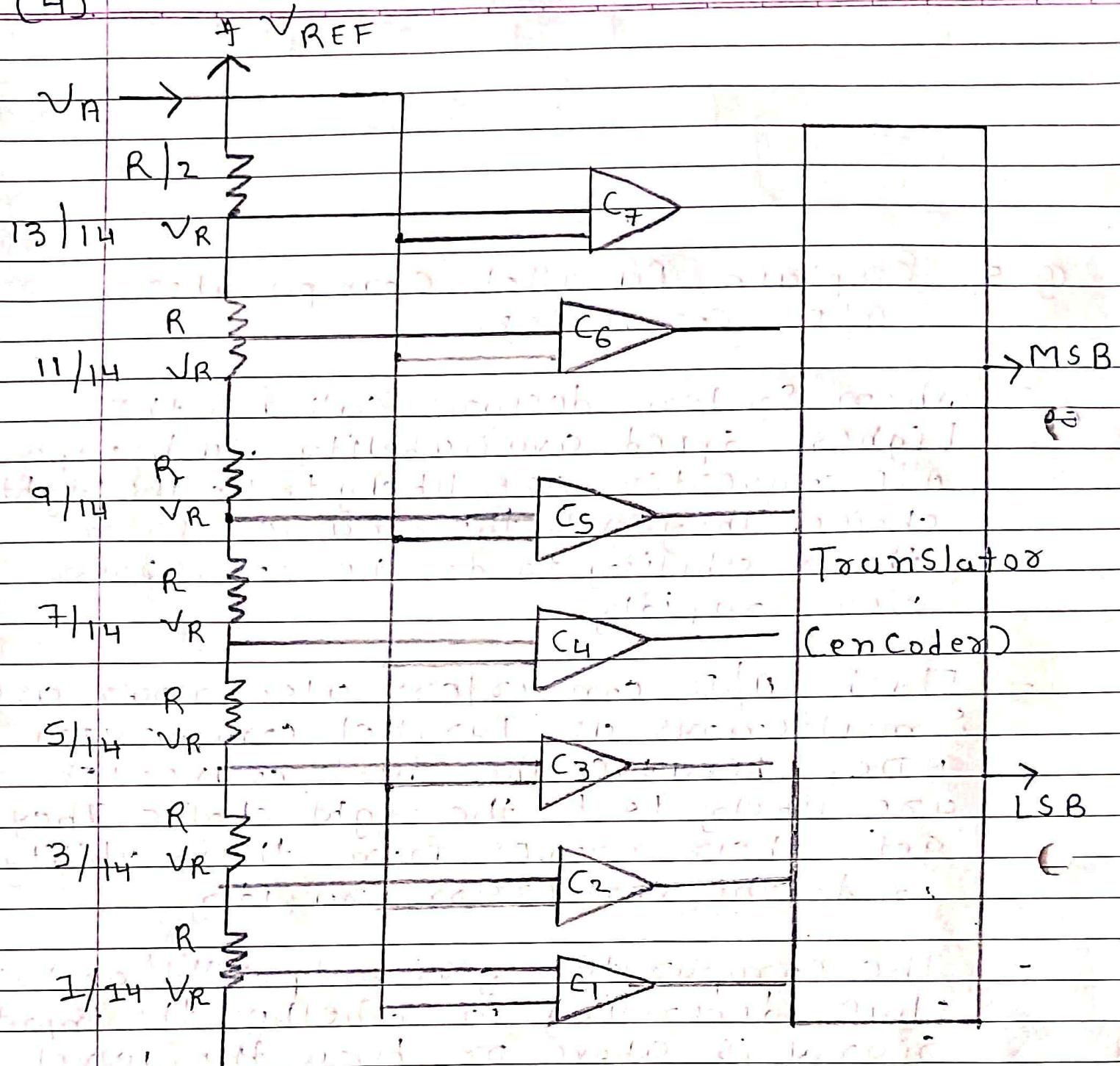
3) A-4



Q-5. Explain Parallel Comparators
A/D converters.

- When system designs call for the highest speed availability flash-type A/D converters are likely to be the right choice. They get their names from their ability to do the conversion very rapidly.
- Flash A/D converters, also known as simultaneous parallel comparators ADC, because the fast converters are likely to be the right choice. They get their names from their ability to do the conversion rapidly.
- The comparators give output "1" or "0" state depending on whether the input signal is above or below the level at that instant. Those comparators depressed above the input signal, remain turned-off representing "0" state the comparators at or below the input signal "1" state.
- The code resulting from this compare is converted a binary code by the encoder.

(4)



3-bit Flash converter

Assignment - 5

CO 5 : Implement PLDS for the given logical Problem.

Q-1 Explain content addressable memory.

- ⇒ Many data-processing applications perform the search of items in a table stored in memory. They use object names or numbers to identify the location of the named or numbered object within a memory space.
 - for example, an account number may be searched in a file to determine the holder's name and account status.
 - To search an object, the number of accesses to memory depends on location of object and the efficiency of the search algorithm.
 - The time required to find an object stored in memory can be reduced considerably if objects are selected based on their contents, not on their locations. A memory unit accessed by the content is called an associative memory or content addressable memory (CAM). This type of memory is accessed simultaneously and in parallel on the basis of data content rather than by specific address or location.

Cache

* Block diagram of cache memory

Segment register

Key Register

Input
Read
Write

Associative
memory array
Logic to add
n-bits per word

Match

Output

*Charge coupled device
memory (CCD)

Mosigate

Insulation
(SiO₂)

P-Substrate

- CCD memory is a type of dynamic memory in which packets of charge are continuously transferred from one mos device to another.

(2). A-5

- When a high voltage is applied to the metal gate, holes are repelled from a region beneath the gate in the P-type.
- The charge-coupled devices are built as all serial-in, serial-out MOS shift registers, each shift register being a line of charge coupled devices.
- The main advantage of CCD is that its simple cell structure.
- It makes it possible to construct large capacity memories at low cost.
- CCDs can be used for digital or analog dewy, and us serial data memories. Another exciting application of CCDs is as the light sensitive image sensor in television cameras.

Q-3 Explain classification of memory.

Non-Volatile memory	Volatile memory
Read only memory (ROM) memory	Read / write memory (RAM)
Masks - Programmable ROM	EPROM
Programmable ROM	EEPROM
FLASH	SRAM
SRAM	DRAM
SRAM	FIFO
SRAM	LIFO
SRAM	Shift register

- * - ROM : Read only memory
- PROM : Programmable ROM
- EPROM : Erasable PROM
- EEPROM : Electrically Erasable PROM
- SRAM : Static Random Access memory
- DRAM : Dynamic Random Access memory
- FIFO : First-in-First-out
- LIFO : Last-in-First-out

Q.4

Describe Semi-conductors:-

- ⇒ Semi-conductors are materials which have a conductivity between conductors and non-conductors or insulators.
- Semi-conductors can be pure elements such as Si or Ge, or compounds such as Ge, As or Cd, Se. In a process called doping, small amounts of impurities are added to pure semi-conductors causing changes in the conductivity of the material.
 - Due to their role of electronic-devices; semiconductors are an important part of our lives imagine life without electronic device. There would be no radios, no TVs and computers, no ultrasound and poor medical diagnostic equipment. Although many electronic devices could be made using vacuum tube technology, the developments in semiconductor technology during the post 50 years have made electronic devices smaller, faster and more reliable.

(3). A-5

Q-5. Explain Field-Programmable Gate Array (FPGA).

- Field-Programmable Gate Array provide the next generation in the programmable logic device.
- The word Field in the name refers to the gate arrays to be programmed for a specific function by the user instead of by the manufacturer of the device.
- The word array is used to indicate a series of columns and rows of gates that can be programmed by the end user.
- As compared to standard gate arrays, the field programmable gate array are larger devices.
- The basic cell structure for FPGAs is somewhat complicated than the basic cell structure of standard gate array.
- The programmable logic blocks of FPGAs are called logic blocks or configurable logic blocks (CLBs).
- The basic architecture of FPGAs consists of an array of logic blocks with programmable row and column.

interconnecting channels surrounded by Programmable I/O blocks.

- Many FPGA architectures are based on a type of memory called LUT (Look-up-table) rather than on (sum of product) SOP AND/OR circuit as CPLDs are.

Q-3) Broadly semi-conductors memories are classified as volatile memories and non-volatile memories.

- On the other hand, non-volatile memories can hold data even if power is turned off. Read, write memories which allows both read and write operations; they are used in application where data has to change continuously.

- EPROM and EEPROM are erasable memories in which the stored data can be erased and new data can be stored. The semi-conductor memories are also classified as bipolar and most memories depending upon the type of transistor used to constructs the individual cell.