Loop Detector Logic

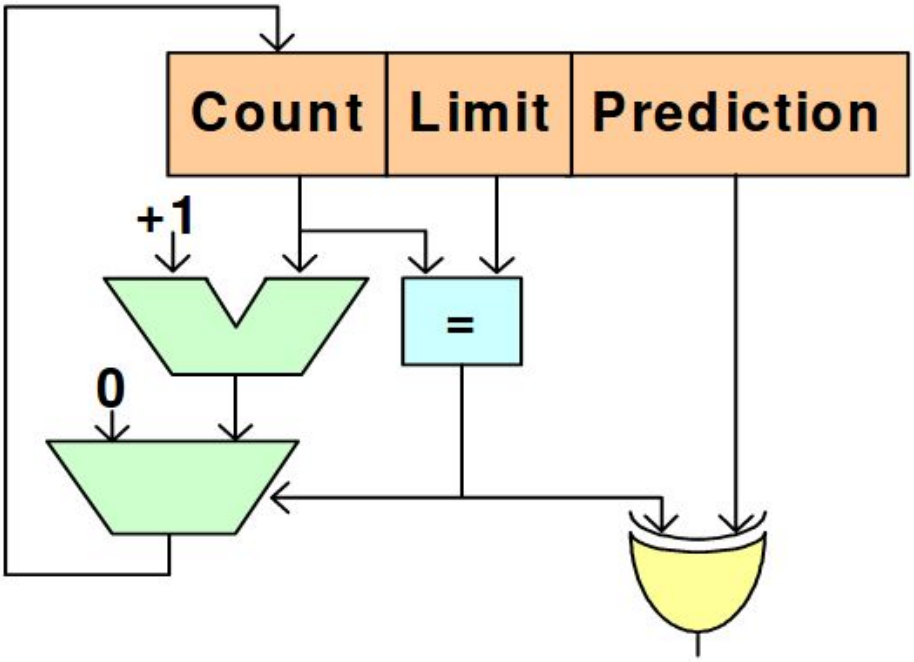

Figure 2: The Loop Detector logic

Loop is characterized with one-direction motion of branch (*taken* or *not taken*) ending with a single motion in opposite direction.
The processor includes a loop stream unit with logic to identify from the branch instruction that the branch operation is a loop operation, determine whether the loop operation will include a fixed or effectively-infinite number of iterations, load decoded instructions of a loop iteration of the loop operation, and cyclically issue the decoded instructions of the loop iteration in a manner based upon whether the loop operation will include a fixed or effectively-infinite number of iterations. [Xekalakis, Polychronis (Barcelona, ES), Collins, Jamison D. (San Jose, CA, US), Ahuja, Sumit (Mountain View, CA, US) 2016 Instruction and Logic for Loop Stream Detection United States INTEL CORPORATION (Santa Clara, CA, US) 20160179549 http://www.freepatentsonline.com/y2016/0179549.html]
A counter is maintained by the predictor to keep track of the loop completion.
Thus, the given circuit allows accurate predictions for larger iteration counts and also prevents it from influencing other branch predictions.

Indirect Branch Predictor Logic

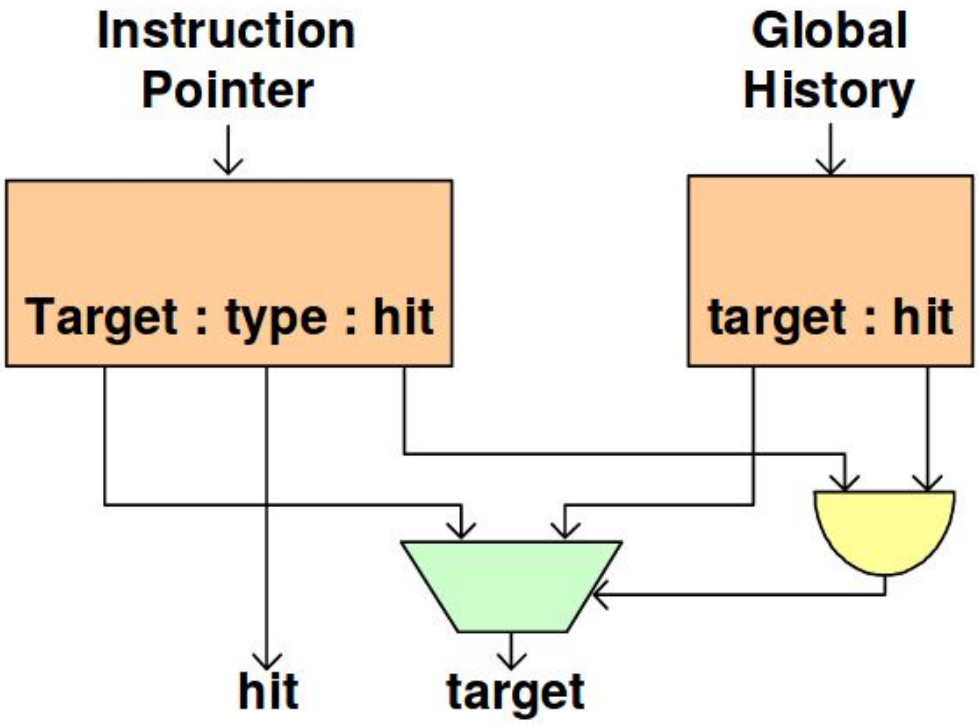

Figure 3: The Indirect Branch Predictor logic

The indirect branch predictor chooses targets based on *global control flow history*. Targets are always allocated in the instruction pointer tagged table along with type of branch. When there is a misprediction in an indirect branch, the target address gets allocated to this table as a new entry for the corresponding global history pattern. Also, the indirect branch can allocate many target addresses for different global history patterns. Thus, the indirect branches can predict correct from this IP-based target array. Entries in this IP-based target array are based on the hit and type information to prevent “false positives” from indirect branch predictor to lead to mispredictions.