Design of Digital Systems Laboratory

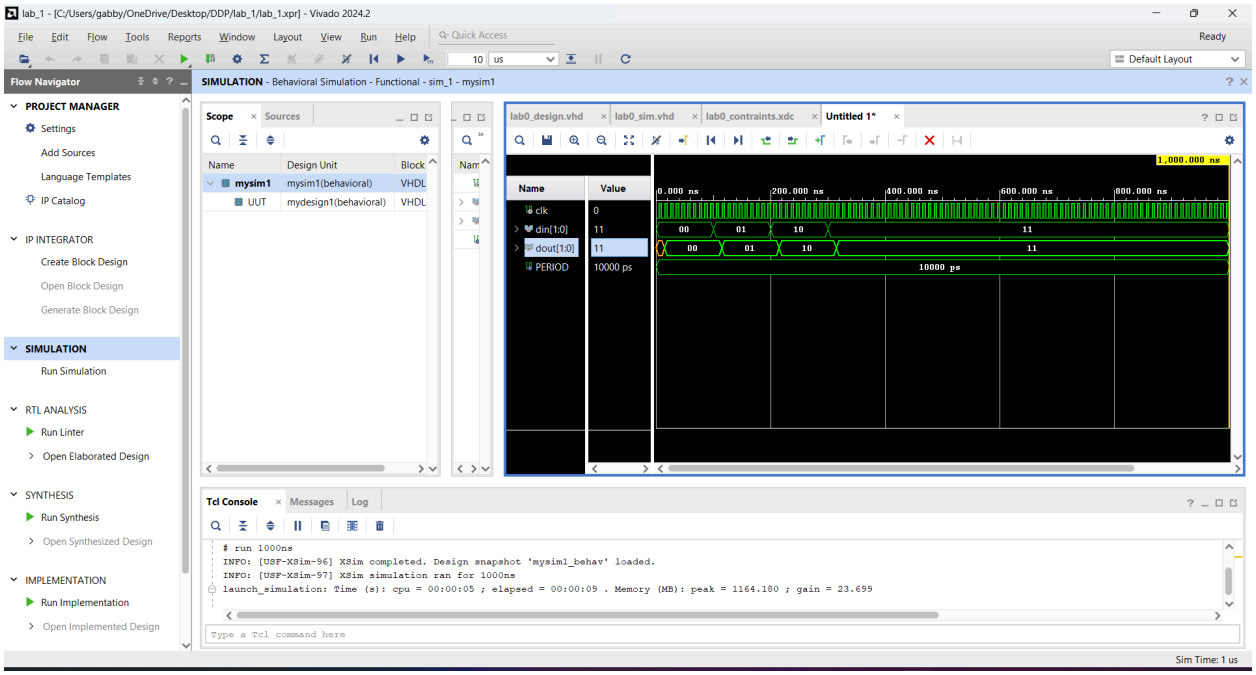
Assignment lab 0

Gabrielle McCrae

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

SIMULATION RESULTS



The clk signal is a clock that toggles consistently between 0 and 1, with a period of 10,000 picoseconds (10 nanoseconds). This signal drives the timing for the rest of the design.
The din[1:0] signal is a 2-bit input that changes value at specific intervals during the simulation. It transitions from 00 to 01 at around 200 nanoseconds, then to 10 at around 400 nanoseconds, and finally to 11 at around 600 nanoseconds.
The dout[1:0] signal is a 2-bit output that mirrors the value of din[1:0] at each point in time. This indicates that the output is either directly assigned from the input or passed through a very simple logic that introduces no visible delay.
The period signal is shown as a constant value of 10,000 picoseconds, which corresponds to the clock period and serves as a reference for timing

AREA IMPLEMENTATION RESULTS

Look-up-table(LUT)	Flip Flops(FF)
0	4

TIMING IMPLEMENTATION RESULTS

Worst Negative Slack (WNS)	Critical Path Delay (CPD)	Maximum Frequency
9.134	10 - 9.134 = 0.866	1000 / 0.866 = 1154.734

FPGA DEMO

Youtube link: https://www.youtube.com/watch?v=-rc3QdkneJM