Design of Digital Systems Laboratory

Assignment lab 2

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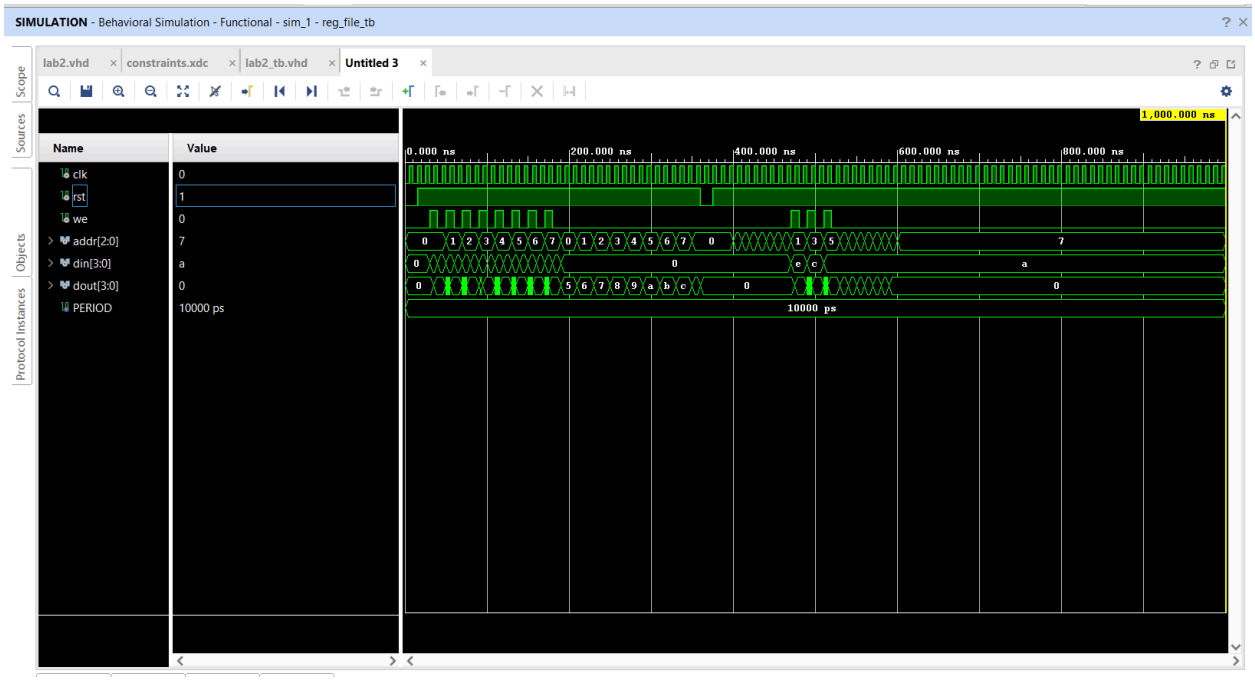
By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

SIMULATION RESULTS



Initially, when reset (rst) is low, all outputs (dout) are zero. Once reset is high (rst = 1), write operations begin (we = 1), storing values into registers at different addresses (addr). After writing, we is disabled and the testbench reads back the values, confirming they were stored correctly. A second write cycle updates the registers with new values, which are again read back successfully. Finally, asserting reset again clears all registers, and returns zeros, letting us know that the reset works.

AREA IMPLEMENTATION RESULTS

Look-up-table(LUT)	Flip Flops(FF)
17	32

TIMING IMPLEMENTATION RESULTS

N/A

FPGA DEMO

Youtube link: https://www.youtube.com/watch?v=I8cG7enCuq0