Design of Digital Systems Laboratory

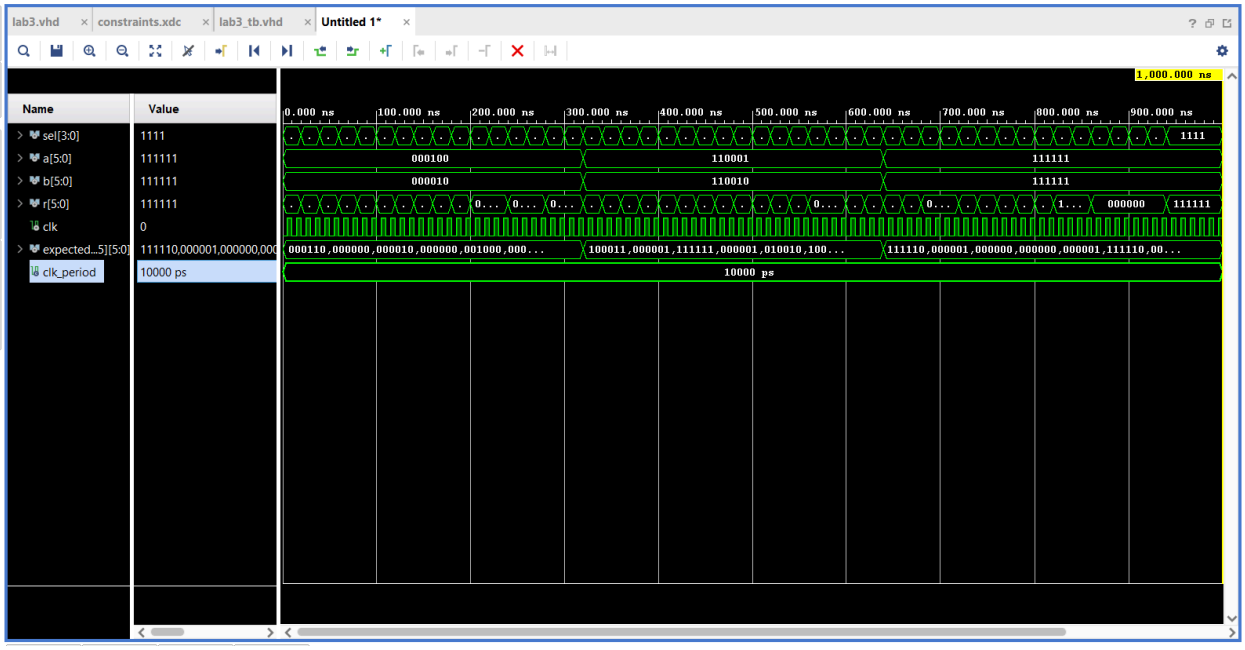
Assignment lab 3

Gabrielle McCrae

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

SIMULATION RESULTS



This waveform shows a simulation of the ALU design, where the output signal (r) matches the expected output signal (expected_s) at every step. The ALU is tested with all combinations of the (sel) control signal (from 0000 to 1111), which correspond to operations such as addition, subtraction, multiplication (low/high bits), logical functions (NOT, AND, OR, XOR), and shift operations (logical and arithmetic shifts)
At each interval, the operands a and b, and the resulting r value produced by the ALU aligns with the expected_s value.

AREA IMPLEMENTATION RESULTS

Look-up-table(LUT)	Flip Flops(FF)
82	0

TIMING IMPLEMENTATION RESULTS

N/A

FPGA DEMO

Youtube link: https://www.youtube.com/watch?v=NBnlOppWSJg