

Design of Digital Systems Laboratory

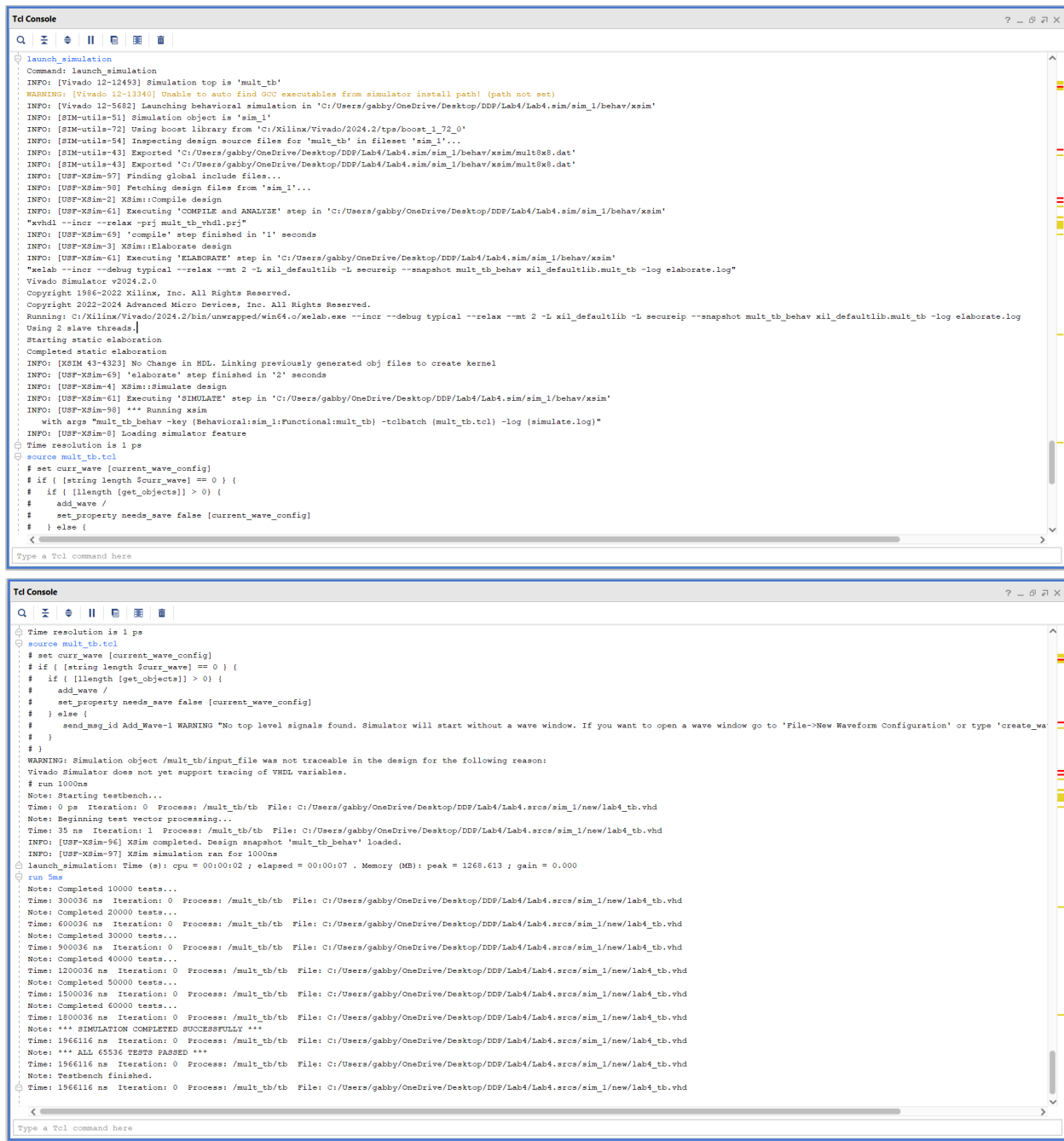
Assignment lab 4

Gabrielle McCrae

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

TCL CONSOLE RESULTS



```
Tcl Console
Launch_simulation
Command: launch_simulation
INFO: [Vivado 12-12492] simulation top is 'mult_tb'
WARNING: [Vivado 12-13340] Unable to auto find GCC executables from simulator install path! (path not set)
INFO: [Vivado 12-5682] Launching behavioral simulation in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim'
INFO: [SIM-utils-51] Simulation object is 'sim_1'
INFO: [SIM-utils-72] Using boost library from 'C:/Xilinx/Vivado/2024.2/tps/boost_1_72_0'
INFO: [SIM-utils-54] Inspecting design source files for 'mult_tb' in fileset 'sim_1'...
INFO: [SIM-utils-43] Exported 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim/mult8x8.dat'
INFO: [SIM-utils-43] Exported 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim/mult8x8.dat'
INFO: [USF-XSim-97] Finding global include files...
INFO: [USF-XSim-98] Fetching design files from 'sim_1'...
INFO: [USF-XSim-2] XSim::Compile design
INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim'
'xvhdl --incr --relax -prj mult_tb_vhdl.prj'
INFO: [USF-XSim-69] 'compile' step finished in '1' seconds
INFO: [USF-XSim-3] XSim::Elaborate design
INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim'
'xelab --incr --debug typical --relax --mt 2 -L xil_defaultlib -L secureip --snapshot mult_tb_behav xil_defaultlib.mult_tb -log elaborate.log'
Vivado Simulator v2024.2.0
Copyright 1986-2024 Xilinx, Inc. All Rights Reserved.
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Running: C:/Xilinx/Vivado/2024.2/bin/unwrapped/win64.o/xelab.exe --incr --debug typical --relax --mt 2 -L xil_defaultlib -L secureip --snapshot mult_tb_behav xil_defaultlib.mult_tb -log elaborate.log
Using 2 slave threads
Starting static elaboration
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel
INFO: [USF-XSim-69] 'elaborate' step finished in '2' seconds
INFO: [USF-XSim-4] XSim::Simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.sim/sim_1/behav/xsim'
INFO: [USF-XSim-98] *** Running xsim
with args 'mult_tb_behav -key {Behavioral:sim_1:Functional:mult_tb} -tclbatch {mult_tb.tcl} -log {simulate.log}'
INFO: [USF-XSim-8] Loading simulator feature
Time resolution is 1 ps
source mult_tb.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create_wa
#   }
# }
WARNING: Simulation object /mult_tb/input_file was not traceable in the design for the following reason:
Vivado Simulator does not yet support tracing of VHDL variables.
# run 1000ns
Note: Starting testbench...
Time: 0 ps Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Beginning test vector processing...
Time: 35 ns Iteration: 1 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
INFO: [USF-XSim-96] Xsim completed. Design snapshot 'mult_tb_behav' loaded.
INFO: [USF-XSim-97] Xsim simulation ran for 1000ns
Launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:07 . Memory (MB): peak = 1269.613 ; gain = 0.000
run 5ms
Note: Completed 10000 tests...
Time: 300036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Completed 20000 tests...
Time: 600036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Completed 30000 tests...
Time: 900036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Completed 40000 tests...
Time: 1200036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Completed 50000 tests...
Time: 1500036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Completed 60000 tests...
Time: 1800036 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: *** SIMULATION COMPLETED SUCCESSFULLY ***
Time: 1966116 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: *** ALL 65536 TESTS PASSED ***
Time: 1966116 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
Note: Testbench finished.
Time: 1966116 ns Iteration: 0 Process: /mult_tb/tb File: C:/Users/gabby/OneDrive/Desktop/DDP/Lab4/Lab4.srcs/sim_1/new/lab4_tb.vhd
```

The TCL Console output confirms that the simulation ran without errors, displaying progress updates for every 10,000 tests. At the end of the run, the output confirms.

This result demonstrates that the design is functionally correct across the full space. Additionally, pipeline registers were implemented to clock the inputs and outputs, preparing the design for realistic timing and area analysis

To conclude, the lab successfully met its objective of building a parameterized, pipelined carry-save multiplier and verifying its correctness through exhaustive simulation

AREA IMPLEMENTATION RESULTS

<u>Look-up-table(LUT)</u>	<u>Flip Flops(FF)</u>
85	32

TIMING IMPLEMENTATION RESULTS

Worst Negative Slack (WNS)	Critical Path Delay (CPD)	Maximum Frequency
3.566	$10 - 3.566 = 6.434$	$1000 / 6.434 = 157.654$

FPGA DEMO

Youtube link: <https://www.youtube.com/watch?v=NR4wsMkFGYA>