Design of Digital Systems Laboratory

Assignment lab 4

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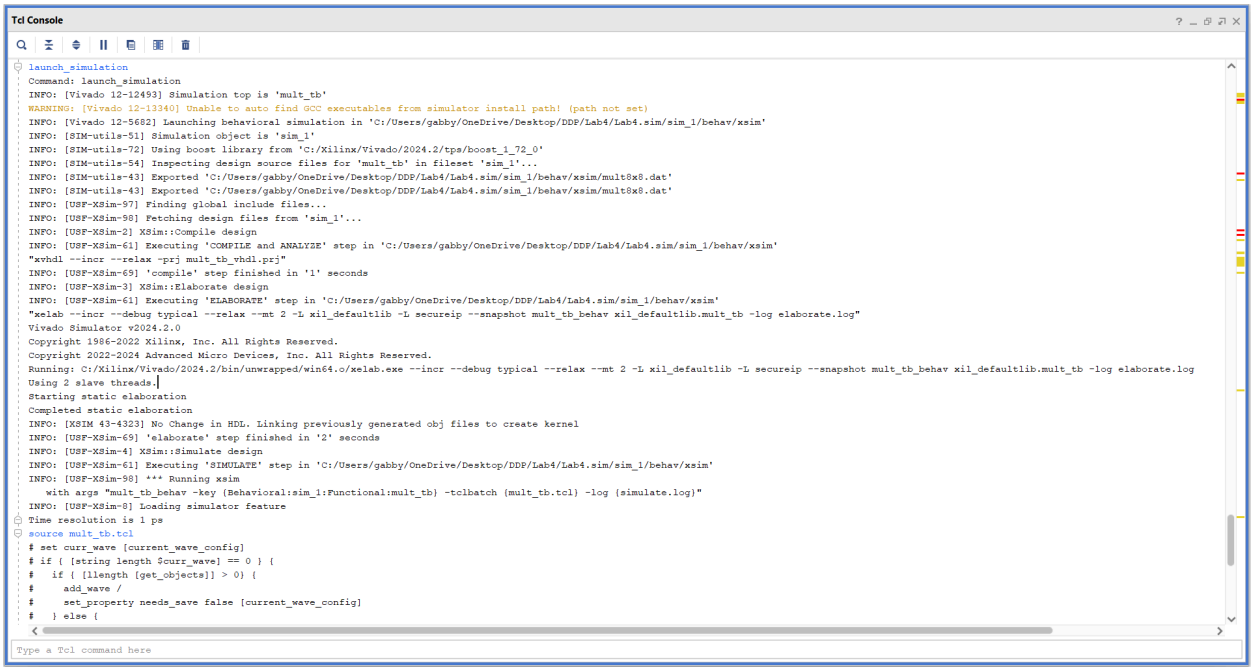
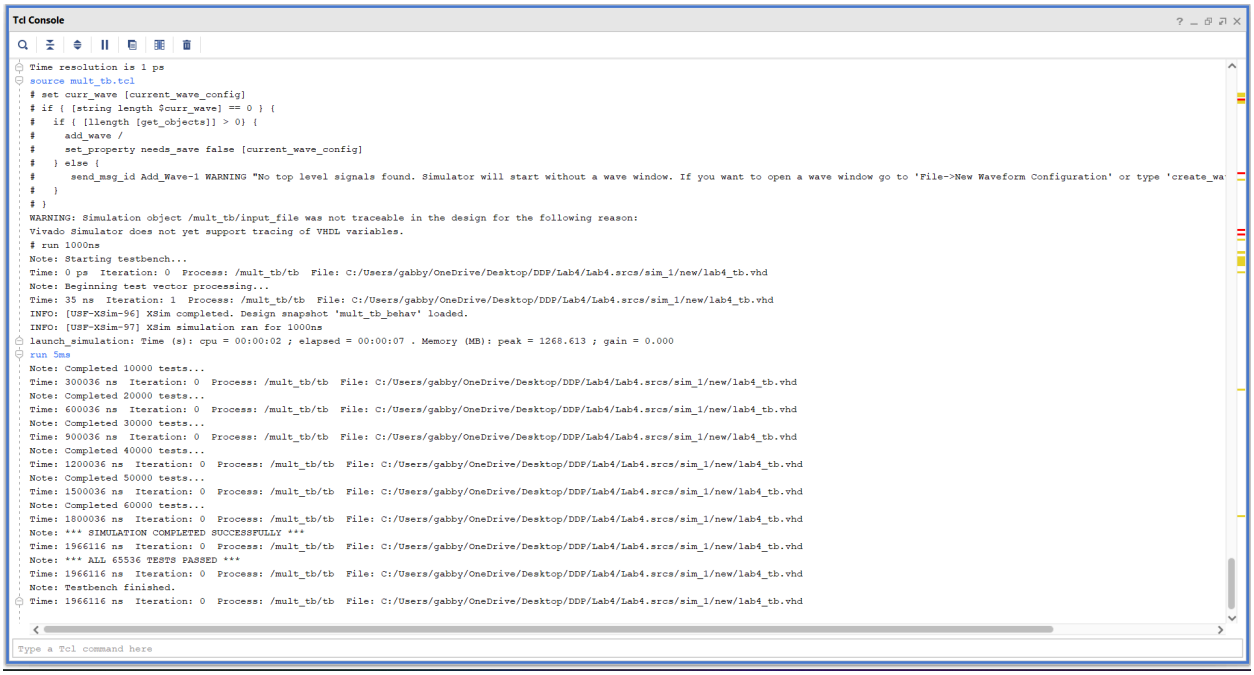
By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

TCL CONSOLE RESULTS





The TCL Console output confirms that the simulation ran without errors, displaying progress updates for every 10,000 tests. At the end of the run, the output confirms.

This result demonstrates that the design is functionally correct across the full space. Additionally, pipeline registers were implemented to clock the inputs and outputs, preparing the design for realistic timing and area analysis

To conclude, the lab successfully met its objective of building a parameterized, pipelined carry-save multiplier and verifying its correctness through exhaustive simulation

AREA IMPLEMENTATION RESULTS

Look-up-table(LUT)	Flip Flops(FF)
85	32

TIMING IMPLEMENTATION RESULTS

Worst Negative Slack (WNS)	Critical Path Delay (CPD)	Maximum Frequency
3.566	10 - 3.566 = 6.434	1000 / 6.434 = 157.654

FPGA DEMO

Youtube link: https://www.youtube.com/watch?v=NR4wsMkFGYA