Design of Digital Systems Laboratory

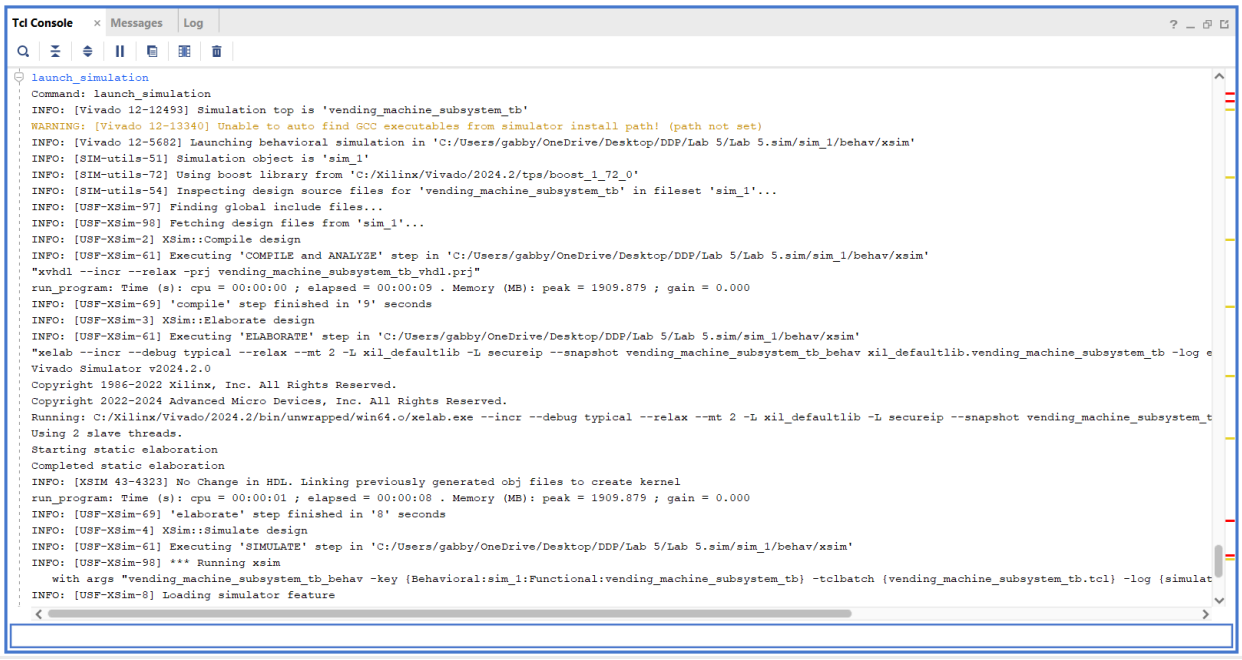
Assignment lab 5

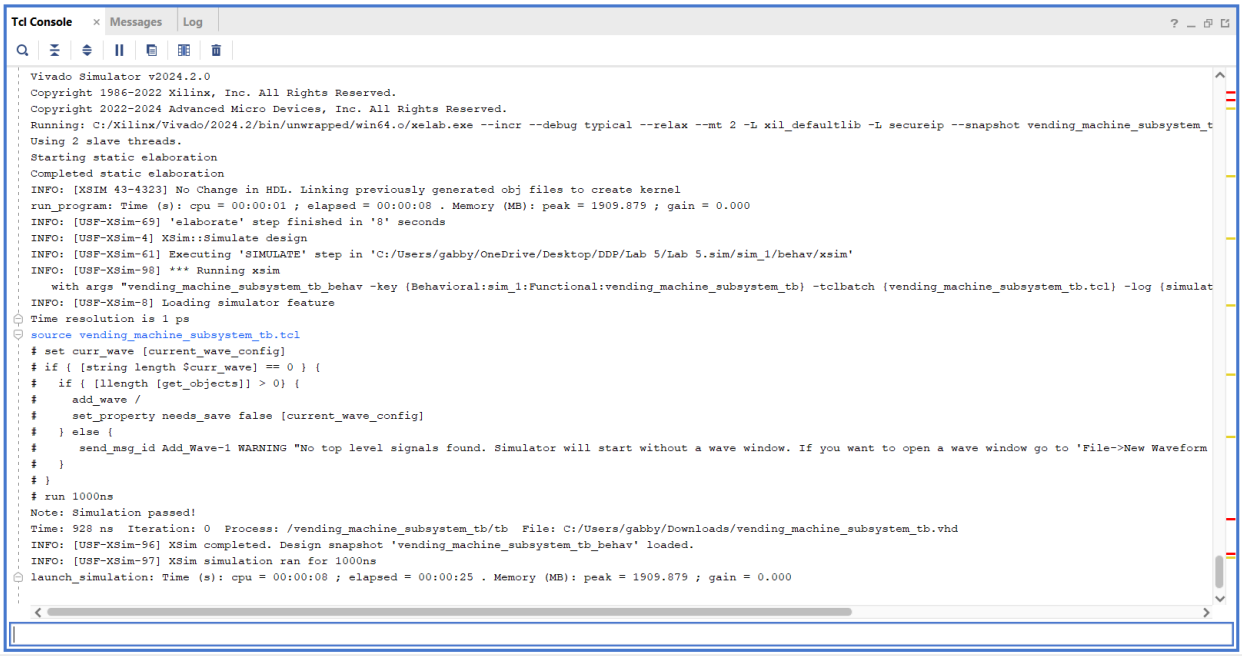
Gabrielle McCrae

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

TCL CONSOLE RESULTS





The TCL Console output confirms that the simulation ran without errors, displaying step-by-step updates for the compile, elaborate, and simulate phases. The simulation was run for 1000 nanoseconds using the testbench, and the output confirms that the simulation passed successfully. The simulation setup ensures that the design is ready for further steps such as waveform analysis and, if applicable, realistic timing and area evaluation through synthesis and implementation.

AREA IMPLEMENTATION RESULTS

Look-up-table(LUT)	Flip Flops(FF)
150	318

TIMING IMPLEMENTATION RESULTS

Worst Negative Slack (WNS)	Critical Path Delay (CPD)	Maximum Frequency
6.473	10 - 6.473 = 3.527	1000 / 3.527 = 283.527

FPGA DEMO

Youtube link: https://www.youtube.com/watch?v=m7qc6wyBths