

## **Design of Digital Systems Laboratory**

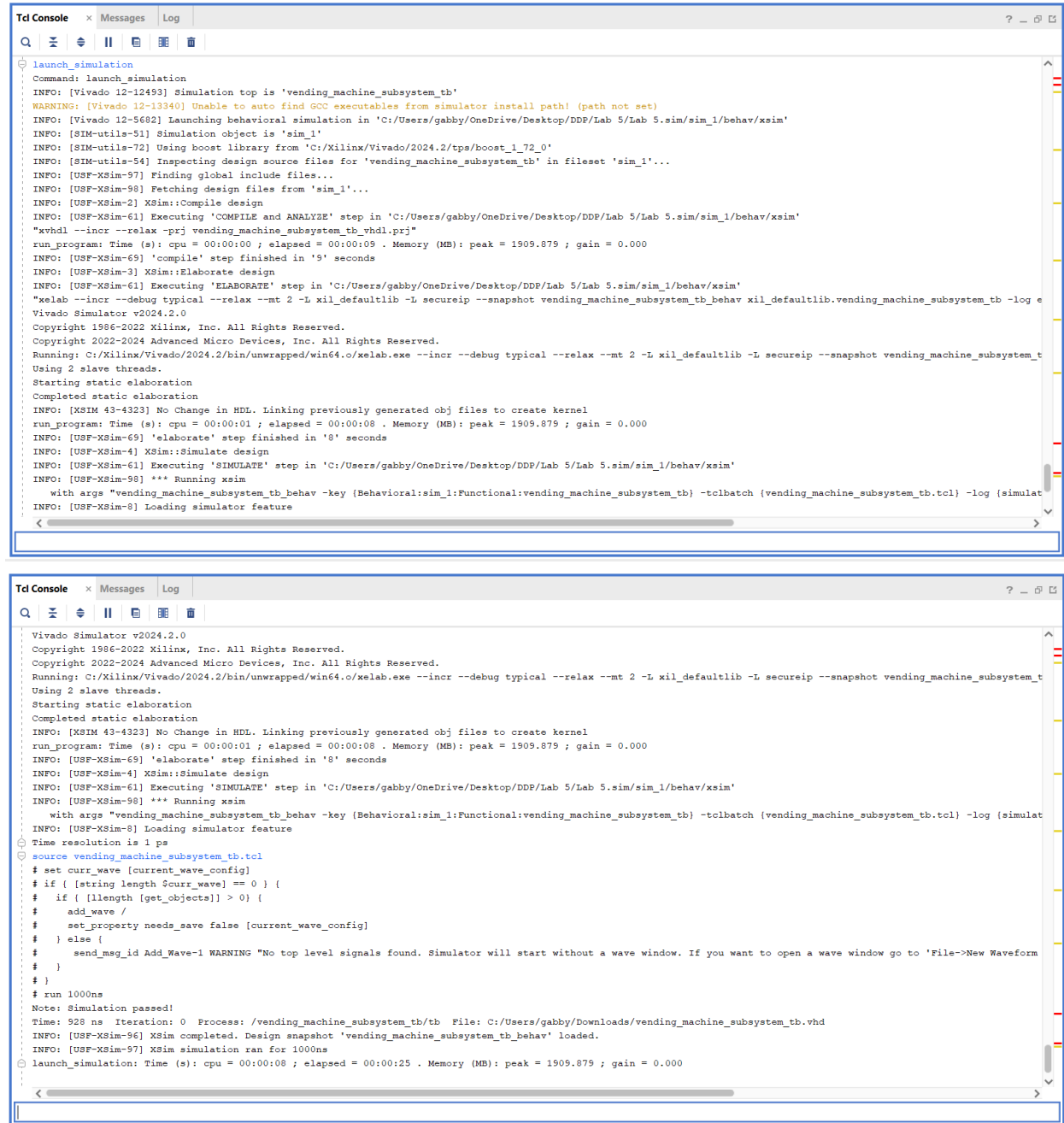
### **Assignment lab 5**

Gabrielle McCrae

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Gabrielle McCrae

# TCL CONSOLE RESULTS



```
launch_simulation
Command: launch_simulation
INFO: [Vivado 12-12493] Simulation top is 'vending_machine_subsystem_tb'
WARNING: [Vivado 12-13340] Unable to auto find GCC executables from simulator install path! (path not set)
INFO: [Vivado 12-5682] Launching behavioral simulation in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab 5/Lab 5.sim/sim_1/behav/xsim'
INFO: [SIM-utils-51] Simulation object is 'sim_1'
INFO: [SIM-utils-72] Using boost library from 'C:/Xilinx/Vivado/2024.2/tps/boost_1_72_0'
INFO: [SIM-utils-54] Inspecting design source files for 'vending_machine_subsystem_tb' in fileset 'sim_1'...
INFO: [USF-XSim-97] Finding global include files...
INFO: [USF-XSim-98] Fetching design files from 'sim_1'...
INFO: [USF-XSim-2] XSim::Compile design
INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab 5/Lab 5.sim/sim_1/behav/xsim'
"xvhdl --incr --relax -prj vending_machine_subsystem_tb_vhdl.prj"
run_program: Time (s): cpu = 00:00:00 ; elapsed = 00:00:09 . Memory (MB): peak = 1909.879 ; gain = 0.000
INFO: [USF-XSim-69] 'compile' step finished in '9' seconds
INFO: [USF-XSim-3] XSim::Elaborate design
INFO: [USF-XSim-61] Executing 'ELABORATE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab 5/Lab 5.sim/sim_1/behav/xsim'
"xelab --incr --debug typical --relax --mt 2 -L xil_defaultlib -L secureip --snapshot vending_machine_subsystem_tb_behav xil_defaultlib.vending_machine_subsystem_tb -log e
Vivado Simulator v2024.2.0
Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
Copyright 2022-2024 Advanced Micro Devices, Inc. All Rights Reserved.
Running: C:/Xilinx/Vivado/2024.2/bin/unwrapped/win64.o/xelab.exe --incr --debug typical --relax --mt 2 -L xil_defaultlib -L secureip --snapshot vending_machine_subsystem_t
Using 2 slave threads.
Starting static elaboration
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel
run_program: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 1909.879 ; gain = 0.000
INFO: [USF-XSim-69] 'elaborate' step finished in '8' seconds
INFO: [USF-XSim-4] XSim::Simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab 5/Lab 5.sim/sim_1/behav/xsim'
INFO: [USF-XSim-98] *** Running xsim
with args "vending_machine_subsystem_tb_behav -key {Behavioral:sim_1:Functional:vending_machine_subsystem_tb} -tclbatch {vending_machine_subsystem_tb.tcl} -log {simulat
INFO: [USF-XSim-8] Loading simulator feature

Vivado Simulator v2024.2.0
Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
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Running: C:/Xilinx/Vivado/2024.2/bin/unwrapped/win64.o/xelab.exe --incr --debug typical --relax --mt 2 -L xil_defaultlib -L secureip --snapshot vending_machine_subsystem_t
Using 2 slave threads.
Starting static elaboration
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel
run_program: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 1909.879 ; gain = 0.000
INFO: [USF-XSim-69] 'elaborate' step finished in '8' seconds
INFO: [USF-XSim-4] XSim::Simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'C:/Users/gabby/OneDrive/Desktop/DDP/Lab 5/Lab 5.sim/sim_1/behav/xsim'
INFO: [USF-XSim-98] *** Running xsim
with args "vending_machine_subsystem_tb_behav -key {Behavioral:sim_1:Functional:vending_machine_subsystem_tb} -tclbatch {vending_machine_subsystem_tb.tcl} -log {simulat
INFO: [USF-XSim-8] Loading simulator feature
Time resolution is 1 ps
source vending_machine_subsystem_tb.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform
#   }
# }
# run 1000ns
Note: Simulation passed!
Time: 928 ns Iteration: 0 Process: /vending_machine_subsystem_tb/tb File: C:/Users/gabby/Downloads/vending_machine_subsystem_tb.vhdl
INFO: [USF-XSim-96] XSim completed. Design snapshot 'vending_machine_subsystem_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:25 . Memory (MB): peak = 1909.879 ; gain = 0.000
```

The TCL Console output confirms that the simulation ran without errors, displaying step-by-step updates for the compile, elaborate, and simulate phases. The simulation was run for 1000 nanoseconds using the testbench, and the output confirms that the simulation passed successfully. The simulation setup ensures that the design is ready for further steps such as waveform analysis and, if applicable, realistic timing and area evaluation through synthesis and implementation.

## AREA IMPLEMENTATION RESULTS

<u>Look-up-table(LUT)</u>	<u>Flip Flops(FF)</u>
150	318

## TIMING IMPLEMENTATION RESULTS

Worst Negative Slack (WNS)	Critical Path Delay (CPD)	Maximum Frequency
6.473	$10 - 6.473 = 3.527$	$1000 / 3.527 = 283.527$

## FPGA DEMO

Youtube link: <https://www.youtube.com/watch?v=m7qc6wyBths>