# David Lo

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United States of America Citizen
Able to relocate anywhere for job/internship opportunity
Overall GPA: 3.15 | Spring 2017 GPA: 3.481 | Summer 2017 GPA: 3.571

## Summary

Engineer looking to transition into the workforce to apply knowledge gain from the classroom while continuing to learn and improve my technique and communication skills to meet the requirements of projects I participate in.

## Key Skills

- Probability Theory
- C++
- Java
- RobotC
- Assembly Language
- Verilog/SystemVerilog - ASIC
- Operating Systems in C
- VHDL
- Bilingual - English, Cantonese
- Tcl scripts - ASIC
- Matlab
- BASIC

## Programs/Equipment Used

- Xilinx Vivado - VHDL (ZedBoard Zynq Evaluation and Development Kit)
- Synopsys Tools (Verilog/SystemVerilog - ASIC)
- Microsoft Visual Studios (C++)
- JGrasp (C++, Java)
- Tektronix Oscilloscopes
- Digital Multimeters
- Unix/Linux Servers
- Integrated Circuits (ICs)
- Resistors, Capacitors, Inductors
- Keil uVision (UM10139)
- Inventor
- Notepad++
- RobotC for Vex
- Pspice
- Mathworks Matlab
- Autodesk Inventor

## Education

**California State University - Northridge** **Graduated 2017**
Bachelor of Science: Computer Engineering Northridge, CA

## Job Experience

**Abercrombie & Fitch** **August 2014 - May 2015**
Impact Los Angeles, CA

## _____ Projects _____

**RISC-Y Processor (Verilog)**

Utilizing a variety of modules created throughout the semester of Spring 2016, a RISC-Y processor was created as part of the final project for my “Digital Design with Verilog and SystemVerilog” course at California State University - Northridge. A program counter, read-only memory, arithmetic logic unit, multiplexer, random access memory, and multiple registers were coded and connected to their respective subsystems. Once all of the modules were completed and their functionality verified, a top-level module was created to connect all of the subsystems together.

**Pulse Width Modulator**

With only discrete parts, the circuit created with take in an analog voltage and convert it to a pulse width. The output square wave ranges from 10 microseconds corresponding to 1 V to 1 microsecond corresponding to 10 V.
This project was created as part of my senior project at California State University - Northridge.

**Smiles and Leniency Engineering Experiment (Matlab)**

A case study has been conducted in the past on how smiling can influence judgments a person who committed an act of wrongdoing. In the experiment, groups saw images of individuals with different types of smiles and gave a leniency score. Our professor assigned various data to each student based on our student identification number and our job was to create matlab code to take in the data and obtain statistical information and display the information in various graphs.

**Crazy Poker (Java)**

The purpose of this project is to create program that can take in command line arguments for the cards dealt to an unknown number of players, calculate the scores for each player, sort the scores, and output the player number in order from the highest scorer to the lowest scorer. The program can calculate scores for any number of players up to 15 since the game utilizes only one deck of cards, so there is a limit of 52 cards used

## _____ Languages _____

**Assembly Language**

- Learned how to utilize LEDs as notifiers
- Coded LCD screen to display messages
- Step Motor Control with Timers
- Interrupts
    - Software Interrupt
    - Hardware Interrupt
- Loops, Branches, Subroutines

**RobotC**

- Worked with peers from various Engineering background - Mechanical, Electrical, Computer
- Programmed Vex controller to allow for robot movement
- Set sonar sensor to trigger a function when the sensor detects an object n centimeters away
- Assisted in the autonomous mode

**Java**

- Trees - BST, AVL, 2-3, 2-3-4, Red-Black
- Linked Lists - Singly, Doubly, Circular Singly, Circular Doubly
- Implemented Dijkstra's algorithm
- Basic GUI

**Verilog/SystemVerilog - ASIC**

- Optimized designs for Speed/Area
- Created cell models
- Built models, along with their respective testbenches, leading up to RISC-Y processor final project (ALU, Carry Select Adder, etc)

**Cantonese**

- Grew up watching Cantonese speaking dramas/variety shows
- Speak the language with parents as well as friends from Hong Kong
- Have visited Asia twice in the past during Summer vacations
    - Hong Kong, Beijing, Guangzhou, Shenzhen

**Spanish**

- Took Spanish language classes in High school
- Lived in El Paso, TX in the past

_____ Extracurricular _____

**Leadership**

Former Dance Coordinator for the International Student Forum Banquet
Founder and Team Manager of CSUN's Esports Club Hearthstone competitive team

**Teamwork**

Former member of dance team Off the Grid (OTG)
Former member of Vex Robotics
Former violinist in the High School Orchestra at Northwest Career and Technical Academy