

Laboratory 3

Expected delivery of lab_03.zip must include:

- **program_1_a.s, program_1_b.s and program_1_c.s**
- **this file compiled and if possible in pdf format.**

Please, configure the winMIPS64 simulator with the *Base Configuration* provided in the following:

- Code address bus: 12
- Data address bus: 12
- Pipelined FP arithmetic unit (latency): 6 stages
- Pipelined multiplier unit (latency): 8 stages
- Divider unit (latency): not pipelined unit, 24 clock cycles
- **Forwarding is enabled**
- Branch prediction is disabled
- Branch delay slot is disabled
- *Integer ALU: 1 clock cycle*
- *Data memory: 1 clock cycle*
- *Branch delay slot: 1 clock cycle.*

Set Architecture

Code Address Bus	12
Data Address Bus	12
FP Addition Latency	6
Multiplier Latency	8
Division Latency	24

OK Cancel

Warning: This will cause a reset!

1) Starting from the assembly program you created in the previous lab called **program_1.s**:

```
for (i = 0; i < 60; i++){
    v5[i] = ((v1[i]+v2[i]) * v3[i])+v4[i];
    v6[i] = v5[i]/(v4[i]*v1[i]);
    v7[i] = v6[i]*(v2[i]+v3[i]);
}
```

- Detect manually the different data, structural and control hazards that provoke a pipeline stall
- Optimize the program by re-scheduling the program instructions in order to eliminate as many hazards as possible. Compute manually the number of clock cycles the new program (**program_1_a.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
- Starting from **program_1_a.s**, enable the *branch delay slot* and re-schedule some instructions in order to improve the previous program execution time. Compute manually the number of clock cycles the new program (**program_1_b.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.
- Unroll 3 times the program (**program_1_b.s**), if necessary re-schedule some instructions and increase the number of used registers. Compute

manually the number of clock cycles the new program (**program_1_c.s**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

Complete the following table with the obtained results:

Program	program_1.s (*)	program_1_a.s (*)	program_1_b.s	program_1_c.s
Clock cycle computation				
By hand	3667	3547	3488	1960
By simulation	3667	3547	3488	1977

(*) branch delay slot disabled

Compare the results obtained in point 1, and provide some explanation in the case the results are different.

Eventual explanation:

In program_1_c.s the number of instructions *by hand* and *by simulation* is different. The cause of this could be that WinMips64 runs the FP operations different, particularly it puts raw stalls inside the execution stage. To the opposite, I considered the raw stalls only before or after the execution stage during developing.

The attached file pipeline_program_1.xls shows the simulation by hand for each program.