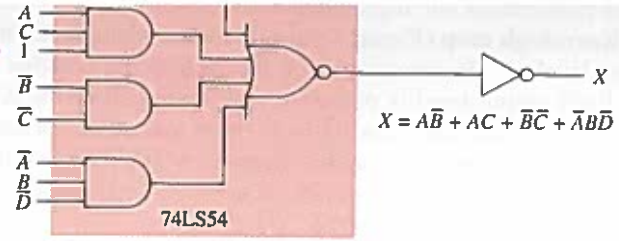

Figure 5–65 Using an AOI IC to implement the simplified SOP equation for Example 5–22.

What other options are available instead of inputting a 1 to the second AND gate?

Team Discussion

How could you create the AND–OR logic function using 5 NAND gates? (*Hint*–Use bubble pushing.)

Programmable Logic Devices (PLDs)

It is worth mentioning here that the latest technology for implementing large AOI functions is the programmable logic device (PLD) IC. It is covered in detail in Chapter 14 and Appendix E. PLDs provide the designer with a means to specify the exact contents of the gating inside an AOI function. For example, instead of being limited to the four AND terms feeding into a single NOR, as in the 74LS54, PLDs provide much more flexibility. Some PLDs provide for up to 16 inputs into each of 48 AND gates, with all the AND gates capable of being routed to any of eight different OR gate outputs. The exact configuration of the AND–OR combinations is programmable by the designer to meet his or her specific needs. Thus, a company needs to stock only a few different PLD parts, and the specific logic function is defined and programmed by the user right at his or her own workstation.

Review Questions

5–14. Which form of Boolean equation is better suited for completing truth tables and timing diagrams, SOP or POS?

5–15. AOI ICs are used to implement _____ (SOP, POS) expressions.

5–16. The equation $X = AB + BCD + DE$ has only three product terms. If a 74LS54 AOI IC is used to implement the equation, what must be done with the three inputs to the unused fourth AND gate?

5–7 Karnaugh Mapping

We learned in previous sections that by using Boolean algebra and De Morgan's theorem, we can minimize the number of gates that are required to implement a particular logic function. This is very important for the reduction of circuit cost, physical size, and gate failures. You may have found that some of the steps in the Boolean reduction process require ingenuity on your part and a lot of practice.