6.5 Arithmetic/Logic Units (ALUs) 253 6.6 Multipliers 259 6.7 Decoders 262 6.7 Code Converters 268	- 112
Encoders 271 Multiplexers 279	
M 68	
Reference 290 Problems 290	
Programmable Logic 292	
_	
7.3.2 Oil-life-Street Implementations 301 7.3.3 Multiple-Module Implementations 306 7.4 Programmable Logic Arrays (PLAs) 306 7.4 Programmable Logic Arrays (PLAs) 309	
7.5 Programman 316 7.5.1 Types of PALs 319 7.5.2 Off-the-Shelf PALs 319	
~ .c	
7.8 Summary 329 References 329 Problems 330	
8 Synchronous Sequentia: Circuits 331	
8.1 Introduction 331 8.2 Flip-Flops 334 8.2.1 Set-Reset (SR) Flip-Flops 338 8.2.2 D Flip-Flops 339 8.3.3 IK Flip-Flops 339	
8.2.5 8.2.5 Timin 8.3.1 8.3.2	
8,4 Filp-riop 103	

Circuits 352		Sircuits 367	e Devices 374			385			ircuits 400	402			
Analysis of Synchronous Sequential Circuits	Mealy and Moore Models 366	Design of Synchronous Sequential Circuits	8.7.1 Designing with Programmable Devices	8.7.2 Circuit Minimization 377	on 384	8.8.1 Equivalence Partitioning	8.8.2 Implication Charts 387	ient 389	Incompletely Specified Sequential Circuits	8.10.1 State Reduction Procedure 402	405	406	
	Mealy and Mo	Design of Syn	8.7.1 Design	8.7.2 Circuit	State Reduction 384	8.8.1 Equiva	8.8.2 Implica	State Assignment 389	Incompletely	8.10.1 State	Summary	References	
8.5	9.8	8.7			00 00 *			6.8*	8.10		8.11		

Counters 447 Counters 447 9.7.1 Design of Synchronous Counters 450 9.7.2 Design of Ripple Counters 454 9.7.3 Divide-by-N Circuits 458 9.7.4 IC Counters 460 Designing with ICs 467 9.8.1 Generation of Timing Signals 468 9.8.2 Clock Skewing 472 Summary 476 Shift Registers 422 9.4.1 Static Shift Registers 422 9.4.2 Dynamic Shift Registers 430 Register Transfer Logic 435 9.5.1 Register Transfer Schemes 437 9.5.2 Register Transfer Languages 441 Register Files 444 Registers 415 Latches 421 Introduction 9.1 9.2 9.3 9.4 9.5 9.6 8.6

9 Popular Sequential Circuits 414

10 Memory and Control 479

Summary References Problems

9.9

			482
		480	Ž
Iroduction 479	ypes of Memory 480	.2.1 Random-Access Memory	10.2.2 Content-Addressable Memory
Int	Ţ	<u>.</u>	2
1.01	10.2		