157

4.3.3 NAND-NAND Circuits 144
4.3.4 NOR-NOR Circuits 144
4.4 Other Two-Level Circuits 155
4.5 EXCLUSIVE-OR and EQUIVALENCE 1
4.6 Multiple-Level Circuits Revisited 162
4.7 Timing Analysis 165
4.7.1 Hazards 168
4.8 Loading Analysis 170
4.9 Designing with ICs 171
4.10 Special ICs 173
4.10.1 Buffers 173
4.10.2 Special Outputs 173
4.11 Summary 179
References 179
Problems 179

S	Contents	
	A 2 Bonality of Expressions 59	
	Ý	
2.5	Functions and Their Representations	
	2.5.1	
	2.5.2 Vent Diagrams 63 2.5.3 Algebraic Representations 63	
2.6	Theore	
	2.6.1 Expansion to Canonical Forms	
	2.6.3 Simplifying Boolean Functions 78	
7		
ı		
61	Multiple-Input Cates and Con-	
. 4	Negativ	
	Loading and Fan-Dut	
	2.9.5	
	or o	
(1)	Minimization of Boolean Functions 102	
	103 103 103 105 106 106 106 106 106 106 106 106 106 106	
	3.1.1 Representation of Functions on K-maps	
	Plotting the POS Form	
	3.1.4 Minimization	
	128	
	_	
	References	
	Problems 135	
4	Combinational Circuits 137	
ř		
	80	

Integrated Circuits 183	5.1 Introduction 183	5.2 IC Fabrication 184	*5.3 Bipolar IC Technologies 186	5.3.1 Diode Logic Gates 187	5.3.2 Transistor Logic Gates 190	5.3.3 RTL Gates 195	5.3.4 DTL Gates 196	5.3.5 TTL Logic 197	5.3.6 ECL Gates 210	*5.4 Metal Oxide Semiconductor (MOS) IC Technology	5.4.1 NMOS Logic Gates 216	5.4.2 CMOS Logic 218	*5.5 Gallium Arsenide IC Technology 223	5.6 Summary 227	References 227	Problems 228		Popular Combinational Circuits 231	6.1 Introduction 231	Adders 233	6.2.1 Parallel Binary Adder (PBA) 233	Off-the-Shelf Adde	6.2.4 Decimal Adder 246	Shifters 249	
: : ::																		9							

214