Unleash Innovation

N3E FB29 V0.5 MB-Latch Optimization

SCLD/DTP/TSMC
2022/03/15

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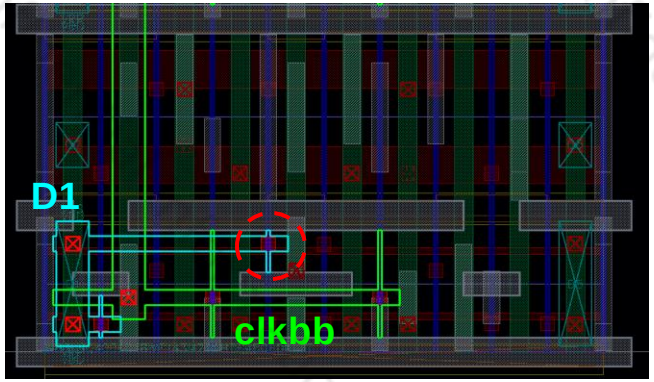
- Two feedback from customer regarding N3E MB-Latch : Leakage and MPW
  - MPW is due to strong layout effect on critical 1fin device; increasing clock size won't help



Node	Cell	sim value(ns)		Bit
		Corner	3 Sigma	
N3E	MB8LHQ_NOM4222_D1_143MH286	0.375	1.204	Q1
N3E	MB8LHQ_NOM4422_D1_143MH286	0.316	1.171	Q1

RC: Qcap C651 benchmark
Model N3E: cln3e_1d2_sp_v0d5_2p1_for_C651_usage.l
-Timing slew:INVDx-predriver, -cload: INVDx-FO4 @ SSGNP/0.48V/m25c for MPW
-Timing slew:INVDx-predriver, -cload: INVDx-FO4 @ SSGNP/0.5V/m25c for PPA
-power slew: INVDx-predriver, -cload: 0.001fF @ FFGNP/0.75V/85C

  - Leakage is also due to CPO-related layout effect

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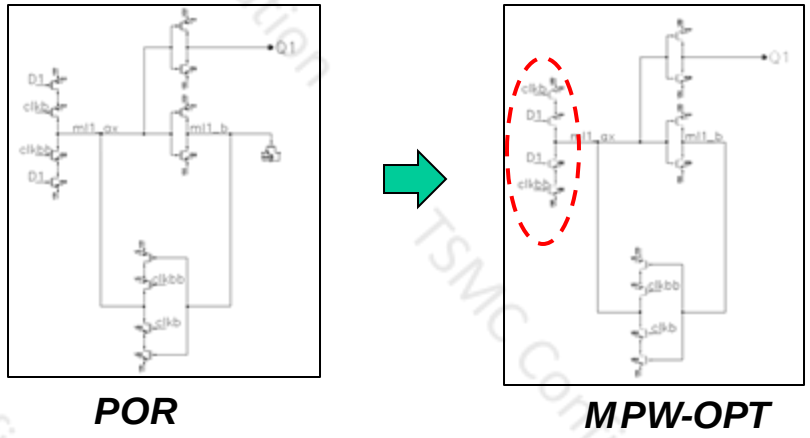
- **Leakage Optimization**
  - **Change CPO location on 1st stage PMOS (at the cost of speed)**

ULVT	N3E POR						N3E (LLKG)						Ratio (LLKG/POR)			
	Setup AVG(ps)	CP2Q AVG(ps)	Speed (GHz)	Pwr-10% (uW)	Leakage (nW)	Area (CPP)	Setup AVG(ps)	CP2Q AVG(ps)	Speed (GHz)	Pwr-10% (uW)	Leakage (nW)	Area (CPP)	Speed	Power	Leakage	Area
MB4LHQ_NOM4222_D1_143MH286	21.7	61.1	12.1	2.1	586.3	20	25.4	63.7	11.2	2.0	465.9	20	-7.07%	-2.21%	-20.54%	0
MB6LHQ_NOM4222_D1_143MH286	19.8	67.5	11.5	2.8	821.8	30	23.4	70.0	10.7	2.7	641.2	30	-6.53%	-2.40%	-21.98%	0
MB8LHQ_NOM4222_D1_143MH286	18.0	73.8	10.9	3.5	1057.4	40	21.5	76.3	10.2	3.5	816.5	40	-6.19%	-2.59%	-22.78%	0

- **MPW Optimization**
  - **Do stack swapping and remove CPO (completely)**



POR

MPW-OPT

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- **PPA Comparison**
  - The leakage-opt version shows speed/leakage trade-off; however, no change on mpw-critical device (no mpw improvement)
  - The mpw-opt version shows more speed degradation; however, both mpw and leakage got improved
  - Suggest to take mpw-opt version as a replacement of POR (not footprint compatible) or as an addition

ULVT	N3E POR						N3E (LKG Opt)						N3E(MPW Opt)					Ratio (LKG Opt/N3E POR)				Ratio (MPW Opt/N3E POR)		
	Setup AVG(ps)	CP2Q AVG(ps)	Speed (GHz)	Pwr-10% (uW)	Leakage (nW)	Area (CPP)	Setup AVG(ps)	CP2Q AVG(ps)	Speed (GHz)	Pwr-10% (uW)	Leakage (nW)	Area (CPP)	Setup AVG(ps)	CP2Q AVG(ps)	Speed (GHz)	Pwr-10% (uW)	Leakage (nW)	Speed	Power	Leakage	Area	Speed	Power	Leakage
MB4LHQ_NOM4222_D1_143MH286	21.7	61.1	12.1	2.1	586.3	20	25.4	63.7	11.2	2.0	465.9	20	24.46	65.73	11.09	1.81	267.38	-7.07%	-2.21%	-20.54%	0	-8.35%	-13.81%	-54.40%
MB6LHQ_NOM4222_D1_143MH286	19.8	67.5	11.5	2.8	821.8	30	23.4	70.0	10.7	2.7	641.2	30	22.73	72.32	10.52	2.44	366.46	-6.53%	-2.40%	-21.98%	0	-8.52%	-12.86%	-55.41%
MB8LHQ_NOM4222_D1_143MH286	18.0	73.8	10.9	3.5	1057.4	40	21.5	76.3	10.2	3.5	816.5	40	21.10	79.10	9.98	3.07	464.84	-6.19%	-2.59%	-22.78%	0	-8.44%	-12.29%	-56.04%

ULVT	N3 POR		Ratio (LKG Opt/ N3)		Ratio (MPW Opt/ N3)	
	Speed (GHz)	Leakage (nW)	Speed	Leakage	Speed	Leakage
MB4LHQ_NOM4222_D1_143MH286	10.5	257.09	6.67%	81.22%	5.62%	4.00%
MB6LHQ_NOM4222_D1_143MH286	9.7	361.98	10.31%	77.14%	8.45%	1.24%
MB8LHQ_NOM4222_D1_143MH286	9.1	466.82	12.09%	74.91%	9.67%	-0.42%

Cell (LVTLL)	Sim Value(ns)		Bit
	Corner	3 Sigma	
MB4LHQ_NOM4222_D1_143MH286	0.320	1.348	Q1
MB4LHQ_NOM4222_D1_143MH286**(MPW Opt)**	0.263	0.780	Q1
MB6LHQ_NOM4222_D1_143MH286	0.353	1.525	Q1
MB6LHQ_NOM4222_D1_143MH286**(MPW Opt)**	0.239	0.685	Q1
MB8LHQ_NOM4222_D1_143MH286	0.375	1.260	Q1
MB8LHQ_NOM4222_D1_143MH286**(MPW Opt)**	0.321	0.724	Q1

RC: Qcap C651 benchmark
Model N3E: cln3e_1d2_sp_v0d5_2p1_for_C651_usage.l
-Timing slew:INVDx-predriver, -cload: INVDx-FO4 @ SSGNP/0.48V/m25c for MPW
-Timing slew:INVDx-predriver, -cload: INVDx-FO4 @ SSGNP/0.5V/m25c for PPA
-power slew: INVDx-predriver, -cload: 0.001fF @ FFGNP/0.75V/85C