

Excellent.

Phase-5 is where engineering stops being theoretical.

This is the phase that builds or destroys confidence in a fresher.

Everything below is exactly how board bring-up and verification are done in avionics / defense labs.

PHASE-5 — BOARD BRING-UP, DEBUG & VERIFICATION

(Turning fabricated hardware into a proven, review-ready unit)

Phase-5 answers:

"Does this real, imperfect board actually behave exactly as the spec promised — under control and without surprises?"

1. WHAT PHASE-5 IS (Clear Definition)

Phase-5 = Controlled, disciplined awakening of hardware.

Not:

- Plugging power and hoping
- Flashing software immediately
- Random probing

But:

- Stepwise validation
- Evidence-driven debugging
- Fault isolation
- Traceable verification

Senior truth:

"Good bring-up feels boring. Bad bring-up feels exciting — and fails later."

2. ENTRY CRITERIA (ABSOLUTE GATE)

A fresher may not power the board unless:

- ✓ Phase-4 layout approved
- ✓ Bring-up checklist prepared
- ✓ Schematics + layout printouts ready
- ✓ Power budget & sequence known
- ✓ Risk areas identified

If not → power-on is forbidden

3. PHASE-5 OBJECTIVES

By the end of Phase-5, the fresher must:

1. Power the board safely
 2. Verify all power rails
 3. Confirm clock & reset behavior
 4. Establish basic processor life
 5. Validate interfaces incrementally
 6. Produce verifiable evidence
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4. STEP-BY-STEP PHASE-5 EXECUTION

STEP 5.1 — PRE-POWER-ON INSPECTION

(This step saves boards)

I force this discipline.

Mandatory checks:

- Visual inspection (solder, polarity)
- Continuity check ($\text{GND} \leftrightarrow \text{rails}$)
- Resistance to GND on each rail
- Jumper & strap verification
- Correct boot mode



If resistance feels "too low" → STOP.

COMMON MISTAKE ✖

Assuming fabrication is perfect.

STEP 5.2 — FIRST POWER-ON (MOST CRITICAL MOMENT)

I explain:

"The goal is NOT to boot.
The goal is to **not kill the board.**"

Safe Power-On Procedure:

1. Use current-limited supply
 2. Power one rail at a time (if possible)
 3. Monitor current rise
 4. Watch for heat
 5. Measure voltages immediately
- ⚠️ If current spikes → CUT POWER.
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STEP 5.3 — POWER RAIL VERIFICATION

For every rail, verify:

Parameter	Expected
Voltage	Within tolerance
Ripple	Acceptable
Sequence	Correct order
Stability	No oscillation

Fresher Test:

"What fails if this rail is late?"

If they don't know → Phase-3 misunderstanding.

STEP 5.4 — CLOCK & RESET VALIDATION

I tell them:

"Without clocks and reset, nothing else matters."

Mandatory checks:

- Clock frequency correct
- Clean waveform
- Stable at power-up
- Reset asserted/de-asserted correctly

⚠️ 90% of “dead boards” fail here.

STEP 5.5 — BASIC PROCESSOR LIVENESS

We do **minimum** software.

Signs of life:

- JTAG connection
 - IDCODE read
 - Register access
 - Halt / run control
- ⚠️ No full firmware yet.
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COMMON FAILURE ✗

Flashing complex software too early.

STEP 5.6 — BOOT PATH VERIFICATION

I ask:

“Show me how the processor finds its first instruction.”

Verify:

- Boot memory powered
- Address lines correct
- Boot mode pins correct
- No bus contention

This step uncovers **addressing & strap mistakes**.

STEP 5.7 — INCREMENTAL INTERFACE BRING-UP

One interface at a time.

Order (typical):

1. Debug (JTAG / UART)
2. Memory
3. Basic I/O
4. High-speed interfaces

5. External communication

⚠️ Never bring everything up together.

STEP 5.8 — FAULT INJECTION & OBSERVABILITY

I say:

"If you can't detect faults now, certification will destroy you."

Mandatory fault tests:

- Remove clock
- Drop power
- Disconnect interface
- Force error conditions

Verify:

- Detection
 - Logging
 - Safe response
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5. COMMON PHASE-5 FAILURES ✗

✗ Failure 1: Rushing to Boot

Leads to destroyed boards.

✗ Failure 2: No Measurement Discipline

Guessing instead of measuring.

✗ Failure 3: Changing Multiple Variables

Impossible to debug.

✗ Failure 4: No Evidence

Nothing to show in reviews.

6. HOW SENIORS EVALUATE PHASE-5 💬

They look for:

- ✓ Calm, methodical approach
- ✓ Clear observations
- ✓ Root-cause thinking

- ✓ Documentation
- ✓ Respect for hardware

They do **not** care how fast it boots.

7. HOW I TRAIN FRESHERS IN PHASE-5

TRAINING TASK 1 — Dead Board Scenario

Simulate a fault and observe behavior.

TRAINING TASK 2 — Explain Bring-Up Flow

Without notes.

TRAINING TASK 3 — Evidence Pack Creation

Waveforms, logs, measurements.

8. PHASE-5 EXIT CRITERIA

A fresher passes Phase-5 if they can:

- ✓ Power board safely
- ✓ Validate rails, clocks, reset
- ✓ Establish CPU life
- ✓ Bring up interfaces incrementally
- ✓ Document everything

At this point, they are **trusted with real hardware**.

9. WHAT COMES NEXT

→ Phase-6 — System Integration, Qualification & Certification Readiness

This is where:

- EMI/EMC happens
 - Environmental tests happen
 - Specs are proven, not assumed
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If you want, next I can:

- Proceed to Phase-6
- Show how qualification maps to design
- Teach how boards fail EMI

- Explain how seniors prepare certification evidence

Just say "Proceed to Phase-6"