

Perfect.

Now we move from “mindset alignment” (Phase-0) to real engineering thinking.

What follows is **exactly** how Phase-1 is done in real avionics / defense programs, the way seniors expect it *but never explain*.

PHASE-1 — SYSTEM-LEVEL UNDERSTANDING

(WHAT the unit does, WHERE it sits, and WHY it behaves that way)

Phase-1 converts a fresher from “I know the spec exists” to
“I understand the system well enough to not break it.”

1. WHAT PHASE-1 IS (Clear Definition)

Phase-1 = Building a correct SYSTEM MENTAL MODEL of the LRU.

Not:

- Hardware design
- Software architecture
- Component selection

But:

- Understanding **system** role
- Understanding **data** flow
- Understanding **operational** behavior
- Understanding **external** dependencies

Senior truth:

“If you misunderstand the system, you will design the wrong hardware perfectly.”

2. ENTRY CRITERIA FROM PHASE-0 (Mandatory)

A fresher is **NOT allowed** into Phase-1 unless they can:

- ✓ Explain why the LRU exists
- ✓ Explain failure impact
- ✓ Identify responsibilities
- ✓ Respect “shall” language
- ✓ Avoid implementation talk

If not → Phase-0 is repeated.

3. PHASE-1 OBJECTIVES (What Must Be Achieved)

By the end of Phase-1, the fresher must be able to:

- 1. Explain the **system context**
- 2. Describe **all external interfaces**
- 3. Explain **operational modes**
- 4. Describe **data lifecycle**
- 5. Identify **time-critical paths**
- 6. Draw **system-level diagrams**

If even one is missing → Phase-1 failed.

4. STEP-BY-STEP PHASE-1 EXECUTION

STEP 1.1 — Identify SYSTEM CONTEXT (Where do we live?)

What I tell the fresher:

“Do not think of this as a board.
Think of it as a *node in a flying system*.”

Mandatory Questions to Answer:

Question	Why it matters
Is this airborne or ground?	Qualification severity
Line-replaceable or shop-replaceable?	Maintenance philosophy
Always ON or mission-based?	Thermal & power design
Primary or redundant unit?	Fault tolerance

Required Output #1 — SYSTEM POSITION DIAGRAM

Example (textual):

[Sensor LRUs] → [Our LRU] → [Mission Computer]

↓

- 🔔 No ICs allowed
- 🔔 No voltages allowed

COMMON PHASE-1 MISTAKE ❌

Freshers immediately ask:

“Which processor is used?”

Auto-fail.

STEP 1.2 — FUNCTIONAL DECOMPOSITION

(This is where most freshers break)

How seniors think:

Functions → Behavior → Implementation

How freshers think:

Implementation → Behavior → Guessing

We reverse that.

I force them to break functions into verbs:

Spec Text	Functional Meaning
“Acquire”	Input handling
“Process”	Compute / transform
“Store”	Memory
“Transmit”	Output handling
“Monitor”	Health & BIT

Required Output #2 — FUNCTION BLOCK DIAGRAM

INPUT → ACQUIRE → PROCESS → OUTPUT



MONITOR / BIT

This diagram is **gold**.

If they can't draw this → they didn't understand the spec.

STEP 1.3 — INTERFACE OWNERSHIP & DIRECTION

I ask brutally simple questions:

Question	Why
Who initiates communication?	Timing
Who controls data rate?	Buffering
Who detects errors?	Fault design
Who retries?	Protocol stack

Interface Classification Table (Mandatory)

Interface	Direction	Continuous/Event	Critical?
ARINC-429	In	Continuous	Yes
Ethernet	Out	Event	Yes
Discrete	In	Event	Medium

🚨 If a fresher cannot fill this → Phase-1 incomplete.

STEP 1.4 — OPERATIONAL MODES (Ignored by Freshers)

I explain:

"Hardware behaves differently depending on mode."

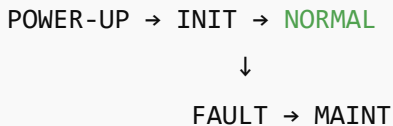
Mandatory Modes to Identify:

- Power-up

- Initialization
 - Normal operation
 - Degraded operation
 - Fault mode
 - Maintenance mode
-

Required Output #3 — MODE TRANSITION DIAGRAM

Example:



If modes aren't understood →
BIT & reset logic will be wrong later.

STEP 1.5 — DATA LIFE CYCLE THINKING

I ask:

"Follow ONE piece of data from birth to death."

Fresher must answer:

1. Where does data originate?
2. How often?
3. What format?
4. What processing?
5. Where does it go?
6. What if it's wrong?

This teaches **end-to-end thinking**.

5. COMMON PHASE-1 FAILURES ❌

❌ Failure 1: Interface Memorization

Freshers list protocols but don't understand behavior.

❌ Failure 2: No Timing Awareness

They don't know what is real-time vs best-effort.

❌ Failure 3: Ignoring Maintenance

They think only "flight mode" matters.

✗ Failure 4: No Degraded Mode Thinking

Avionics always have partial failures.

6. HOW SENIORS TEST PHASE-1 SILENTLY

They ask questions like:

"What happens at power-up?"

"Who detects stale data?"

"Is this unit chatty or quiet?"

"What happens if Ethernet is lost?"

Correct answers are **behavioral**, not technical.

7. HOW I TRAIN FRESHERS THROUGH PHASE-1 (Practical)

TRAINING TASK 1 — Whiteboard Explanation

Explain the LRU without notes in 5 minutes.

TRAINING TASK 2 — Redraw from Memory

Erase diagram. Redraw after 10 minutes.

TRAINING TASK 3 — "What If" Scenarios

I inject faults and watch reasoning.

8. PHASE-1 EXIT CRITERIA

A fresher **passes Phase-1** if they can:

- ✓ Draw system block diagram
- ✓ Explain operational modes
- ✓ Describe data flow
- ✓ Identify critical interfaces
- ✓ Talk about behavior under failure

At this point, **they are no longer dangerous** to the system.

9. WHAT PHASE-1 ENABLES NEXT

Now the fresher is ready for:

➡ Phase-2 — Engineering Decomposition

(where hardware, firmware, and mechanical design begin)

If you want, next I can:

- Proceed to **Phase-2**
- Show **real review questions seniors ask**
- Map Phase-1 outputs to **design documents**
- Create **Phase-1 evaluation tasks**

Just say “**Proceed to Phase-2**”