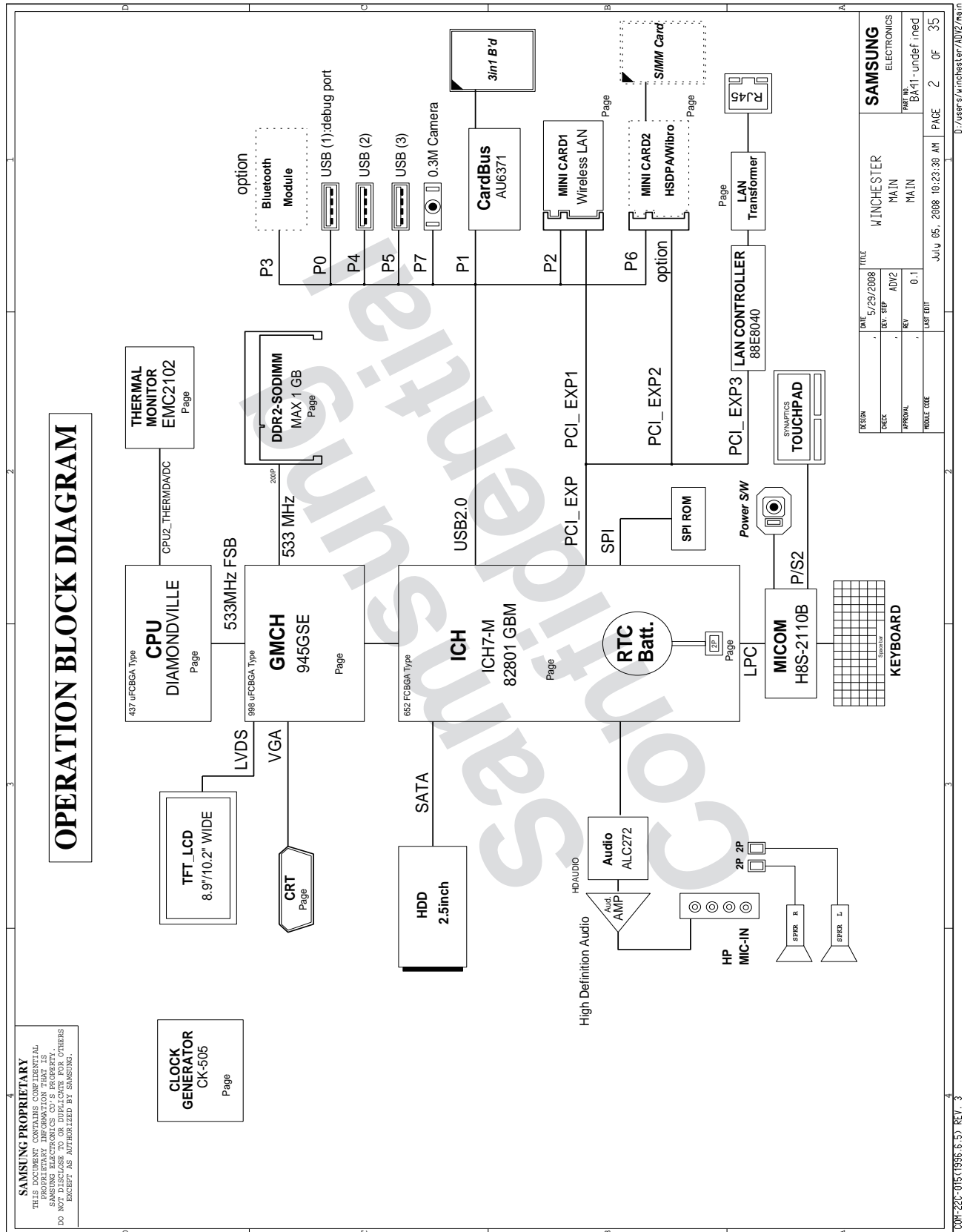


# Table of Contents

Page. 1	---	COVER
Page. 2	---	OPERATION BLOCK DIAGRAM
Page. 3	---	POWER SEQUENCE
Page. 4	---	CLOCK DISTRIBUTION
Page. 5	---	BOARD INFORMATION
Page. 6	---	CLOCK GENERATOR (CK-505M)
Page. 7	8	DIAMONDVILLE (N270)
Page. 9	---	THERMAL MONITOR
Page. 10	13	CALISTOGA (INTEL945GSE)
Page. 14	15	DDR2 ON BOARD
Page. 16	---	DDR2 TERMINATION
Page. 17	---	DDR2 SODIMM
Page. 18	21	ICH7-M
Page. 22	---	BIOS CODE
Page. 23	---	LCD (LVDS) CONN.
Page. 24	---	CRT CONN.
Page. 25	---	HDD CONNECTOR (SATA)
Page. 26	---	MICOM
Page. 27	29	LAN (GIGABIT)
Page. 30	---	USB
Page. 31	---	MINI-CARD (Wireless)
Page. 32	33	CARDBUS CONTROLLER (AU6371)
Page. 34	---	3IN1 SUB
Page. 35	---	AUDIO CODEC (ALC262-GR)
Page. 36	---	AMP & SPEAKER & MIC
Page. 37	---	KBD CONN & DEBUG PORT
Page. 38	---	CHARGER
Page. 39	---	P3. 3V_AUX & P5V_AUX
Page. 40	---	DDR2 POWER
Page. 41	---	CHIPSET POWER (P 1.05V & P
Page. 42	---	CPU VRM POWER (VCC_CORE)
Page. 43	---	POWER DISCHARGE
Page. 44	---	SWITCHED POWER
Page. 45	---	LED FPC CONNECTOR POWER S/W
Page. 46	---	TRANSMITTER
Page. 47	---	MOUNT HOLE
Page. 49	50	TEST POINTS

DESIGN	BAE, SC	5/29/2008	TITLE		WINCHESTER		SAMSUNG ELECTRONICS	
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## 8. Block Diagram and Schematic



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## 8. Block Diagram and Schematic

## BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB		0	E, F, G
Hub to PCI			
LPC Bridge/IDE/AC97/SMBUS			
Internal MAC			
	AD23 (internal)		
	AD30 (internal)		
	AD31 (internal)		
	AD24 (internal)		

## I<sup>2</sup>C / SMB Address

Devices	Address	Hwz	Bus
IC16	Master		SM1US Master
CK505M (Clock Generator)	1101 001 X	Dzh	Clock, Unused
SO30MM	1010 000 X	Adh	Output Disable
MICOM	Master		
BATTERY	0001 011 h	16h	
W83L77IG	1010 111 X	5Eh	
W83L786NG	0101 110 X	5Ch	

## USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	1	UHCL_2	4
	USB PORT		USB PORT
	3-IN-1		5
			6
	X		HSDPA
			CAMERA
UHCL_1	2	UHCL_3	7
	BLUETOOTH		
UHCL_1	3		

## System Power States

Power Rail	Devices (Page Number)
P5V	ICH6-M20 (24) MICOM(26) DMB(28) USB(29) Min-PQ(30) RQ384(31) STAC925(32) Audio AMP(33) DDR POWER(39) LED B(44)
P3.3V	CLOCK(6) Thermal sensor(9) SODIMM(7) ICH6-M(19) FWH(23) LCD(23) HDD(25) MICOM(26) DMB(28) DQ(29) Min-PQ(30) RQ384(31) STAC925(32) CPU VRM(40) MICOM POWER(43) LED B(44) BLUE(45) LED(46)
P1.5V	CPU(8) 915GMS(11) ICH6-M(20)
P2.5V	915GMS(11) ICH6-M(20) LCD(23) MICOM(26)
P0.9V	DDR2 Terminator(18) SODIMM(7)
P5V_AUX	Thermistor(9) ICH6-M(20) DDR POWER(39) P5V(42)
P3.3V_AUX	Thermal Member(9) ICH6-M(19) MICOM(26) LAN(27) MDC(29) Min-PQ(30) LB1 LED(56) P3.3V(42) P2.5V(43) MICOM POWER(43)
P1.8V_AUX	915GMS(11) DDR2 ON BD(14) SODIMM(7)
P1.5V_AUX	ICH6-M(20) P1.5V(42)
VCCP VCC CORE	CLOCK(6) CPU(7) 915GMS(10) ICH6-M(19) MICOM(26) CPU (8)

## Voltage Rails

Power Rail	Descriptions
Power_BAT	Power input, 2.0V min. to 3.0V max. (in 3.3V steps) supply for the RTC well.
VCC	Primary DC input, 2.0V min. to 3.0V max. (in 3.3V steps) supply for the RTC well.
MCOM_PSV	Output voltage of MAX1989. (If VCC is removed, it will be off)
P3.0V	3.3V power rail (off in S4-S5)
P3.1V_LAN	3.3V power rail (off in S4-S5)
P3.1V_LAN	3.3V power rail (off in S4-S5)
P3.2V_LAN	3.3V power rail (off in S4-S5)
P3.3V_AUX	Internal Regulator's Power of LAN Controller
P3.3V_AUX	Internal Regulator's Power of LAN Controller
P1.8V_AUX	3.3V power rail (off in S4-S5)
P3.3V	3.3V power rail (off in S4-S5)
P3.3V	3.3V power rail (off in S4-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
VCCP	1.05V power rail, GMCH core, CPU/GMCH FSB Termination.
VCCP	Core voltage for TONCH-ULV CPU (0.7A ~ 3.0V)
VCC CORE	1.5V (Direct Media Interface Compensation)
P1.5V_DMI	1.5V (Direct Media Interface Compensation)
VCCP	1.05V power rail, GMCH core, CPU/GMCH FSB Termination.
VDD3V3V	3.3V (LCD)
VDD3V3V	3.3V (LCD)
VCC CRT	5.0V (CRT)
VCC CRT	5.0V (CRT)
CB3 VCC	3.3V (CF card)
AUD_PSV	5.0V switched power rail (off in S3-S5)
AUD_PSV	5.0V switched power rail (off in S3-S5)
AMP	5.0V (AUX AMP)
VDD	5.0V (AUX AMP)

## CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.198 V
0	0	0	0	0	1	1.196 V
0	0	0	0	0	0	1.164 V
0	0	0	0	0	1	1.148 V
0	0	0	0	0	0	1.116 V
0	0	0	0	0	1	1.100 V
0	0	0	0	0	0	1.052 V
0	0	0	0	0	1	1.084 V
0	0	0	0	0	0	1.028 V
0	0	0	0	0	1	1.004 V
0	0	0	0	0	0	0.995 V
0	0	0	0	0	1	0.956 V
0	0	0	0	0	0	0.940 V
0	0	0	0	0	1	0.908 V
0	0	0	0	0	0	0.892 V
0	0	0	0	0	1	0.860 V
0	0	0	0	0	0	0.844 V
0	0	0	0	0	1	0.812 V
0	0	0	0	0	0	0.788 V
0	0	0	0	0	1	0.780 V
0	0	0	0	0	0	0.748 V
0	0	0	0	0	1	0.732 V
0	0	0	0	0	0	0.700 V

YONAH-ULV  
HIGH-FREQUENCY MODE

YONAH-ULV  
LOW-FREQUENCY MODE

YONAH-ULV  
DEEPER SLEEP MODE

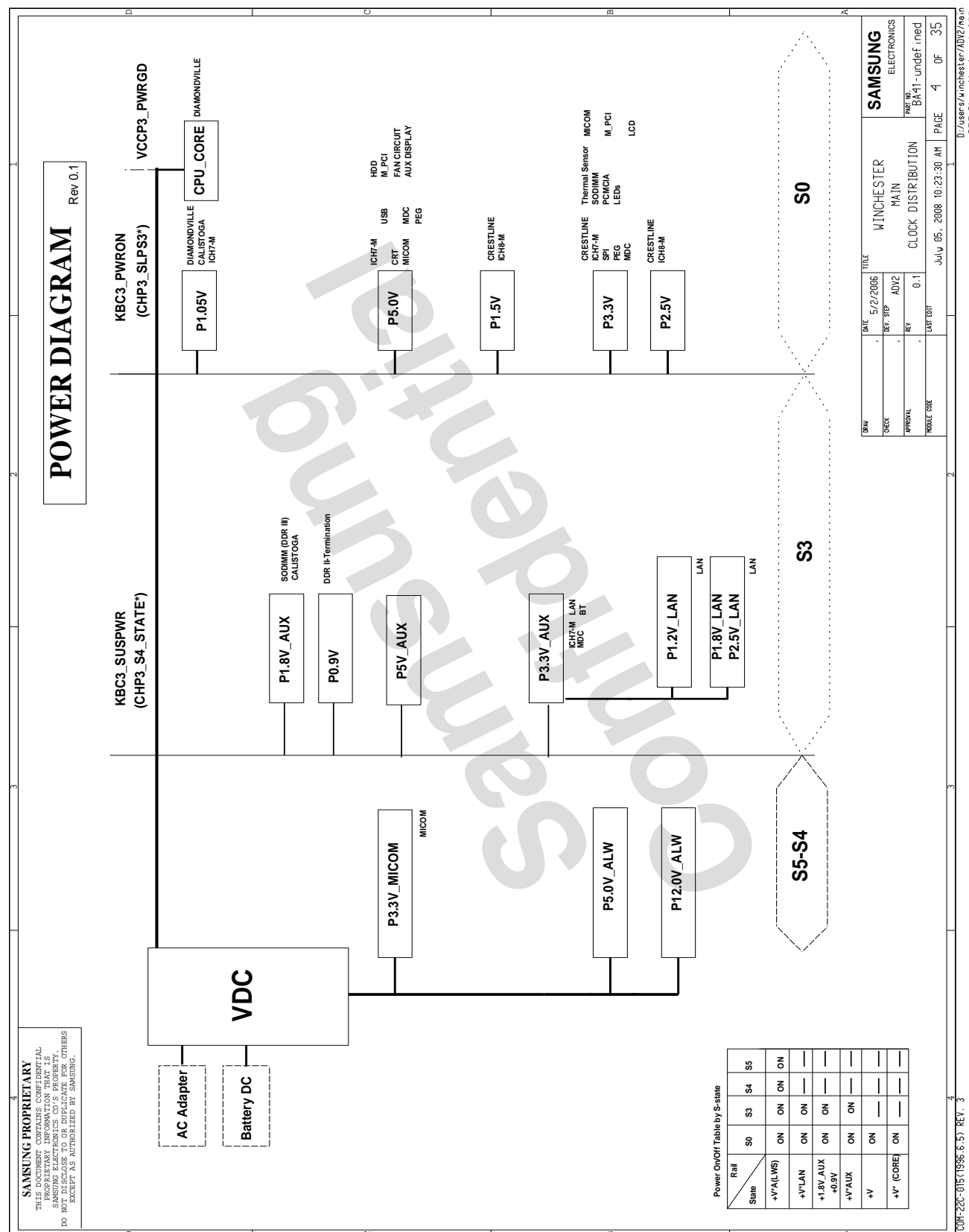
Need to be updated!!

	VID5	VID4	VID3	VID2	VID1	VDD0	Voltage	VID5	VID4	VID3	VID2	VID1	VDD0
0	0	0	0	0	0	0	1.703 V	0	0	0	0	0	0
1	0	0	0	0	0	0	1.696 V	0	0	0	0	0	0
2	0	0	0	0	0	0	1.689 V	0	0	0	0	0	0
3	0	0	0	0	0	0	1.680 V	0	0	0	0	0	0
4	0	0	0	0	0	0	1.674 V	0	0	0	0	0	0
5	0	0	0	0	0	0	1.668 V	0	0	0	0	0	0
6	0	0	0	0	0	0	1.662 V	0	0	0	0	0	0
7	0	0	0	0	0	0	1.656 V	0	0	0	0	0	0
8	0	0	0	0	0	0	1.650 V	0	0	0	0	0	0
9	0	0	0	0	0	0	1.644 V	0	0	0	0	0	0
10	0	0	0	0	0	0	1.638 V	0	0	0	0	0	0
11	0	0	0	0	0	0	1.632 V	0	0	0	0	0	0
12	0	0	0	0	0	0	1.626 V	0	0	0	0	0	0
13	0	0	0	0	0	0	1.620 V	0	0	0	0	0	0
14	0	0	0	0	0	0	1.614 V	0	0	0	0	0	0
15	0	0	0	0	0	0	1.608 V	0	0	0	0	0	0
16	0	0	0	0	0	0	1.602 V	0	0	0	0	0	0
17	0	0	0	0	0	0	1.596 V	0	0	0	0	0	0
18	0	0	0	0	0	0	1.590 V	0	0	0	0	0	0
19	0	0	0	0	0	0	1.584 V	0	0	0	0	0	0
20	0	0	0	0	0	0	1.578 V	0	0	0	0	0	0
21	0	0	0	0	0	0	1.572 V	0	0	0	0	0	0
22	0	0	0	0	0	0	1.566 V	0	0	0	0	0	0
23	0	0	0	0	0	0	1.560 V	0	0	0	0	0	0
24	0	0	0	0	0	0	1.554 V	0	0	0	0	0	0
25	0	0	0	0	0	0	1.548 V	0	0	0	0	0	0
26	0	0	0	0	0	0	1.542 V	0	0	0	0	0	0
27	0	0	0	0	0	0	1.536 V	0	0	0	0	0	0
28	0	0	0	0	0	0	1.530 V	0	0	0	0	0	0
29	0	0	0	0	0	0	1.524 V	0	0	0	0	0	0
30	0	0	0	0	0	0	1.518 V	0	0	0	0	0	0
31	0	0	0	0	0	0	1.512 V	0	0	0	0	0	0
32	0	0	0	0	0	0	1.506 V	0	0	0	0	0	0
33	0	0	0	0	0	0	1.500 V	0	0	0	0	0	0
34	0	0	0	0	0	0	1.494 V	0	0	0	0	0	0
35	0	0	0	0	0	0	1.488 V	0	0				

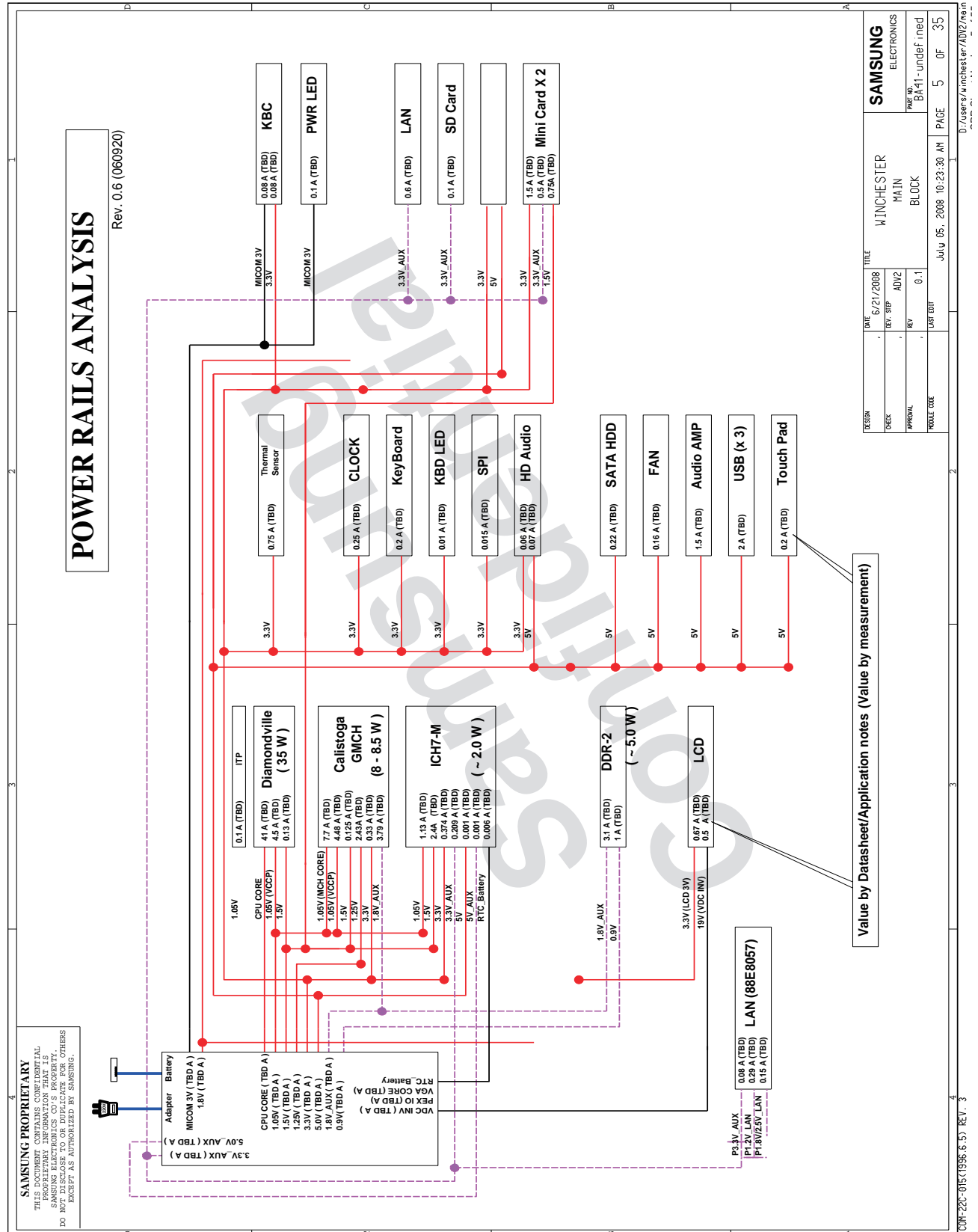
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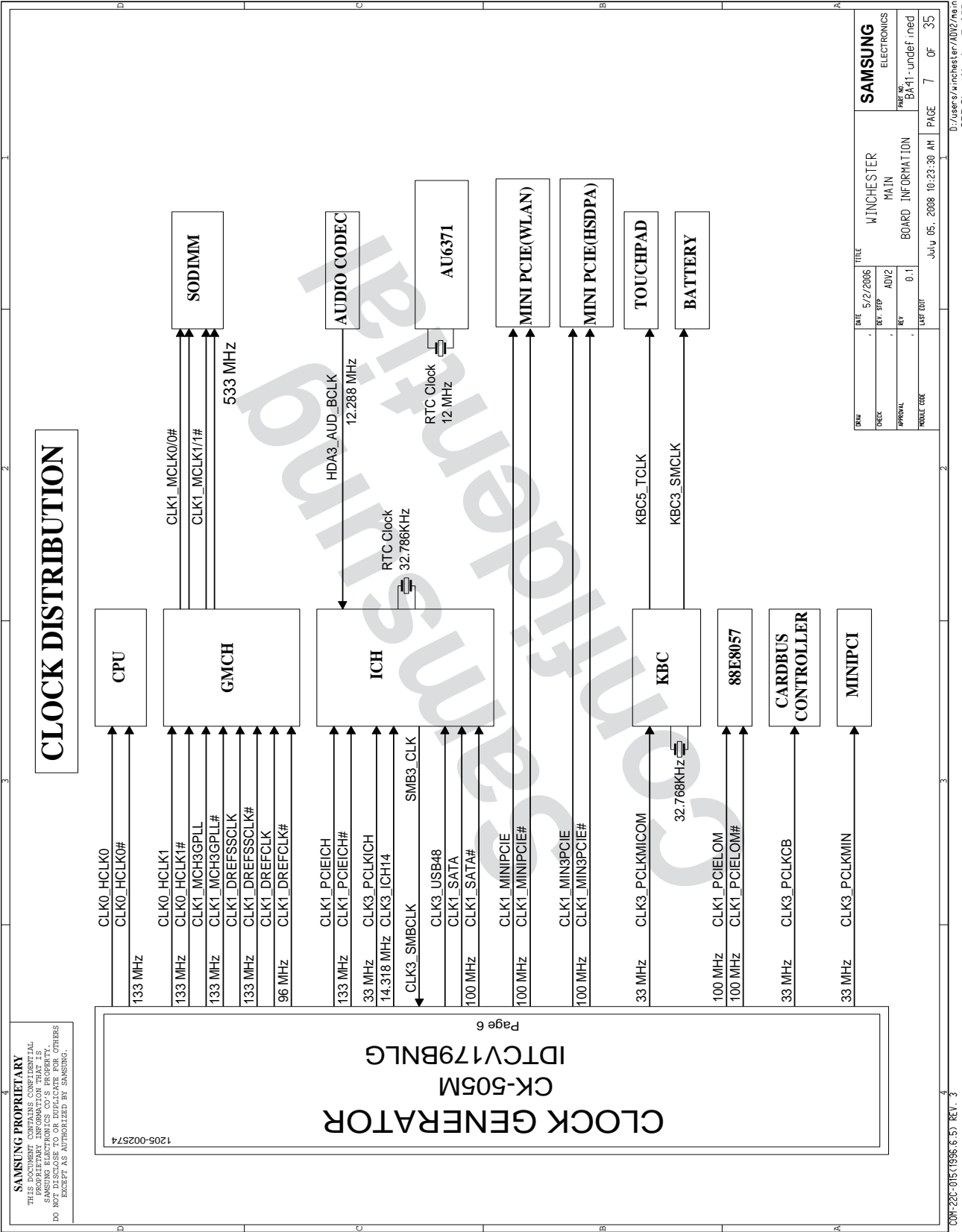


## 8. Block Diagram and Schematic





8. Block Diagram and Schematic



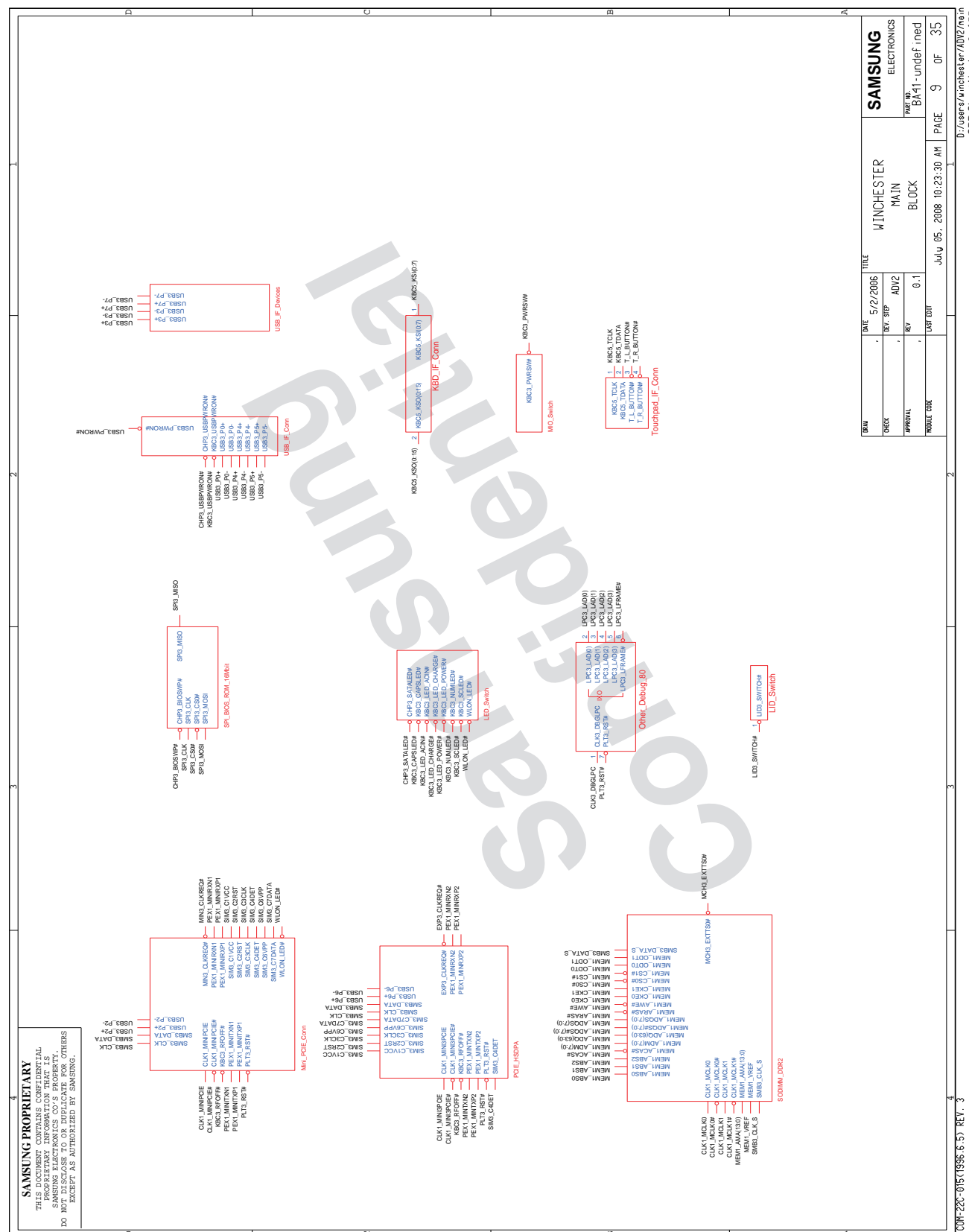
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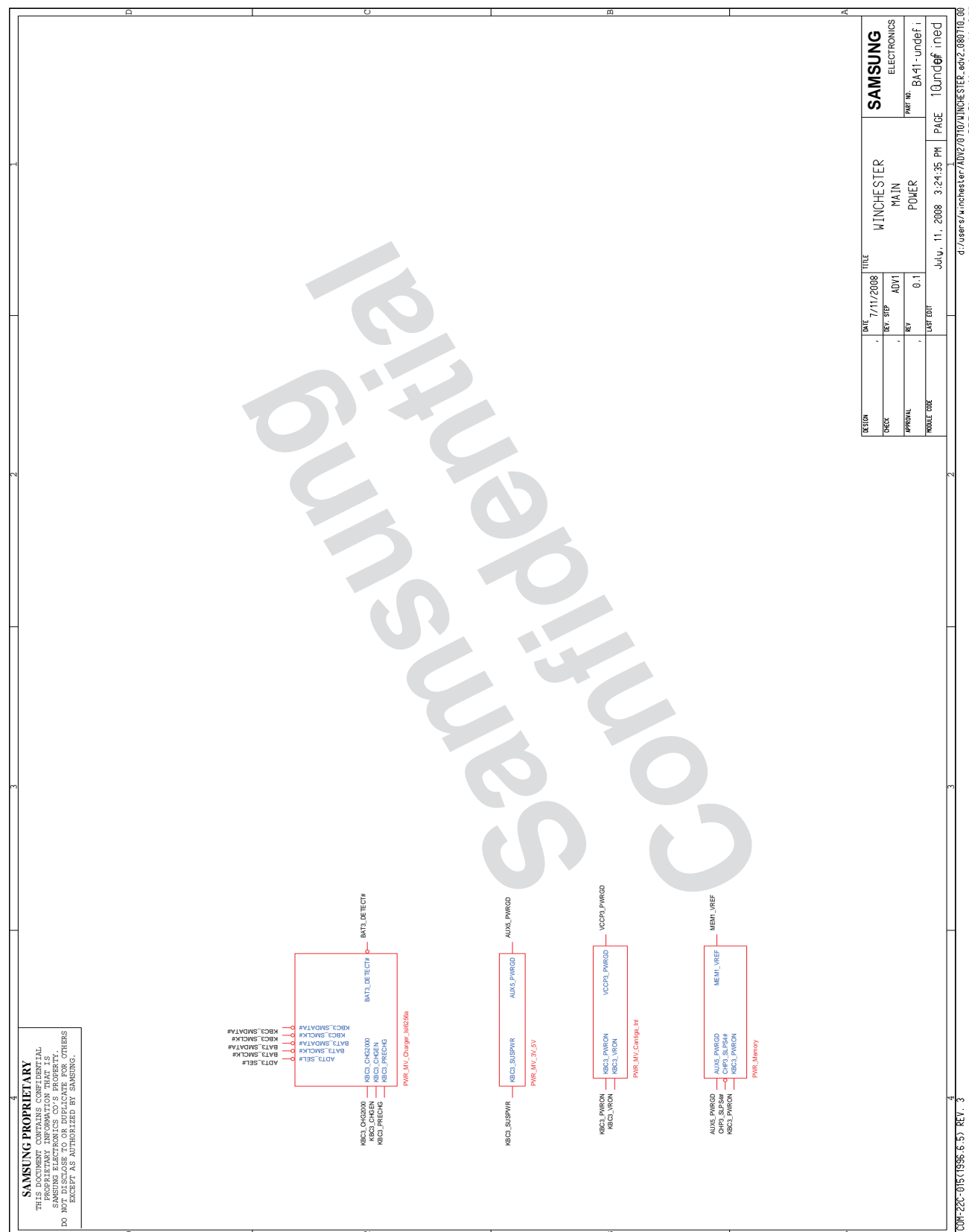
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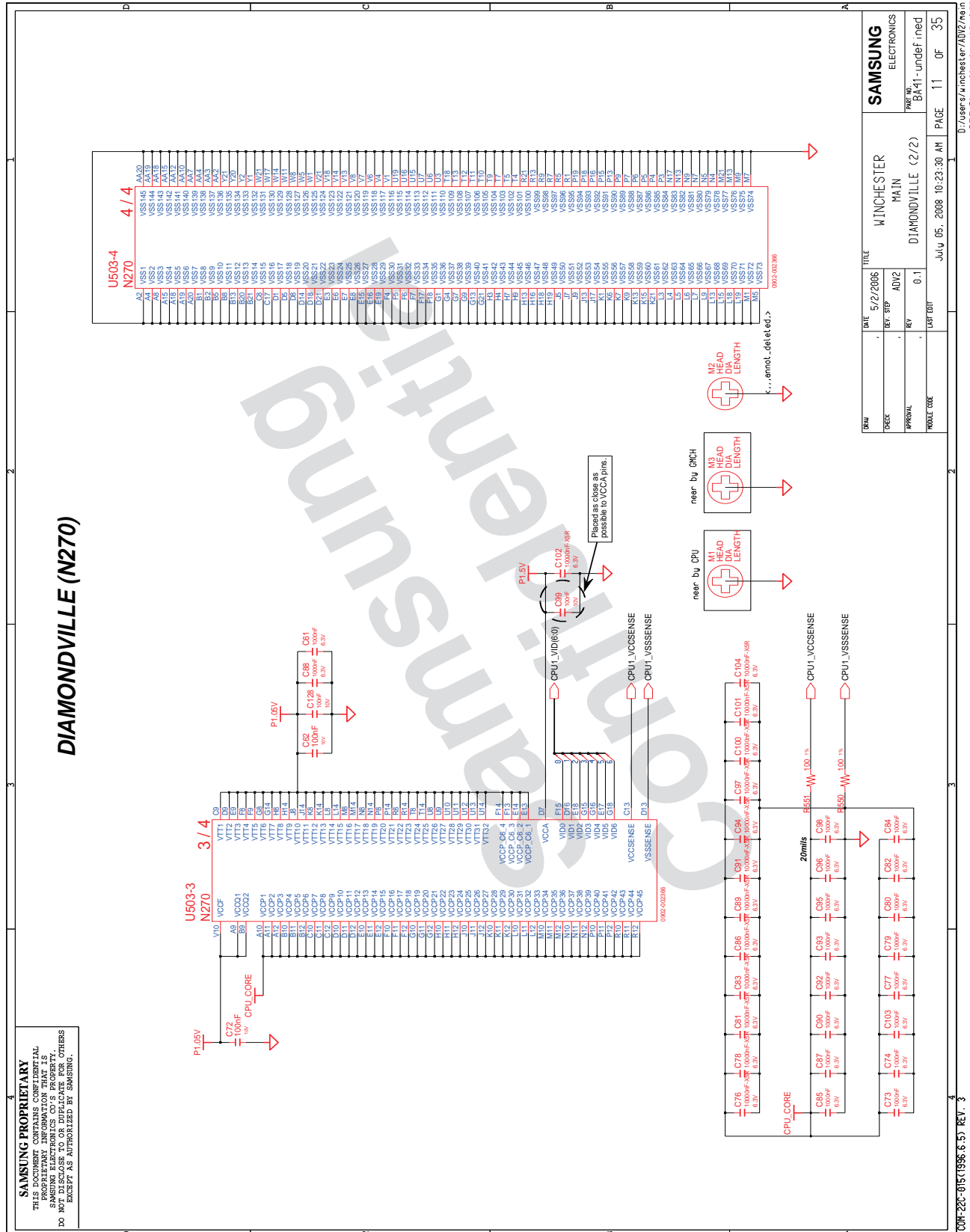
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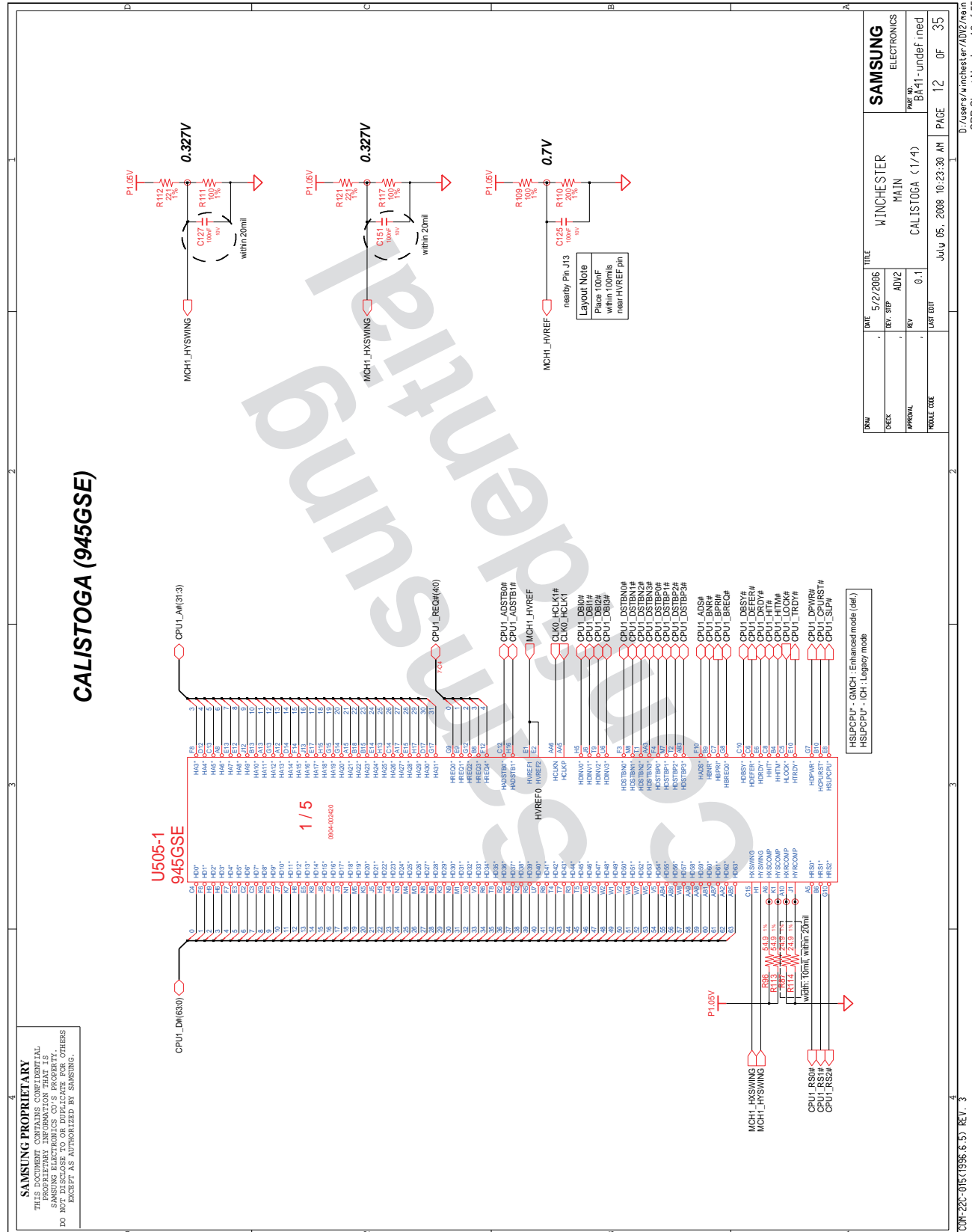




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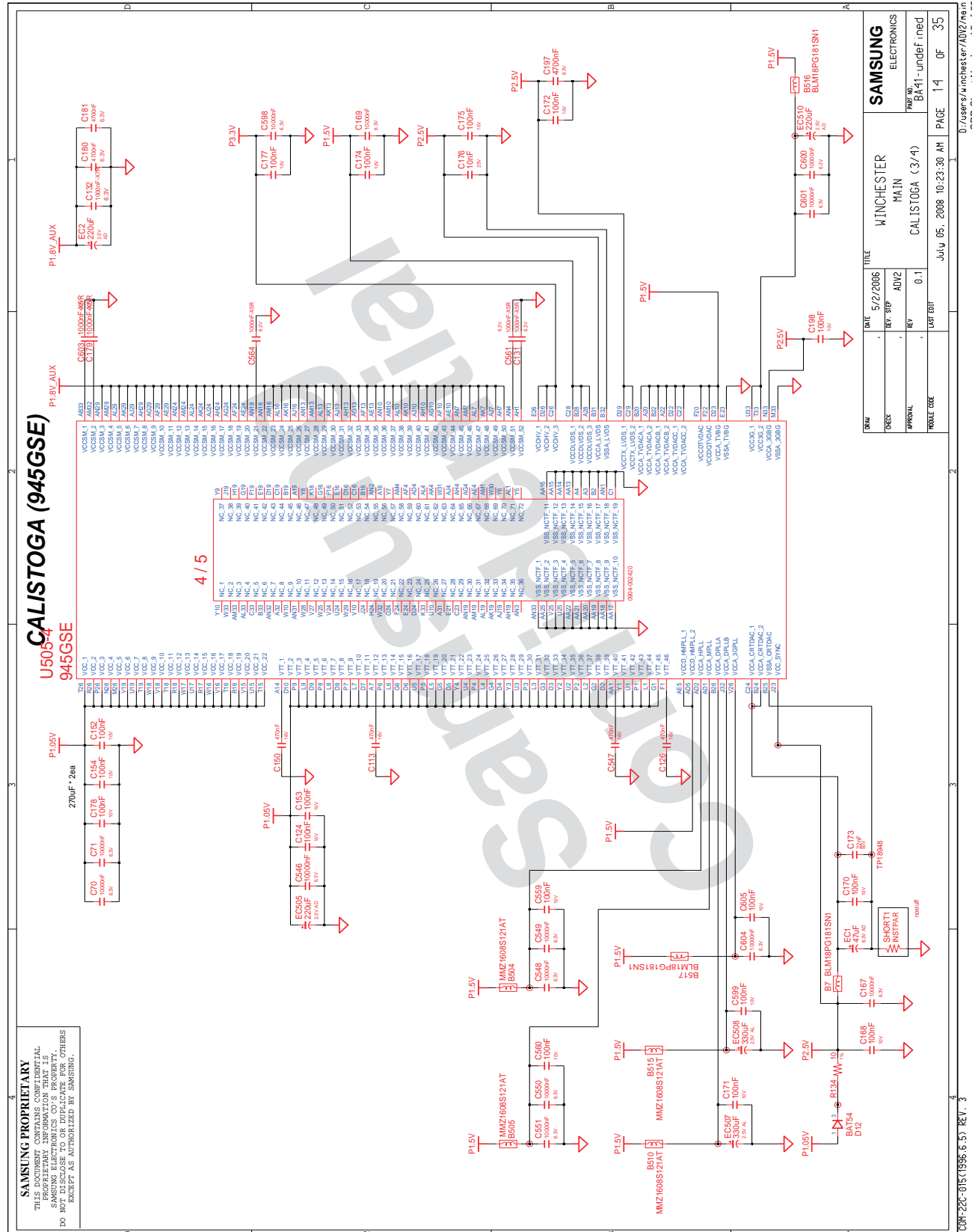


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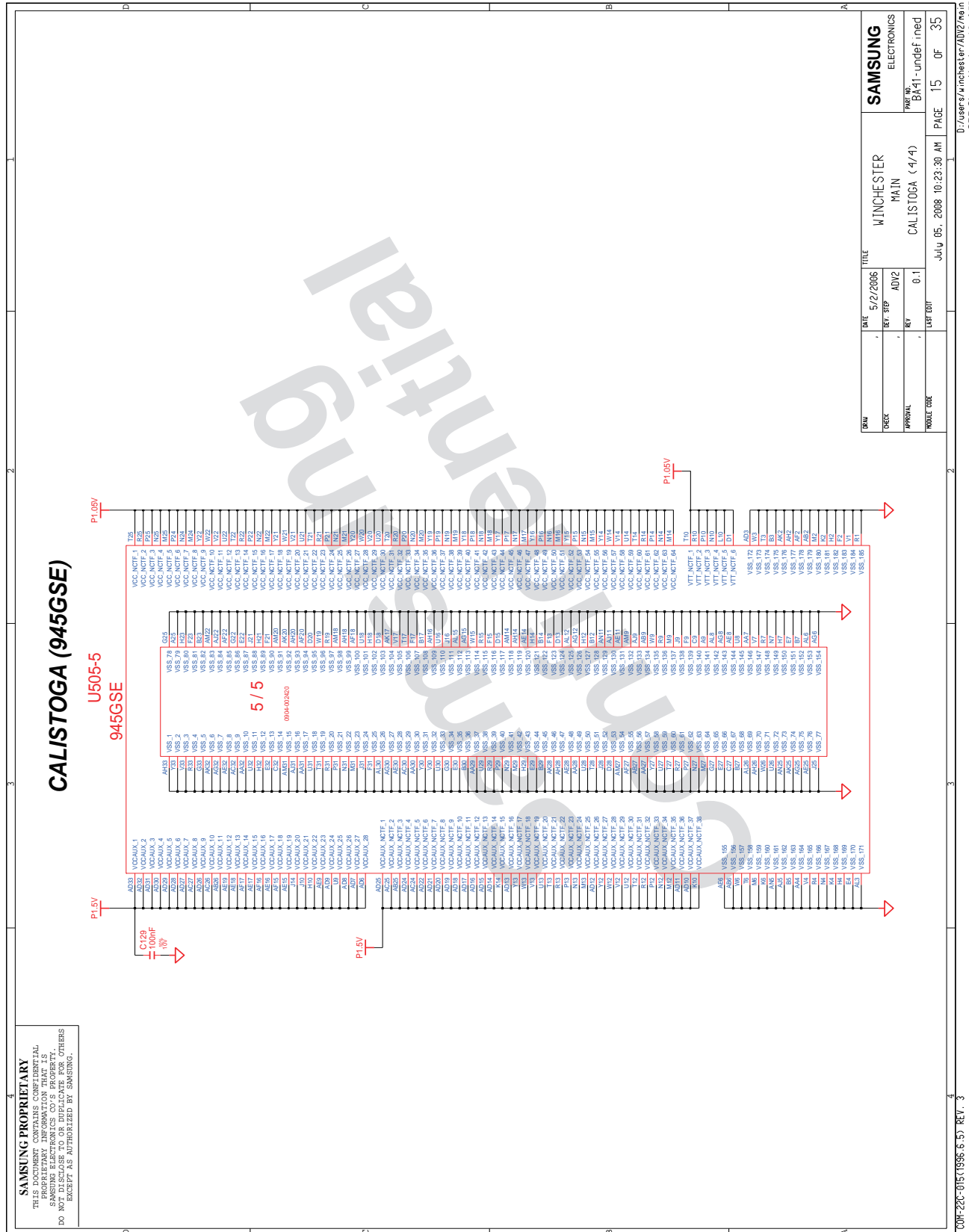




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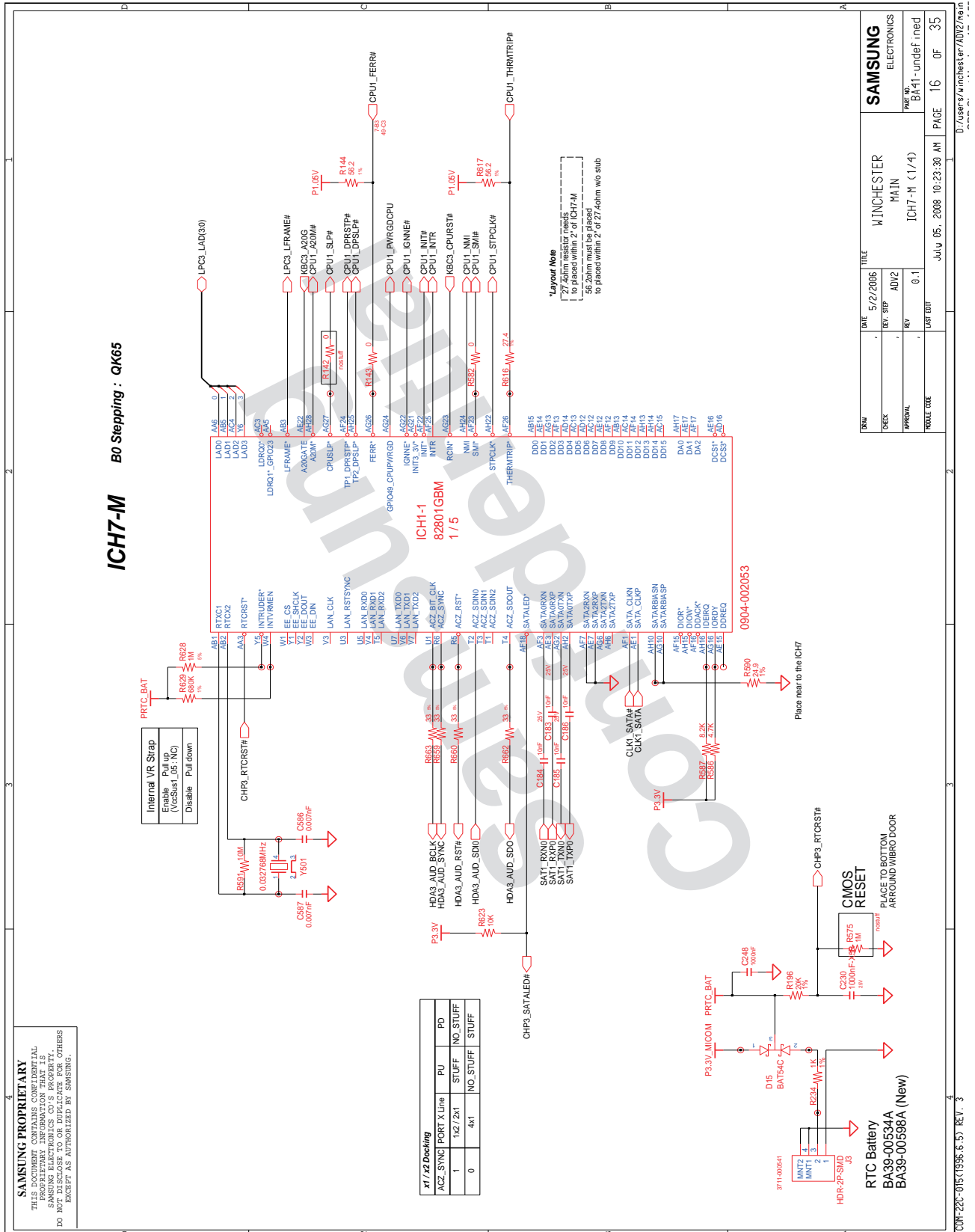


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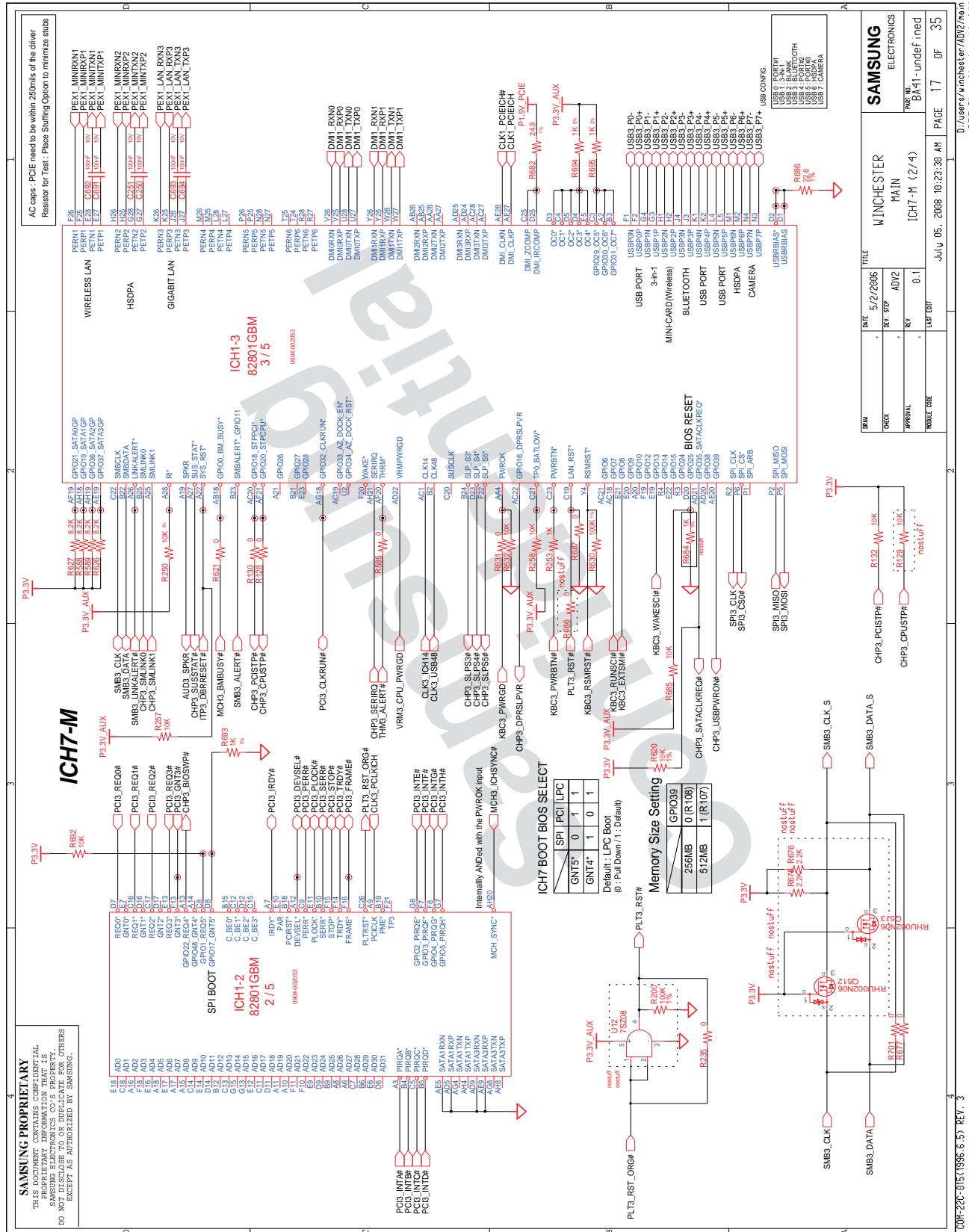




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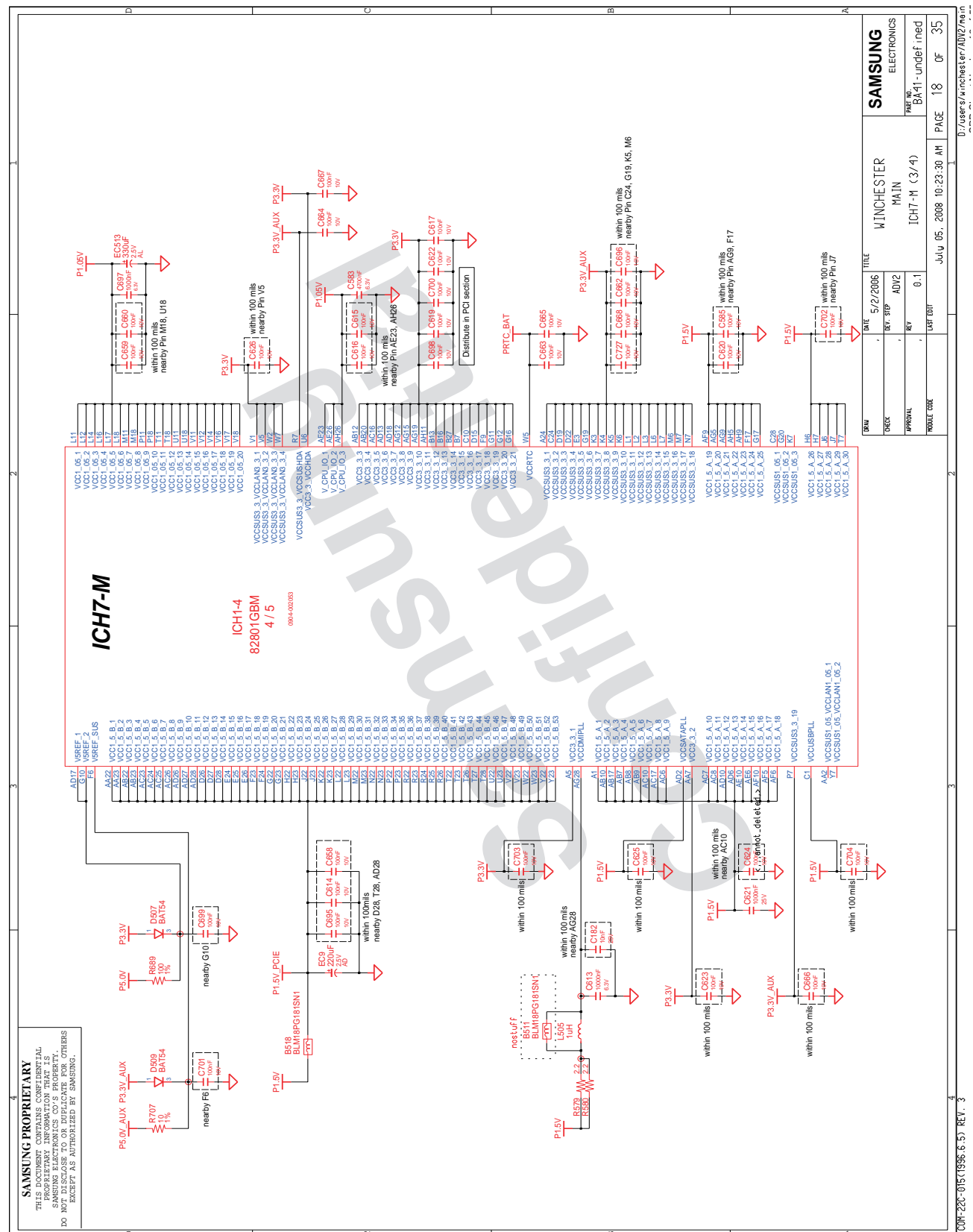


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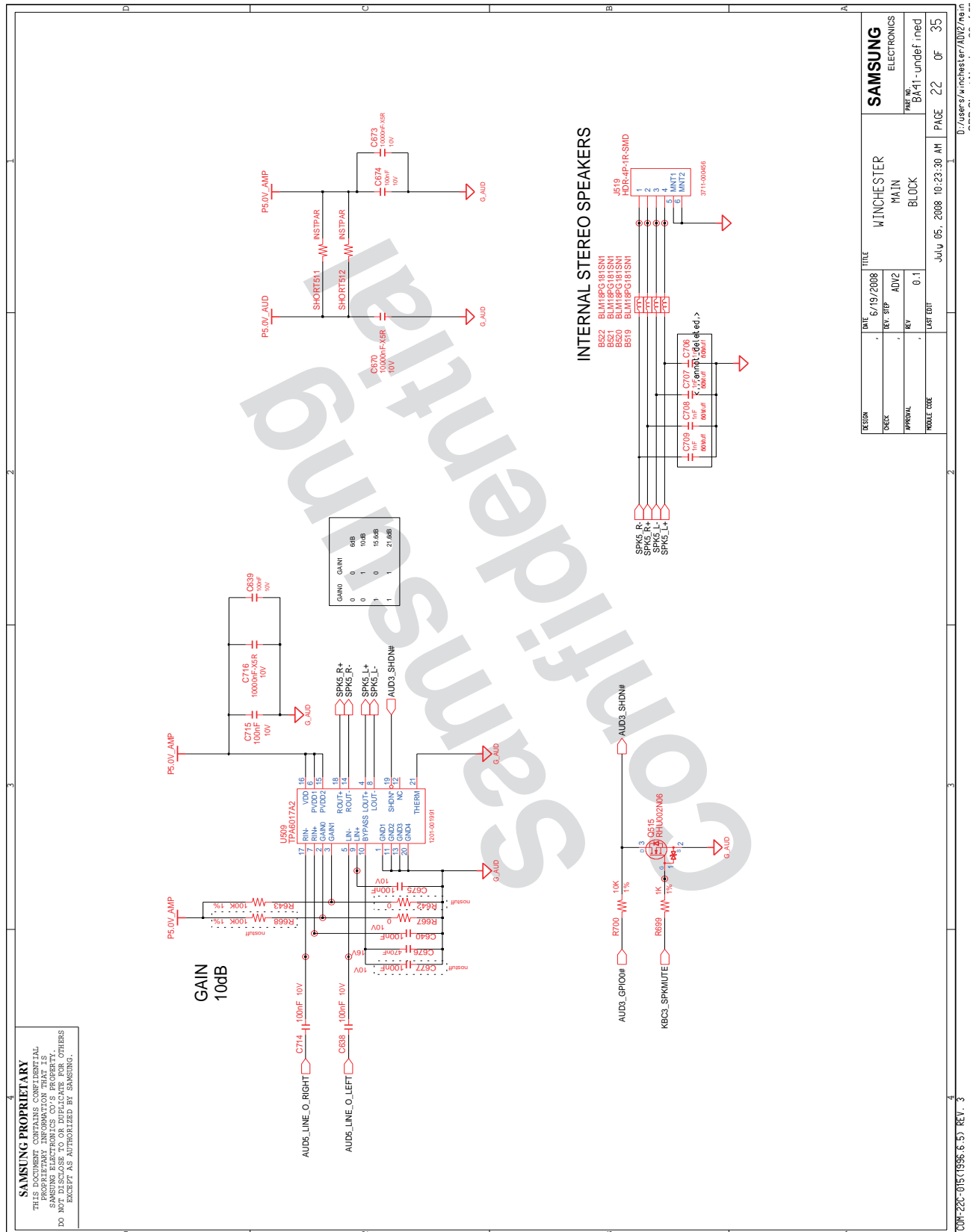
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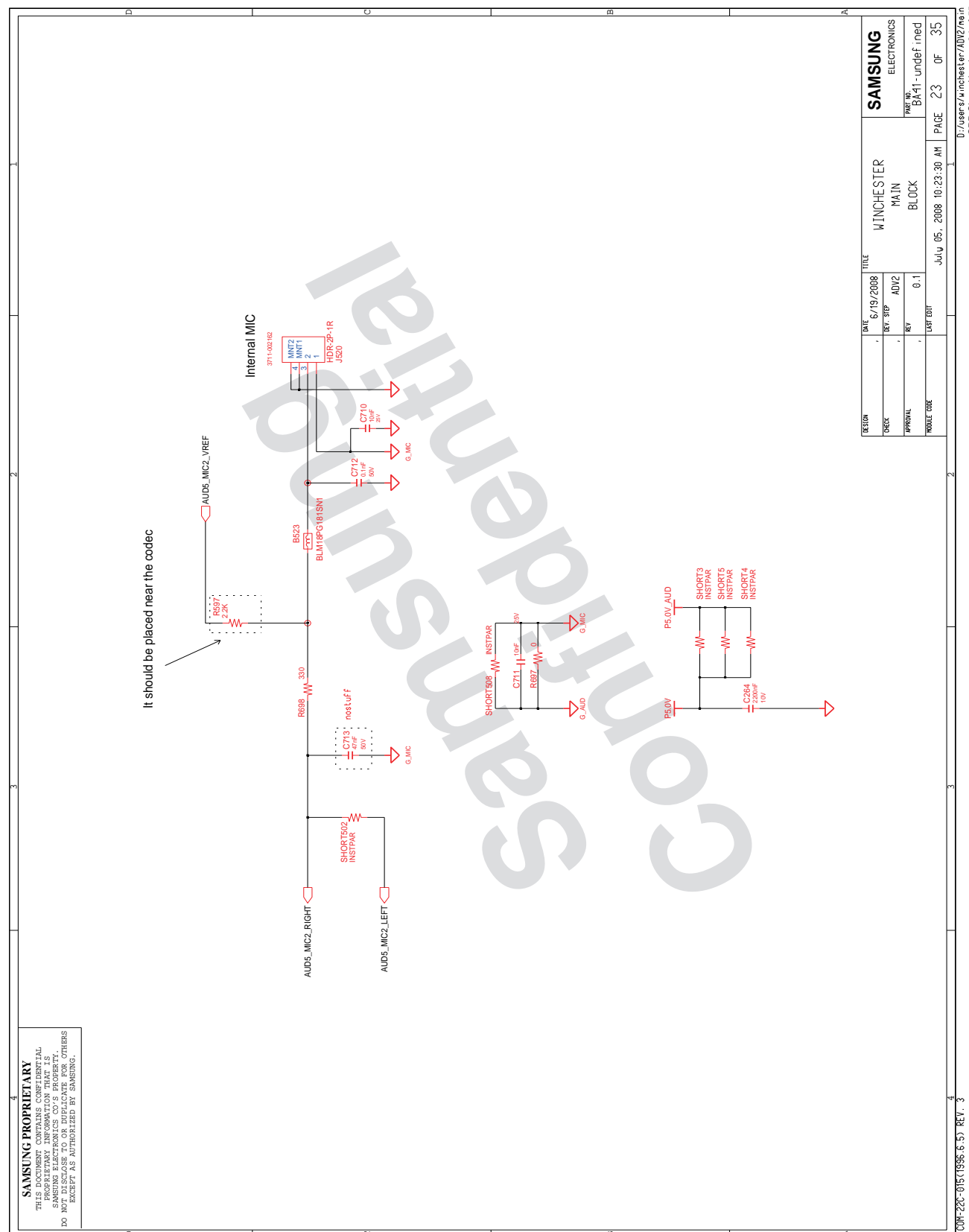
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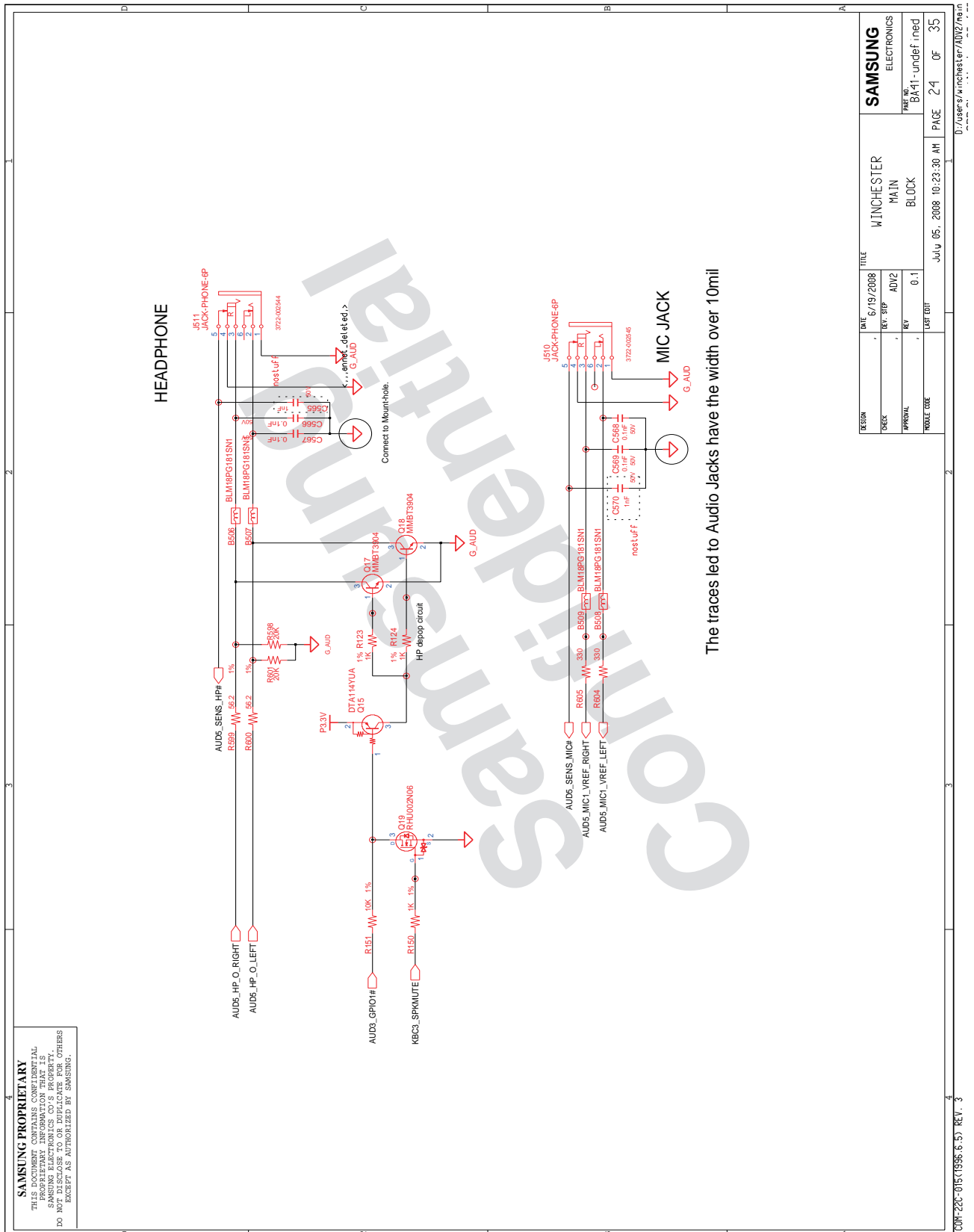
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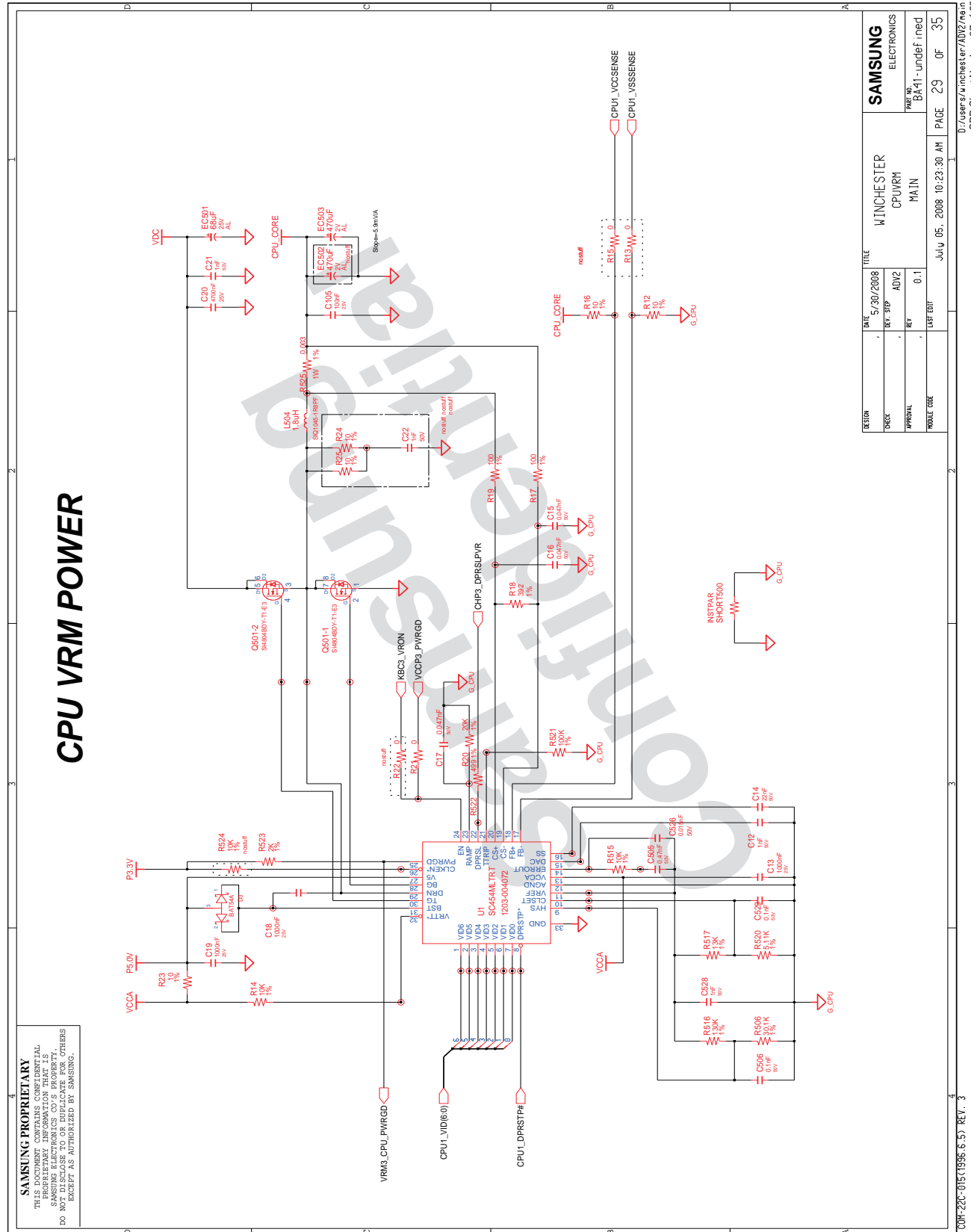
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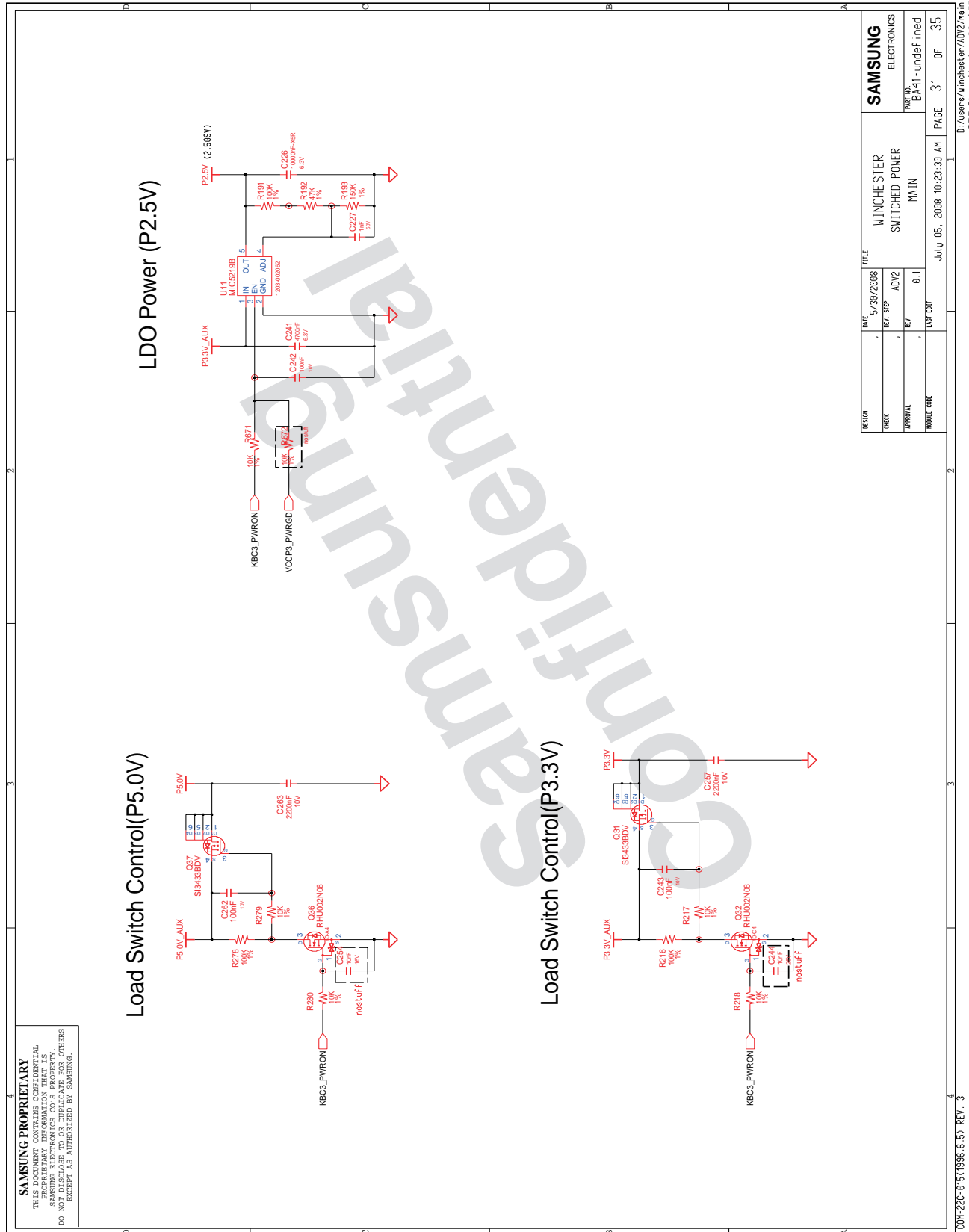


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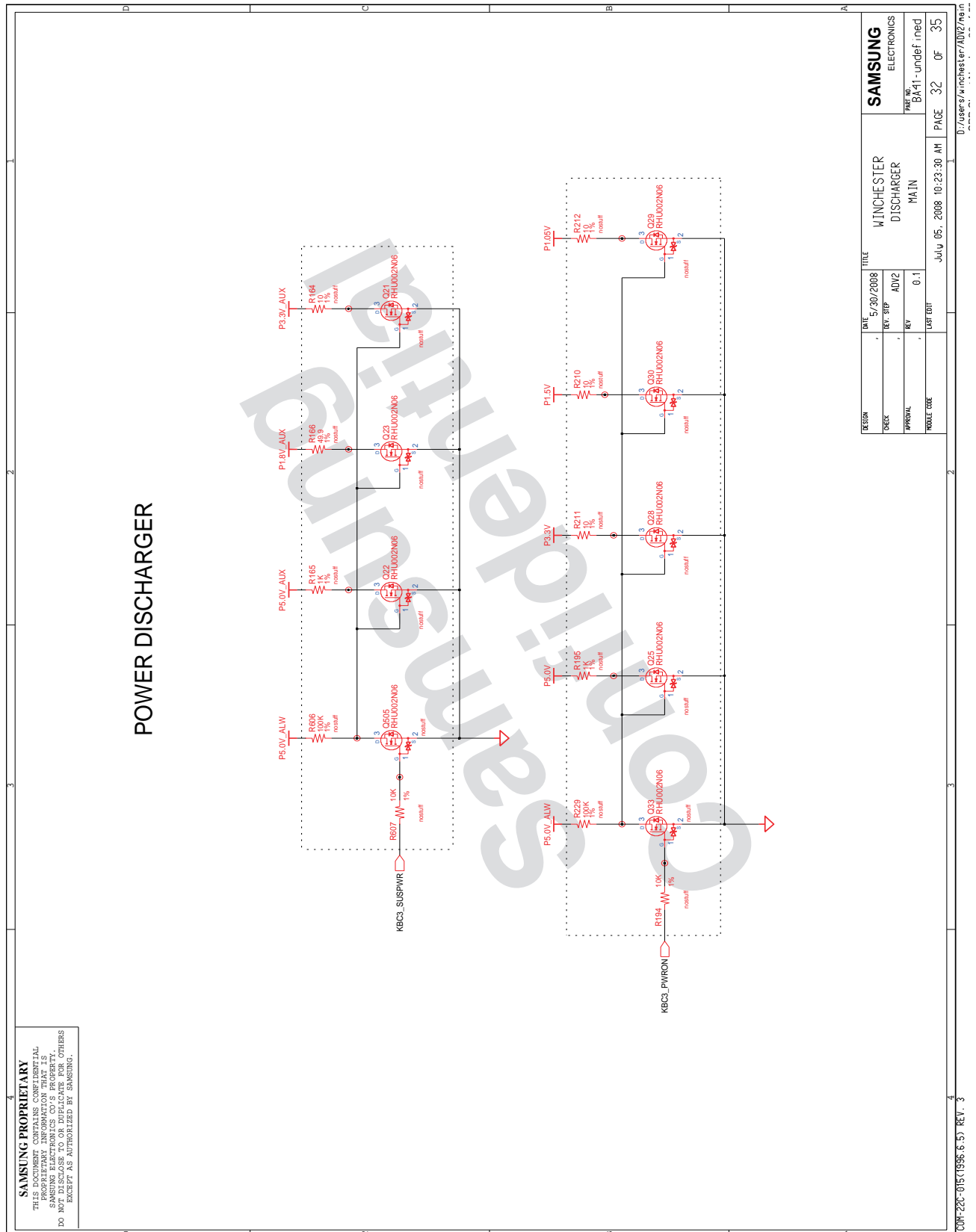
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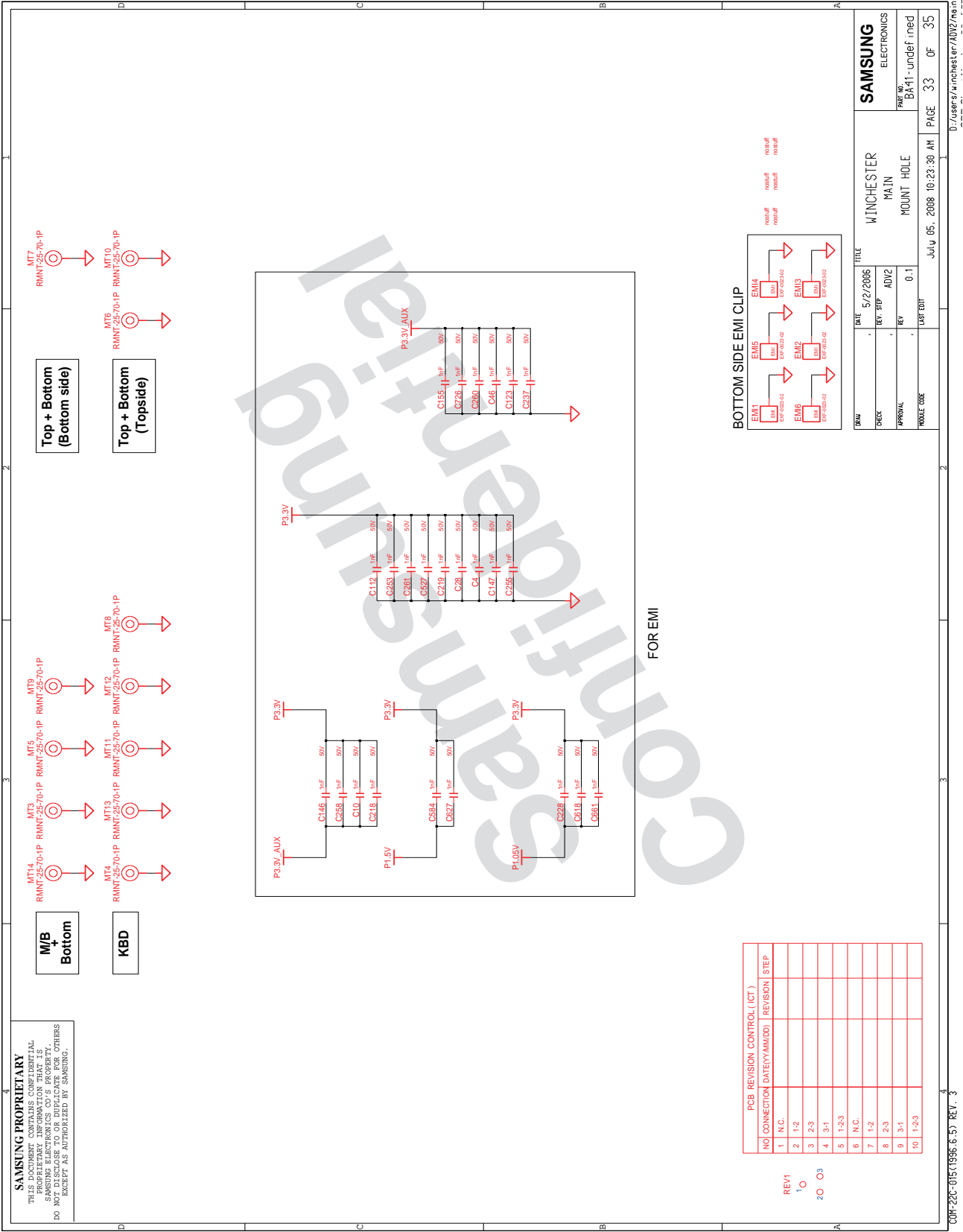
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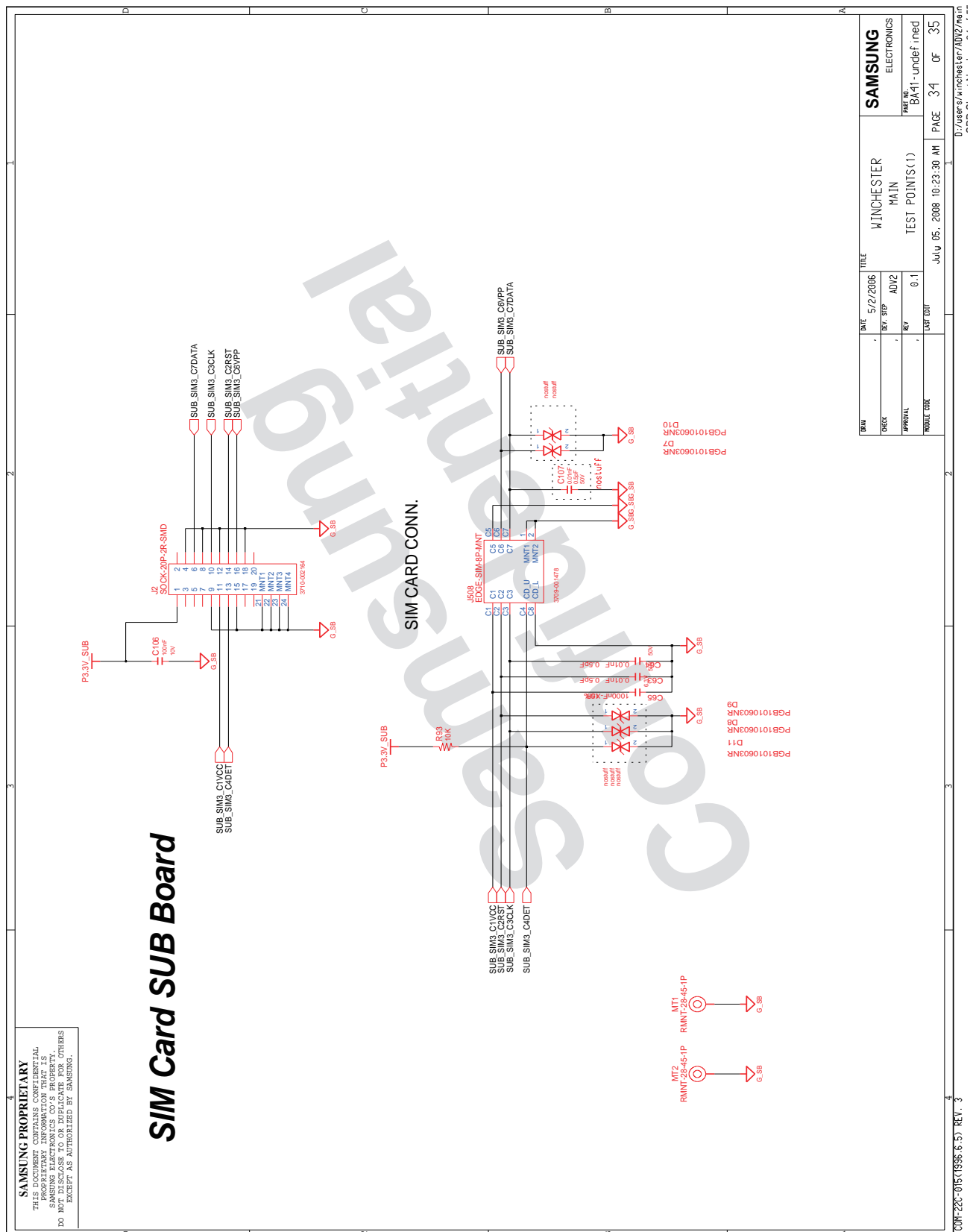
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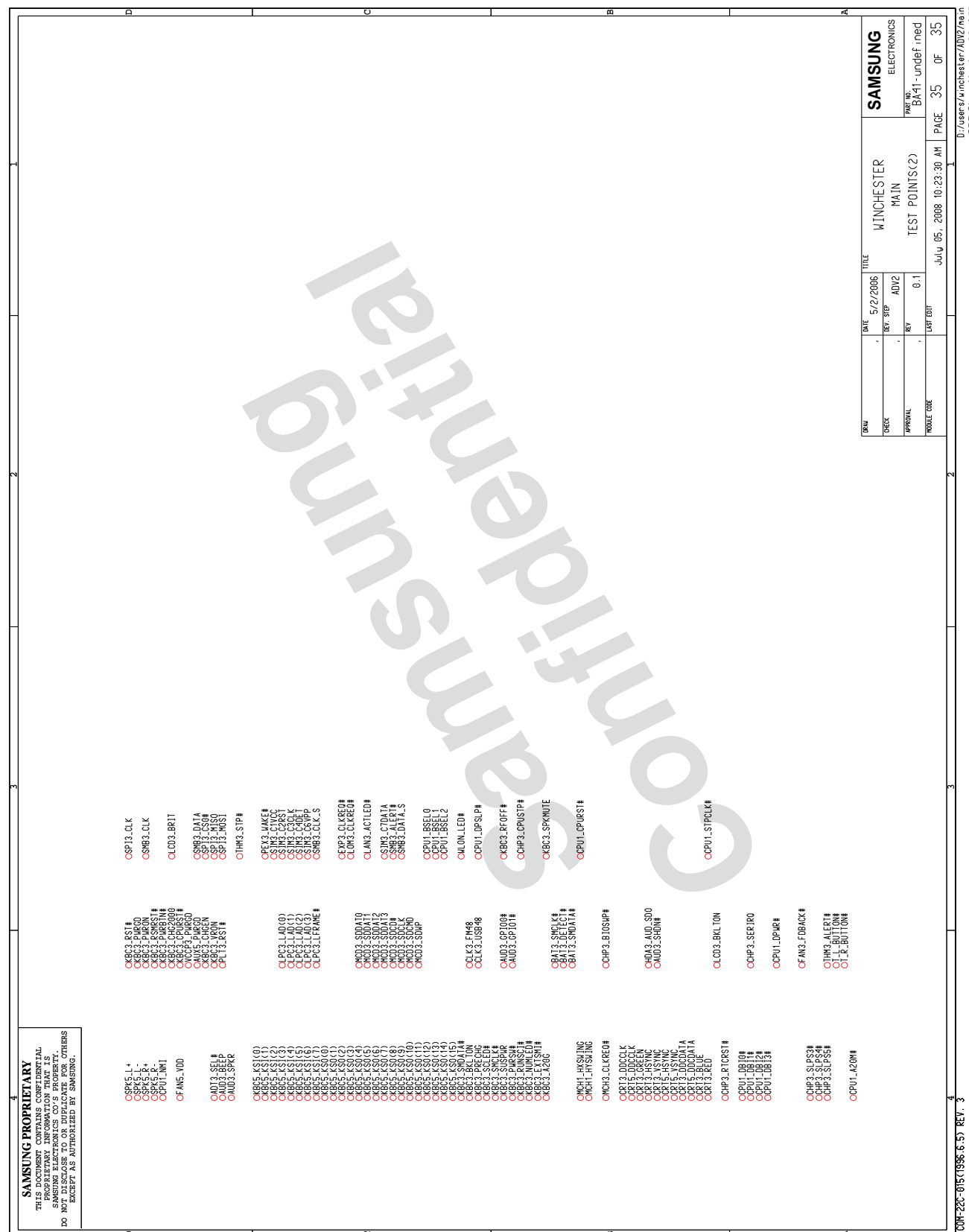
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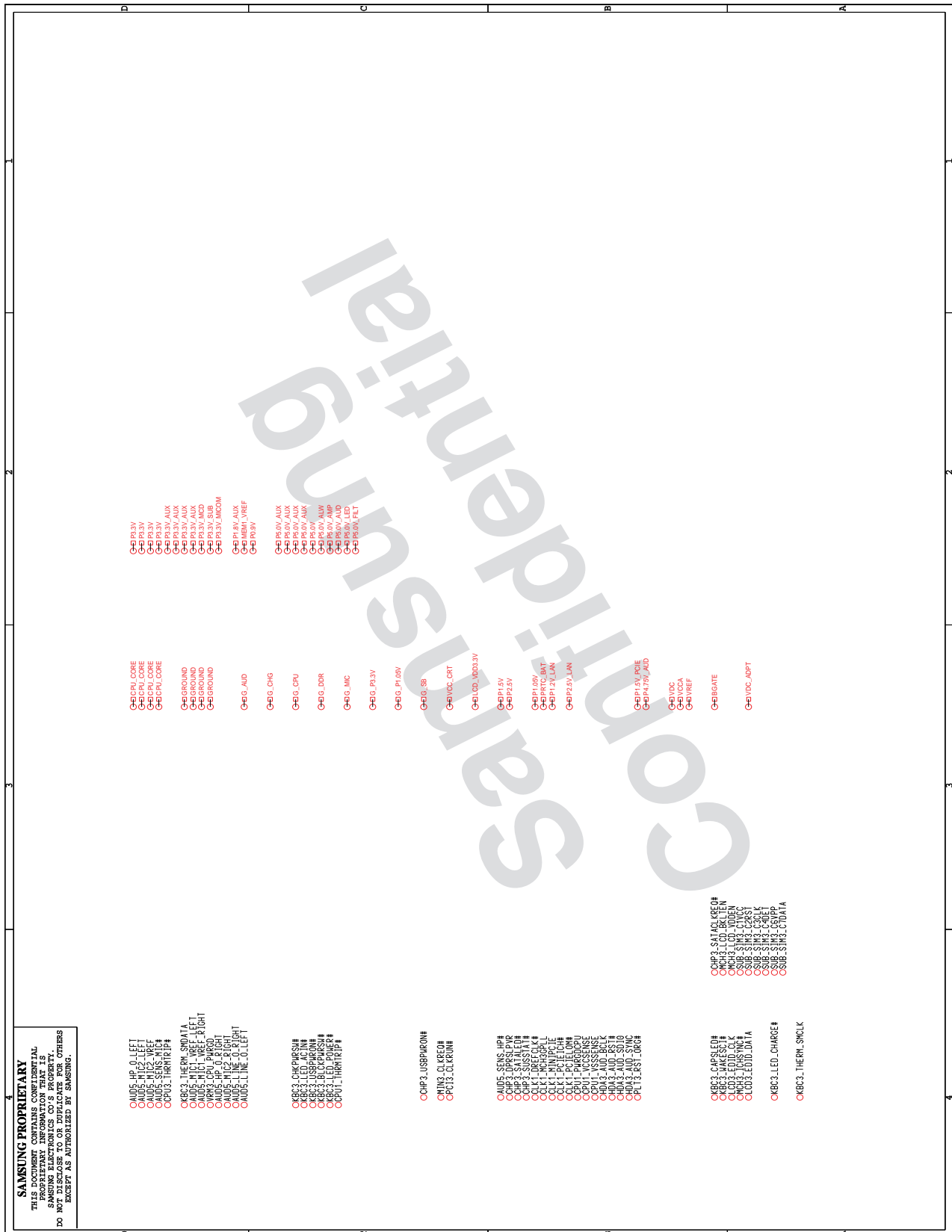
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- ## 8. Block Diagram and Schematic



- ## 8. Block Diagram and Schematic

# THERMAL SENSOR & FAN CONTROL



DATE	8/12/2006	TITLE	WINCHESTER	<b>SAMSUNG</b> ELECTRONICS 1 OF 1	
REV	REV	REV	REV		
CHECK	AD12	Thermal_Sensor_SWSC_Enc2102	Thermal_Sensor_SWSC_Enc2102		
APPROVAL	REV	0.1	Thermal_Sensor_SWSC_Enc2102		
NOUVEAU CODE	LEFT EDIT				
JUL 05, 2008 10:23:30 AM				PRICE	1

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- ## 8. Block Diagram and Schematic



## 8. Block Diagram and Schematic



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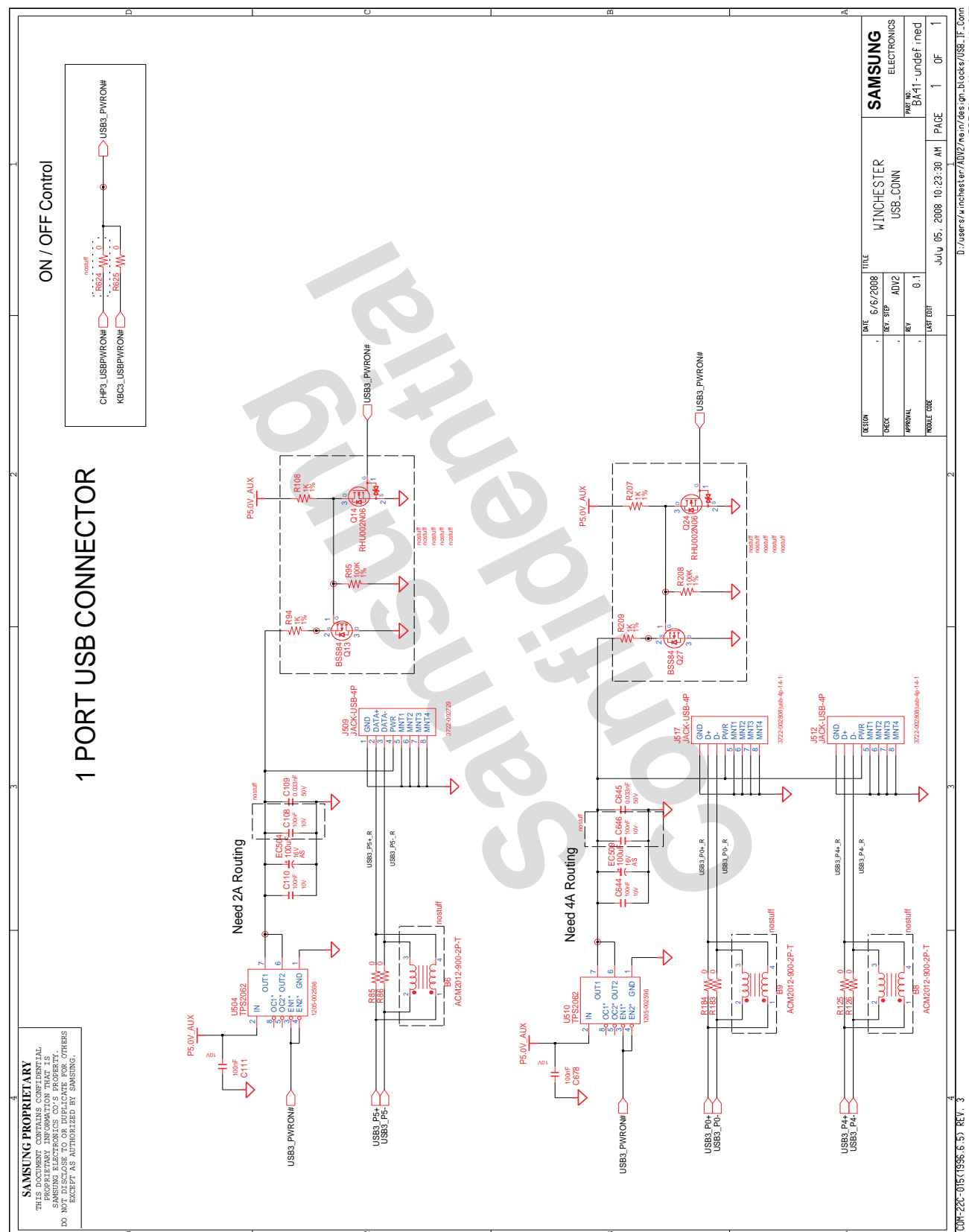


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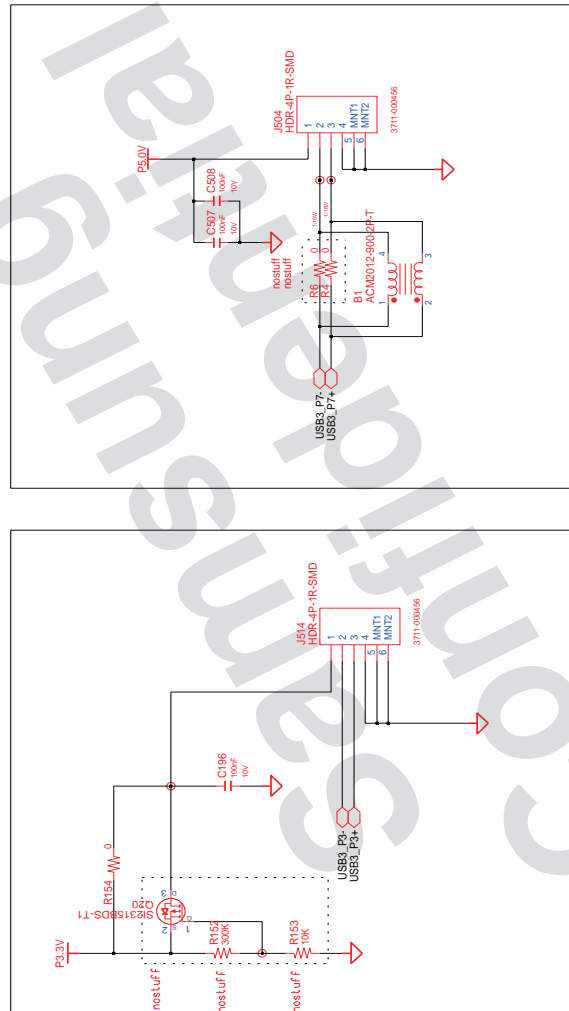
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## USB I/F Devices

# CAMERA

## Bluetooth Interface



REVISION	DATE	TITLE	<b>SAMSUNG</b> ELECTRONICS BK41+, undefined
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APPROVAL	REV	ADV2 0-1	
MODULE CODE	LAST EDIT		
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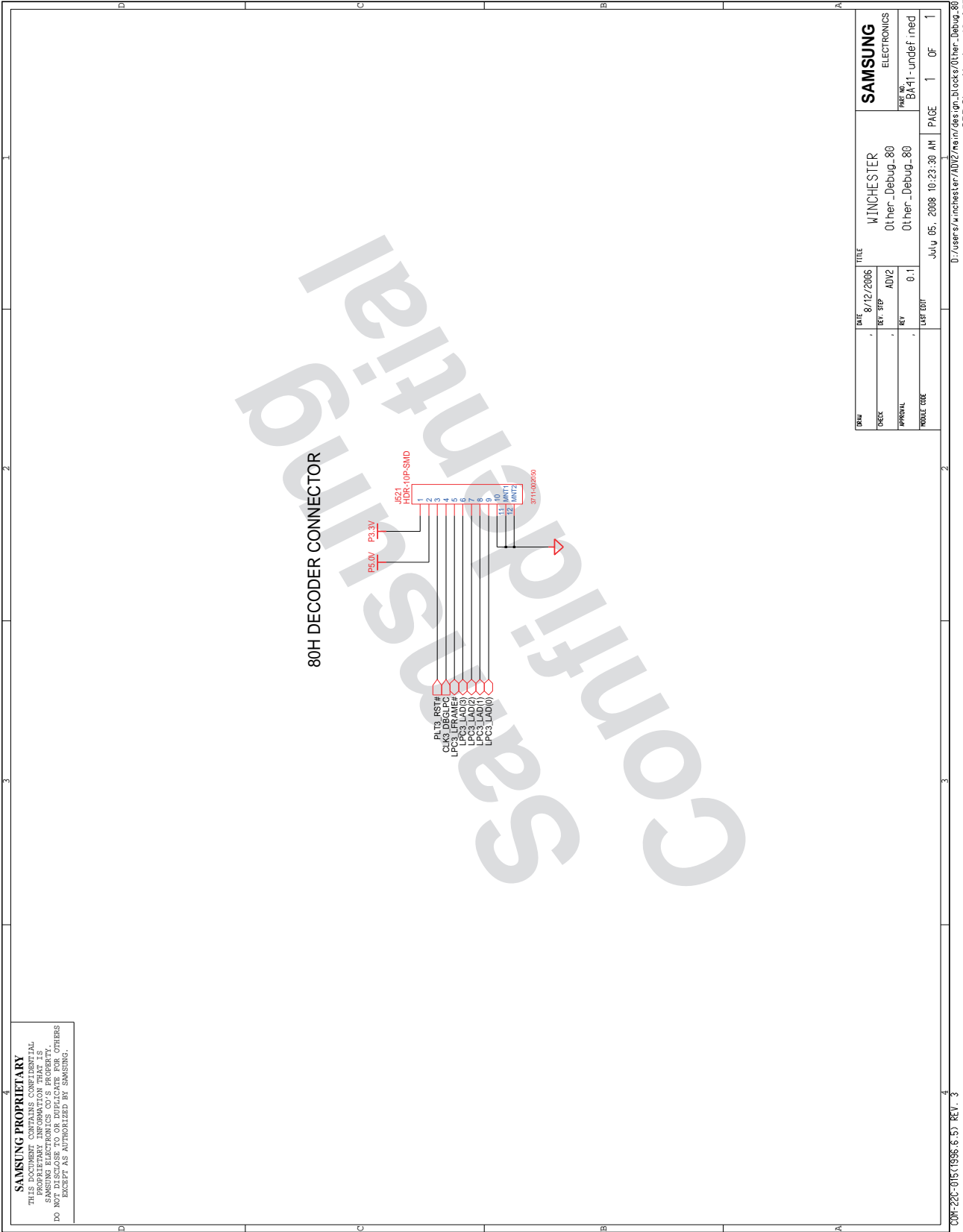
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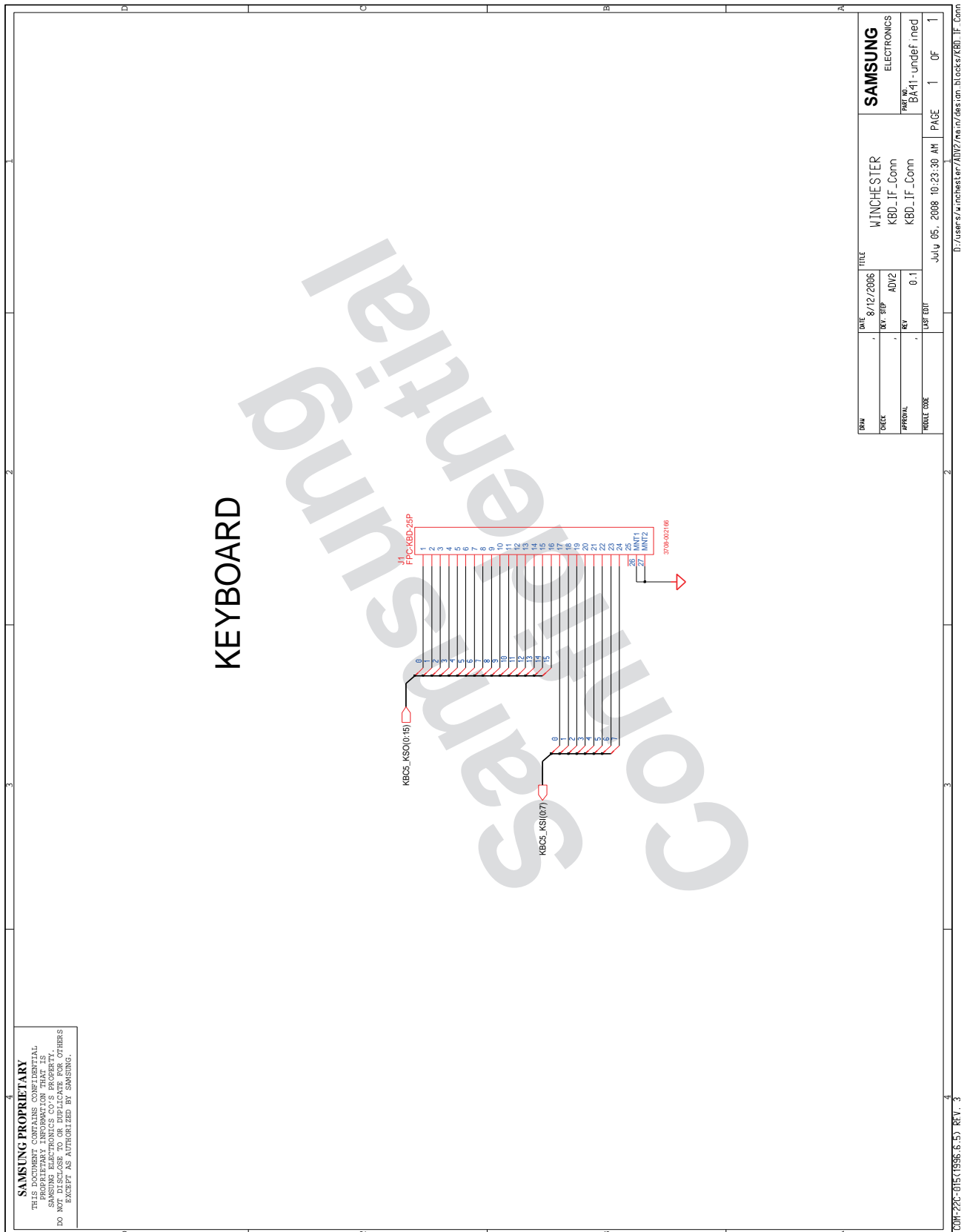


- ## 8. Block Diagram and Schematic



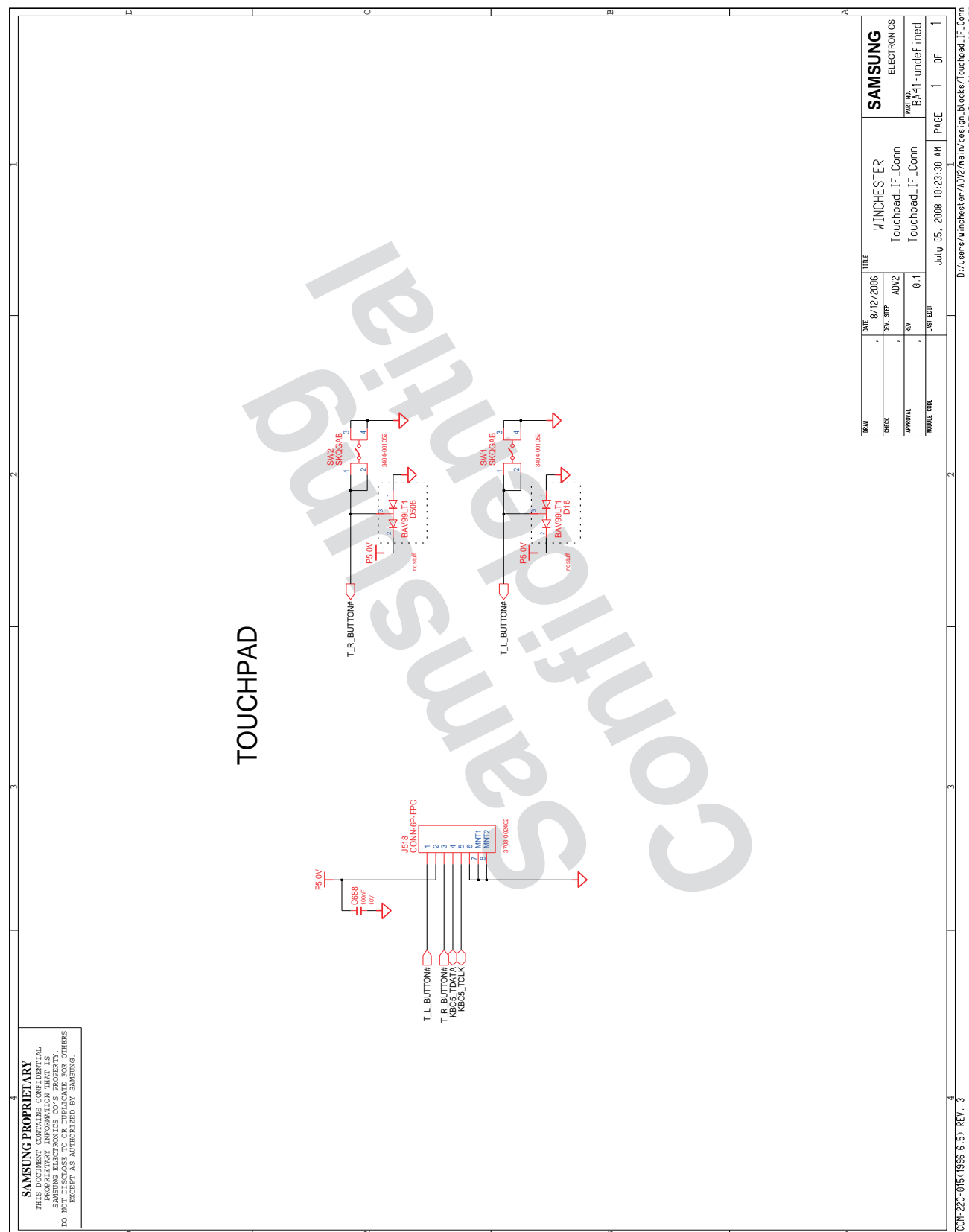
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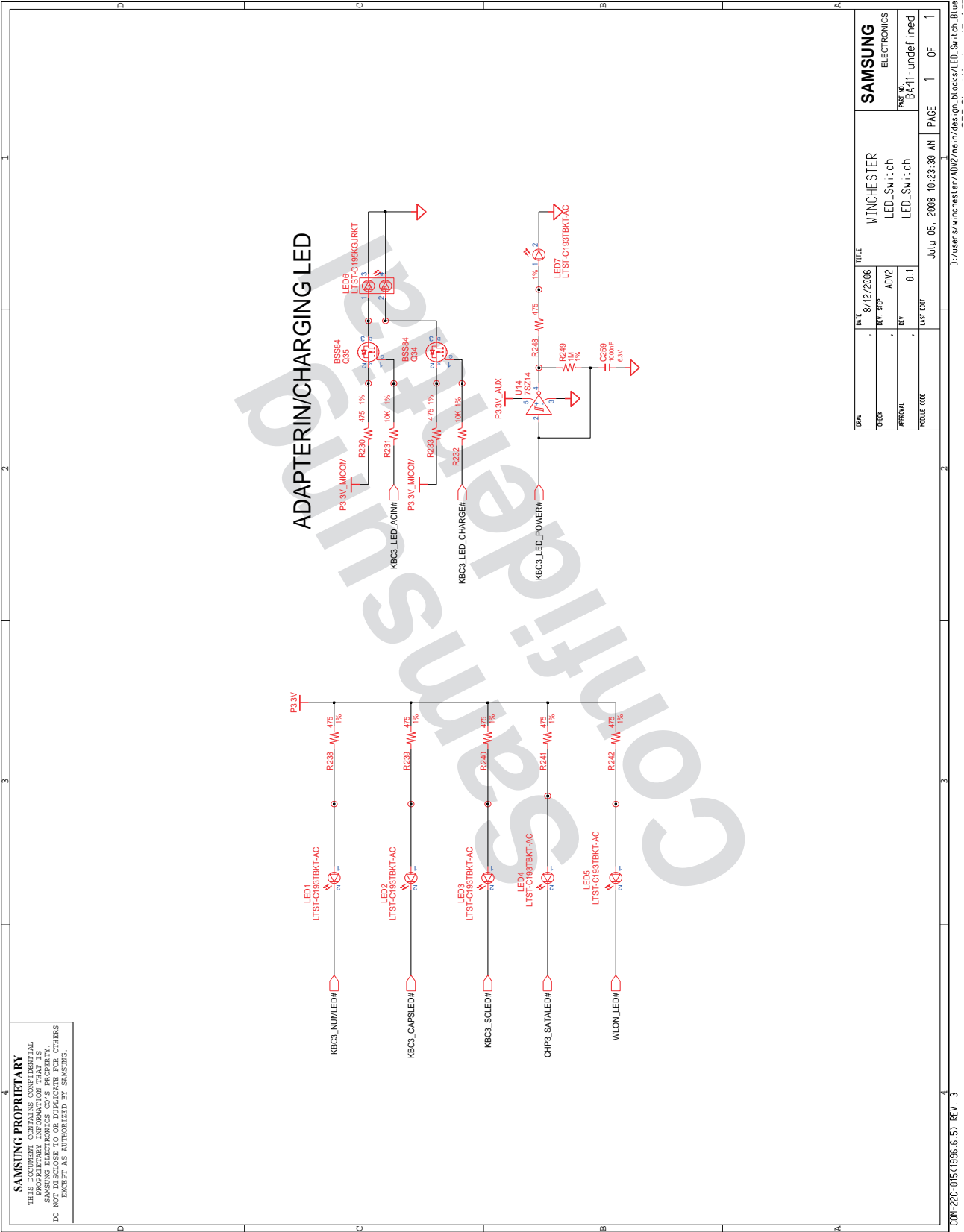


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## 8. Block Diagram and Schematic



8. Block Diagram and Schematic



- ## 8. Block Diagram and Schematic



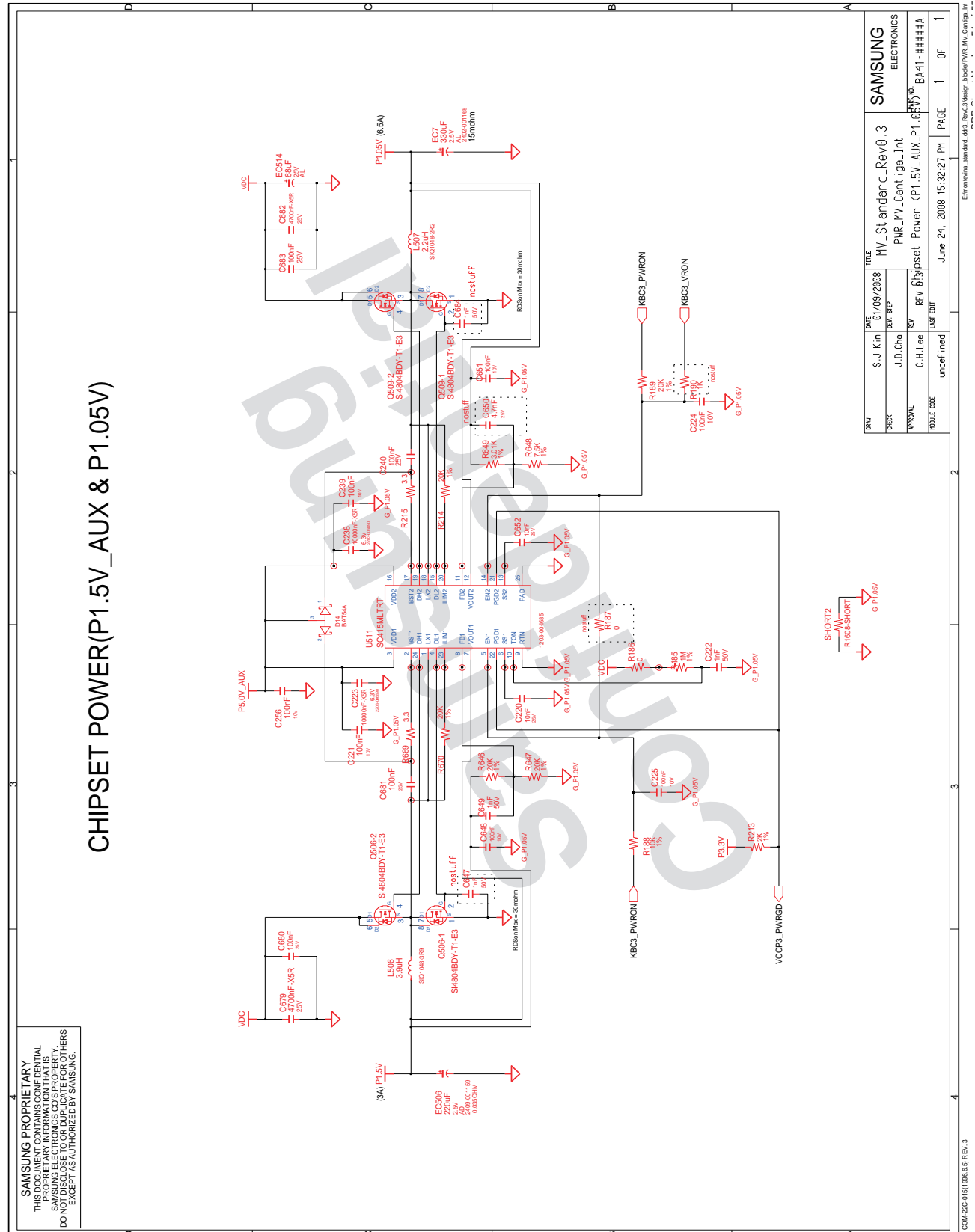




- ## 8. Block Diagram and Schematic



## 8. Block Diagram and Schematic



- ## 8. Block Diagram and Schematic

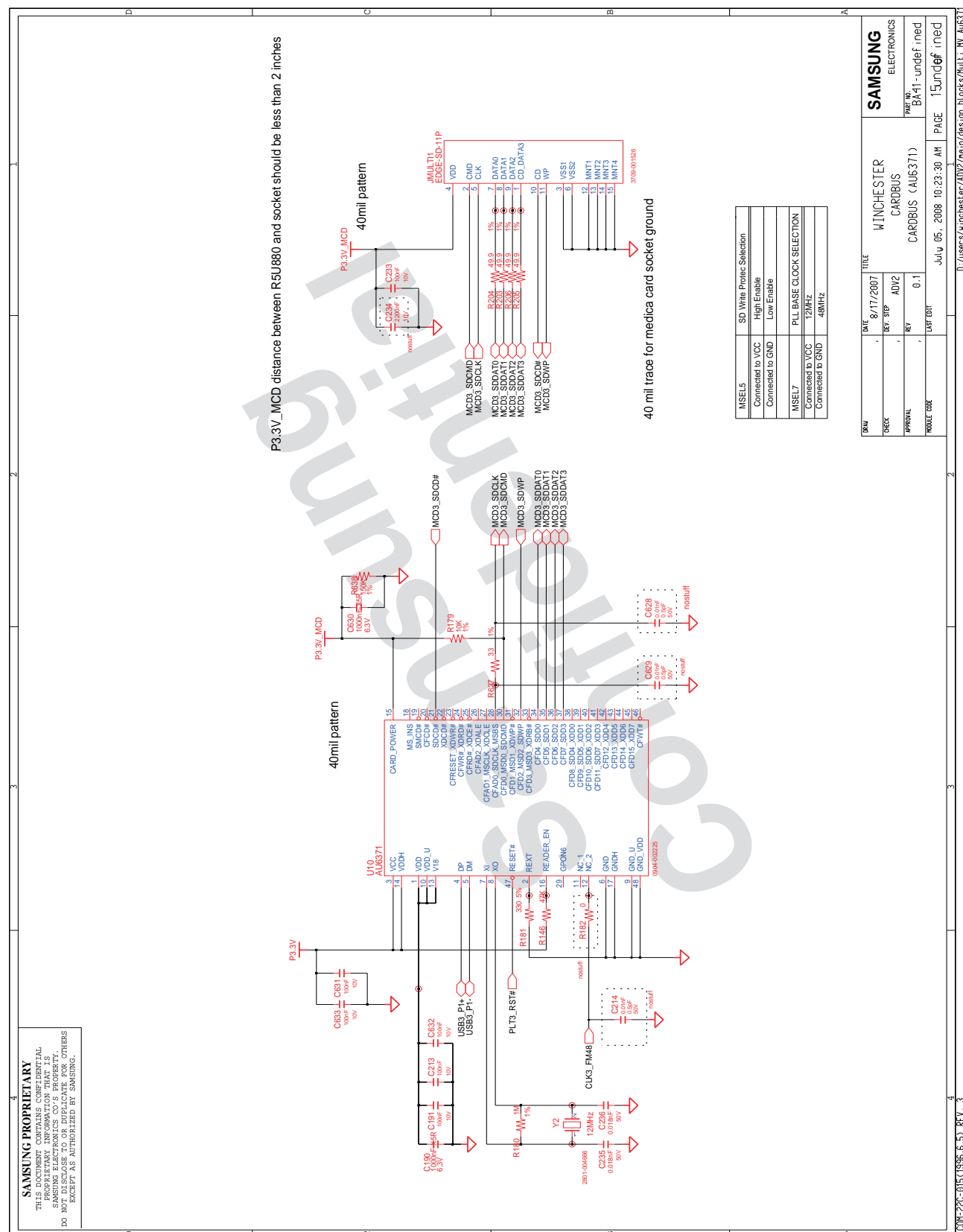


- ## 8. Block Diagram and Schematic

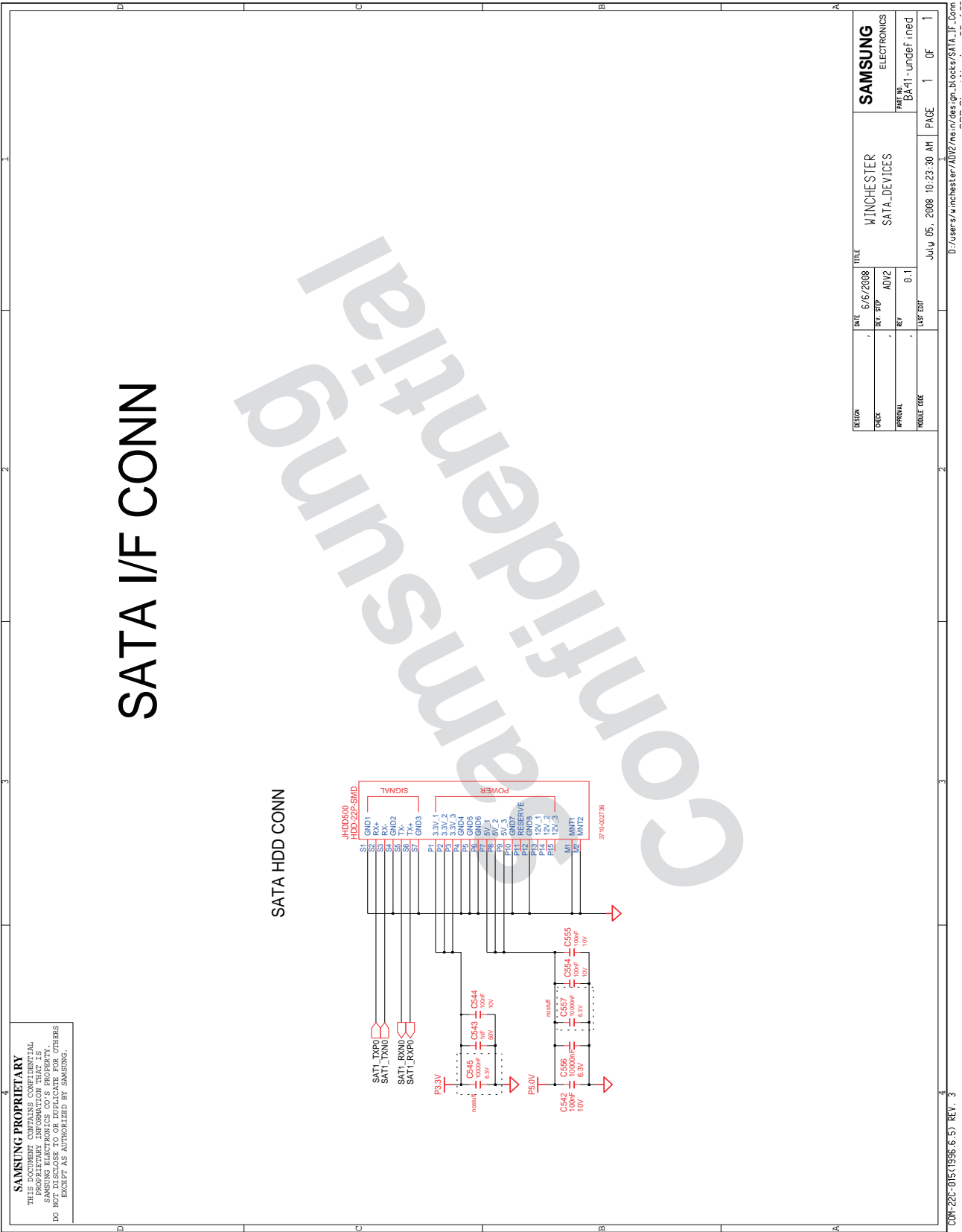


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## 8. Block Diagram and Schematic



8. Block Diagram and Schematic



## 8. Block Diagram and Schematic

08/21/108  
17:56:36

Index\_Page

1

Sheet51 ----- PWR\_MV\_Cantiga\_Int[sheet1]  
Sheet52 ----- PWR\_MV\_Charger\_Isi6256a[sheet1]  
Sheet53 ----- Mini\_PCIE\_Conn[sheet1]  
Sheet54 ----- Multi\_MV\_Au6371[sheet1]  
Sheet55 ----- SATA\_IF\_Conn[sheet1]

Sheet1 ----- Root[sheet1]  
Sheet2 ----- Root[sheet2]  
Sheet3 ----- Root[sheet3]  
Sheet4 ----- Root[sheet4]  
Sheet5 ----- Root[sheet5]  
Sheet6 ----- Root[sheet6]  
Sheet7 ----- Root[sheet7]  
Sheet8 ----- Root[sheet8]  
Sheet9 ----- Root[sheet9]  
Sheet10 ----- Root[sheet10]  
Sheet11 ----- Root[sheet11]  
Sheet12 ----- Root[sheet12]  
Sheet13 ----- Root[sheet13]  
Sheet14 ----- Root[sheet14]  
Sheet15 ----- Root[sheet15]  
Sheet16 ----- Root[sheet16]  
Sheet17 ----- Root[sheet17]  
Sheet18 ----- Root[sheet18]  
Sheet19 ----- Root[sheet19]  
Sheet20 ----- Root[sheet20]  
Sheet21 ----- Root[sheet21]  
Sheet22 ----- Root[sheet22]  
Sheet23 ----- Root[sheet23]  
Sheet24 ----- Root[sheet24]  
Sheet25 ----- Root[sheet25]  
Sheet26 ----- Root[sheet26]  
Sheet27 ----- Root[sheet27]  
Sheet28 ----- Root[sheet28]  
Sheet29 ----- Root[sheet29]  
Sheet30 ----- Root[sheet30]  
Sheet31 ----- Root[sheet31]  
Sheet32 ----- Root[sheet32]  
Sheet33 ----- Root[sheet33]  
Sheet34 ----- CK\_Clock\_505M\_Int[sheet1]  
Sheet35 ----- Thermal\_Sensor\_SMSC\_Emc2102[sheet1]  
Sheet36 ----- SODIMM\_DDR2[sheet1]  
Sheet37 ----- SPI\_BIOS\_ROM\_16Mbit[sheet1]  
Sheet38 ----- PCIE\_HSDPA[sheet1]  
Sheet39 ----- MICOM\_Renas2110\_100p[sheet1]  
Sheet40 ----- USB\_IF\_Conn[sheet1]  
Sheet41 ----- USB\_IF\_Devices[sheet1]  
Sheet42 ----- Other\_Debug\_80[sheet1]  
Sheet43 ----- Graphics\_IF\_CRT[sheet1]  
Sheet44 ----- MIO\_Switch[sheet1]  
Sheet45 ----- KBD\_IF\_Conn[sheet1]  
Sheet46 ----- Touchpad\_IF\_Conn[sheet1]  
Sheet47 ----- LED\_Switch\_Blue[sheet1]  
Sheet48 ----- LID\_Switch[sheet1]  
Sheet49 ----- PWR\_Memory[sheet1]  
Sheet50 ----- PWR\_MV\_3V\_5V[sheet1]