Revisiting the impedance matching for CS-LNA

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***Abstract*— This article reconsiders the impedance matching problem for common source CMOS LNA (CS-LNA) and proposes several improved equivalent models that take into account both C_{gd} capacitance and the type of load, resistive or inductive, normally not considered by the classical approach. These newly developed models might offer valuable insights about the input impedance, amplifier stability and quality of impedance matching, all these being of great interest in LNA design. The simulation results show good agreement, in terms of frequency response, between the proposed models and transistor based CS-LNA. Hence, it would justify further consideration of C_{gd} when designing the matching network while taking into account the load, as well. The analysis covered the frequency range 0.1-7 GHz.**

I. INTRODUCTION

The common source CMOS low noise amplifier (CS-LNA) has several advantages over common gate LNAs (CG-LNA) such as lower noise figure (NF) [1, 2] and higher gain values [3]. However, the price is not only narrower bandwidth but also difficult input impedance matching. In this regard, using on-chip gate and source inductors, as shown in Fig. 1, is already standard solution to match the input of CS-LNA to the output of the previous RF block. As mentioned in literature, most architectures make use of a third inductor (L_d), as load, to alleviate the amplifier gain decrease with frequency and for output impedance matching purpose.

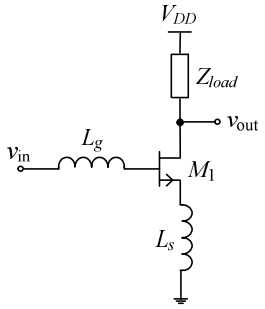

Figure 1. Common source CMOS LNA matched at the input.

As expressed by (1) and (2), the main benefit of using L_g and L_s is to convert the pure capacitive transistor input impedance into a resistance (ideally 50Ω) at the frequency of interest which is set by L_g, L_s and C_{gs}, where C_{gs} is the gate to source transistor parasitic capacitance and g_m is transistor transconductance.

$$Z_{in}(s) = s(L_g + L_s) + 1/sC_{gs} + g_m L_s / C_{gs} \qquad (1)$$

As can be noticed, L_s alone creates the resistive term while L_g, yet optional, is useful for gaining extra control of the resonant frequency.

The CS-LNA input impedance expressed by (1) and widely mentioned in literature, including RFIC/microwave books [4], conferences [5] and journals [6], seems to be sufficient for LNA design. In addition, this mathematical form can be uniquely obtained using the small signal model shown in Fig. 2.

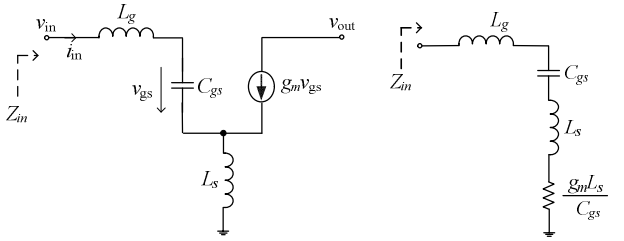

Figure 2. Small signal and equivalent passive models for CS matching.

However, as it can be noticed from both mathematical form and the above small signal equivalent model, the input impedance is evaluated with no output load and even with no gate to drain capacitance which is not realistic in RFIC design. Usually the CS transistor used as input stage of the LNA is quite large, hence C_{gd} becomes quite significant to deteriorate the amplifier frequency performances. In addition, the load always affects the input impedance even though the output can be more or less isolated of the input terminal (by using cascode transistor). Hence, the load should be taken into account when computing Z_{in}, a more realistic small signal model, as shown in Figure 3, being used in our study. In this regard, even though a small resistive load is used especially when targeting noise compensation in LNAs, as proposed in [7], an inductor is preferred in most CMOS LNAs for single stage [8] or multiple stages LNAs [9].

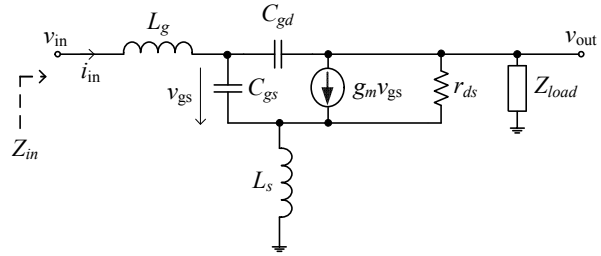

Figure 3. Complete small signal model for CS-LNA.

An extensive study of the CS-LNA input impedance is covered in this paper, with two cases discussed hereinafter (resistive and inductive load), equivalent passive models being developed and proposed.

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II. CS-LNA WITH RESISTIVE LOAD AND C_{GD}=0

This is the first case study investigated in our research, an equivalent passive model, similar to the series L-C-L branch expressed by (1), being developed. The small signal model used in this case study is shown in Figure 4, C_{gd} not being into account for simplicity. However, g_{ds} should have some negative effects on the LNA frequency behavior.

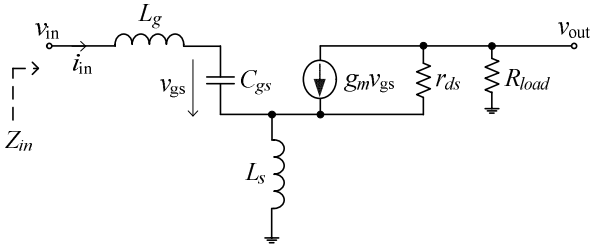

Figure 4. Complete small signal model for CS-LNA (w/ R_{load}).

The input impedance corresponding to the circuit shown above has the following form, as expressed by (2)-(4).

$$Z_{in}(s)=\frac{as^3+bs^2+cs+d}{sC_{gs}(sg_{ds}L_s+g_{ds}R_L+1)} \quad (2)$$

$$a=g_{ds}C_{gs}L_sL_g,\ c=g_{ds}L_s+g_mL_s,\ d=g_{ds}R_L+1 \quad (3)$$

$$b=C_{gs}(L_s+L_g)+g_{ds}R_LC_{gs}(L_s+L_g) \quad (4)$$

Since its equivalent passive model should be similar, to some extent, to the basic series L-C-L branch reported in literature (Figure 2), extracting L_g and C_{gs} should be the first steps when synthesizing $Z_{in}(s)$. After corresponding processing, $Z_{in}(s)$ has the final form as expressed by (5)-(7) while its equivalent model is shown in Figure 5.

$$Z_{in}(s)=sL_g+\frac{1}{sC_{gs}}+\frac{sL_s(R_L+1/g_{ds})}{sL_s+R_L+1/g_{ds}}+\frac{A}{B} \quad (5)$$

$$A=\frac{1}{sC_{gs}g_{ds}/g_m}\cdot\frac{g_mL_s}{C_{gs}(g_{ds}R_L+1)} \quad (6)$$

$$B=\frac{1}{sC_{gs}g_{ds}/g_m}+\frac{g_mL_s}{C_{gs}(g_{ds}R_L+1)} \quad (7)$$

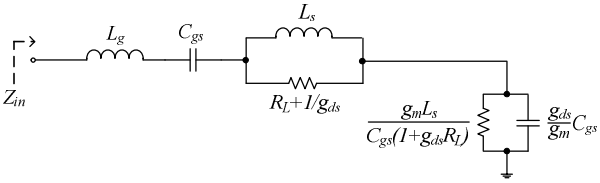

Figure 5. Proposed equivalent passive model for CS-LNA with resistive load.

Several major differences can be noticed and should be emphasized regarding this improved model:

- the classical model, consisting of L-C-L series branch, can be recognized in the first three elements of this scheme, hence the improved model is developed correctly;
- the equivalent model still remains a series branch, yet more complicated;
- R_L deteriorates the inductor quality factor of the source inductance L_s, this being more realistic since smaller values (< 1 kΩ) are used in most cases reported in literature;
- R_L decreases the resistance value seen at the input, which might be good taking into account that resistances as small as 50Ω are envisaged;
- the channel resistance r_{ds} has two side effects over the input resistance, decreasing its value while deteriorating its frequency behavior by inserting a "parasitic" parallel capacitor.

Since changing R_L value alters the transistor biasing, therefore making difficult the comparison between any two distinct particular cases in terms of stability and equivalent input resistance, this case study is limited to proposing this improved model only. However, since tuning the inductance value has no significant effect on transistor biasing, this particular case is extensively studied in the following sections.

III. CS-LNA WITH INDUCTIVE LOAD AND C_{GD}=0

This second case study considers inductive load for low noise amplifier whose equivalent small signal model is shown in Figure 6, C_{gd} being neglected for simplicity. Channel resistance is still considered.

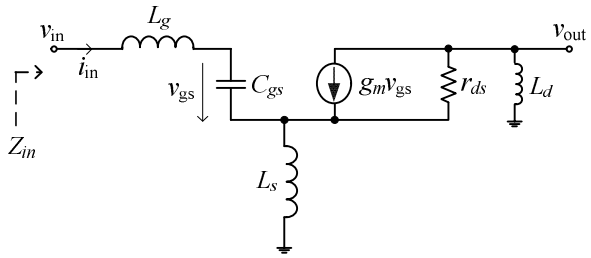

Figure 6. Small signal model for CS-LNA with inductive load (w/o C_{gd}).

The input impedance computed for this circuit has a mathematical form as expressed by (8)-(10), with a, b and c changed correspondingly. As it can be noticed, a supplementary 's' appears at denominator, due to the presence of the load inductance.

$$Z_{in}(s)=\frac{as^3+bs^2+cs+1}{sC_{gs}(s(g_{ds}L_s+g_{ds}L_d)+1)} \quad (8)$$

$$a=g_{ds}C_{gs}(L_sL_g+L_sL_d+L_gL_d),\ b=C_{gs}(L_g+L_s) \quad (9)$$

$$c=g_{ds}L_s+g_mL_s+g_{ds}L_d \quad (10)$$

Similar to the previous case, synthesizing Z_{in} should start with extracting C_{gs} and L_g first, further continuous fraction expansion conducting us to a mathematical form as expressed by (11)-(13), with A and B changed correspondingly. It has the equivalent passive model shown in Figure 7.

$$Z_{in}(s)=sL_g+\frac{1}{sC_{gs}}+\frac{sL_s(sL_d+1/g_{ds})}{sL_s+sL_d+1/g_{ds}}+\frac{A}{B} \quad (11)$$

$$A = \frac{g_m L_s}{C_{gs}} \cdot \frac{1}{sC_{gs}g_{ds}/g_m(1+L_d/L_s)} \quad (12)$$

$$B = \frac{g_m L_s}{C_{gs}} + \frac{1}{sC_{gs}g_{ds}/g_m(1+L_d/L_s)} \quad (13)$$

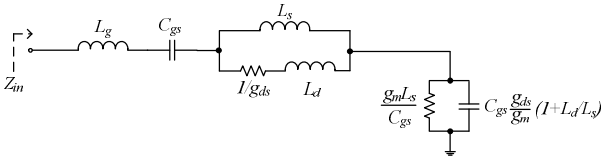

Figure 7. Proposed equivalent passive model for CS-LNA with inductive load (C_{gd}=0).

It is interesting to notice that L_d value affects the equivalent source inductance value, therefore requiring an extra optimization step during the circuit design.

IV. CS-LNA WITH INDUCTIVE LOAD AND $C_{GD}\neq 0$

The third and last case from our study takes into account the gate to drain capacitance C_{gd} which is by far closer to reality since CS transistor usually has larger size to accommodate high density current for lower noise figure, hence significant value for C_{gd}. The equivalent small signal circuit is updated as shown in Figure 8. For the sake of simplicity, the transistor output resistance is neglected, otherwise the input impedance becomes more complicated and difficult to synthesize.

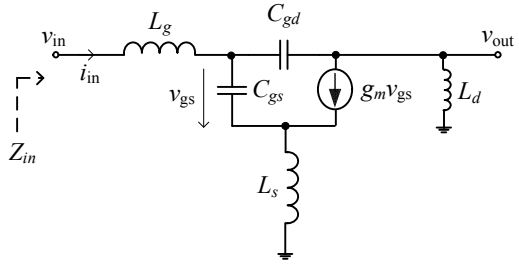

Figure 8. Small signal model for CS-LNA with inductive load (w/ C_{gd}).

Similarly to the previous cases, the input impedance is found as described by (14)-(18), with a, b and c changed correspondingly.

$$Z_{in}(s) = \frac{as^4 + bs^3 + cs^2 + sg_m L_s + 1}{s(ds^2 + es + C_{gs} + C_{gd})} \quad (14)$$

$$a = C_{gs}C_{gd}(L_s L_g + L_s L_d + L_g L_d) \quad (15)$$

$$b = g_m C_{gd}(L_s L_g + L_s L_d + L_g L_d) \quad (16)$$

$$c = C_{gs}(L_s + L_g) + C_{gd}(L_g + L_d) \quad (17)$$

$$d = C_{gd}C_{gs}(L_s + L_d), e = g_m C_{gd}(L_s + L_d) \quad (18)$$

As can be noticed, C_{gd} affects the amplifier performances, with the obvious effect of making $Z_{in}(s)$ more complicated and difficult to synthesize. However, based on previous experience, synthesizing Z_{in} gets easier if L_g and/or C_{gs} are extracted first. In this case, the first step consists of extracting L_g only which further imposes synthesizing a second impedance $Z'(s)$ seen at the gate input, as expressed by (19)-(21).

$$Z_{in}(s) = sL_g + Z'(s) \quad (19)$$

$$Z'(s) = \frac{fs^4 + gs^3 + hs^2 + sg_m L_s + 1}{s(ds^2 + es + C_{gs} + C_{gd})} \quad (20)$$

$$f = C_{gd}C_{gs}L_s L_d, g = g_m C_{gd} L_s L_d, h = C_{gd}(L_s + L_d) \quad (21)$$

Since the channel resistance is neglected for M_1 while C_{ds} capacitance is too small for inducing noticeable effects at the frequency of interest, it can be considered that there no RF path exists between drain and source terminals. Hence, the gate input impedance can be seen as two distinct parallel branches:

- a series one following the path $gate_{M1} - C_{gs} - source_{M1} - L_s$ – ground with input impedance Z_1';
- a series one following the path $gate_{M1} - C_{gd} - drain_{M1} - L_d$ – ground with input impedance Z_2'.

Consequently, it can be considered that:

$$Y'(s) = \frac{1}{Z'(s)} = Y_1'(s) + Y_2'(s) \quad (22)$$

These admitances are found to have the following values, with expected form for Y_2' as expressed by (24):

$$Y_1' = \frac{s^2 C_{gs}C_{gd}L_d + sC_{gd}g_m L_d + C_{gs}}{(s^2 C_{gd}L_d + 1)(s^2 C_{gs}L_s + sg_m L_s + 1)} \quad (23)$$

$$Y_2' = \frac{1}{sL_d + 1/sC_{gd}} \quad (24)$$

By using (23) and (24) to evaluate and synthesize $Z'(s)$ instead of (20) while applying continuous fraction expansion, a new impedance form is achieved as follows.

$$Z'(s) = sL_s + \frac{1}{\frac{1}{1/sC_{gs}} + \frac{1}{z_1 + z_2 + z_3}} \quad (25)$$

$$z_1 = \frac{C_{gd}L_d}{g_m(C_{gd}L_d - C_{gs}L_s)}, \quad z_2 = \frac{L_s}{s(C_{gd}L_d - C_{gs}L_s)} \quad (26)$$

$$z_3 = \frac{1}{s^2 g_m(C_{gd}L_d - C_{gs}L_s)} \quad (27)$$

Some simplifications can be further processed as expressed by (28)-(31).

$$k = C_{gd}L_d - C_{gs}L_s \quad (28)$$

$$z_1 = \frac{C_{gd}L_d}{kg_m} = \frac{1}{g_m} \cdot \frac{C_{gd}L_d}{k} = r_1 \quad (29)$$

$$z_2 = \frac{L_s}{sk} = \frac{1}{s\frac{k}{L_s}} = \frac{1}{sC_{eq}} \quad (30)$$

$$z_3 = \frac{1}{s^2 kg_m} \rightarrow z_3(\omega) = -\frac{1}{g_m} \cdot \frac{1}{\omega^2 k} = -r_2(\omega) \quad (31)$$

It follows that the equivalent passive model of the CS-LNA with inductive load, shown in Figure 9, has a ladder (Cauer) like topology, with series and parallel elements or branches. In

addition, it contains a frequency dependent nonlinear (negative) resistance which could affect the circuit stability for certain particular cases.

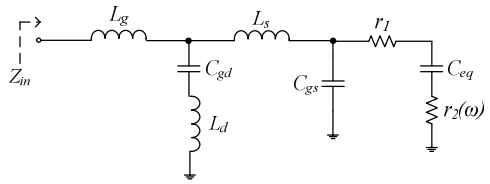

Figure 9. Proposed equivalent passive model for CS-LNA with inductive load (w/ C_{gd}).

V. Simulation Results

The basic CMOS LNA architecture shown in Figure 1 has been simulated in a 0.18um CMOS process, with circuit parameters chosen as close as possible to real case (W/L=100um/0.18um, L_g=5 nH, L_d=3 nH, L_s=0.35nH, V_{DD}=1.8 V). The transistor parameters were extracted from Cadence environment and used to size the proposed passive networks together with the classical one at 7 particular frequencies, the input resistance being of interest. The CMOS implementation showed a frequency dependence of the input impedance as sketched in Figure 10, good matching being noticed at 4.9 GHz (Figure 11).

TABLE I. Input Resistance: Computed vs. Simulated (CMOS)

Model	Frequency [GHz]						
	0.1	***0.5***	***1***	***2***	***3***	***5***	***7***
CMOS (simulated)	52.6	**-22.2**	**-13.7**	**20.5**	**39.1**	**53.4**	**58**
Classic (computed)	117.3	117.3	117.3	117.3	117.3	117.3	117.3
Model 1 (computed)	117.3	116.8	115.3	111.6	108.9	106.3	105.4
Model 2 (computed)	-33.4	**-26.9**	**-11.1**	**19.4**	**37.2**	**52**	**57.4**

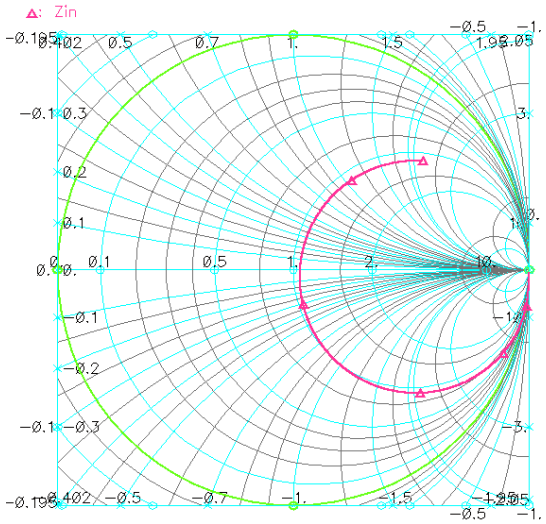

Figure 10. Input impedance variation for CMOS implementation in the frequency range 0.1-7 GHz

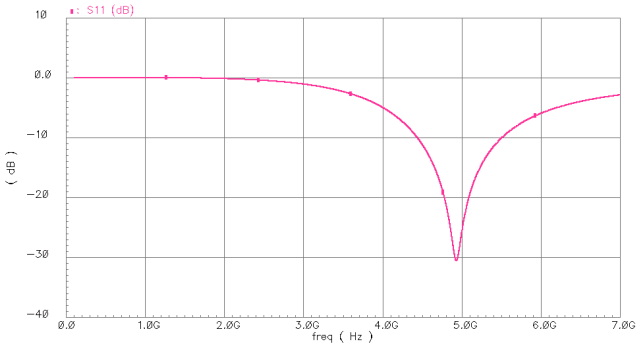

Figure 11. S_{11} for CMOS implementation in the frequency range 0.1-7 GHz (input matched at 4.9 GHz)

VI. Conclusion

The input impedance matching has been reconsidered for common source CMOS LNA and improved models were developed and proposed in this paper. Simulation results show good agreement between frequency performances and transistor based implementation, justifying further consideration of C_{gd} when designing matching network while taking into account the load (inductive or resistive) as well.

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