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A 3.55 dB NF Ultra-Compact Noise-Optimized LNA for 5G mm-Wave Bands in 65nm CMOS

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***Abstract*—A noise-optimized LNA at 30GHz for 5G millimeter-wave bands is designed in this paper. The focus is on the optimization of the input device for noise performance and reducing the difference between noise figure (NF) and minimum noise figure (NFmin). The conventional approach of input biasing that maximizes f_T/f_{max} to improve noise figure is found to be sub-optimal. The dependence of NF, NFmin and noise-optimum impedance (Z_{opt}) on the input transistor is studied and the existence of an optimal biasing point is demonstrated and explained. The dependence of Z_{opt} on the gate inductor is exploited to bring NF closer to NFmin. A two stage cascode LNA is designed at 30GHz in a commercial 65nm CMOS process. Having a core area of 0.42x0.32mm^2, the LNA achieves 22.3dB gain and 3.55dB noise figure at a DC power consumption of only 7mW.**

***Index Terms*—mm-wave LNA, low noise amplifier, noise optimum biasing, 5G LNA.**

I. INTRODUCTION

The fifth generation (5G) of mobile communication technology offers enhanced bandwidth to deal with high data rates and user density, massive connectivity and ultra-reliable and low latency communications. The mm-wave frequency bands ranging from 24-40GHz support high bandwidth yielding high data rates upto 10Gbps. As a result of continuous scaling, unity-current-gain frequency (f_T) and maximum oscillation frequency (f_{max}) have increased which enable the mm-wave integrated circuits to be fabricated in CMOS technology. This enables low-cost, low-power and compact solutions as CMOS offers higher level of integration of RF, analog and digital blocks on the same die to realize true SoCs.

The Low Noise Amplifier (LNA) is one of the most critical block in a transceiver and its performance is characterized by different metrics such as NF, gain, linearity, power dissipation and input/output matching. A two stage inductively-degenerated CS LNA presented in [1] uses f_T and f_{max} plots to determine the width and current density of transistors. A series inductor at the drain-source interconnection of CS and CG transistors tune out the parasitic capacitance. The series inductor is optimized to maximize f_T of cascoded LNA. In [2], a single-ended capacitive feedback neutralization (SCFN) technique is used to improve overall transducer gain. But it necessitates the design of neutralization capacitance equal to gate-drain capacitance of transistor. Transformer based matching techniques introduces undesired parasitics due to poor coupling factor. Transmission line based matching employed in [3] utilizes a round table layout for transistors to reduce gate resistance, thereby increasing the f_{max} of the transistor. Coplanar waveguide (CPW) structures used in matching networks limit the usage in low footprint applications.

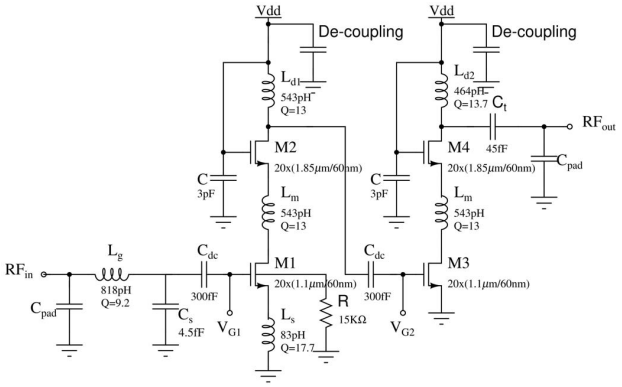

Fig. 1: Schematic of proposed LNA

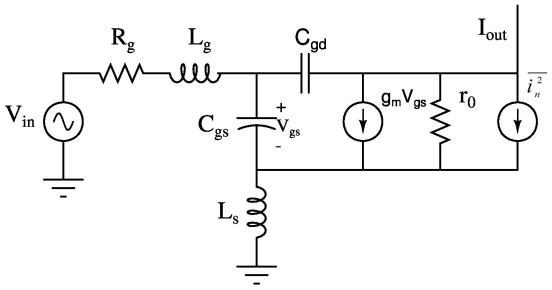

Fig. 2: Simplified small-signal noise model of input section.

Most published literature focuses on optimizing for f_T/f_{max} while designing the input transistor. Therefore, it is imperative to study the noise behavior of mm-wave LNAs to analyse whether maximizing f_T/f_{max} is coincidental with best achievable noise figure. This paper focuses on the impact of transconductance of input transistor on NF, NFmin and noise optimal impedance (Z_{opt}), thus paving way for the design of a noise-optimized LNA. Section II explains the noise optimization methods. Section III discusses the circuit design and implementation techniques. Section IV discusses the simulation results and comparisons.

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II. NOISE-OPTIMIZATION OF INPUT TRANSISTOR

A two stage LNA employing a cascode topology shown in Fig. 1 uses an inductively degenerated common source (IDCS) configuration at the input. A degenerating inductor at the source of the input CS transistor along with a pi-network at the gate of transistor forms the input matching network. The first stage components namely input transistor and series inductor being major noise contributors, their optimization affects the performance of the LNA. Figure 2 shows the simplified small-signal noise model of input section. A smaller series resistance will reduce the noise contribution of inductor. Hence the inductors are optimised for high Q-factor.

The classical textbook equations of noise figure predict a monotonic behaviour with respect to transconductane of input transistor.

$$NF = 1 + g_m Rs\gamma \left(\frac{f_o}{f_T}\right)^2 \tag{1}$$

$$\omega_T = \frac{g_m}{C_{gs}} \qquad ; \omega_T = 2 * \pi * f_T \tag{2}$$

$$NF \propto \frac{C_{gs}^2}{g_m} \tag{3}$$

NF is inversely proportional to g_m and is proportional to C_{gs}^2. Thus textbooks conclude that a higher g_m, achieved through a lower device dimension result in the best noise figure and the monotonic behaviour is only limited by the achievable value of series gate inductor. Hence the reported literature focus on designing the transistor, both current density and width for maximum f_T/f_{max}.

Figure 3 plots f_T and f_{max} with respect to finger width and gate-source voltage of the input transistor. A finger width (W_f) of 1.1μm, number of fingers (N_f) of 20 and gate-source voltage (V_{gs}) 750mV is observed to provide maximum of f_T and f_{max}. The f_T and f_{max} obtained are 155GHz and 165GHz respectively.

Noise spectral current density ($\overline{I_n^2}$) of a transistor is proportional to its transconductance (g_m).

$$\overline{I_n^2} = 4KT\gamma g_m \tag{4}$$

Noise performance of the two stage LNA matched to 50Ω is analysed for its dependence on the transconductance of the input transistor. As transconductance is a function of width and gate-source voltage, NF and NFmin is analysed for varying widths and gate-source voltages.

Each point in Figs. 4-5 represents an LNA which has been matched to a 50Ω input source impedance. In Fig. 4, the transconductance of the input transistor is changed by scaling the width of the transistor while retaining the bias voltage constant. The finger width (W_f) of the transistor is varied while keeping the number of fingers (N_f) 20 as obtainted from f_T and f_{max} plots. The passive components consisting of series gate inductor (L_g), source inductor (L_s) and load inductor (L_{d1}) have been designed such that the input match is obtained for each LNA represented by a point in the figures. This analysis shows that there is an optimal finger width which yields the best noise figure and the best NFmin. In Fig. 5, the transconductance of the input transistor is varied by changing

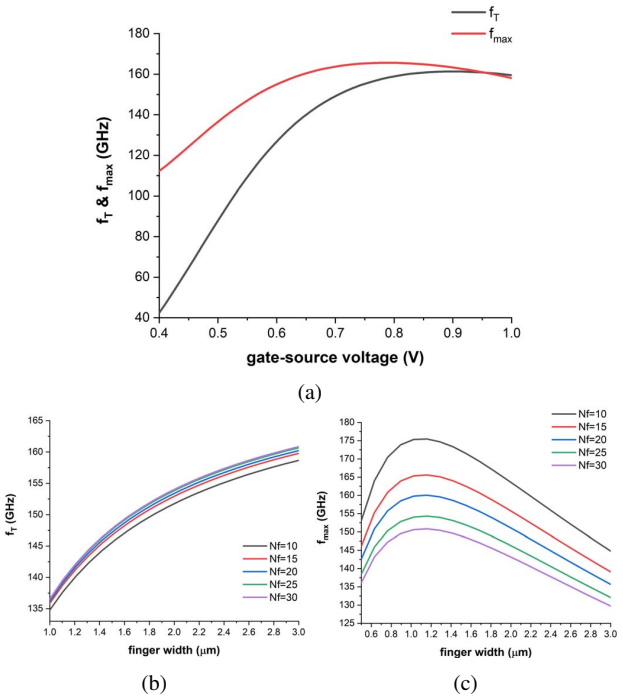


Fig. 3: (a) Simulated f_T and f_{max} as a function of V_{gs}. (b) Simulated f_T as a function of finger width. (c) Simulated f_{max} as a function of finger width.

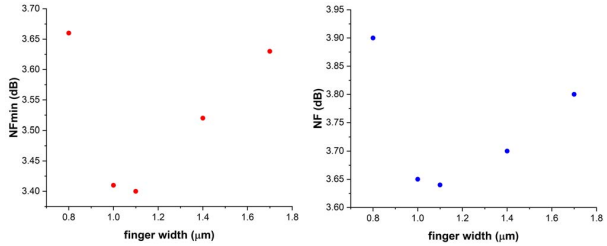


Fig. 4: NFmin and NF as a function of finger width ($N_f = 20$).

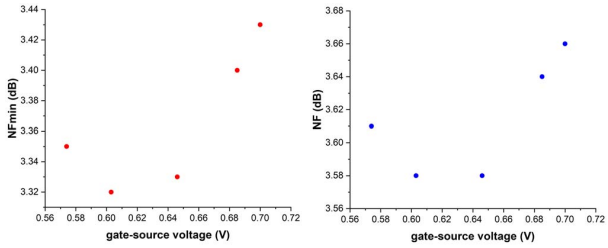


Fig. 5: NFmin and NF as a function of gate-source voltage.

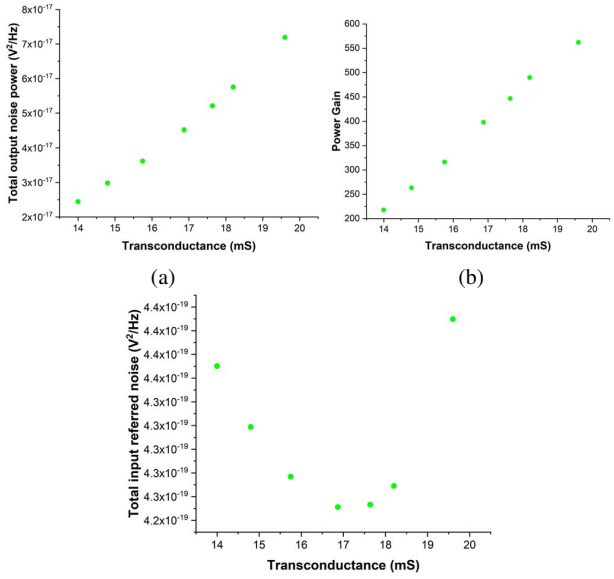


Fig. 6: (a) Total output noise power (b) Power gain (c) Total input referred noise as a function of transconductance.

the bias voltage and keeping the dimensions constant. The optimal finger width of 1.1μm from the previous analysis is chosen. The other passive elements, series gate inductor (L_g) and load inductor (L_{d1}) are tuned such that the input matching is achieved for each LNA represented by a point in the graph. The cascode transistor is also appropriately scaled to handle the bias current. It is observed from the design exercise that both NF and NFmin vary with the transconductance and both achieve a minimum value at a given transconductance. Hence there exists an optimum transconductance of the input transistor which provides the best noise performance for IDCS LNA.

The finger width, number of fingers and gate-bias voltage obtained for best f_T or f_{max} are 1.1μm, 20 and 750mV respectively. The optimum values obtained from above analysis are 1.1μm, 20 and 620mV. These optimum values are not coincident with the biasing which provides the best f_T or f_{max}. The reason behind this interesting result is explained as follows. Figure 6 plots the total output noise power, power gain and input referred noise as a function of transconductance. Total output noise power and power gain increase with increase in transconductance, but rate of increase is different. Therefore, input referred noise achieves a minimum value which validates the existence of optimum transconductance for the noise figure of the LNA.

III. DESIGN OF NOISE-OPTIMIZED LNA

The LNA achieves minimum noise figure when the input impedance is equal to noise optimum input impedance (Z_{opt}). This is achieved by designing an optimised series gate inductor which tunes out the capacitive component at the input. The

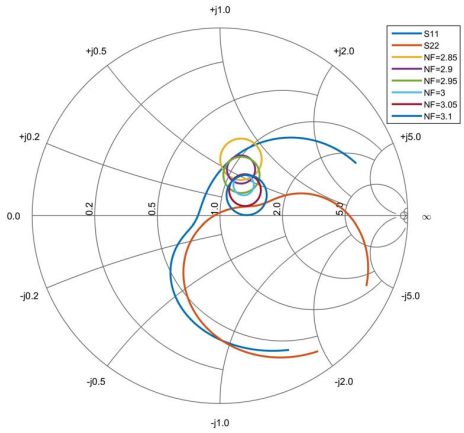


Fig. 7: Smith Chart of S_{11} and S_{22} and the variation of noise-optimal impedance circle with L_g.

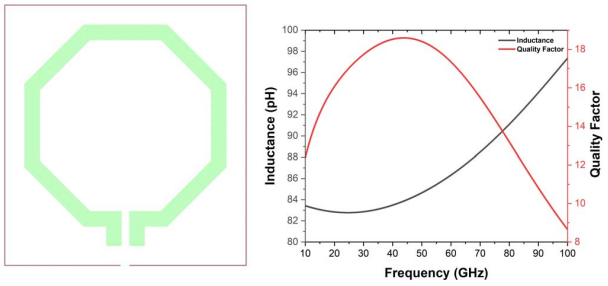
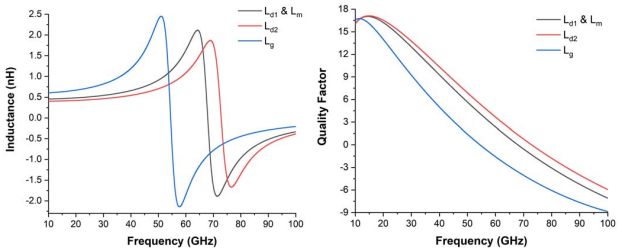


Fig. 8: (a) Layout of source inductor (L_s). (b) Inductance and Quality Factor as a function of frequency.

figure 7 plots Smith's chart showing the movement of optimum input impdance (Zopt) circle with varying series gate inductor (L_g).

The S_{11} and S_{22} plots are overlaid with the Z_{opt} circles. The goal is to attain Z_{opt} closer to 50Ω. The series gate inductor (L_g) is optimized such that the LNA achieves very small difference between NF and NFmin while maintaining good input matching.

The load inductor of first and second stage is designed such that the parasitic capacitance at that node is cancelled. Both stages use an intra-stage inductor (L_m) between the drain of input transistor and the source of the cascode transistor is used to tune out the parasitic capacitance at that node.The impedance seen at the inter-stage node is reflected back to the input through the C_{gd} of the input transistor. Similarly the inter-stage impedance affects the output matching. Hence the interstage inductor is designed such that the input and output reflection co-efficients (S_{11} and S_{22}) have a resonant behaviour at 30 GHz. MIM and MOM capacitors are optimized for ac coupling and output conjugate matching. The matching network incorporates the capacitive effects of RF pads, which



(a) (b)

Fig. 9: (a) Inductance (b) Quality Factor of the inductors as a function of frequency.

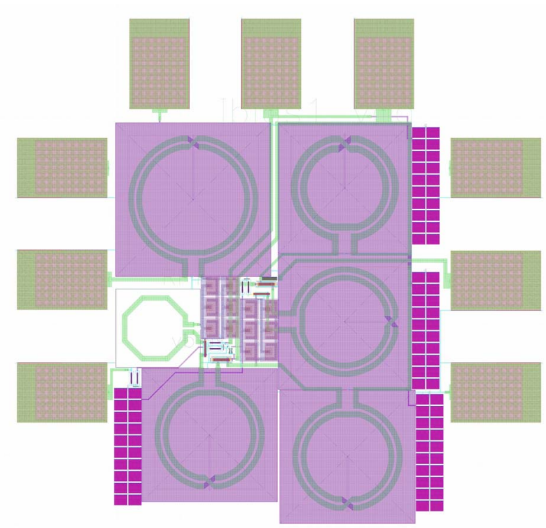


Fig. 10: Layout of LNA.

occupies an area 72x47μm^2 and utilizes top metal layer to reduce the parasitic capacitance to substrate (C_{pad}=17fF from EM simulation).

The pad capacitance, series gate inductor and shunt capacitor (C_s) forms the input pi-matching network. The MIM capacitor is used for dc coupling between the pi-match network and the input transistor. The MIM capacitor suffers from parasitic capacitance between bottom plate and substrate. The MIM capacitor is placed such that the shunt capacitor C_s is replaced by the bottom plate capacitor in the pi-match network. The pad capacitance, load inductor and dc block capacitor C_t forms tapped-capacitor output matching network. The dc block capacitor C_t is designed such that LNA achieves good matching at 30GHz. MOM capacitor is used as DC block capacitor to reduce the effect of parasitics.

The performance of the inductors is critical for the LNA, especially at the millimeter-wave frequencies and hence full-wave EM simulations were performed for all the inductors. The source inductor (L_s) has a value of 83 pH. This inductor was custom-designed and implemented as a single-turn octagonal spiral to improve the quality factor as shown in Fig. 8.

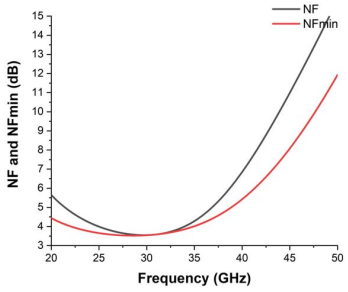


Fig. 11: Noise figure (NF) of LNA.

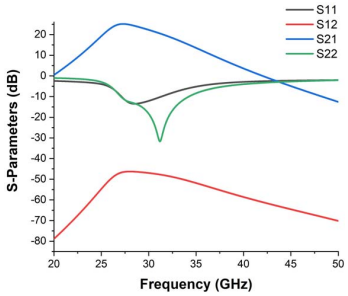


Fig. 12: S-Parameter results of LNA.

Inductance of the spiral depends on its metal width and inner and outer diameters and hence are optimized to obtain desired inductance. While Q-factor depends on the lateral and vertical dimensions, it is further improved by optimizing the length of the inductor terminals and separation between the terminals. Full-wave EM simulations are performed to characterise the inductor. Figure 9 shows the graphs obtained after performing EM simulations for all inductors.

A large resistor connected at the body of the input transistor neutralises the effect of source-bulk and drain-bulk capacitances. This improved the noise performance of LNA by isolating the bulk node.

Iterative layout design was done to make the design compact. All the signal routings were kept to a minimum to reduce the loss. Top metal layer is used for routing wherever possible due to its low resistance. Supply decoupling is implemented with MOM capacitors to establish a good AC ground. These MOM capacitors are designed such that their self-resonant frequencies are higher than the Ka-band.

IV. SIMULATION RESULTS

The complete layout of LNA implemented in a commercial 65nm RF CMOS process with 8 metal layers is shown in Fig. 10. The active core occupies an area of 420x320μm^2. RC parasitics of interconnects and components are extracted and simulated. All passive devices are modelled by performing full-wave EM simulations. The results obtained at room temperature 27^0C is presented here.

Noise simulation results in Fig. 11 shows that the implemented design achieved a minimum NF of 3.55dB and NFmin

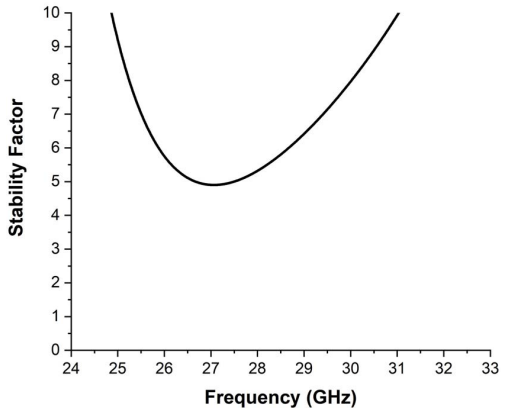


Fig. 13: Stability factor of LNA.

of 3.54dB at 30GHz. The very small difference between NF and NFmin concludes that the input admittance of LNA is close to noise optimum source admittance. The LNA achieves NF below 4dB from 25-34GHz.

Figure 12 shows the S-parameter simulation results and achieves input and output matching better than -12dB and -18dB respectively at 30GHz. The input return loss is below -10dB for the frequency range 27.1-31.3GHz and below -8dB for the frequency range 26.7-32.6GHz. The achieved gain at 30GHz is 22.3dB and has a maximum of 25.2dB at 27.3GHz. Gain is above 20dB for frequencies from 25.1GHz to 31.5GHz. Reverse isolation is very good for the entire frequency range. LNA remains stable as evidenced by stability factor in Fig. 13.

The third order intercept point ($IIP3$) and 1-dB compression point (P_{1dB}) is simulated by varying the input power and using two tones around 30GHz separated by 100MHz and obtained $IIP3$ of -14dBm and P_{1dB} of -32dBm.

Table I summarizes the performance of recently reported mm-wave amplifiers. The proposed design achieves highest maximum gain of 25.2dB with lowest DC power consumption of 7mW and low active footprint of $0.083\mathrm{mm}^2$ while providing one of the best noise performance when compared with previous works in Ka band. Additionally, the difference between the NF and NFmin of the implemented design is less than 0.01dB.

V. CONCLUSION

A 30GHz low noise amplifier was implemented in 65nm commercial CMOS process. The method of optimization of LNA based on the f_T/f_{max} of transistor is found to be sub-optimal. An iterative analysis of LNA based on the novel method based on the transconductance of MOSFET generated an optimum transconductance which gives noise figure very close to NFmin. Noise optimal biasing is explored and techniques to reduce the difference between NF and NFmin is presented and implemented. The proposed LNA achieved high noise performance while consuming very low power and area, which make it applicable for 5G communications.

TABLE I: Comparison with state of the art.

Reference	**This Work**	[1]	[2]	[4]	[3]
CMOS Technology	**65nm LL**	28nm LP	65nm	65nm	90nm
Frequency (GHz)	**30**	33	24	55-64	30
Topology	**2 cascode stages**	2 cascode stages	2 stage CS	2 cascode stages	CS-cascode
Gain (dB)	**25.2@ 27.3GHz**	18.6	23.5	12.8±0.5	20@ 28.5GHz
NF (dB)	**3.55**	4.9	3.3	3.6@ 61GHz	2.9@ 28GHz
$\mathbf{P_{DC}}$ (mW)	**7**	9.7	12	8.8	16.25
Supply Voltage (V)	**1.2**	1.2	1.2	1	1
Area** ($\mathbf{mm^2}$)	**0.13***	0.23	0.15	0.33	0.67

** Core area includes RF GSG pad area but without DC pads.
* Active area $0.083\mathrm{mm}^2$.

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