28-32 GHz Wideband LNA for 5G Applications

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***Abstract*—In order to meet the ever-increasing demands of bandwidth in modern communication systems, mm-Wave frequency bands emerge as a possible way forward. LNA is the most critical component in an RF receiver chain. This article presents a two-stage mm-Wave LNA for 5G applications. The first stage is used to provide a major portion of overall LNA gain and partial noise cancellation. The use of Common Gate as an input impedance provides wideband matching at the input. Without any significant power and area consumption, the second stage is used to further increase the gain along with noise cancellation. Two small inductors are employed to resonate the circuit at 30GHz to mitigate the effect of capacitance in mm-Wave frequency band. The proposed LNA is designed and simulated using TSMC 65nm Bulk CMOS technology. Post simulation results show that the designed LNA achieves a peak S21 of 18.48dB with a wideband 3-dB bandwidth in the range of 26 to 33.6 GHz. The NF is also less than 3dB over the entire band of interest. The proposed LNA occupies a 300×100 µm^2 area with a power consumption of 17 mW including the output buffer stage.**

Keywords — LNA, Wideband LNA, 5G LNA, mmWave, MIMO LNA, CMOS LNA, 65nm CMOS, MMIMO LNA

I. INTRODUCTION

To meet the ever-increasing demands for bandwidth, mm-Wave frequency bands appear as a viable solution effective enough to meet the ever-increasing demand for mobile data rates [1]. In a conventional RF receiver chain, a low noise amplifier (LNA) is the first and the critical component that dramatically affects the overall sensitivity of the system depending on its performance. As LNA is the first component in the chain hence, it must provide high gain to the received RF signal. Similarly, it must add minimum noise because that will impact the overall noise figure (NF) of the whole receiver chain. Modern 5G technology is going to be based on Massive MIMO (Multiple Input-Multiple Output) based architecture. Therefore, to make this technology commercially viable, an LNA is required, which consumes minimum power (longer operation) and silicon area (cost efficiency). At the same time, wide bandwidth, high linearity and wideband input matching are also key requirements [2]. Simultaneously meeting all these specifications for a mm-Wave LNA is a challenging design problem for RF circuit designers, serving as one of the bottlenecks in the commercial rollout of 5G systems based on mm-Wave frequencies.

Advanced CMOS technology nodes enable the implementation of mm-Wave circuits but also pose certain critical challenges in RF circuit design [3]. These challenges include low voltage headroom (VDD is shrinking), low intrinsic gain of transistor, the requirement of large inductors (for gain peaking) and large transistors (to decrease NF). Similarly, common gate matching requires large size transistors for 50Ω input impedance match, which ultimately results in higher power consumption. The requirement of substantial bandwidths in wideband LNAs introduces critical challenges as compared with multiband or narrowband LNAs. There exist high parasitic capacitances associated with the CMOS transistors, which can be resonated and tuned out using inductors in narrowband LNA designs. These techniques are inherently narrowband in nature and do not work well for wideband LNA designs. Also , the gain of a wideband LNAs at mm-Wave frequencies is restricted by the capacitive loading at the output stage [4].

An inductor-less wideband LNA for sub 6GHz frequencies was presented in [5] employing the techniques of current reuse for the reduction of current through the load resistor and at the same time improving the gain, noise performance, and power consumption. Similarly, 50Ω wideband input matching and partial noise cancellation were achieved in [5] by utilizing the common drain stage in the feedback path.

Likewise, a novel architecture for wideband input impedance matching utilizing two common gate (CG) transistors was presented in [6]. One of the CG transistors is positioned above the other in a current reuse mode, such that they appear parallel at the input. By using this technique, the input transconductance needed is reduced by half as compared to the basic CG LNA without any impact on the overall gain for each NMOS transistor. Similarly, an LNA for 5G applications is presented in [7] utilizing positive feedback, which inherently cancels the noise produced by the input CG transistor.

A gm-boosting based Common Gate (CG) LNA using a passive transformer was proposed in [8]. This technique is utilized to meet the trade-off between noise and input matching while consuming lower power. Likewise, a compact wideband low-noise amplifier (LNA) using source degeneration topology for the purpose of bandwidth extension was presented in [9]. Transformer-based gate-drain feedback is utilized to attain a wideband response by achieving the maximum gain at high frequencies. Likewise, two resonance points (using transformer) independently positioned at low and high frequencies inside the band of operation are utilized to achieve wideband input matching.

[10] proposed an LNA for millimeter-wave (mm-Wave) band utilizing gm-boosting technique along with transformers. It not only improves the stability of the circuit but also alleviates the gain while suppressing the noise figure. Likewise, [11] presented a novel continually-stepped variable gain (CSVG) 2-stage LNA by incorporating a tunable-transformer at the 2nd-stage for millimeter-wave

(mm-Wave) operation.

Similarly, another wideband LNA based on complementary common gate (CCG) stage and common source (CS) stages was presented in [12]. In this architecture, the CCG stage saves dc power by the current reuse technique. Similarly, replacing two inductors with a single transformer reduces chip area. Load reuse technique is utilized to simultaneously achieve wideband gain, wideband input matching, and flat noise figure (NF).

[13] presented a design of low power LNA in 65nm CMOS using multi-cascode configuration along with noise reduction topology. Inductors have been designed and positioned between the transistors of the cascode arrangement to decrease the NF, while at the same time increasing the small-signal gain. Based on this technique, power of 28.8 mW is consumed while they achieved a peak gain of 14.3 dB with a noise figure of 3.8 dB at 38 GHz. The chip size of the proposed LNA (comprising all the testing pads) was 0.55 x 0.45 mm^2 [13].

The designs of [9], [11], [12] and [13] use a relatively large silicon area, whereas power consumption is higher in [10]. Our design aims to improve both of these aspects simultaneously while maintaining all other performance parameters like gain, NF, linearity and BW.

The paper is arranged as follows. In section-II, the proposed circuit/architecture of the LNA is discussed. Section-III reports the implementation and simulation results for the proposed LNA, followed by section-IV, in which performance comparison with state-of-the-art LNAs is given. The last Section-V concludes the paper.

II. Proposed LNA Architecture

The proposed LNA consists of two stages. The first stage is used to provide a major portion of overall LNA gain along with partial noise cancellation. Since the input impedance of CG configuration is $1/g_m$, it is used to provide wideband matching at the input. The second stage is used to further increase the gain along with noise cancellation and 50Ω output matching. The schematic of the proposed LNA is shown in Fig. 1, where Vb1 and Vb2 are bias voltages used to bias the transistor M2, M4 and M7.

The first stage employs two transistors M0 and M1, to provide forward voltage gain. Transistor M2 acts as a cascode which increases the output resistance of stage 1 which in turn increases the voltage gain for this stage which is given by (2). The mathematical expressions for output resistance and voltage gain for stage 1 are given in (1) and (2) respectively.

$$R_{out\_stage1} = r_{o2} + (r_{o0} || r_{o1}) + g_{m3}\, r_{o2}(r_{o0} || r_{o1}) \quad (1)$$

$$A_{v\_stage1} = \frac{V_{o1}}{RF_{in}} = \frac{g_{m0}+g_{m1}}{g_{ds0}+g_{ds1}+g_{m2}} * (R_{out\_stage1}) \quad (2)$$

A voltage to current feedback through transistor (M3) is employed to achieve wideband input matching. This feedback is different from the simple common gate matching in the manner that the transconductance required is decreased by a factor of $(1 + A_{v\_stage1})$. This reduces the size of the M3 transistor as well as the power consumption. For conventional common gate matching at input, the required transconductance for 50Ω matching is 20mS. In the proposed circuit, for the first stage gain of 9, the transconductance requirement decreases to 2mS, which can

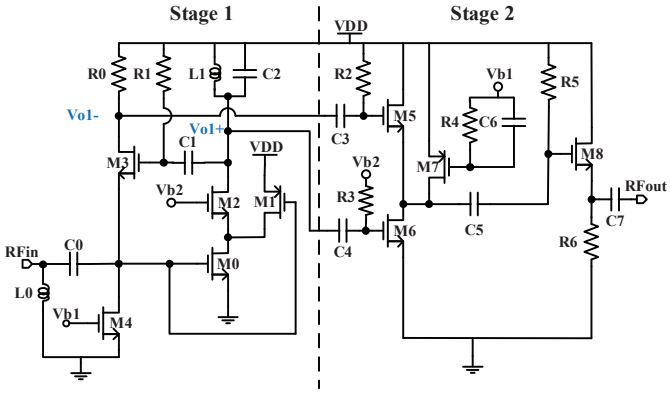

Fig. 1. Schematic of Proposed two-stage mm-Wave LNA for 5G Applications

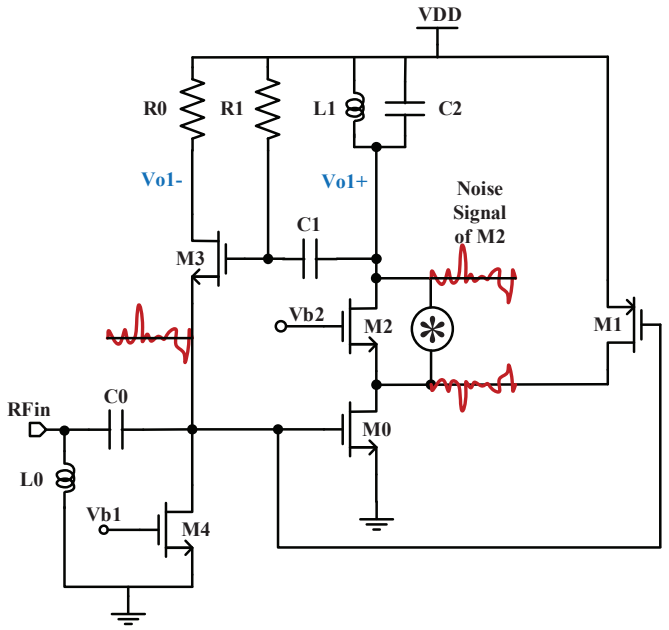

Fig. 2. Noise Cancellation Mechanism via the feedback in Stage 1

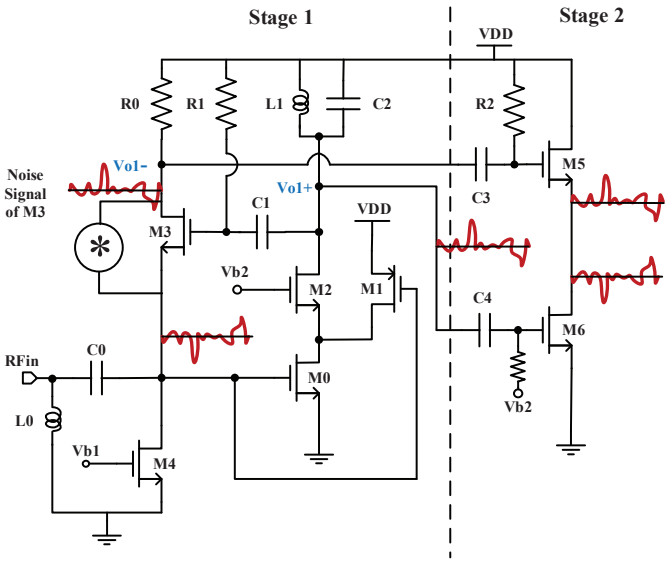

Fig. 3. Noise cancellation mechanism for feedback transistor in Stage 2

be obtained with much smaller transistor. The expression for input impedance (Zin) is given in (3).

$$Zin = \frac{1}{g_{m3}(1+A_{v\_stage1})} \quad (3)$$

Transistor M4 acts as a current source for the transistor M3 and also establishes gate bias for transistors M0 and M1.

The current reuse technique employed in transistor M1 increases the voltage gain. The partial noise cancellation mechanism employed in the first stage using feedback is shown in Fig. 2. Input Referred Noise of main transistor (M0) is given in (4).

$$V_{ni} = \frac{KT\gamma}{g_m}\left(1 + \frac{1}{1+A_{v\_stage1}}\right)^2 \quad (4)$$

From (4), it is clear that noise can be optimized by either increasing forward voltage gain (A_{v_stage1}) or increasing forward transconductance (g_m). So, for a large value of voltage gain, the reduced expression is shown in (5), which is four times (6 dB) less than the input noise of a simple common source amplifier.

$$V_{ni} = \frac{KT\gamma}{g_m} \quad (5)$$

The second stage basically adds outputs signal from two nodes of 1st stage, but at the same time, noise is cancelled. Voltage from Vo1+ and Vo1− is added to increase the overall output voltage. This enables to cancel the noise of the feedback transistor (M3), whose noise is not cancelled through feedback noise cancellation in stage 1. The complete noise cancellation mechanism for the second stage is shown in Fig. 3. The forward noise cancel condition for transistor M3 is given in (6).

$$g_{m_6} = \frac{g_{m_5} * R_S}{A_{v\_stage1} * R_o} \quad (6)$$

Overall gain under noise-cancelling and input match conditions is given in (7).

$$Gain = \frac{RF_{out}}{RF_{in}} = R_L * \frac{R_0}{R_s} * g_{m5} * \frac{2}{A_{v\_stage1} + 2} \quad (7)$$

The last part of the second stage is the common drain amplifier which acts as an output buffer to serve the purpose of 50Ω matching.

III. Implementation and Simulation Results

The proposed LNA is implemented using TSMC 65nm bulk CMOS technology. The layout of the proposed LNA is given in Fig. 4. The LNA occupies a 300 x 100 µm2 area. It is clear from the layout that more than half of the area is consumed by small inductors, which were employed to resonate the capacitance. Analog Design Environment of Cadence is used to perform S-parameters analysis for the proposed circuit. Fig. 5 and Fig. 6 show the comparison of schematic and post layout S21 and NF results for the designed LNA respectively. It can be seen from the post-layout results that this work achieved a peak S21 value of 18.48dB. Wideband 3-dB bandwidth for the designed LNA is in the range of 26 to 33.6 GHz. The NF is also less than 3dB over the entire band of interest, including the effect of the buffer. Fig. 7 shows the plot of S11 and S22. Both S11 and S22 are less than -10dB in the band of interest depicting the 50Ω input and output matching of LNA. Fig. 8 and Fig. 9 show the linearity plots for the proposed LNA with a 1dB compression point of -24.5 dBm and IIP3 of -20 dBm. Power consumption for the complete LNA circuitry including the buffer stage is 17 mW.

IV. Performance Comparison

Table I shows a performance comparison of the wideband state-of-the-art LNAs with the designed LNA. As clear from

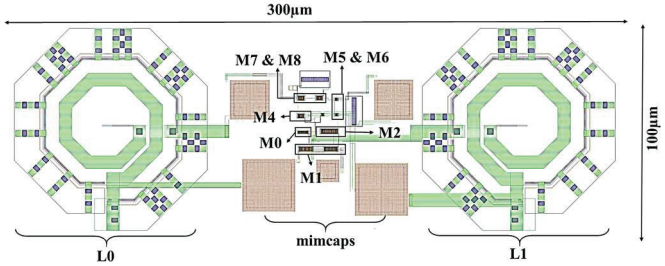

Fig. 4. Layout of the proposed LNA

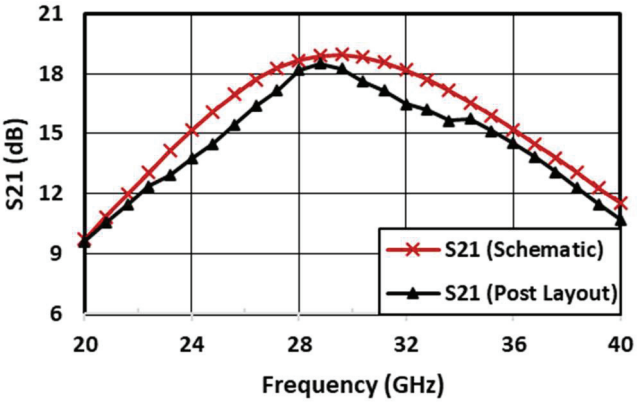

Fig. 5. Comparison of Schematic and Post Layout S21 of proposed LNA

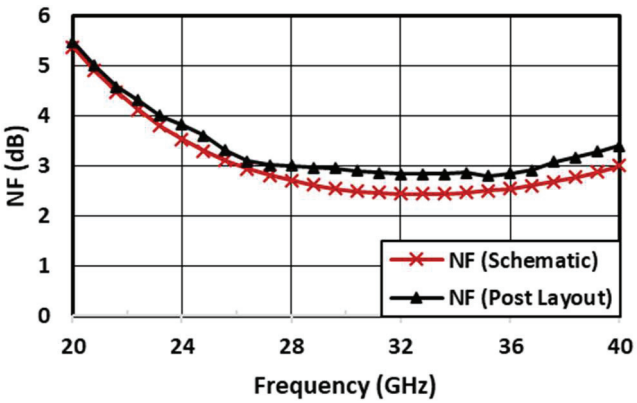

Fig. 6. Comparison of Schematic and Post Layout NF of proposed LNA

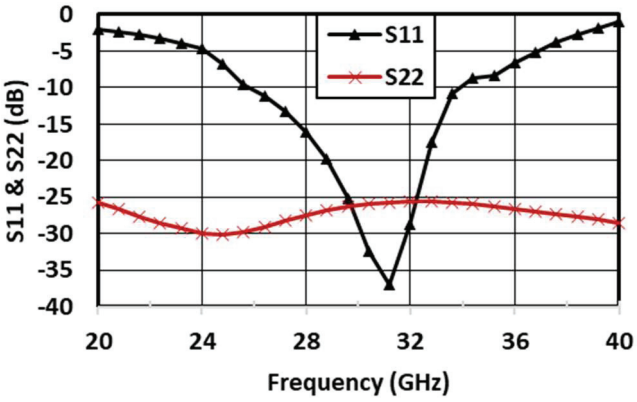

Fig. 7. Post Layout S11 and S22 plot of proposed LNA

the table, the proposed LNA exhibits a wide bandwidth as well as superior performance in terms of parameters like input matching, gain, NF, power consumption and Si area. In order to visualize the combined effect of these parameters, the figure of merit (FoM) given in (8) is used to compare this work with state-of-the-art LNAs [14].

$$FoM = 20\log_{10}\left(\frac{BW[GHz]\,.\,Gain\,[lin]}{P_{DC}[mW]\,.\,(NF_{min}[lin]-1)\,.\,A[mm^2]}\right) \quad (8)$$

The large FOM of the proposed design is due to the small inductors (~200pH). Since the inductors constitute most of the circuit area, the reduction in the inductor area results in a smaller overall silicon area and increase the FOM of the proposed design. The linearity, in contrast, is inferior to the state of art and it could be improved further by different linearity improvement techniques presented in literature [4].

V. Conclusion

In this article, a two-stage mm-Wave LNA for 5G applications is presented where the first stage is used to provide a major portion of overall LNA gain along with partial noise cancellation. Without any significant power and area consumption, the second stage is used to further increase the gain along with noise cancellation. The proposed LNA is designed and simulated using TSMC 65nm Bulk CMOS technology. Results show that the designed LNA achieved a peak S21 value of 18.48dB with a wideband 3-dB bandwidth in the range of 26 to 33.6 GHz. The NF is also less than 3dB over the entire band of interest. Two small inductors were used to resonate the circuit at mm-Wave frequencies in order to mitigate the effect of capacitance. As shown earlier, inductors occupy more than half of the chip area. Getting rid of these inductors to have an inductor less mm-Wave LNA can be one of the research avenues for future research.

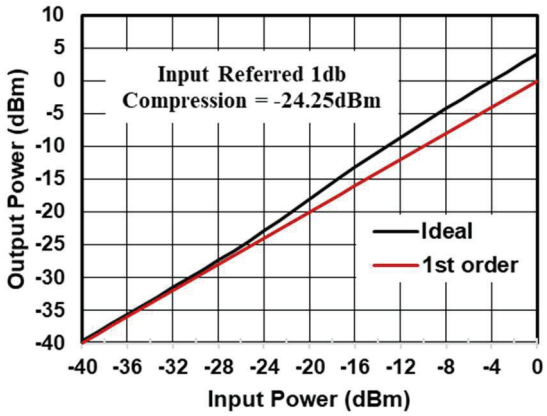

Fig. 8. 1dB Compression plot of the proposed LNA

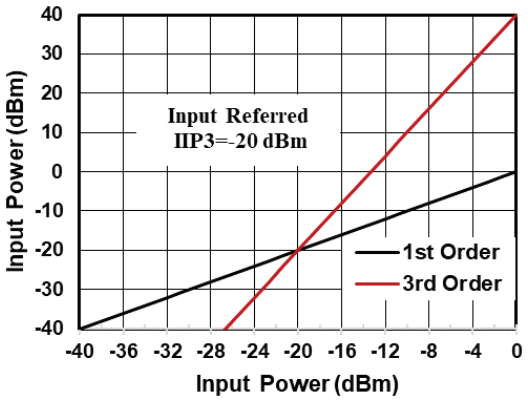

Fig. 9. IIP3 plot of the proposed LNA

TABLE I. PERFORMANCE COMPARISON OF STATE-OF-THE-ART LNAs WITH PROPOSED LNA

Parameter	[9]	[10]	[11]	[12]	[13]	Our Work
Technology	65 nm CMOS					
S21 (dB)	10.2	18.3	18.2	10.7	14.3	**18.48**
Freq. (GHz)	15.8-30.3	24.9-32.5	22-34	7.6-29	35-43	**26-33.4**
3dB BW (GHz)	14.5	7.6	12	21.4	8	**7.4**
NF (dB)	3.3	3.25	3.9	4.5	3.8	**3**
Area (mm^2)	0.18	0.11	0.16	0.23	0.25	**0.08**
P_{DC} (mW)	12.4	20.5	9.8	12.1	28.8	**17**
P1dB (dBm)	-	-24	-21	-	-	**-24.5**
IIP3 (dBm)	-0.5	-	-	1.4	-9.5	**-20**
FoM	25.33	27.94	32.62	23.22	12.23	**33.23**

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