3–9-GHz CMOS LNA Using Body Floating and Self-Bias Technique for Sub-6-GHz 5G Communications

Jin-Fa Chang, *Member, IEEE*, and Yo-Sheng Lin, *Senior Member, IEEE*

***Abstract*— We propose the body floating and self-bias technique, in which the body of the transistor is connected to its drain through a resistance (13.6 kΩ in this work). A low-power 3–9-GHz CMOS low-noise amplifier (LNA) using the technique for sub-6-GHz 5G systems is reported. An enhancement in S_{21} and noise figure (NF) of the LNA is achieved due to the forward body-to-source bias (V_{BS}) (i.e., small threshold voltage V_{th}) and the transistors being free from the substrate leakage. Low power is achieved since low supply voltage (V_{DD}) of 1 or 0.8 V is applicable because of small V_{th}. At V_{DD} of 1 V, the LNA consumes 3.3 mW and achieves prominent S_{11} of −10.1 to −41.6 dB, S_{21} of 10.7 dB, and NF of 2.89 dB for 3–9 GHz. At V_{DD} of 0.8 V, the LNA consumes 1.36 mW and achieves S_{11} of −10 to −45.8 dB, S_{21} of 9.4 dB, and NF of 3.46 dB. To the authors' knowledge, both are one of the lowest power values ever reported for CMOS LNAs with bandwidth greater than 6 GHz and NF under 3.5 dB.**

***Index Terms*— Body floating resistor, CMOS, low noise amplifier (LNA), low power (LP), self-body bias, wideband.**

I. Introduction

TO DATE, several sub-6-GHz CMOS low-noise amplifiers (LNAs) have been reported [1]–[9]. But, the overall performance still has room for improvement. For example, in [3], a sub-6-GHz LNA in 65-nm CMOS is demonstrated. Though low noise figure (NF) of 3.3 dB, S_{21} of 12.8 dB, and bandwidth (BW) of 19 GHz are attained, its power dissipation (P_D) of 20.3 mW is not good enough. For an nMOSFET, instead of connection of its body to source [B-to-*S*, see Fig. 1(a)], its body can be connected to a 5–10-kΩ grounded resistor (i.e., B-to-*S* with R). This makes the body floating at RF and V_{BS} equal to 0 at dc. It is useful for insertion-loss reduction in switch applications [10], [11]. Instead of connection of its body to drain [B-to-D, see Fig. 1(b)], its body can be connected to drain through a high resistance R_B [B-to-D with R, see Fig. 1(c)]. This makes the body floating at RF and V_{BS} (equal to $V_{DS} - I_B R_B$) being forward-biased at dc (i.e., smaller V_{th}). I_B is the substrate leakage current in Fig. 2(a). This is the proposed body floating and self-bias technique. From Fig. 2(b), I_B decreases with the increase of R_B, while V_{th} increases with the increase of R_B due to the decrease of I_B and V_{BS}. To obtain reasonable V_{th} and low I_B (such as smaller than 0.1 μA/μm), a high R_B (13.6 kΩ in this work) can be used. In this work, we report a CMOS LNA using body floating and self-bias technique for sub-6 GHz 5G systems. An enhancement in S_{21} and NF is achieved. This is because the transistors have smaller V_{th} due to forward-biased V_{BS}, and are free from I_B (through the ON-resistance $R_{on,BS}$ of the parasitic body-source diode) due to large R_B [see Fig. 2(c)]. Low power (LP) is achieved since low V_{DD} of 1 or 0.8 V is applicable due to small V_{th}.

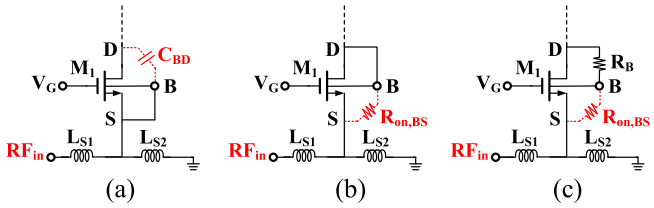

Fig. 1. CG input transistor with (a) B-to-*S*, (b) B-to-D, and (c) B-to-D with R.

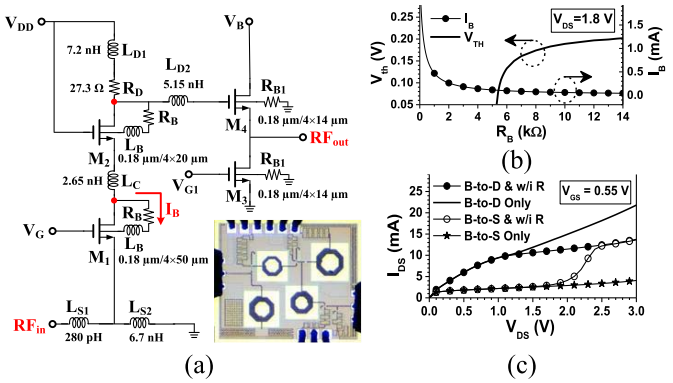

Fig. 2. (a) Circuit diagram and photograph of the LNA. Simulated (b) V_{th}–R_B and I_B–R_B and (c) I_{DS}–V_{DS} curves of transistor M_1.

II. Circuit Design

The LNA is designed by a 1P6M 0.18-μm CMOS process. Fig. 2(a) shows the schematic and chip photo. The chip area is 0.739 mm^2. The transistor sizes and important device parameters are labeled. The transmission lines (TLs) and the inductors are placed on the 2.34-μm-thick topmost metal to minimize the resistive loss. The LNA consists of a cascoded common-gate (CG) input stage followed by a buffer stage.

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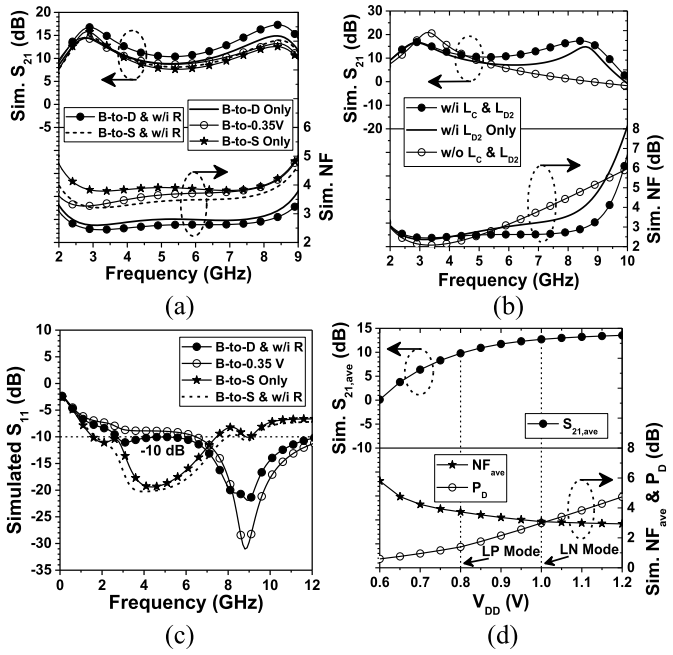

Fig. 3. Simulated (a) S_{21} and NF, (b) L_C–L_{D2} effect on S_{21} and NF, (c) S_{11}, and (d) V_{DD} effect on S_{21} and NF of the LNA.

The input impedance (Z_{in}) of the LNA is given by

$$Z_{in} \approx sL_{S1} + \left(sL_{S2} \left\| \frac{1}{sC_{gs1}} \right\| \frac{1}{g_{m1}} \right) \tag{1}$$

in which C_{gs1} and g_{m1} are the gate–source capacitance and transconductance, respectively, of transistor M_1. g_{m1} decreases with the increase of R_B because of the increase of V_{th}. The lower corner frequency (3–4 GHz) is a function of the peaking inductor L_{D1}. L_C and the capacitance at drain of M_1 and source of M_2 are parallel resonant around the midband (5–6 GHz), while the peaking inductor L_{D2} and C_{gs4} are series resonant at the upper corner frequency (8–9 GHz). As a whole, flat and high S_{21} and flat and low NF are achieved. Fig. 2(c) shows the simulated I_{DS}–V_{DS} curves of transistor M_1 in various conditions. For V_{DS} smaller than 1.1 V, compared with B-to-S and B-to-S with R, higher I_{DS} is obtained for B-to-D and B-to-D with R due to smaller V_{th}. Compared with B-to-D with R, sharper increase of I_{DS} (for V_{DS} larger than 1.1 V) is obtained for B-to-D due to the small $R_{on,BS}$ between drain and source. For B-to-S with R (i.e., body being floating) at V_{DS} larger than 2.5 V, the body-to-drain diode is reversely conducted. Its I_{DS} curve is close to that of the B-to-D with R because the resistance between drain and source is $R_{on,BD}+R_B$, which is roughly equal to $R_B + R_{on,BS}$.

Fig. 3(a)–(c) shows the simulation results at V_{DD} of 1 V (the low-noise (LN) mode). For the configurations with R, the TL between R and the transistor is 6-μm-wide and 127.1-μm-long. Its equivalent inductance [L_B in Fig. 2(a)] is 84.9 pH. L_B has no effect on V_{th} due to short at dc, but is helpful for the slight S_{11} enhancement according to simulation. Fig. 3(a) shows the simulated S_{21} and NF in various conditions. Compared with the traditional B-to-S (and B-to-S with R), the proposed B-to-D with R (13.6 kΩ in this work) achieves notable improvement in S_{21} and NF due to smaller V_{th} of the transistors. For instance, V_{th} is reduced from 0.42 V (for V_{BS} equal to 0 V) to 0.33 V for V_{BS} equal to 0.35 V (this work), and 0.27 V for V_{BS} equal to 0.7 V. Compared with B-to-D and B-to-0.35 V (i.e., body connected to a fixed bias of 0.35 V, the same as the dc bias at drain), B-to-D with R achieves better S_{21} and NF mainly due to free from the substrate leakage [see Fig. 2(c)]. Moreover, the LNA achieves input third-order intercept point (IIP3) of -8.8, -9, -10, -10.3, and -10.8 dBm, respectively, at 5 GHz in the configuration of B-to-S only, B-to-S w/i R, B-to-0.35 V, B-to-D only, and B-to-D w/i R (not shown here). The voltage gain (A_v) and output impedance (Z_{out}) of the buffer stage are given by

$$A_v \approx \frac{1}{1+s^2L_{D2}C_{gs4}} \cdot \frac{g_{m4}(r_{o3}\|r_{o4}\|50\,)}{1+g_{m4}(r_{o3}\|r_{o4}\|50\,)} \tag{2}$$

$$Z_{out} \approx \frac{1+s^2L_{D2}C_{gs4}}{g_{m4}+sC_{gs4}} \|r_{o3}\|r_{o4}\|50 \tag{3}$$

in which r_{o3} is the output resistance of transistor M_3. C_{gs4}, g_{m4}, and r_{o4} are the gate–source capacitance, transconductance, and output resistance, respectively, of transistor M_4. Instead of the connection of body to ground, the proposed B-to-D with R can be used at the buffer stage. Simulation shows a slight increase in average S_{21} ($S_{21,ave}$) from 12.7 to 14.3 dB because of the increase of g_{m4} (due to the decrease of V_{th}). Average NF (NF_{ave}) remains roughly the same (from 3.08 to 3.09 dB) since it mainly depends on the input stage. Fig. 3(b) shows the simulated S_{21} and NF of the LNA in various L_C and L_{D2} conditions. L_{D2} and L_C are effective to improve S_{21} and NF around the upper corner frequency (8–9 GHz) and the midband frequency (5–6 GHz), respectively.

Fig. 3(c) shows the simulated S_{11} of the LNA. For B-to-D with R (this work), S_{11} is smaller than -10 dB for 2.7–12.3 GHz. The corresponding -10 dB matching BW (f_{10dB}) is 9.6 GHz. Moreover, the S_{11} curve of B-to-D with R is close to that of B-to-0.35 V due to roughly the same V_{BS} and V_{th}. The S_{11} curve of B-to-S with R is close to that of B-to-S only also due to roughly the same V_{BS} and V_{th}. Fig. 3(d) shows the simulated $S_{21,ave}$, NF_{ave}, and P_D versus V_{DD} characteristics of the LNA. At LN mode (V_{DD} of 1 V), the LNA consumes low P_D of 2.99 mW and achieves high $S_{21,ave}$ of 12.7 dB and low NF_{ave} of 3.08 dB for 3–9 GHz. At LP mode (V_{DD} of 0.8 V), the LNA consumes ultralow P_D of 1.39 mW and achieves decent $S_{21,ave}$ of 9.8 dB and NF_{ave} of 3.74 dB for 3–9 GHz.

III. Results and Discussions

On-wafer S-parameters measurement was performed by a Keysight 5247A network analyzer. The LNA has two operation modes, the LN mode and the LP mode. At LN mode, the LNA consumes 3.3 mW from V_{DD} of 1 V. At LP mode, the LNA consumes 1.36 mW from V_{DD} of 0.8 V. Both are one of the lowest powers ever reported for a CMOS LNA with BW greater than 6 GHz and NF under 3.5 dB (will discuss later). The LNA is unconditionally stable at the LN mode and the LP mode due to stability factors μ and μ' being greater than 1 [12]–[13] (not shown here). Fig. 4(a) shows the measured and simulated/calculated S-parameters of the LNA at LN mode. The measured S_{11} and S_{22} are close to the calculated ones. The measured S_{21} and S_{12} are consistent with the simulated ones. The LNA achieves minimum S_{11} of -41.6 dB at 7.2 GHz, and S_{11} smaller than -10 dB for 2.9–10.3 GHz, corresponding to f_{10dB} of 7.4 GHz. The remarkable S_{11} is attributed to the T-match wideband input

TABLE I

SUMMARY OF THE LNA, AND RECENTLY REPORTED STATE-OF-THE-ART CMOS LNAS WITH SIMILAR OPERATION FREQUENCY

	Circuit Configuration	S_{11} (dB)	S_{21} (dB)	Bandwidth (GHz)	NF_{min}/ NF_{ave} (dB)	IIP3 (dBm)	P_D (mW)	FOM (GHz/mW)	CMOS Process
This Work– LN Mode	2-stage: CG+CG	-10.1~ -41.6	7.5-10.7	2.4-9.1	2.89/ 3.41	-6.2	3.3	4.85	0.18 μm
This Work– LP Mode	2-stage: CG+CG	-10~ -45.8	6.4-9.4	2.3-9.1	3.46/ 3.89	-6.8	1.36	8.57	0.18 μm
[3], TMTT 2020	3-stage: CG+CS+CS	< -10	9.8-12.8	1-20	3.3/ 4.3	5.8	20.3	2.03	65 nm
[4], TCAS-II 2019	3-stage: CS+CD+CS	< -10	13.8-16.8	0.5-7	2.87/ 3.32	-4.5	11.3	2.92	65 nm
[5], EE 2019	3-stage: CG+CS+CS	< -10	12.4-13.6	3.1-10.6	3.3/ 3.9	N/A	21.6	1.07	0.18 μm
[6], TMTT 2019 (LP Mode)	3-stage BDDA	< -10	6-9	3-12	5.9/ 6.65	NA	132	0.04	0.18 μm
[7], JSSC 2017	2-stage CS & 2-path	< -10	14.5-17.5	0.1-2	2.9/ 3.2	-10.6	21.3	0.52	0.18 μm
[8], TCAS-II 2018	2-stage (CG+CS) 2-path	< -10	10-13^{+}	2-5	6/ 7	-9.5	1.8	1.56	0.18 μm
[9], JSSC 2007	3-stage: CG+CS+CS	< -11	6.7-9.7	1.2-11.9	4.5/ 4.8	-6.2	20	0.68	0.18 μm

$^{+}$Voltage Gain

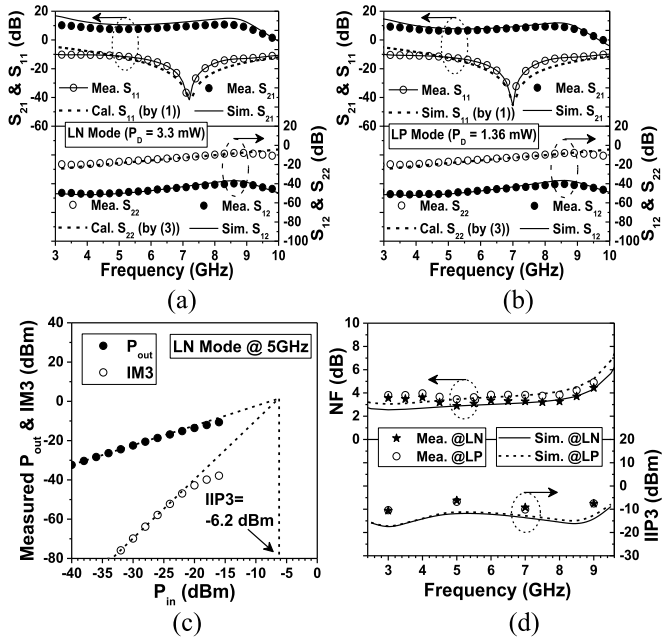

Fig. 4. Measured and simulated/calculated S-parameters at (a) LN and (b) LP mode. (c) Measured P_{out} and IM3 versus P_{in} characteristics. (d) Measured and simulated NF and IIP3.

network comprising L_{S1}, L_{S2}, C_{gs1}, and $1/g_{m1}$. The LNA achieves maximum S_{21} of 10.7 dB at 8.3 GHz, and 3-dB BW (f_{3dB}) of 6.7 GHz (2.4–9.1 GHz). Moreover, the LNA achieves excellent S_{12} of −39.8 to −52.4 dB for 3–11 GHz. The decent S_{12} is attributed to the adoption of the cascoded CG input stage, so the reverse signal through C_{gd} is relatively small. Fig. 4(b) shows the measured and simulated/calculated S-parameters of the LNA at LP mode. The measured S_{11} and S_{22} are close to the calculated ones. The measured S_{21} and S_{12} are consistent with the simulated ones. The LNA achieves minimum S_{11} of −45.8 dB at 7 GHz, and S_{11} smaller than −10 dB for 3–9.9 GHz, corresponding to f_{10dB} of 6.9 GHz. The LNA achieves maximum S_{21} of 9.4 GHz at 8.3 GHz and f_{3dB} of 6.8 GHz (2.3–9.1 GHz). Moreover, the LNA achieves excellent S_{12} of −40.7 to −54 dB for 3–11 GHz.

Fig. 4(c) shows the measured output power (P_{out}) and third-order intermodulation output power (IM3) versus input power (P_{in}) characteristics of the LNA at 5 GHz and LN mode. The corresponding IIP3 is −6.2 dBm. Fig. 4(d) shows the measured and simulated NF and IIP3 of the LNA at LN and LP modes. At LN mode, the LNA achieves remarkable minimum NF (NF_{min}) of 2.89 dB at 5 GHz and NF_{ave} of 3.41 dB for 3–9 GHz, close to the simulation result (NF_{min} of 2.55 dB and NF_{ave} of 3.08 dB). The noteworthy NF is attributed to the adoption of the body floating and self-bias technique. As a whole, an enhancement in NF (and S_{21}) of the LNA is achieved due to the forward-biased V_{BS} (i.e., small V_{th}) and the transistors being free from the substrate leakage. At LP mode, the LNA achieves excellent NF_{min} of 3.46 dB at 5 GHz and NF_{ave} of 3.89 dB for 3–9 GHz, close to the simulation result (NF_{min} of 3.04 dB and NF_{ave} of 3.74 dB). Moreover, the LNA achieves measured IIP3 of −6.2 to −10.6 dBm at LN mode and −6.8 to −10.4 dBm at LP mode for 3–9 GHz, slightly better than the simulated ones (−8.8 to −18.2 dBm at LN mode and −7.9 to −18 dBm at LP mode) due to slightly lower S_{21}. A figure of merit (FOM) adequate for performance evaluation of wideband LNAs is given by Edwards and Sinsky [12]

$$\text{FOM [GHz/mW]} = \frac{S_{21}\ [1] \cdot \text{BW [GHz]}}{(\text{NF} - 1)[1] \cdot P_D\ [\text{mW}]}. \tag{4}$$

S_{21} [1] is the average S_{21} in magnitude, BW [GHz] is the f_{3dB} in GHz, (NF−1) [1] is the excess noise factor (of NF_{ave}) in magnitude, and P_D [mW] is P_D in mW. Table I is a summary of the two-stage LNA, and recently reported state-of-the-art two-stage (with two-path for gain enhancement and noise canceling) and three-stage CMOS LNAs with similar operation frequency. Our LNA at LN mode attains moderate f_{3dB}, S_{21}, and IIP3, low P_D, lowest NF, and the highest FOM. Our LNA at LP mode achieves moderate f_{3dB}, S_{21}, and IIP3, low NF, lowest P_D, and the highest FOM. Moreover, instead of the source-follower output buffer, a common-source (CS) output stage can be used for S_{21} enhancement (from 12.7 to 19.6 dB according to simulation). The remarkable results of our LNA indicate that it is promising for 5G systems.

IV. CONCLUSION

We demonstrate a 3–9-GHz CMOS LNA using body floating and self-bias technique. An enhancement in S_{21} and NF of the LNA is achieved due to the forward-biased V_{BS} (i.e., small V_{th}) and the transistors being free from the substrate leakage. Low P_D is achieved since low V_{DD} of 1 or 0.8 V is applicable because of small V_{th}. The eminent LP and LN performance (such as NF of 2.89 dB at P_D of 3.3 mW) of the LNA indicates that it is suitable for sub-6-GHz 5G systems.

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