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A 30-GHz Low-power CMOS LNA for 5G Communication Systems

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***Abstract*—This paper presents theoretical analysis and design procedures for low noise amplifiers (LNAs) in advanced CMOS technologies. For demonstration, a 30-GHz LNA designed for 5G millimeter-wave communication systems was fabricated in a 65-nm CMOS process. It provides a power gain of 22.6dB with a noise figure of 3.2dB while drawing 7.3mW from a 1.2V supply.**

***Index Terms*—low-noise amplifier(LNA), CMOS, low power, 5G communication, millimeter-wave(mm-wave), RFIC.**

I.INTRODUCTION

The CMOS process has been advanced into small feature sizes to pursue lower power consumption and higher integration level. Wireless transceiver system circuits also follow this trend and adopt ever more advanced CMOS technologies. In addition, the frequency of commercial wireless communication is being increased to handle higher data rates. Millimeter-wave frequency bands have been applied in the 5th generation wireless communication (5G) [1]~[7]. However, the high operating frequency makes circuits more sensitive to parasitics. Employing nanoscale CMOS process is a promising solution to reducing the parasitic effect. Therefore, it can be concluded that realizing mm-wave frequency bands wireless systems based on advanced CMOS process is of critical importance. This paper researches the design procedure and optimization of LNA which can be integrated into 5G receivers SoC in nanometer-scale CMOS technologies.

A number of inductive source-degeneration LNAs have been reported [8]~[12] proving that this structure still exhibits excellent performances in advanced CMOS technologies. In this work the special emphases are put on intuitive analyses to serve as the design guidelines for circuits design aiming for noise performance optimization. The advantages coming with the advanced small-size CMOS process are apparent, while it brings new features to IC designs. For RF circuits, transistors in the advanced technology have a higher cutoff frequency f_t which increases the operation frequency of amplifiers to mm-wave bands and reduces the noise figure. Noise contribution of transistors becomes relatively less significant, indicating that RF designers should pay more attention to other parasitic noise for the noise optimization.

In this paper, a 30-GHz LNA implemented in 65-nm CMOS is presented together with the detailed theoretical analysis. Section-II discusses the theory of inductive source-degeneration LNA and the emphasis is on one critical parameter, noise figure. Section III discusses the design of the LNA and reports the measurement results. Finally Section IV makes a conclusion.

II.CIRCUIT ANALYSIS

A. Impedance Matching and Noise Analysis

The most important goal of LNA design is to provide sufficient power gain with minimum noise figure. This requires LNA circuits perfectly satisfy the power matching and the noise matching according to two-port noise theory [13]. For the inductive source-degeneration circuit in Fig.1(a), the source impedance should satisfy Eq(1) and Eq(2).

$$Z_S = Z_{in}^* = \frac{g_m}{C_t}L_s - \left[\frac{1}{sC_t} + s\left(L_g + L_s\right)\right] \tag{1}$$

where $C_t = C_{gs} + C_{ex}$.

$$Z_S = Z_{s,opt} \tag{2}$$

so that the LNA will reach its maximum power gain and its noise factor F will reach its minimum F_{min}.

To provide an idea for understanding the noise performance, a deriving process of the noise factor for the single ind-degenerated CS stage is presented below.

Based on the two-port noise theory, noises in the circuit can be replaced with two noise generators e_n and i_n outside the network (Fig.1(a)). With these two equivalent noise generators, the noise factor can be expressed as:

$$F = \frac{\overline{e_s^2} + \overline{|e_n + Z_s i_n|^2}}{\overline{e_s^2}} = \frac{\overline{e_s^2} + \overline{|e_{nu} + e_{nc} + Z_s i_n|^2}}{\overline{e_s^2}}$$

$$= 1 + \frac{\overline{e_{nu}{}^2} + |Z_c + Z_s|^2 \overline{i_n^2}}{\overline{e_s^2}} = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} \tag{3}$$

where e_{nu} and e_{nc} are the noise voltage uncorrelated and correlated to the noise current i_n, Z_c is the correlated impedance. The noise sources can be regarded as resistors:

$$R_u = \frac{\overline{e_{nu}{}^2}}{4kT\Delta f} \tag{4}$$

$$R_s = \frac{\overline{e_s{}^2}}{4kT\Delta f} \tag{5}$$

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$$G_n = \frac{\overline{i_n^2}}{4kT\Delta f} \tag{6}$$

Let $\partial F/\partial Z_s = 0$, we can get the optimum noise source impedance and F_{min}:

$$R_{s,opt} = \sqrt{\mathrm{R}_u/G_n} \tag{7}$$

$$X_{s,opt} = -X_c \tag{8}$$

$$F_{min} = 1 + 2\sqrt{\mathrm{R}_u G_n} \tag{9}$$

For the single ind-degenerated CS stage, as shown in Fig.1, the two correlated noise generators represent the effect of the drain noise current i_{nd} and the induced gate noise i_{ng}:

$$e_n = \mathrm{j}\omega L_s i_{ng} + \frac{(1-\omega^2 C_t L_s)}{g_m} i_{nd} \tag{10}$$

$$i_n = i_{ng} + \frac{j\omega C_t}{g_m} i_{nd} \tag{11}$$

where $C_t = C_{gs} + C_{ex}$ is the capacitance taking the extra capacitor into account. The correlation factor ρ of e_n and i_n can be defined similar to the correlation factor c of i_{nd} and i_{ng}.

$$c = \frac{\overline{i_{ng}\, i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}}} = j|c| \tag{12}$$

$$\rho = \frac{\overline{e_n\, i_n^*}}{\sqrt{\overline{e_n^2}}\sqrt{\overline{i_n^2}}} \tag{13}$$

Then R_u, G_n, $R_{s,opt}$, and F_{min} can be indicated by actual noises i_{nd} and i_{ng}. Further, they are functions of g_m (the detailed derivation is given in the appendix).

$$G_n = \frac{1}{4kT\Delta f}\overline{i_n^2} = \omega^2 {C_t}^2 \frac{\gamma}{\alpha g_m}(1 + 2|c|p\alpha\chi + p^2\alpha^2\chi^2) \tag{14}$$

$$R_u = \frac{1}{4kT\Delta f}\frac{\frac{1-|c|^2}{{g_m}^2}\overline{i_{ng}^2}\,\overline{i_{nd}^2}}{\overline{i_n^2}} = \frac{\omega^2 {C_{gs}}^2 \frac{\gamma^2\chi^2}{{g_m}^2}(1-|c|^2)}{\omega^2 {C_t}^2 \frac{\gamma}{\alpha g_m}(1+2|c|p\alpha\chi+p^2\alpha^2\chi^2)} \tag{15}$$

$$R_{s,opt} = \sqrt{\mathrm{R}_u/G_n} = \frac{p\alpha\chi\sqrt{(1-|c|^2)}}{\omega C_t(1+2|c|p\alpha\chi+p^2\alpha^2\chi^2)} \tag{16}$$

$$F_{min} = 1 + 2\sqrt{\mathrm{R}_u G_n} = 1 + \frac{2}{\sqrt{5}}\sqrt{\gamma\delta(1-|c|^2)}\,\frac{\omega}{\omega_T} \tag{17}$$

where $p = C_{gs}/C_t$, $\alpha = g_m/g_{d0}$, $\chi = \sqrt{\delta/(5\gamma)}$.

These equations show the influence factors in the noise matching. Equations(16) and (17) indicate that the extra capacitor can adjust the optimum noise source impedance without affect F_{min}. However, there is always a gap between the actual noise factor F and its theoretical minimum F_{min} for the following reasons: 1) There is a small gap between power matching and noise matching theoretically. 2) Parasitism and higher-order effects influence the noise matching. 3) Process variation.

$$F - F_{min} = \frac{G_n}{R_s}\left[\left(R_s - R_{s,opt}\right)^2 + \left(X_s - X_{s,opt}\right)^2\right] \tag{18}$$

Eq(18) indicates that besides noise matching the gap between F and F_{min} is directly proportional to G_n which is larger with higher frequency and lower power (Eq(14)).

The matching procedure can be shown in the Smith chart (Fig.1(b)) intuitively. First, an extra capacitor C_{ex} is used to increase the real part of Z_{opt} up to R_S because the parasitic capacitance C_{gs} of M_1 is too small in the scaled CMOS process. The next step is to make the real part of Z_{in}^* equal to R_S by adjusting the degeneration inductor L_s. Then a series inductor L_g is put to change the imaginary parts of Z_{in}^* and Z_{opt} to zero simultaneously.

B. Optimization Techniques

i) Size of the CS MOSFET

According to the expressions of F_{min} (Eq(17)) and $(F - F_{min})$(Eq(18)), a larger gate width of MOSFET can improve these two indexes because ω_T and g_m are increased. But, of course it will consume more power. What's more, larger gate width means larger parasitic gate resistance which will worsen noise performance. As CMOS technology scaled, noise contributed by parasitism is increasing compared to MOSFETs. So there is a tradeoff when designing the gate width of CS MOSFET. For demonstration, the first stage M_1 of LNA in this paper is designed as: finger width=1.26μm, number of fingers=10.

ii) The extra noise-matching capacitor C_{ex}

Although the C_{ex} has no influence on F_{min} according to Eq(17), it reduces the gain of the first stage M_1 and thus reduces its suppression of the noises from the following components. As a result, the C_{ex} increases the F_{min} of the total circuit. So the extra capacitor should not be too large. In this design, it has a value of 14.3*fF*.

C. Effect of Inter-stage inductor

In order to raise the gain, improve input–output reverse isolation and enhance stability, a common gate transistor M_2 is generally used to form a cascode structure. A series inductor L_X between M_1 and M_2 can improve performances of the cascode LNA.

i) L_X improves noise figure

Noise contribution of the first transistor M_1 is relative low in advanced CMOS processes, so the noise after M_1 (such as noise from M_2) is not negligible in this LNA design. Fig.2(a) shows a simplified small signal model to calculate the noise contribution of M_2. C_X stands for the parasitic capacitance of node *X* without L_X, Z_{out1} stands for the output impedance of common source stage, and i_{n2} stands for the total noise current of M_2. Then the output noise current produced by i_{n2} can be expressed as Eq(19).

$$i_{o,noise} = \frac{1}{1+g_{m2}(Z_{out1}//Z_{CX})} i_{n2} \tag{19}$$

$$Z_{out1} = \frac{1+r_{ds1}(g_m+\varphi)}{\varphi} \tag{20}$$

$$\varphi = \frac{\frac{1}{sC_t}+s(L_g+L_s)}{\left(\frac{1}{sC_t}+sL_g\right)sL_s} \tag{21}$$

The parasitic C_X is the primary factor deteriorating noise contribution of M_2, because Z_{out1} is infinity when C_t resonates with L_g+L_s. And this deterioration can be improved by inserting a series inductor L_X.

As shown in Fig.2(a), after inserting L_X the equivalent impedance of L_X, C_{X1} (parasitic capacitance of M_1) and C_{X2} (parasitic capacitance of M_2) is

$$Z' = \frac{1}{sC_{X2}} // (sL_X + sC_{X1}) \tag{22}$$

$Z' = \infty$ when L_X is resonant with C_{X1} and C_{X2}.

$$\frac{1}{sC_{X1}} + \frac{1}{sC_{X2}} + sL_X = 0 \tag{23}$$

So the noise contribution of M_2 is minimized according to Eq(19).

ii) L_X raises gain

Another advantage of adopting L_X is raising the total gain. This can be explained by that L_X improves the power impedance matching between M_1 and M_2. Of course, the optimum inductance of L_X for power matching is different from the value for noise optimization as shown in Fig.2(b). So designers have to make a tradeoff regarding multiple factors.

iii) L_X influences input impedance

The input impedance is influenced by the load of M_1 through the parasitic capacitance C_{gd}. And L_X changes the load of M_1 so that the input impedance of LNA is changed.

III.CIRCUIT DESIGN AND MEASUREMENT RESULTS

Applying simultaneous noise and input matching technique, a cascode LNA (Fig.3) was designed in 65-nm CMOS. To provide sufficient power gain, it has two stages. The noise contribution of the second stage will be suppressed as the first stage has an appropriate gain. Both the two stages employ cascode structure to achieve good isolation and stability. Between the two stages, a capacitor is used to realize ac-coupling and inter-stage conjugate matching. MOSFETs are biased by an optimum current density $J_D \approx 0.2mA/\mu m$, under which the LNA has the best NF. For input and output matching the parasitic capacitance of RF pads must be taken into account.

Measurement results of this LNA are shown in Fig.4 and Table-1. Some other works are also listed to provide a comparison. This LNA possesses an excellent noise factor (NF=3.2dB) with a low power consumption because more attention is paid to the noise matching network and thereby large current is not necessary to reduce NF. The figure of merit (FoM) is calculated for comparison, which is defined as below.

$$\text{FoM} = \frac{Gain(dB) \cdot BW(GHz)}{[NF(dB) - 1] \cdot P_{DC}(mW)}$$

IV. CONCLUSION

This paper presents a 30-GHz LNA fabricated in a 65-nm CMOS process. It achieves lower noise figure while comparing to other state-of-the-art LNAs operating around 30-GHz. In addition, very low power is consumed, making it competitive in micro-equipment and 5G communications.

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APPENDIX

DERIVATION OF THE F_{min} FOR AN MOSFET WITH A SOURCE INDUCTOR AND AN EXTRA CAPACITOR

A noise analysis is given based on the two-port noisy theory (Fig.1(a)). The noise generators e_n and i_n are the equivalents of the noises of M_1.Thus their mean square values can be derived.

$$\begin{aligned}\overline{e_n^2} &= \overline{\left(\jmath\omega L_s \imath_{ng} + \frac{(1-\omega^2 C_t L_s)}{g_m}\imath_{nd}\right)\left(-\jmath\omega L_s \imath_{ng}^* + \frac{(1-\omega^2 C_t L_s)}{g_m}\imath_{nd}^*\right)} \\ &= \omega^2 L_s^2 \overline{\imath_{ng}^2} + \frac{(1-\omega^2 C_t L_s)^2}{{g_m}^2}\overline{\imath_{nd}^2} - 2|c|\omega L_s \frac{(1-\omega^2 C_t L_s)}{g_m}\sqrt{\overline{\imath_{ng}^2}}\sqrt{\overline{\imath_{nd}^2}}\end{aligned} \tag{24}$$

$$\begin{aligned}\overline{i_n^2} &= \overline{\left(\imath_{ng} + \frac{J\omega C_t}{g_m}\imath_{nd}\right)\left(\imath_{ng}^* - \frac{J\omega C_t}{g_m}\imath_{nd}^*\right)} \\ &= \overline{\imath_{ng}^2} + \frac{\omega^2 {C_t}^2}{{g_m}^2}\overline{\imath_{nd}^2} + 2|c|\frac{\omega C_t}{g_m}\sqrt{\overline{\imath_{ng}^2}}\sqrt{\overline{\imath_{nd}^2}}\end{aligned} \tag{25}$$

$$\begin{aligned}\overline{e_n \imath_n^*} &= \overline{\left(\jmath\omega L_s \imath_{ng} + \frac{(1-\omega^2 C_t L_s)}{g_m}\imath_{nd}\right)\left(\imath_{ng}^* - \frac{J\omega C_t}{g_m}\imath_{nd}^*\right)} \\ &= j\left(\omega L_s \overline{\imath_{ng}^2} - \frac{\omega C_t(1-\omega^2 C_t L_s)}{{g_m}^2}\overline{\imath_{nd}^2} + |c|\frac{2\omega^2 C_t L_s - 1}{g_m}\sqrt{\overline{\imath_{ng}^2}}\sqrt{\overline{\imath_{nd}^2}}\right)\end{aligned} \tag{26}$$

$$4kT\Delta f G_n = \overline{i_n^2} \tag{27}$$

$$4kT\Delta f R_u = \overline{\mathrm{e}_{nu}^2} = \overline{\mathrm{e}_n^2} - \overline{\mathrm{e}_n^2}\rho^2 = \overline{\mathrm{e}_n^2} - \overline{\mathrm{e}_n^2}\frac{\left|\overline{e_n \imath_n^*}\right|^2}{\overline{\mathrm{e}_n^2}\overline{\imath_n^2}}$$

$$= \frac{\overline{e_n^2}\overline{i_n^2} - |\overline{e_n i_n^*}|^2}{\overline{i_n^2}} = \frac{\frac{1-|c|^2}{gm^2}\overline{i_{ng}^2}\,\overline{i_{nd}^2}}{\overline{i_n^2}} \quad (28)$$

Inserting $\overline{i_{nd}^2} = 4kT\Delta f\gamma g_{d0}$ and $\overline{i_{ng}^2} = 4kT\Delta f\delta(\omega^2 C_{gs}^2/5g_{d0})$ into (24)-(28) yields

$$F_{min} = 1 + 2\sqrt{R_u G_n} = 1 + 2\frac{1}{4kT\Delta f}\frac{\sqrt{1-|c|^2}}{g_m}\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}}$$

$$= 1 + \frac{2}{\sqrt{5}}\sqrt{\gamma\delta(1-|c|^2)}\frac{\omega}{\omega_T} \quad (29)$$

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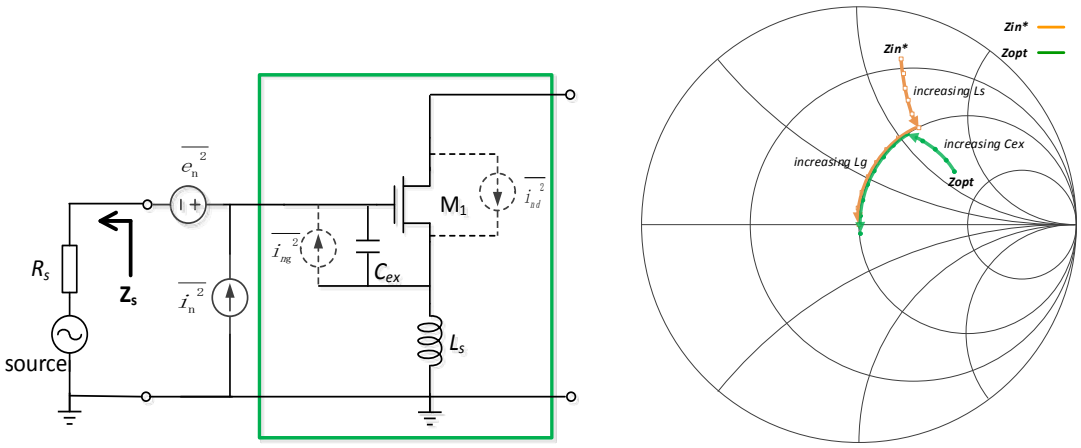


(a) (b)

Fig.1 Noise analysis (a) equivalent circuit based on two-port theory (b) noise matching in Smith chart

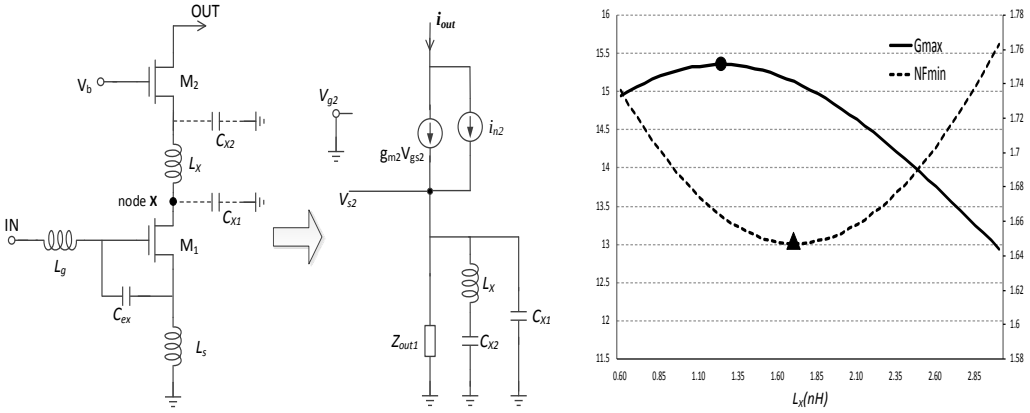


Fig.2 Effect of L_X (a)the simple equivalent circuit (b) simulated G_{max}/NF_{min} varies with L_X

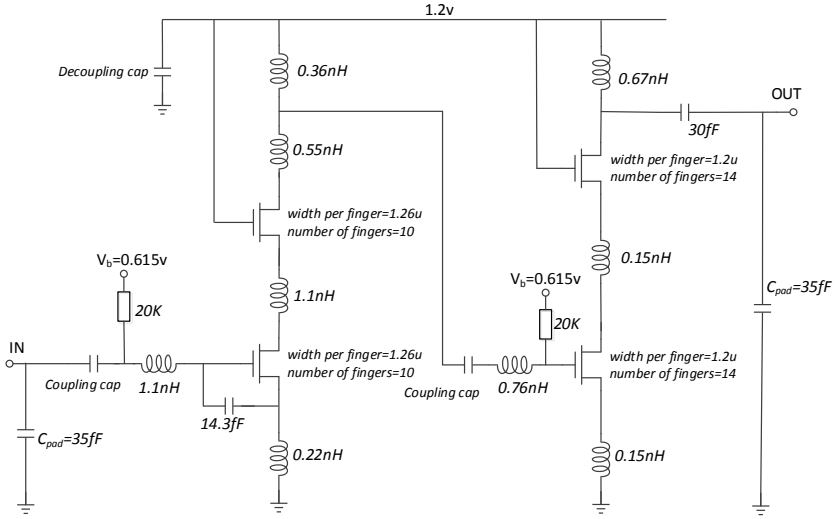
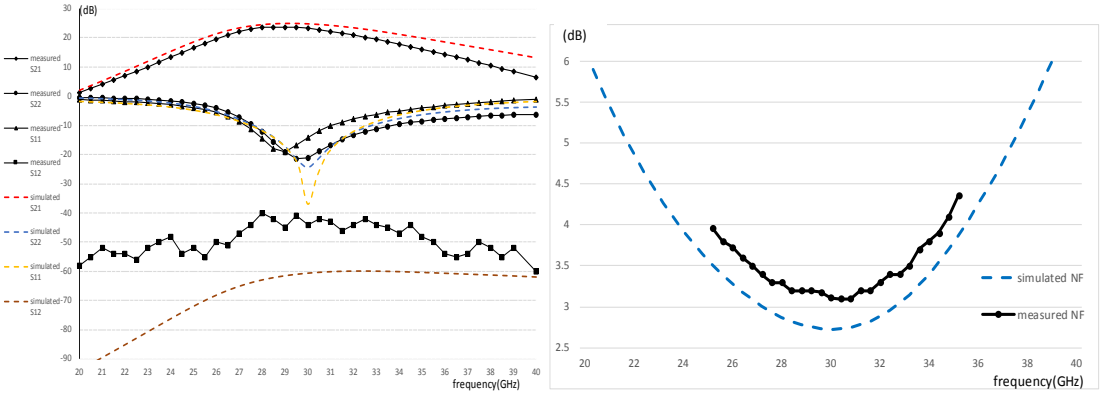


Fig.3 Schematic of the two-stage LNA



(a) (b)

Fig.4 Simulated and measured results (a)S-parameter response (b)noise figure

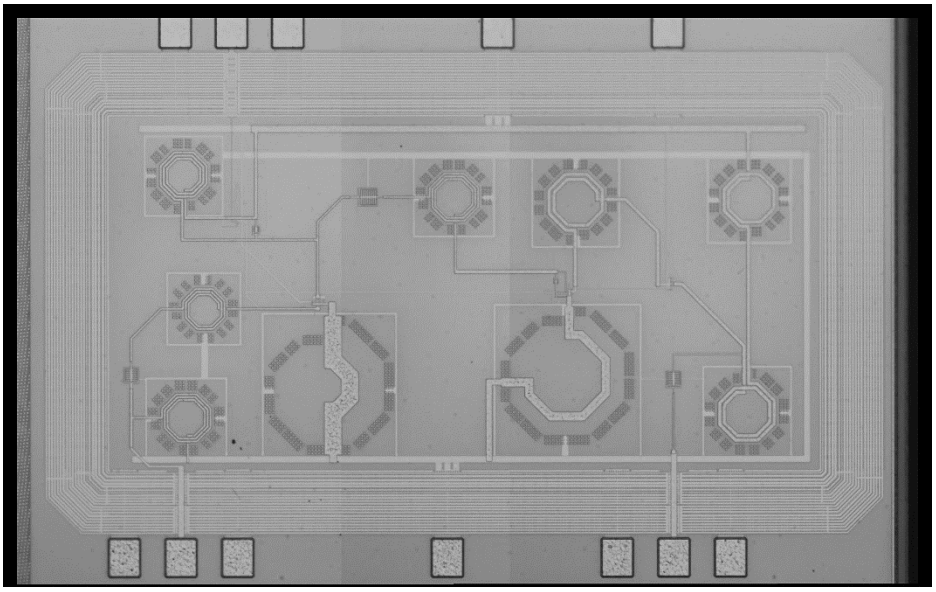


Fig.5 Chip micrograph

Table 1. Performance summary and comparison with 5G LNAs

Ref.	Tech.	Freq. (GHz)	Max Gain (dB)	Min NF (dB)	P_{DC} (mW)	FOM
[20]	65nm	15.8-30.3	10.2	3.3	12.4	5.19
[21]	65nm	46-60	16	4.5	10	6.22
[22]	28nm	91	32	5.3	36	0.21
[9]	28nm	33	18.6	4.9	9.7	0.49
[23]	65nm	28	18.2	3.9	9.8	0.64
This work	65nm	30	22.6	3.2	7.3	1.41