2018 International Conference on Applied Electromagnetics, Signal Processing and Communication (AESPC)

Design, Reliability Investigation and Analysis of 60 GHz band LNA in 65nm CMOS for 5G Mobile Communication

Ramuswaminaath J
Robert Bosch Engineering and Business Solutions Pvt Ltd
CHIL SEZ IT Park
Coimbatore, India

Mageshwaran Swaminathan
Ericsson India Global Services
Bagmane World Technology Centre
Bengaluru, India

Kalyan Bhattacharyya
School of Electronics Engineering
Kalinga Institute of Industrial Technology
Bhubaneswar, India
kalyan.bhattacharyyafet@kiit.ac.in

Abstract—A LNA has been designed in Cadence simulator in 60 GHz band (57-64 GHz) in 65nm CMOS with microstrip as on-chip inductors. LNA has gain of 11.55 dB at 60 GHz. The noise figure is 4.98 dB at 60 GHz. The 3-dB bandwidth for this LNA design is 57-64 GHz. The stability factor (K) is greater than 1 for the entire range. Additionally, the 1-dB gain compression point (P_{1dB}) is -10.0229 dBm and the IIP3 value is -2.2 dBm at 60 GHz. PVT (Process-Voltage-Temperature) simulations is also done for reliability investigation and analysis where the performance of LNA is tested under various process corners, temperatures and voltages. Gain of the amplifier was observed under different process corners, temperatures (from -40°C to 100°C) and voltages. It was observed that the amplifier's gain was invariant in the voltage variation range of 1 - 1.4 V. Moreover, we observed that the higher peak in the gain graph is due to the fast-fast process corner parameter and the lower peak is due to the slow-slow process corner parameter. The highest peak gain was observed for the Fast-Fast process corner and at low temperature of -40°C and lowest peak gain for Slow-Slow process corner and at high temperature of 100°C. FoM (figure of merit) is 0.92 GHz/mW at 60 GHz. Hence a reliable design of LNA is achieved for the 60 GHz band for 5G mobile communication application.

Keywords— LNA, PVT, RF Amplifier, RF CMOS

I. INTRODUCTION

Nano-scale bulk silicon CMOS technologies are used for the design of RF circuits because of the advantages they provide such as small feature size, good performance in high frequency and low cost as compared to fully depleted (FD) Silicon-on-Insulator (SoI) CMOS. The 60 GHz frequency band (57 – 64 GHz) is being used for the 5G mobile communication. This mm-wave frequency provides sufficient bandwidth of high data rate communication. The 60GHz band is used for short distance mobile communication because of the attenuation of RF signals due to huge absorption of signal by the oxygen molecules. Oxygen molecules provides high immunity in terms of interference and security. In reference [1], The LNA has used a three cascode stages and has the noise figure of 7.2dB and has the power consumption of 65mW. Reference [2] has designed a LNA in 65nm technology with f_t of 210GHz and f_{max} of 240GHz .The design uses two common source stage followed by two cascode stage. The noise figure of the circuit is 5.9dB and power consumption of 30.8mW. Reference [3] uses single-ended input and differential output. This LNA has a noise figure of 6.1 dB and current consumption of 29mA.

The main objective of this paper is reliable design of a 60 GHz band LNA with high gain (S_{21}), better noise figure, less input reflection S_{11} and less power consumption PVT tolerant/invariant. The LNA is then tested for reliability using PVT (Process-Voltage-Temperature) simulation in Cadence virtuoso and analyzed. The major problem faced in the design of a Low Noise Amplifier (LNA) is that the amplifier must have a very low noise figure (NF), a very small input reflection (S_{11}) and must have a high gain (S_{21}). Since there is always a trade-off between these parameters, different topologies must be combined to achieve an overall high performance. For instance, common-gate (CG) stage have reduced noise figure but have a very low input impedance. Common-source (CS) stage provides a very high gain but need LNAs in cascade. Cascode stage provides the advantage of high gain and high bandwidth. Common source with source degeneration inductor is used for input matching, for better linearity and is used to achieve low-noise performance. Another problem addressed is that there is no reliability investigation for the 5G LNA design to

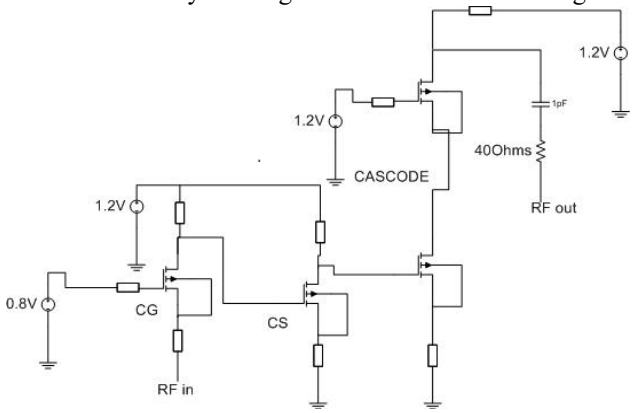

Fig. 1. Simplified Schematic of the common-gate common-source cascode LNA with inductive microstrip lines as on-chip inductors.

978-1-5386-8333-0/18/$31.00 ©2018 IEEE

the best of our knowledge, which happens because of the change in doping concentration related mobility variations

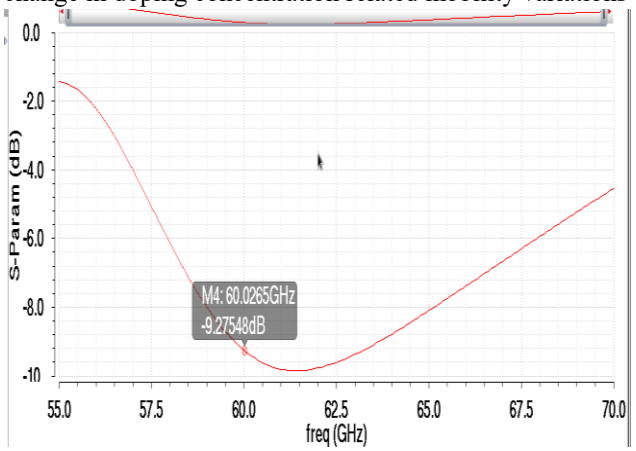

Fig. 2. Input reflection S_{11} for the LNA is around -9.275 dB at 60 GHz for microstrip designs in 65nm.

in 8-inches /12-inches silicon wafer, this causes change in the transconductance g_m of the MOSFET [4], [5]. The change in temperature causes change in mobility (μ) of electrons (higher till -40°C temperature and lower for high 100°C) [5] and fluctuations in voltage levels needs to be addressed.

We have designed this LNA in the 65nm with microstrip transmission lines as on-chip inductor as shown in fig 1. The LNA has a common-gate (CG) stage n-MOSFET followed by a common-source (CS) stage n-MOSFET and then a cascode stage.

II. Design of LNA

First, Noise figure (NF) being a parameter of interest of a cascade of LNAs is found by employing Friis equation in the form

$$NF_{Total} = NF_{1,LNA} + \frac{NF_2 - 1}{G_{1,LNA}} \quad (1)$$

It can be seen that the NF of the first stage governed the NF of the cascade as the subsequent stages play only a little role in determining the overall NF [6] as divided by gain of preceding stage. So using a CG stage at first greatly reduces the overall NF as CG have a smallest NF performance. The next requirement of a LNA is to have a high gain. This is achieved by a CS stage and a cascode stage which provides high gain as well as high stability and bandwidth. Width and the number of fingers of the n-MOSFETs present in the circuit is calculated using parametric sweep. Number of fingers used is 32 for all the transistors in the circuit. Generally more the number of fingers in layout, less is the gate parasitic resistance. The source degeneration (L_S) and the gate matching (L_G) inductors are for canceling the imaginary part of input impedance and making match for real part of nearly 50 ohm, designed using the formula given below.

$$L_S = \frac{Z_0 - R_g - R_S}{2\pi f_T} \quad (2)$$

$$L_G \approx \frac{\omega_T}{\omega^2 g_{meff}} - L_S \quad (3)$$

where, R_g and R_s are gate resistance and source resistance

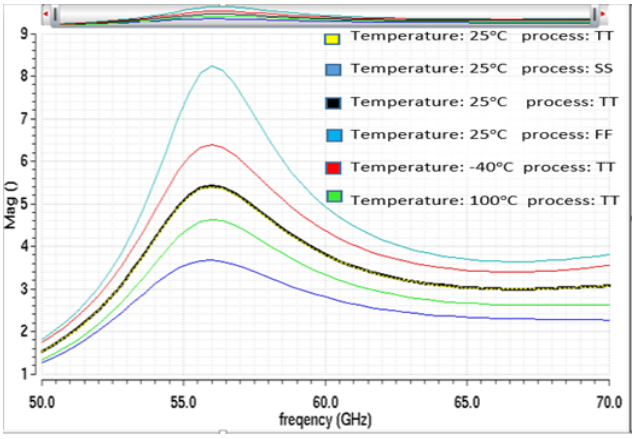

Fig. 3. PVT simulation of Gain (S_{21}) for various temperature and processes.

respectively, f_T is the unity current gain and g_{meff} is the effective transconductance of the first n-MOSFET [6].

III. Simulation Results

A. S-parameter Simulation

S-parameter simulation is carried out to find out the gain, noise figure, reflections etc. using UMC foundry RVTRF transistors.

The LNA has a gain of 11.55dB at 60GHz and has a 3-dB bandwidth of 9GHz ranging from 57-64GHz. The input reflection (S_{11}) of the amplifier is -9.275dB as shown in fig. 2. The noise figure of 4.98 dB is achieved which is shown in Fig.3. The LNA is unconditionally stable in the 57-64GHz band and also highly linear with P_{1dB} being -10.0229 dBm and IIP3 being -2.2 dBm.

B. PVT Simulation

Note in Process-Voltage-Temperature (PVT) simulation, the performance of LNA is tested under different processes, temperatures and voltages. Change in Gain (S_{21}) and Noise Figure (NF) was observed under different conditions. It was observed that for the Fast-Fast process, gain was at its maximum of 18.27 dB at 25°C as shown in Fig. 4. For the Slow-Slow process, gain had the minimum value of 11.2 dB at 25°C. This is because of the change in electron mobility (which may caused due to the change in doping concentration) from higher to lower of Fast-Fast and Slow-Slow MOSFETs. At the temperature of -40°C, gain was 16.25 dB. At the temperature of 100°C, the gain was 13.06 dB, happens because of the decrease in mobility (μ) of the electrons which accounts for around 20% because the increase in temperature causes the phonon scattering effect, results in decrease in μ_n and transconductance (g_m) of the MOSFET [4], [5], [8]. For the change in temperature, the threshold voltage changes by -1mV/°K which works in opposite direction to mobility, but since the effect of change in overdrive voltage ($V_{GS} - V_t$) is a minor as compared to

change in μ_n and gm, the latter dominates stipulating the performances. It can be inferred that for the change of temperature from -40ºC to 100ºC the gain changes from 16.25 dB to 13.06 dB. Likewise, for the Fast-Fast process and for the temperature of -40ºC, minimum NF of 4 dB is achieved and for the Slow-Slow process and for the

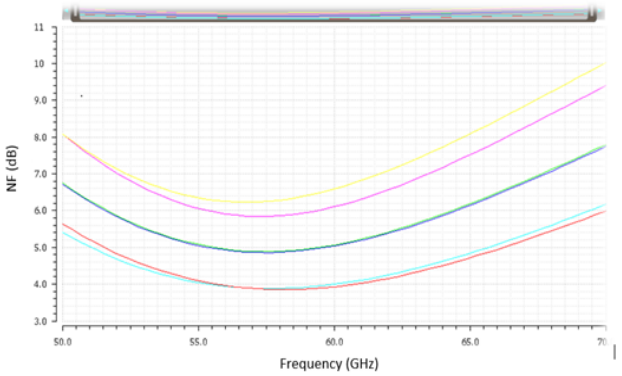

Fig. 4. PVT simulation of Noise Figure (NF) for various temperature and processes.

temperature of 100ºC, the worst NF of 6.5 dB is noted. Also we inferred that the LNA is invariant when the voltage is changed 16.66% from the supply voltage of 1.2V (1V-1.4V). This shows the reliability of the amplifier for the vast range of temperatures, process corners and voltages.

TABLE I
PVT simulation results for current and power consumption

Temperatures (ºC)	Process Corners	Current drawn (mA)	P_{DC} (mW)
25	TT (Typical Typical)	31.40	36.64
25	FF (Fast Fast)	34.73	39.87
25	SS (Slow Slow)	28.56	32.95
-40	TT	32.73	38.31
100	TT	29.86	34.84

IV. Discussion

Table I present the values of current drawn and power consumption for different temperatures and process corners. It can be observed that the Fast-Fast MOSFET with the temperature of 25ºC has the maximum current and power consumption, also maximum gain (S_{21}) and minimum noise figure (NF). Typical-Typical MOSFET with the minimum temperature of -40ºC has the second maximum current consumption and the power consumption, also second maximum gain (S_{21}) and second least noise figure (NF). This is because of the high mobility (μ_n) of the electrons which increases the transconductance (g_m) [5] of the MOSFET in above two cases. Increase in resistivity of metal lines [7] accounts for around 20%, causing change in characteristics impedance Z_0 [8]. The reflection coefficient Γ [8], more precisely the S_{11} is changing by 23% (from TT to SS) and 9% (from TT to FF) during process corners and 11% during temperature variations from nominal (25ºC) to high. By (4), transconductance and drain current (I_D) are directly proportional and hence current drawn also increases [7], [9].

$$g_m = \mu_n C_{OX} W/L (V_{GS} - V_t) \quad (4)$$

For the temperature variation from -40ºC to 100ºC there is

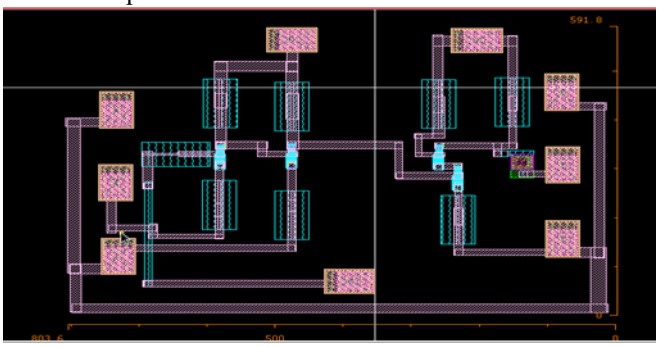

Fig. 5. Layout diagram of 65nm 60GHz LNA.

change of ±3 mW power consumption from room temperature of 25ºC, higher at -40ºC and lower at 100ºC and likewise for process corners also 3mW as reported in Table I. The net effect of increase of g_m, decrease of metal resistivity with better S_{11} (i.e. input matching) responsible for higher gain and improved NF of the LNA at TT process with -40ºC temperature (and opposite performance at 100ºC) [8]. Thus the LNA has reliable performance as there is not much changes in performances for the different processes, temperatures (-40ºC to 100ºC) and voltages (1-1.4V) along with the stable behaviour in 57-64 GHz band. High gain and low noise figure achieved causing good FoM [6] of 0.92 GHz/mW. Fig 5 shows the layout of the LNA has the area of 0.59 x 0.8 mm^2.

V. References

[1] B. J. Huang *et al*., "Design and Analysis for a 60-GHz Low-Noise Amplifier with RF ESD Protection," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 2, pp. 298-305, Feb. 2009.

[2] A. Natarajan, S. Nicolson, Ming-Da Tsai and B. Floyd, "A 60GHz variable-gain LNA in 65nm CMOS," *2008 Digests IEEE Asian Solid-State Circuits Conference*, Fukuoka, pp. 117-120, 2008.

[3] C. Weyers, P. Mayr, J. W. Kunze and U. Langmann, "A 22.3dB Voltage Gain 6.1dB NF 60GHz LNA in 65nm CMOS with Differential Output," Digests *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, pp. 192-606, 2008.

[4] Kalyan Bhattacharyya and T. H. Szymanski, "Temperature Characteristics and Analysis of Monolithic Microwave CMOS Distributed Oscillators With Gm-Varied Gain Cells and Folded Coplanar Interconnects," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 7, pp. 1332-1336, July 2012.

[5] Kalyan Bhattacharyya, "Tunable distributed harmonic voltage controlled oscillator for generating second and third harmonic microwave signals in 180nm CMOS," *2016 Digests International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI-SATA)*, Bangalore, pp. 1-4, 2016.

[6] Sorin Voinigescu, High-frequency integrated circuits, University of Toronto, Cambridge Univ. Press, 2013, pp. 450-467.

[7] B. Razavi, "CMOS technology characterization for analog and RF design," IEEE J. Solid-State Circuits, vol. 34, pp. 268–276, Mar. 1999.

[8] Kalyan Bhattacharyya and M. Jamal Deen, "Microwave CMOS Travelling Wave Amplifiers: Performance and Temperature Effects," IEEE Microwave and Wireless Components Letters, vol. 14, no. 1, pp. 16-18, January 2004.

[9] Kalyan Bhattacharyya and Sharma, D.K., "A comparative study of

different gain cells based microwave CMOS distributed oscillators," Microwave and Optical Technology Letters, vol. 58, no. 11, pp. 2581-2587, November 2016.