

# **CMOS ANALOG COURSE PROJECT**

*TWO STAGE OTA DESIGN*

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# 1 Project I

## 1.1 Handwritten

### NOISE :

$$V_{n_{eq}} = \frac{16kT}{3g_m} \quad \text{Designing for } V_n = 10 \text{ nV}/\sqrt{\text{Hz}}$$

$$(10 \text{ nV}/\sqrt{\text{Hz}})^2 = \frac{16kT}{3g_m}$$

$$g_m = \frac{16kT}{100 \times 3 \times 10^{18}} = \frac{16 \times 1.38 \times 10^{-23} \times 300}{100 \times 3 \times 10^{18}}$$

$$g_m = 220.80 \mu\text{s}$$

### UNITY GAIN FREQUENCY :

$$2\pi f_u \times 1 = \frac{g_m b}{g_c} \times \frac{g_m i}{g_B} \times P_D$$

$$P_D = \frac{g_B / C_C}{g_m b / g_c}$$

$$2\pi f_u = \frac{g_m i}{C_C} \frac{g_m b / g_c}{g_m b / g_c}$$

$$C_C = \frac{g_m i}{2\pi f_u} = \frac{220.80 \text{ pF}}{2\pi \times 70}$$

$$C_C \approx 502.02016 \text{ fF}$$

### SLEW RATE :

$$S.R. = \frac{dV}{dt} = \frac{2\pi f_u}{C_C}$$

$$\text{ slew rate} = \frac{\pm I_{SS}}{C_L} \approx 1 \mu\text{s}$$

$$\Rightarrow I_{SS} = 60 \times 0.5 \text{ mA}$$

$$I_{SS} = 30 \text{ mA}$$

$$I_{DS} = \left(1 + \frac{C_L}{C_C}\right) I_{SS} \text{ mA}$$

$$I_{DS} = 90.121 \mu\text{A}$$

$K_n$  is obtained by performing DC analysis on the native nMOS

### DIFF. PAIR SIZE

$$g_{m_1} = \sqrt{I_{SS} \cdot K_n \cdot (W_L)} \quad K_n = \left(\frac{0.9}{1.5}\right) 658 \mu \text{A/V}^2 \approx 390 \mu \text{A/V}^2$$

$$220.80 = \sqrt{30 \times 10^{-6} \times 390 \times 10^{-6}}$$

$$(W_L)_1 = \frac{220.80}{30 \times 390}$$

$$(W_L)_1 = 4.167$$

### PHASE MARGIN:

$$\text{PM} = 90^\circ - \tan^{-1}\left(\frac{f_{GBW}}{f_{RR}}\right)$$

$$30^\circ = \tan^{-1} \left( \frac{f_{FBW}}{f_{ND}} \right)$$

$$f_{ND} = \sqrt{2} f_{FBW} = 121.243 \text{ MHz}$$

$$2\pi f_{ND} = \frac{g_{m_b}}{C_L}$$

$$g_{m_b} = 2\pi \times C_L \times f_{ND} = 2\pi \times 121.243 \mu\text{s}$$

$$g_{m_b} = 761.795 \mu\text{s}$$

$$k_p = 700 \times 10^6 \times (45/120) = 262.5$$

$$(w_L)_b = \frac{\frac{g^2}{g_{m_b}}}{2I_{oss} \cdot k_p} = \frac{\frac{761.795^2}{2 \times 90.121 \times 262.5}}{12.265}$$

$$(w_L)_b = 12.265$$

$$R_2 = \frac{1}{g_{m_b}} \left( 1 + \frac{C_L}{C_C} \right) = \frac{10^6}{761.795} \left( 1 + \frac{1}{0.50202} \right)$$

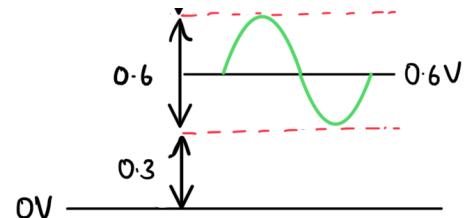
$$R_2 = 3927.49 \Omega$$

$$V_{DQDZ} = \sqrt{\frac{2 \times 78}{262.5 \times 28}} = \frac{0.157}{1.2V - 0.3 \downarrow}$$

CURRENT MIRROR SIZES :

$$K_n = 445 \times \left( \frac{75}{120} \right) u$$

$$= 278.125$$



$$0.3 = \sqrt{\frac{2 \times 78 u}{278.125 (W_L)_7}}$$

$$(W_L)_7 = \frac{2 \times 90}{278.125 \times 0.3^2} = 7.191 \approx 7$$

$$(W_L)_{3,4} = \frac{I_{SS}/2}{I_{DS}} (W_L)_6$$

$$= \frac{30/2 \times 12.265^2}{90.121} = 0.041$$

$$A_{V_1} = \frac{g_{m_1}}{g_{ds_2} + g_{ds_4}} = \frac{220.80}{(\lambda_n + \lambda_p) 30/2}$$

$$= \frac{7.36 \times 2}{11.12} = 14.72$$

$$(\lambda_{n_1} + \lambda_p) \quad (\lambda_{n_1} + \lambda_p)$$

$$Av_2 = \frac{g_{m6}}{g_{ds_6} + g_{ds_7}} = \frac{761.795}{(\lambda_{n_2} + \lambda_p) \cdot 90}$$

$$= \frac{8.464}{(\lambda_{n_2} + \lambda_p)}$$

$$20 \log_{10} \text{gain} = 48 \text{ dB}$$

$$\text{gain} = 251.18$$

$$Av_1, Av_2 \geq 251.18$$

$$\frac{120.59}{(\lambda_{n_1} + \lambda_p)(\lambda_{n_2} + \lambda_p)} = 251.18$$

$$(\lambda_{n_1} + \lambda_p)(\lambda_{n_2} + \lambda_p) = 0.496$$

$$4\lambda^2 = 0.496$$

$$\lambda = 0.352$$

$$\boxed{\lambda_1 L_1 = \lambda_2 L_2}$$

Native nMOS : (dibp pair) :

$$0.696 \times 300 \text{ nm} = 0.352 \times 4 \text{ (in nm)}$$

$$L_2 = 600 \text{ nm}$$

$$(W/L)_2 = 4$$

and  $w_1$  and  $w_4$  same as  $w_2$   
and  $L_2$

$$w_2 = 2.4 \mu$$

LOW  $V_T$  MOSFET DIMENSIONS :

low  $V_T$  nMOS ( $M_7$ ) :

$$0.585 \times 45 \text{ nm} = 0.352 \times L_7 \text{ (in nm)}$$

$$L_7 = 74.78 \text{ nm} \approx 80 \text{ nm}$$

$$(W/L)_7 = 7$$

$$w_7 = 523.46 \text{ nm} \approx 600 \text{ nm}$$

low  $V_T$  pMOS ( $M_6$ ) :

$$0.41 \times 45 \text{ nm} = 0.352 \times L_6 \text{ (in nm)}$$

$$L_6 = 52.41 \text{ nm}$$

$$(W/L)_6 = 12.26$$

$$(W/L)_4 = 2.33$$

$$w_6 = 642.80 \text{ nm}$$

$$w_4 = 122.37 \text{ nm}$$

$$I_{SS} = 30 \mu A$$

$$I_{OSS} = 90 \mu A$$

$$\left(\frac{W}{L}\right)_S^2 = \frac{I_{SS}}{I_{OSS}} \left(\frac{W}{L}\right)_T$$

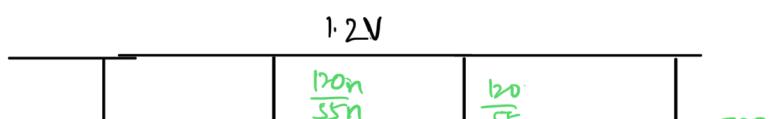
$$= \frac{1}{3} \left(\frac{W}{L}\right)_T$$

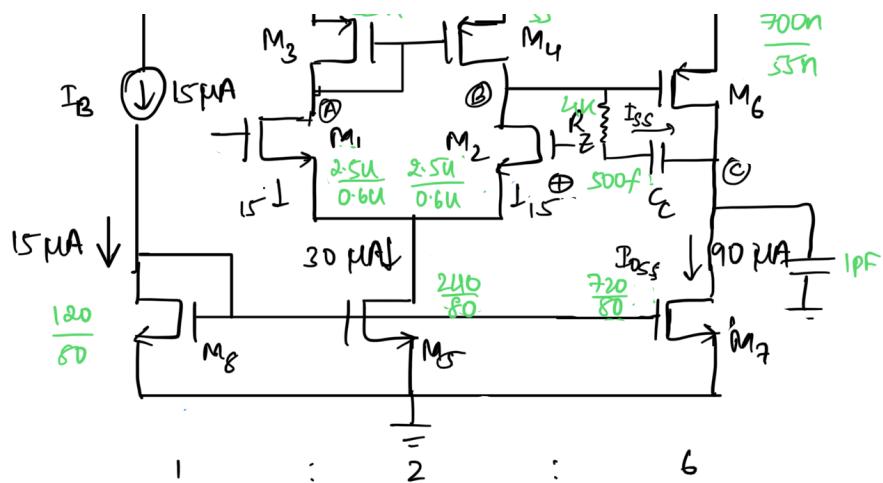
So, we can use an ideal current source of  $15 \mu A$  and scale it by 2 and 6 using current mirrors  $M_5$  and  $M_7$  to generate  $30 \mu A$  and  $90 \mu A$

$$\left(\frac{W}{L}\right)_{\text{ideal}} = \frac{120n}{80n}$$

$$\left(\frac{W}{L}\right)_S = \frac{240n}{80n}$$

$$\left(\frac{W}{L}\right)_T = \frac{720n}{80n}$$





In the schematic length can be increased without altering the  $(W/L)$  ratio to increase the gain.

Also,  $C_c$  is reduced to increase the slew rate.

## 1.2 Schematic

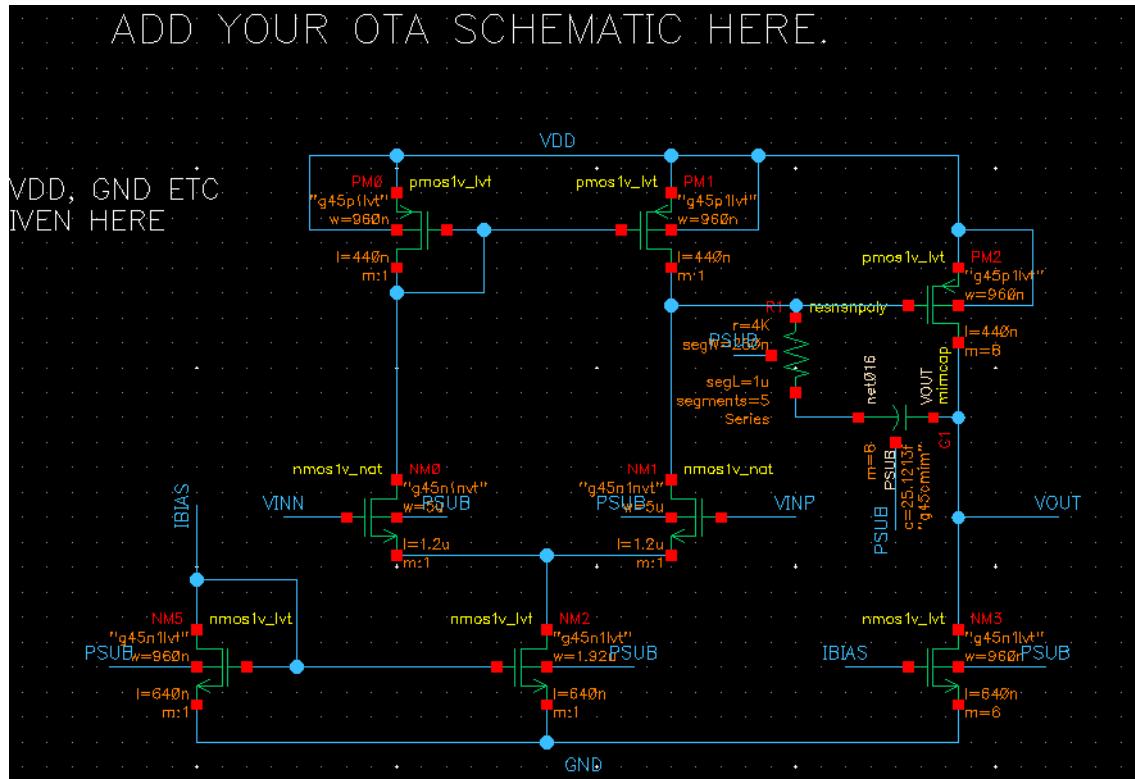


Figure 1: Final Schematic

## 1.3 DC Operating Point

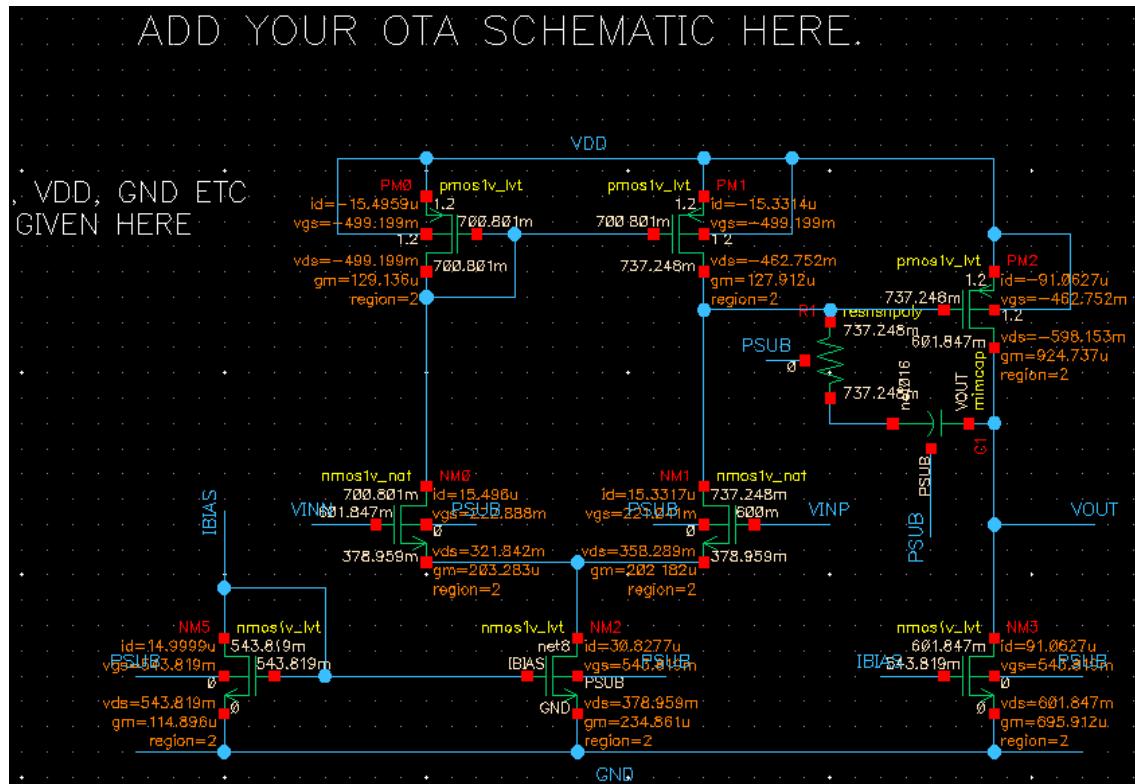


Figure 2: DC operating point

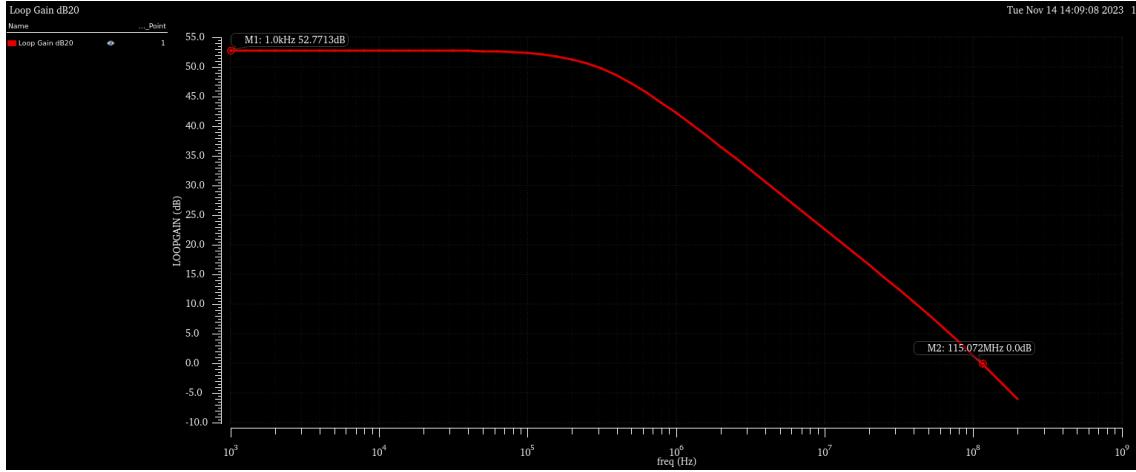


Figure 3: DC Gain Plot

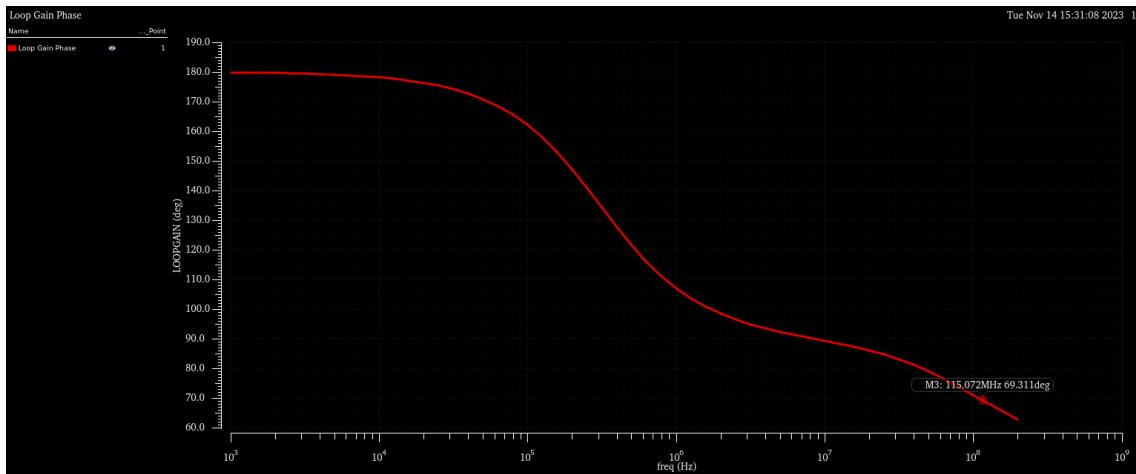


Figure 4: DC Phase Plot

## 1.4 Stability

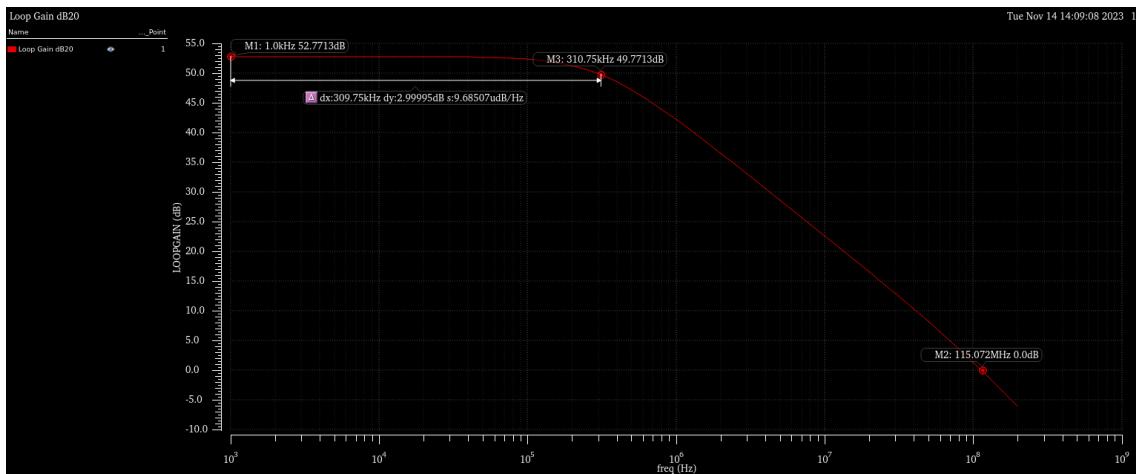


Figure 5: Stability analysis

Stability Summary - circuit "TB_STB_LG" with loop probe "IPRB0"				
Design_Point	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)
1	69.287	114.48M	nan	nan

Figure 6: Stability summary

## 1.5 AC analysis: Differential Gain

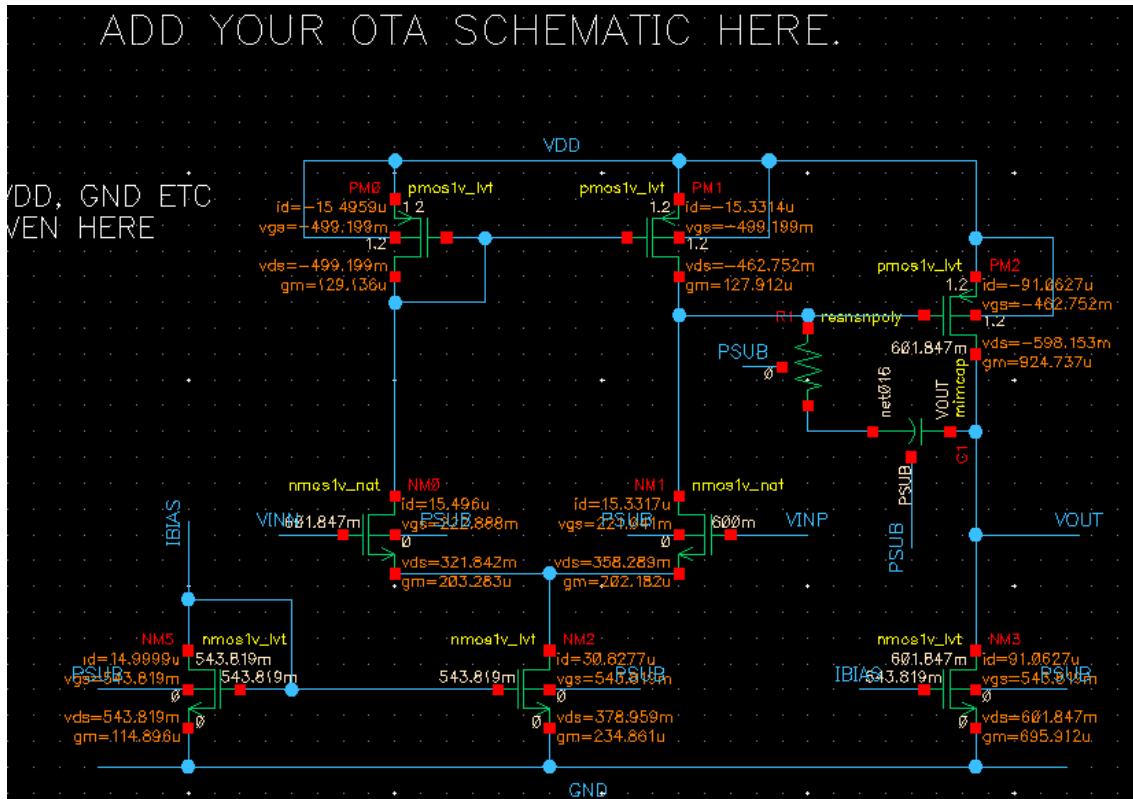


Figure 7: Closed Loop Differential Mode Operating Point

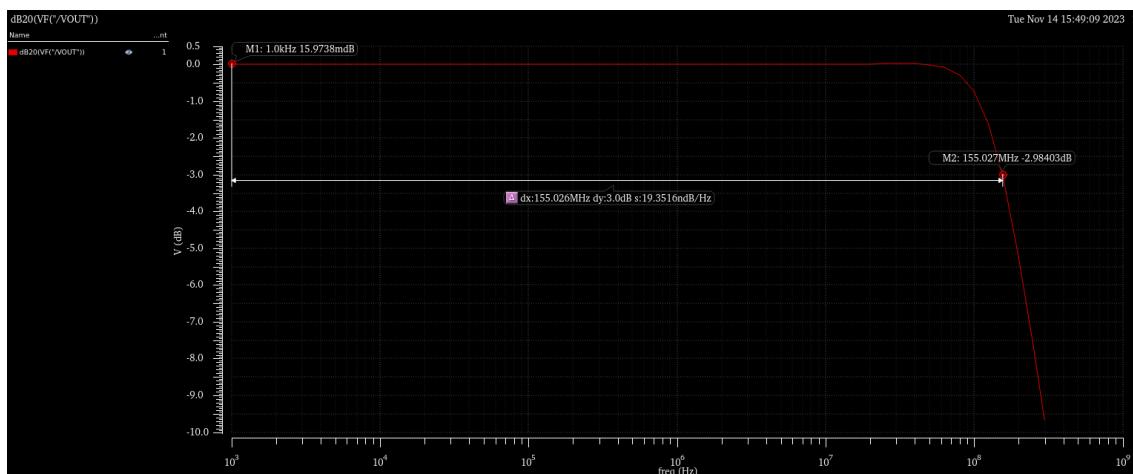


Figure 8: Closed Loop Differential Mode Gain

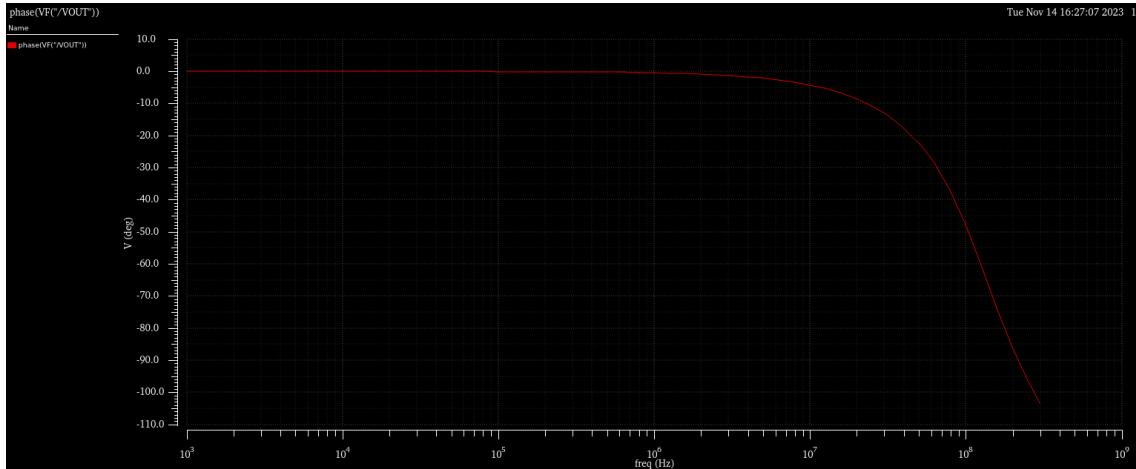


Figure 9: Closed Loop Differential Mode Phase

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_AC_DM:1	dB20(VF"/VOUT")				
EE618_CP1_20D070029:TB_AC_DM:1	phase(VF"/VOUT")				
EE618_CP1_20D070029:TB_AC_DM:1	Input referred offset	-1.847m			

Figure 10: Differential Mode Table

## 1.6 AC analysis: Common mode gain

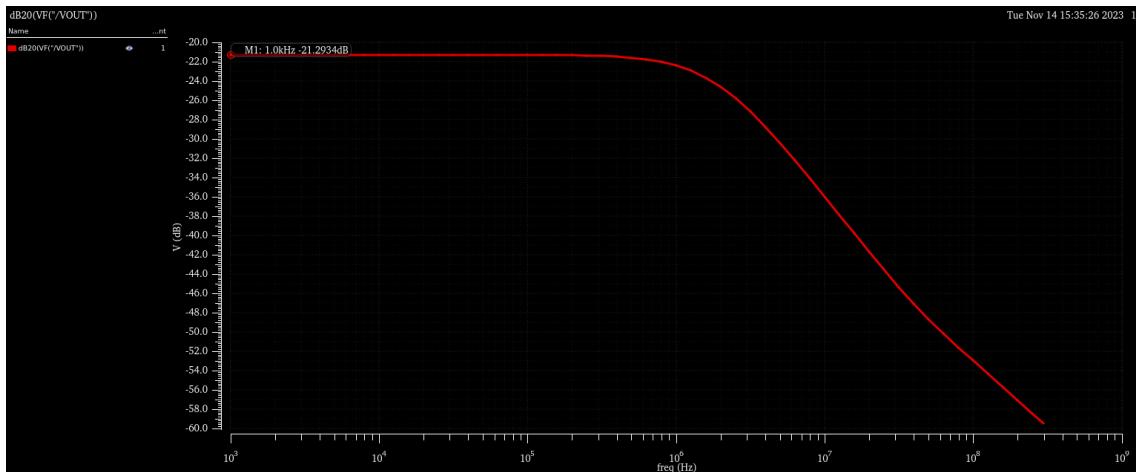


Figure 11: Open Loop Common Mode Gain

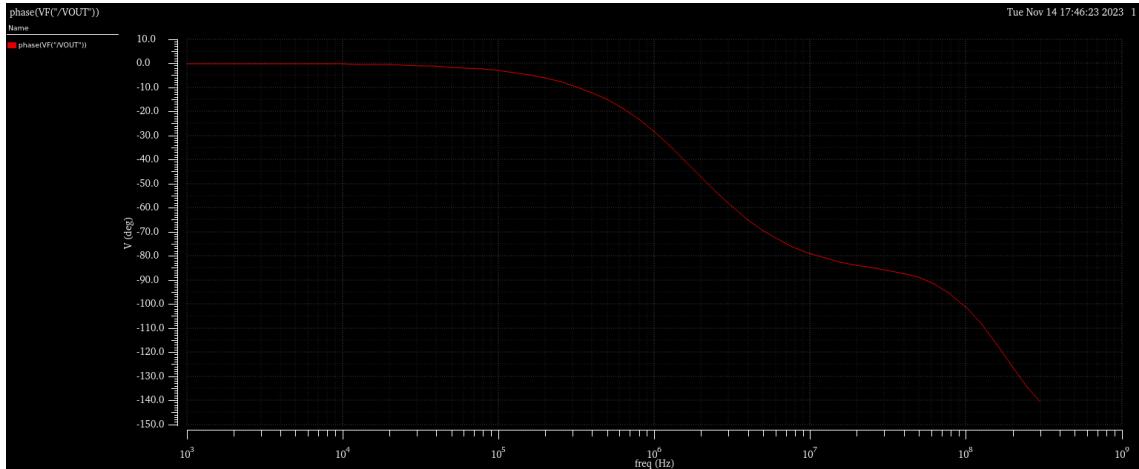


Figure 12: Open Loop Common Mode Phase

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_AC_CM:1	dB20(VR"/VOUT")				
EE618_CP1_20D070029:TB_AC_CM:1	phase(VF"/VOUT")				
EE618_CP1_20D070029:TB_AC_CM:1	ACM (in dB)	-21.29			

Figure 13: Open Loop Common Mode Table

## 1.7 Transient analysis: Sinusoidal input

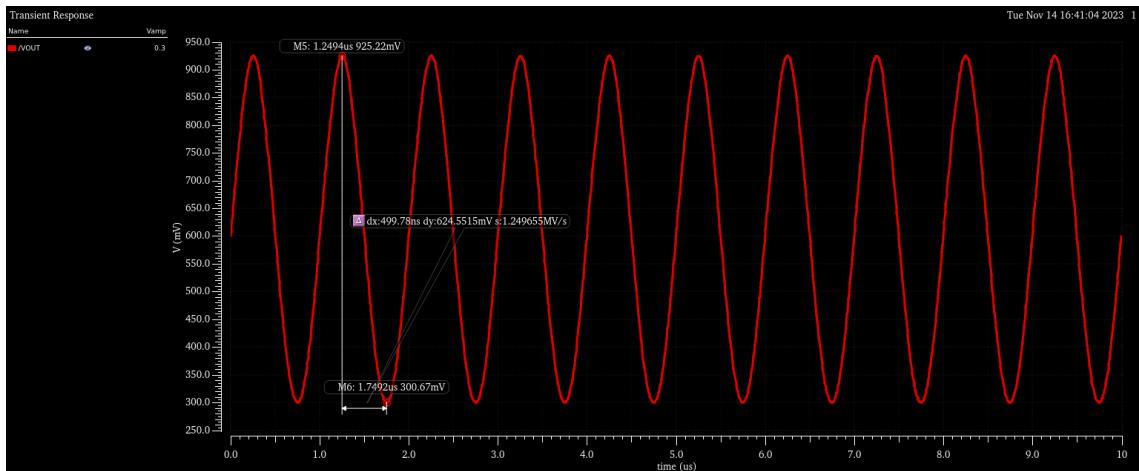


Figure 14: Transient Analysis with Sinusoidal input

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_20D070029:TB_TRAN_SIN:1	/VNP				
EE618_CP1_20D070029:TB_TRAN_SIN:1	VOUT (peak-peak)	624.8m			
EE618_CP1_20D070029:TB_TRAN_SIN:1	VIN (peak-peak)	600m			

Figure 15: Transient Analysis Summary

## 1.8 Transient analysis: Step input

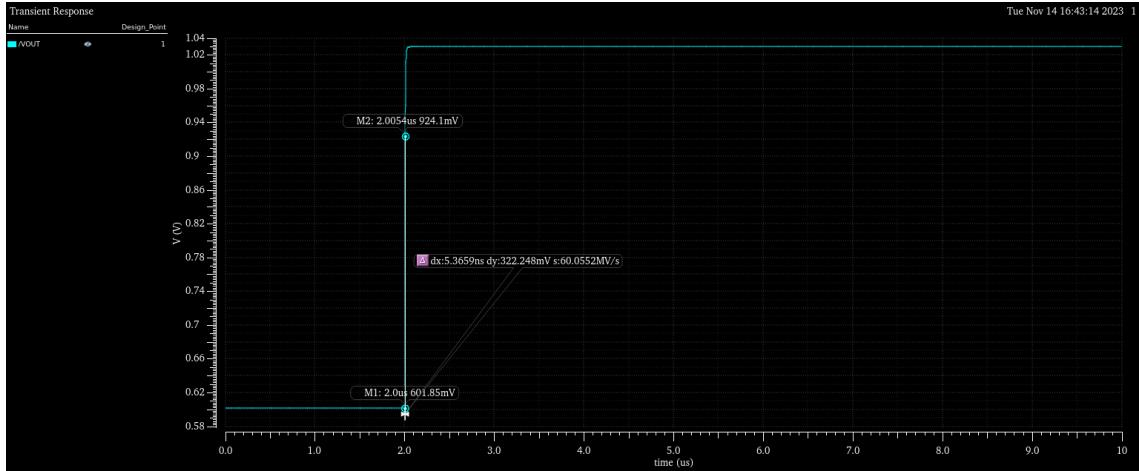


Figure 16: Transient Analysis: Slew Rate

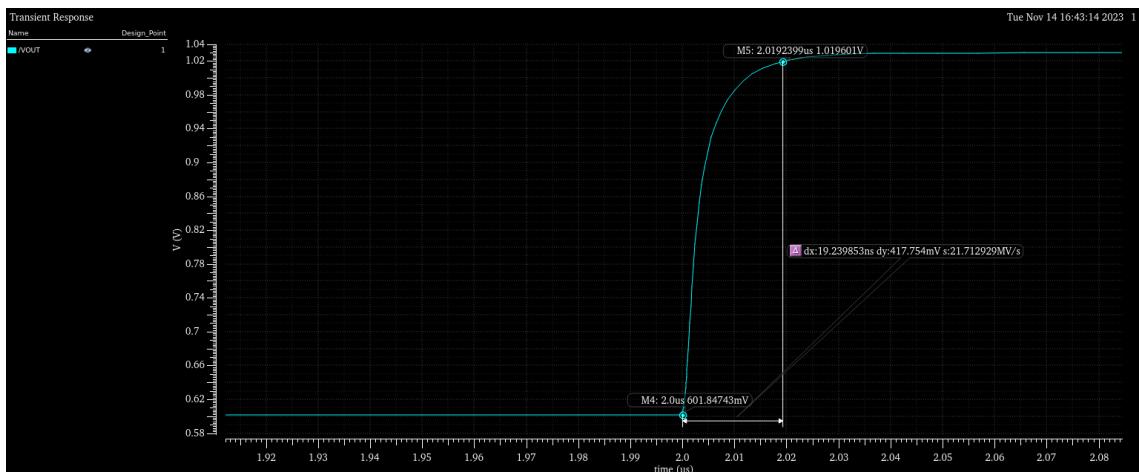


Figure 17: Transient Analysis: Settling Time

## 1.9 Noise analysis

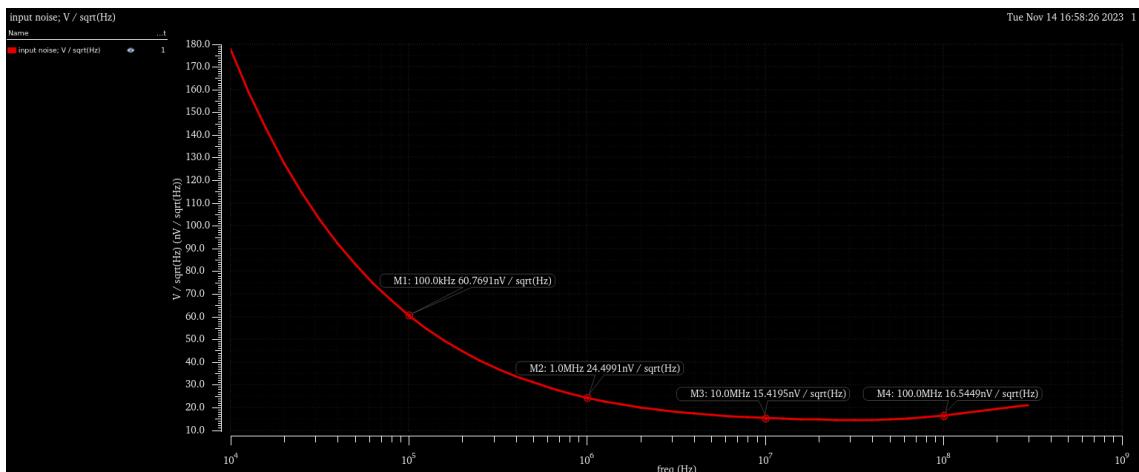


Figure 18: Noise Analysis

---

Integrated Noise Summary (in V^2) Sorted By Device Composite Noise  
 Total Summarized Noise = 5.03659e-08  
 Total Input Referred Noise = 1.00629e-07

Device	Param	Noise Contribution	% Of Total
/I0/NM0	id	1.00192e-08	19.89
/I0/NM1	id	9.57214e-09	19.01
/I0/PM1	id	7.10361e-09	14.10
/I0/PM0	id	5.9025e-09	11.72
/I0/NM5	id	4.25631e-09	8.45
/I0/NM1	fn	2.03667e-09	4.04
/I0/NM0	fn	2.02633e-09	4.02
/I0/PM2	id	1.42209e-09	2.82
/I0/NM3	id	1.07058e-09	2.13
/I0/NM5	fn	3.1335e-10	0.62

Integrated Noise Summary (in V^2) Sorted By Noise Contributors  
 Total Summarized Noise = 5.03659e-08  
 Total Input Referred Noise = 1.00629e-07  
 The above noise summary info is for noise data with Design\_Point = 1.0

Figure 19: Noise Summary

## 1.10 Design Summary

Device	Width(W)	Length(L)	$\frac{W}{L}$	Fingers	Multipliers
M1	5u	1.2u	4.167	5	1
M2	5u	1.2u	4.167	5	1
M3	960n	440n	2.181	1	1
M4	960n	440n	2.181	1	1
M5	1.92u	640n	3	2	1
M6	960n	440n	2.181	1	8
M7	960n	640n	1.5	1	6
M8	960n	640n	1.5	1	1

Table 1: MOSFET parameter summary

Component	Value
$C_c$	200.9704f
$R_c$	4k
$I_{bias}$	15u

Table 2: Summary of passive components

## 2 Project II

### 2.1 Layout

#### 2.1.1 Design

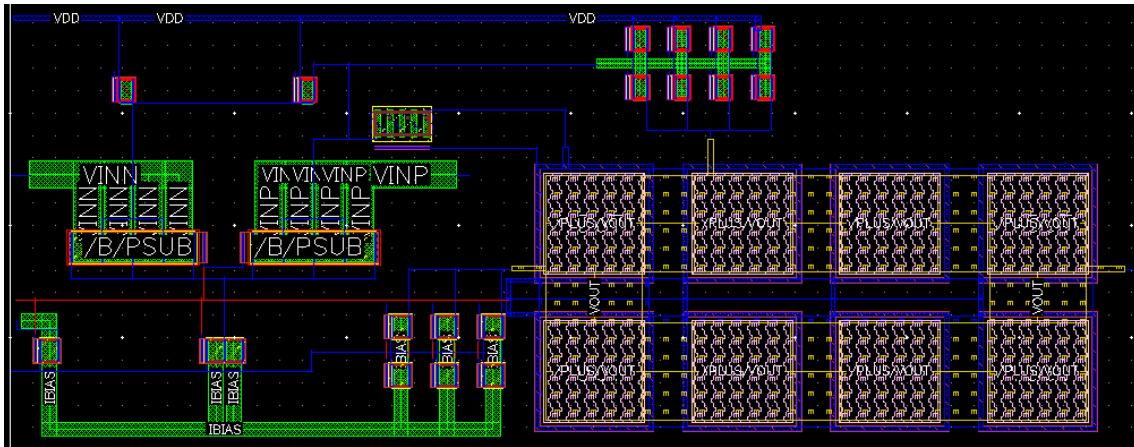


Figure 20: Layout Design

#### 2.1.2 Layout verifications

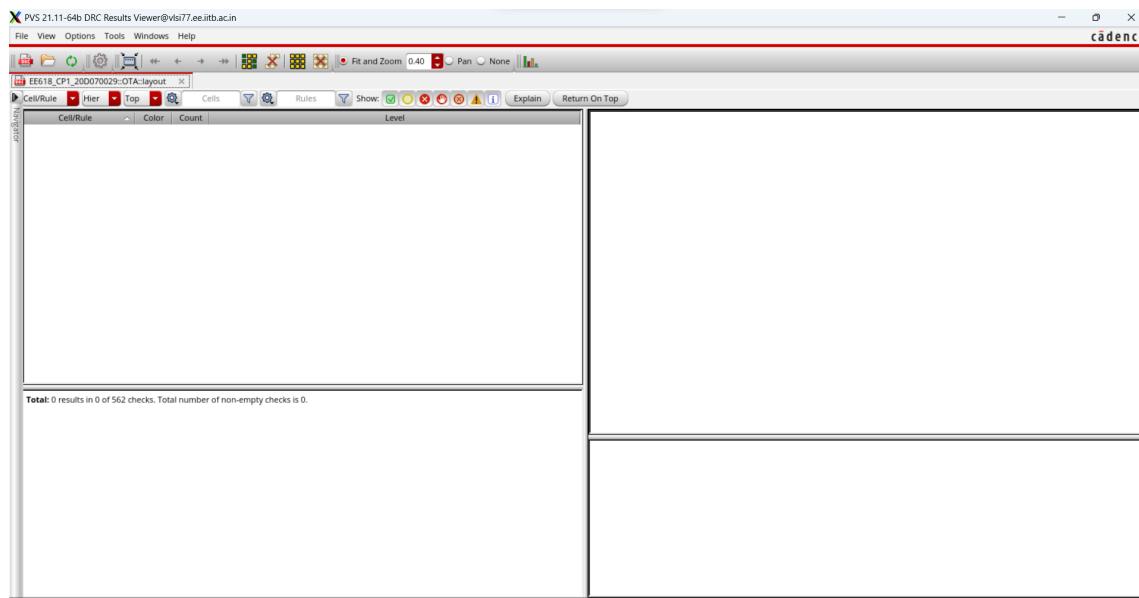


Figure 21: DRC Debug environment without any error

PVS 21.11-64b Reports: Done [DRC] tm...@vlsi77.ee.iitb.ac.in  
[DRC] tmp X

```

NET AREA: Cumulative Time CPU = 0(s) REAL = 0(s)
DENSITY: Cumulative Time CPU = 0(s) REAL = 0(s)
Miscellaneous: Cumulative Time CPU = 0(s) REAL = 0(s)
CONNECT: Cumulative Time CPU = 0(s) REAL = 0(s)
DEVICE: Cumulative Time CPU = 0(s) REAL = 0(s)
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM_FILL: Cumulative Time CPU = 0(s) REAL = 0(s)

Total CPU Time : 2(s)
Total Real Time : 21(s)
Peak Memory Used : 114(M)
Total Original Geometry : 1727(3295)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file OTA.sum
ASCII report database is /home/courseusers/EE618/EE618_12/tmp/OTA.drc_errors.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Tue Nov 14 19:35:16 2023

```

Find |    Match case  Whole word  Use RegExp  Highlight

No errors found Warnings: 22 Info: 600

⚠ \*WARNING\* LIB basic from File /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/composer/cds.lib Line 1 redefines

⚠ \*WARNING\* /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/composer/cds.lib' Line 2: path /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/sheets/US\_Bits already belongs to LIB sheets.

⚠ \*WARNING\* LIB analogLib from File /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/artist/cds.lib Line 1 redefines

⚠ \*WARNING\* LIB brnslib from File /vlsi/cad/cadence/C617/share/cdsetup/cds.lib Line 5 redefines

Find |    Match case  Whole word  Use RegExp

Help Issues  Warnings  Info

Figure 22: DRC successful

X PVS 21.11-64b Reports: Done [LVS] tm...@vlsi77.ee.iitb.ac.in  
[LVS] tmp X

```

Creating cross reference ...
*****
pvs_RCXref 21.11-s013 64 bit (Thu Oct 21 16:13:51 PDT 2021)
Build Ref No.: 013 Production (10-21-2021) [pvs_2111]

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Build O/S: Linux x86_64 3.10.0-693.el7.x86_64
Executed on: vlsi77.ee.iitb.ac.in (Linux x86_64 3.10.0-1160)
Process Id: 8177
Starting Time: Tue Nov 14 19:41:39 2023 (Tue Nov 14 14:11:39
With parameters: -format C -nxf -ixf /home/courseusers/EE618/EE
*****
```

```

Total CPU Time : 0(s)
Total Real Time : 0(s)
Memory Used : 73.60 (M)

pvs_RCXref Done
Checking in all SoftShare licenses.


```

PVS 21.11-64b LVS Run Status@vlsi77.ee.iitb... X

ERC Results: Empty Extraction Results: Warnings Comparison Results: Match

Do you want to start the LVS DE?

Do not show this window again

Find |    Match case  Whole word  Use RegExp  Highlight

No errors found Warnings: 31 Info: 41

⚠ \*WARNING\* LIB basic from File /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/composer/cds.lib Line 1 redefines

⚠ \*WARNING\* /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/composer/cds.lib' Line 2: path /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/sheets/US\_Bits already belongs to LIB sheets.

⚠ \*WARNING\* LIB analogLib from File /vlsi/cad/cadence/C617/tools.lnx86/dfl/etc/cdsDotLibs/artist/cds.lib Line 1 redefines

⚠ \*WARNING\* LIB brnslib from File /vlsi/cad/cadence/C617/share/cdsetup/cds.lib Line 5 redefines

Find |    Match case  Whole word  Use RegExp

Help Issues  Warnings  Info

Figure 23: LVS successful



Figure 24: QRC successful

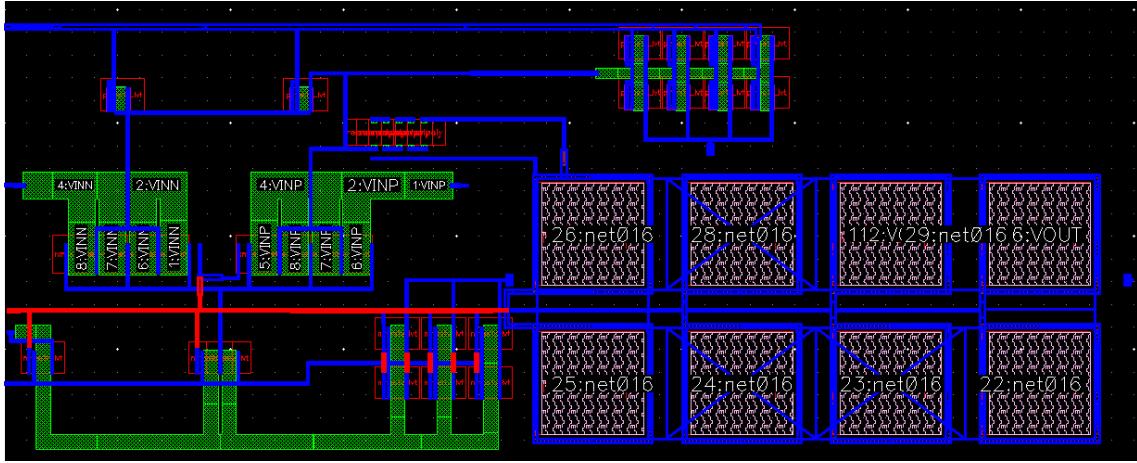


Figure 25: avextracted view

The area of the extracted view is  $50 \text{ um} \times 20\text{um}$

## 2.2 Extracted Layout Simulations

Note the legend for all the following plots would be:

- Red - schematic
- Yellow - av extracted

All the schematic plot labels would be above the graph and layout labels would be below the graph

### 2.2.1 DC Operating Point

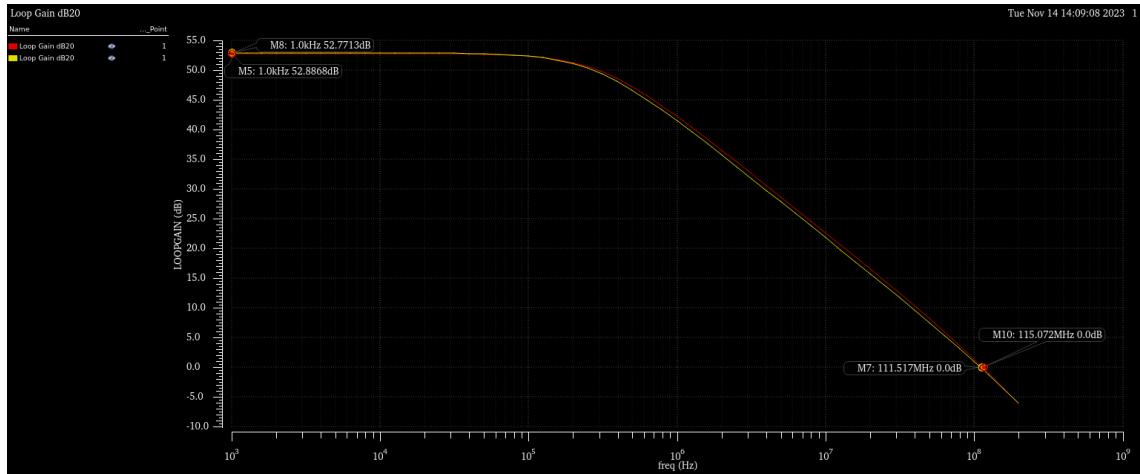


Figure 26: Appended plot of DC gain

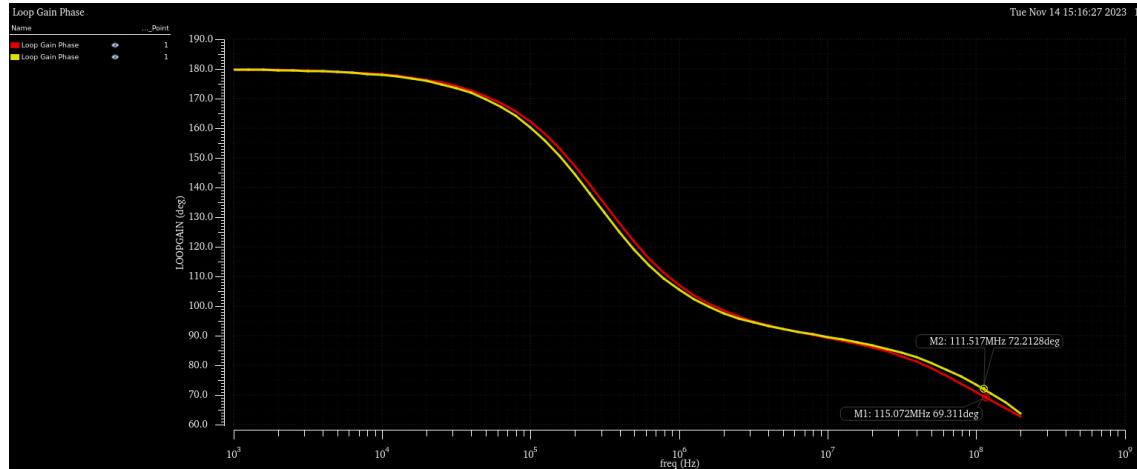
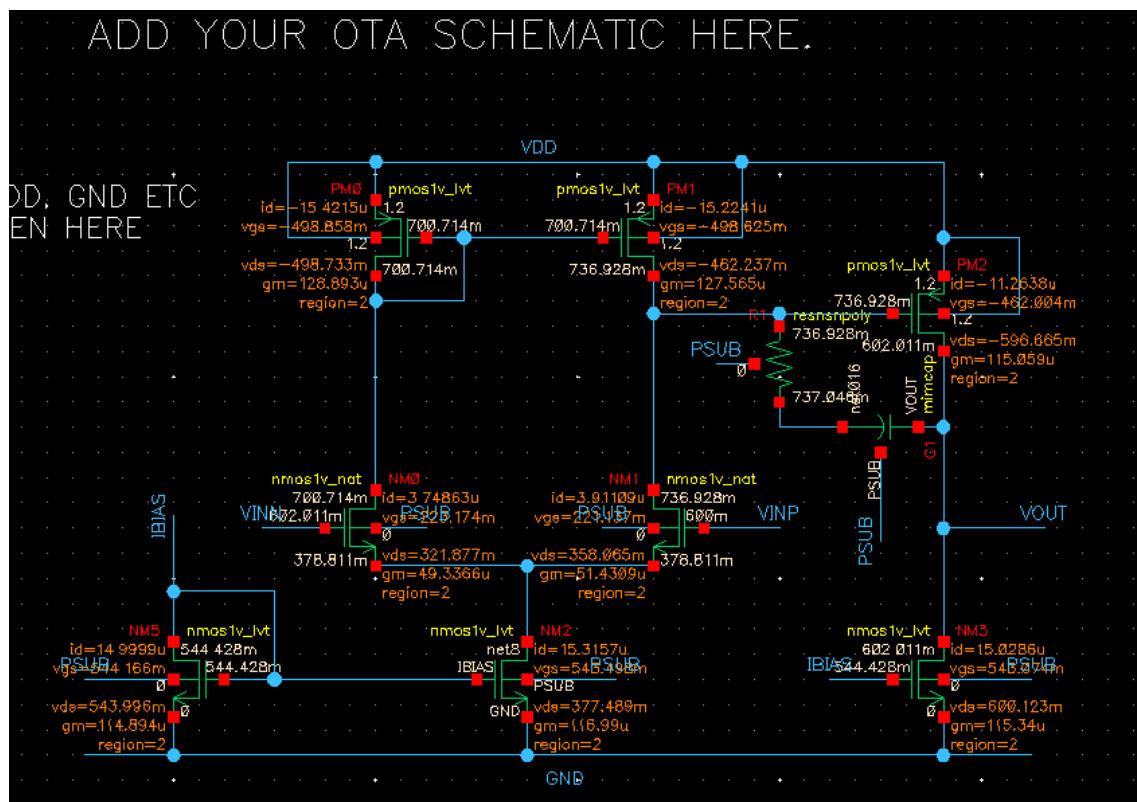


Figure 27: Appended plot of DC phase



### 2.2.2 Stability Analysis

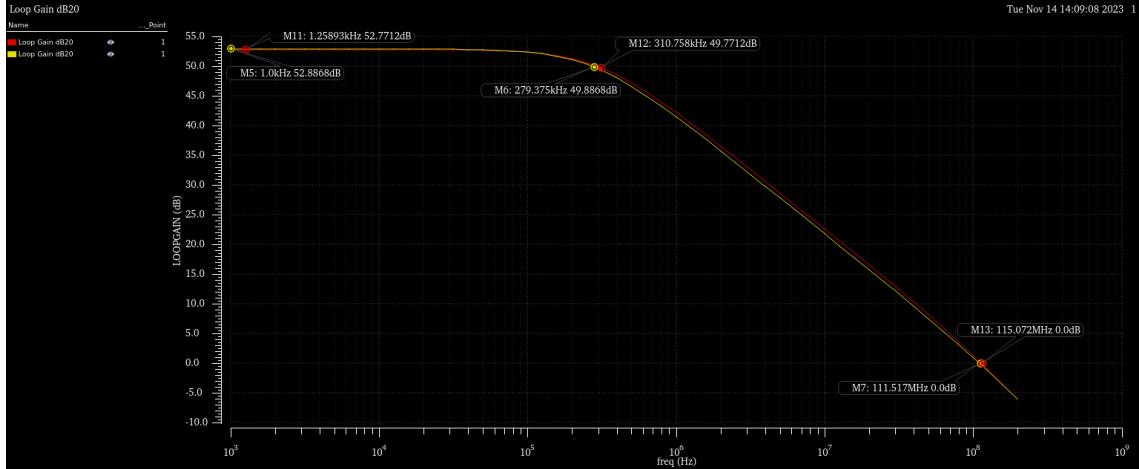


Figure 29: Appended plot of the Stability analysis

Stability Summary - circuit "TB_STB_LG" with loop probe "IPRB0"				
Design_Point	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)
1	72.232	118.89M	nan	nan

Figure 30: Stability summary of the extracted layout

### 2.2.3 AC analysis: Differential Gain

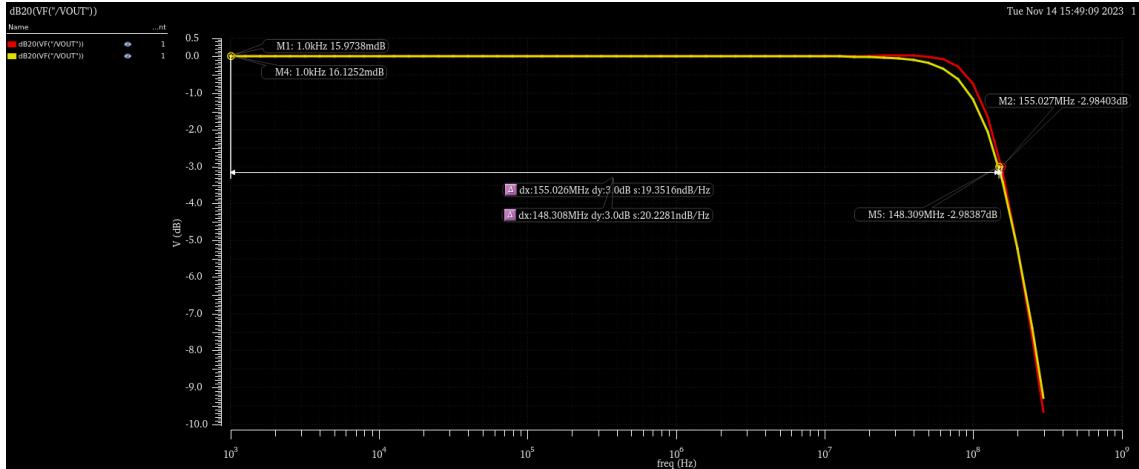


Figure 31: Appended plot of Closed Loop Differential Mode Gain

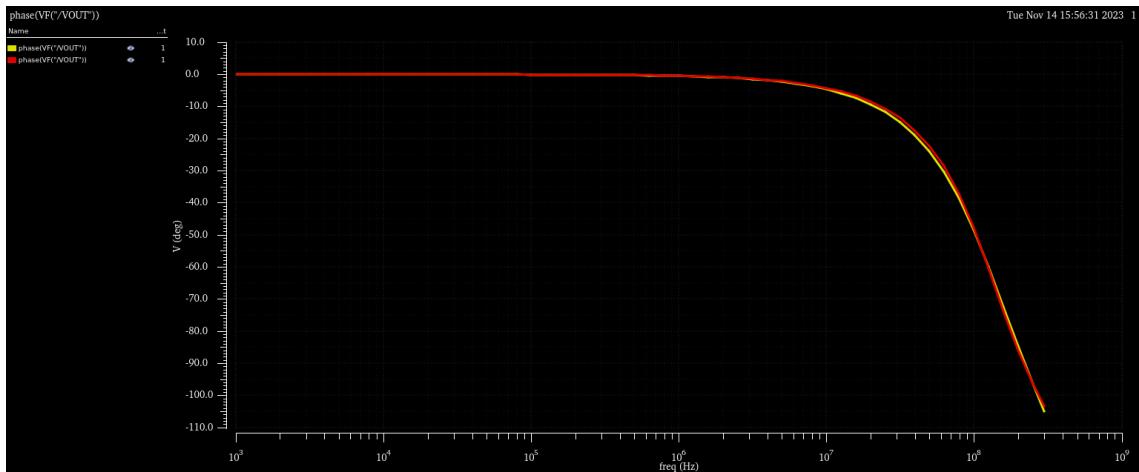


Figure 32: Appended plot of Closed Loop Differential Mode Phase

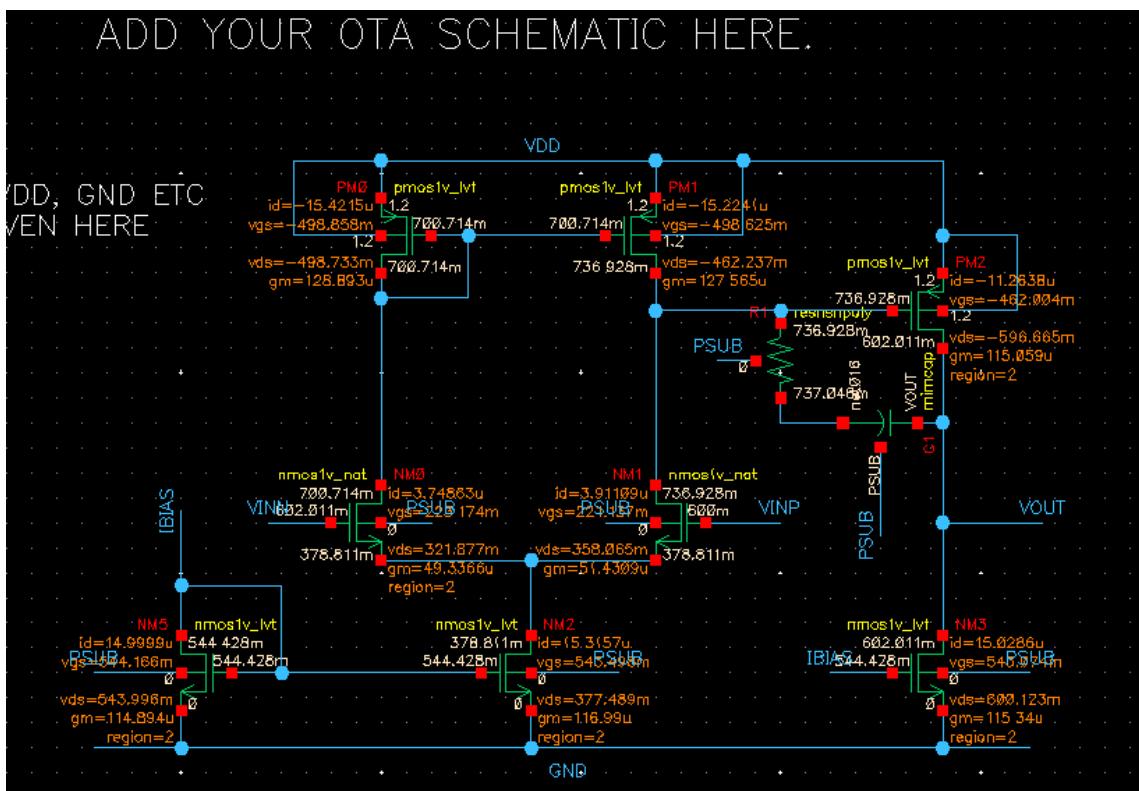


Figure 33: Closed Loop Differential Mode Operating Points

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_AC_DM:1	dB20(VR"/VOUT")				
EE618_CP1_20D070029:TB_AC_DM:1	phase(VF"/VOUT")				
EE618_CP1_20D070029:TB_AC_DM:1	Input referred offset	-2.011m			

Figure 34: Closed Loop Differential Mode Summary

## 2.2.4 AC analysis: Common mode gain

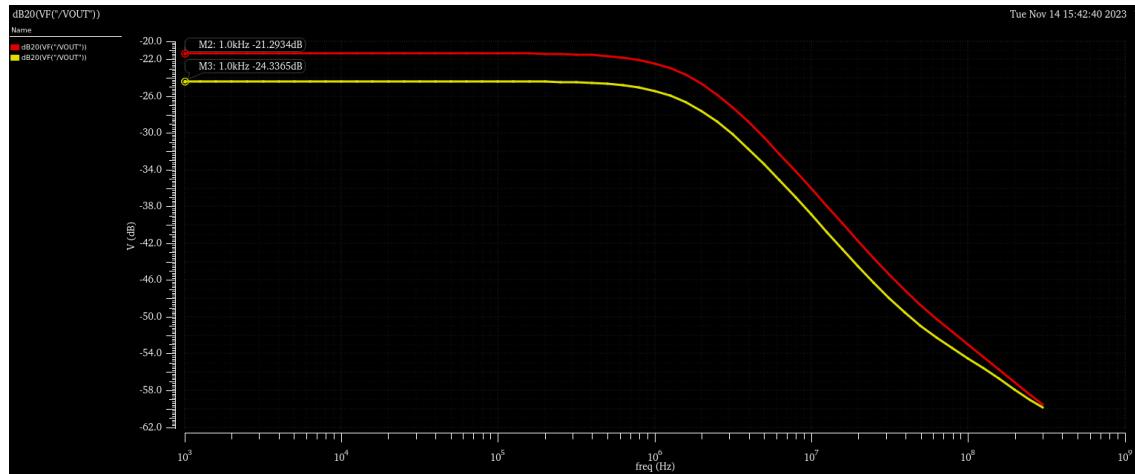


Figure 35: Appended plot of Open Loop Common Mode Gain

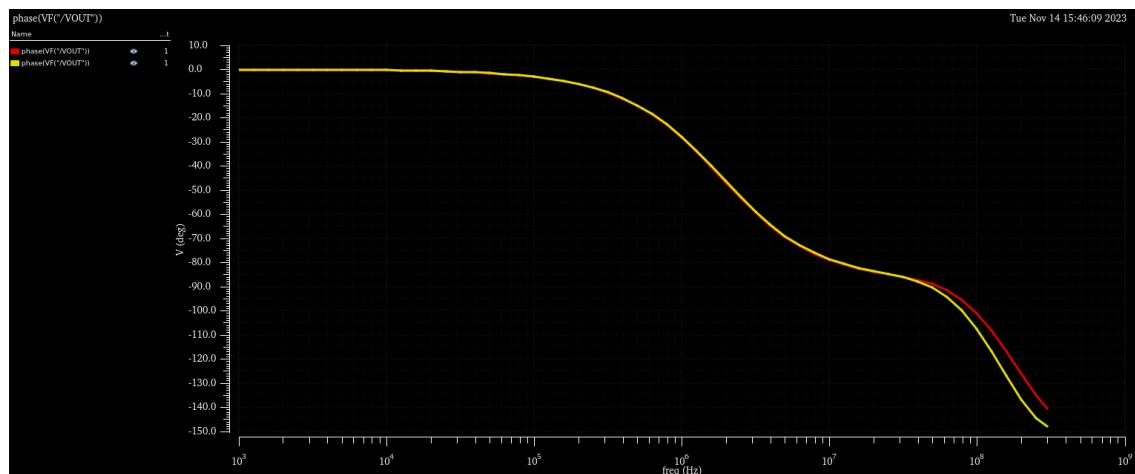


Figure 36: Appended plot of Open Loop Common Mode Phase

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_AC_CM:1	dB20(VR"/VOUT")				
EE618_CP1_20D070029:TB_AC_CM:1	phase(VF"/VOUT")				
EE618_CP1_20D070029:TB_AC_CM:1	ACM (in dB)	-24.34			

Figure 37: Open Loop Common Mode Summary

### 2.2.5 Transient analysis: Sinusoidal input

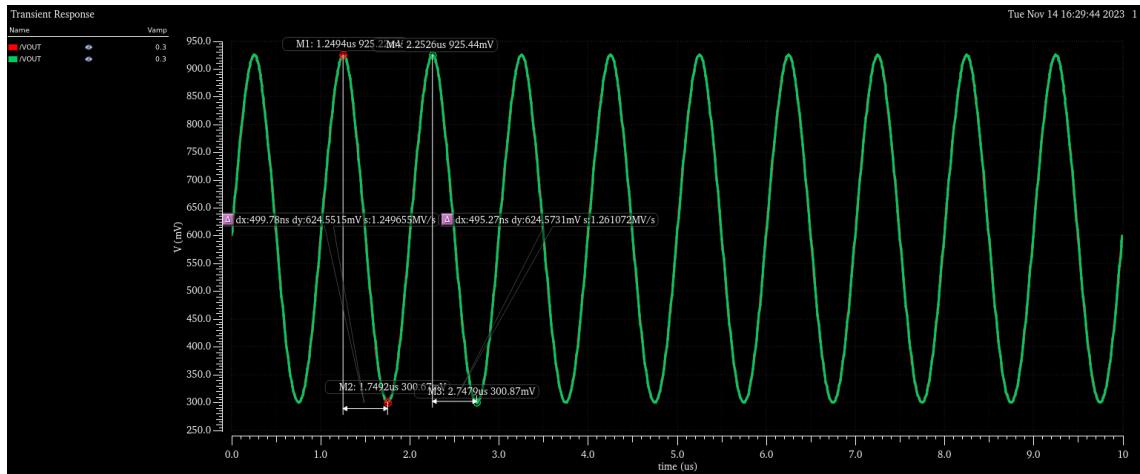


Figure 38: Appended Plot of Transient sinusoidal analysis

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_20D070029:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_20D070029:TB_TRAN_SIN:1	/VNP				
EE618_CP1_20D070029:TB_TRAN_SIN:1	VOUT (peak-peak)	624.6m			
EE618_CP1_20D070029:TB_TRAN_SIN:1	VIN (peak-peak)	599.9m			

Figure 39: Extracted layout Transient Analysis summary

### 2.2.6 Transient analysis: Step input

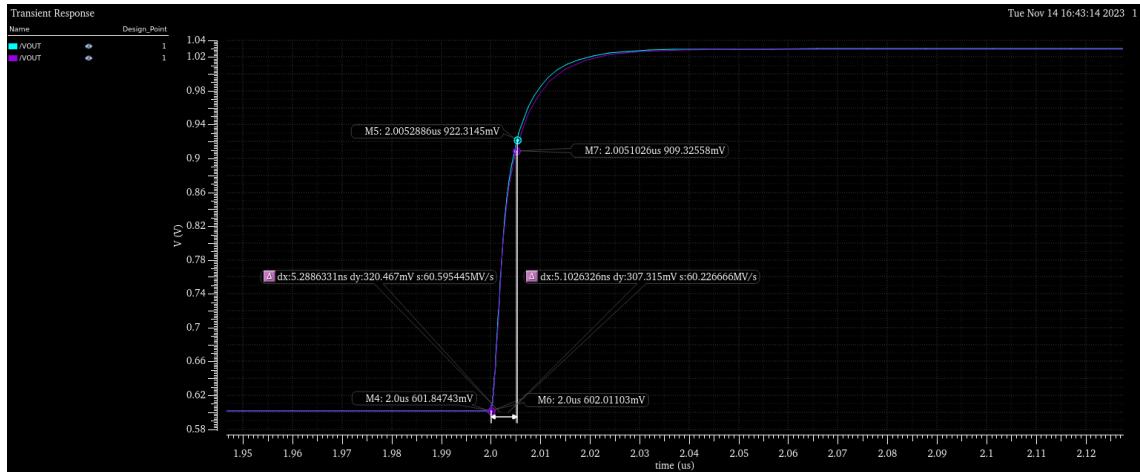


Figure 40: Appended plot of slew rate measurement

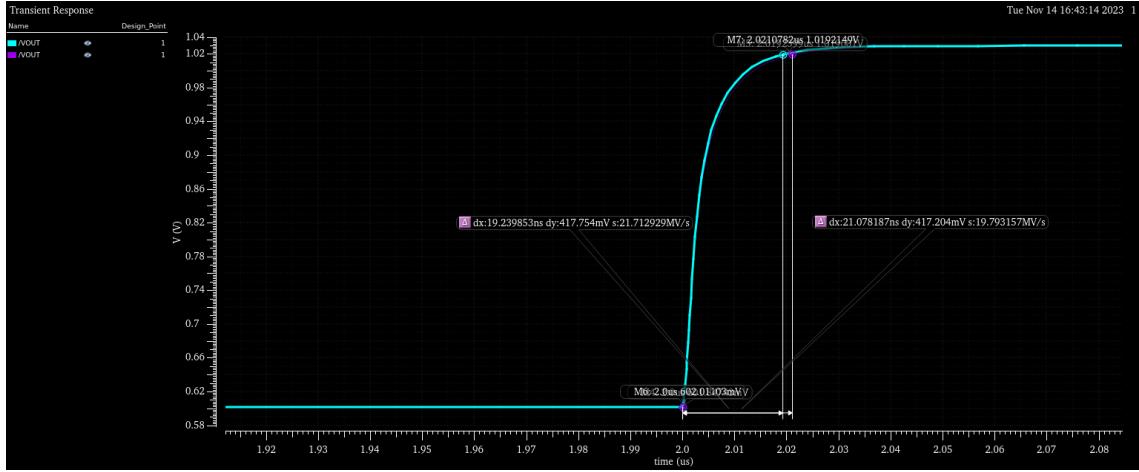


Figure 41: Appended plot of settling time measurement

### 2.2.7 Noise Analysis

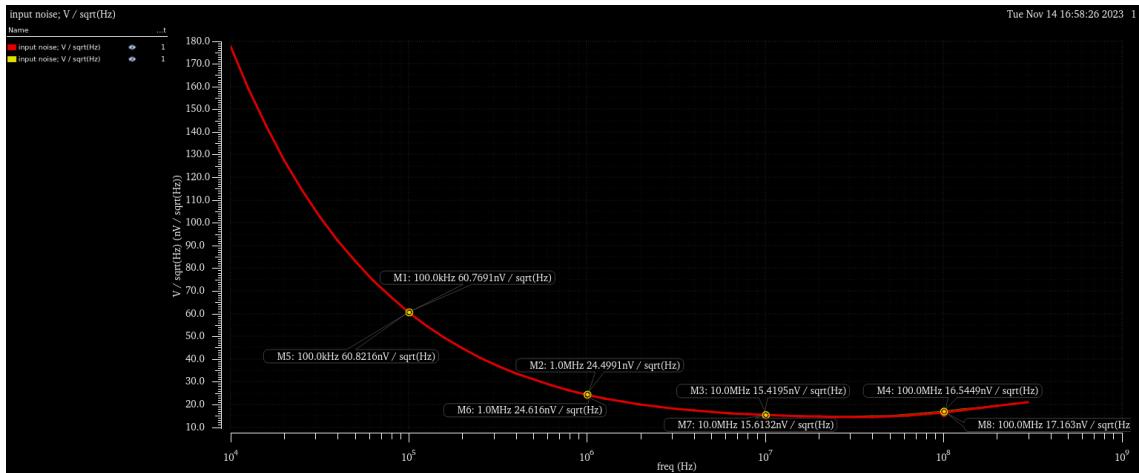


Figure 42: Appended plot of Noise analysis

```
Integrated Noise Summary (in V^2) Sorted By Device Composite Noise
Total Summarized Noise = 5.0717e-08
Total Input Referred Noise = 1.03788e-07
```

Device	Param	Noise Contribution	% Of Total
/I0/PM1	id	6.86536e-09	13.54
/I0/PM0	id	5.68501e-09	11.21
/I0/NM5	id	3.86922e-09	7.63
/I0/NM0_2_rcx	id	2.47692e-09	4.88
/I0/NM0_3_rcx	id	2.47692e-09	4.88
/I0/NM0_1_rcx	id	2.36602e-09	4.67
/I0/NM0	id	2.36363e-09	4.66
/I0/NM1_1_rcx	id	2.36019e-09	4.65
/I0/NM1	id	2.36019e-09	4.65
/I0/NM1_3_rcx	id	2.2544e-09	4.45

```
Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 5.0717e-08
Total Input Referred Noise = 1.03788e-07
The above noise summary info is for noise data with Design_Point = 1.0
```

Figure 43: Integrated Noise Summary

Q.No	Parameters	Layout Results	Schematic Results
2	Power Consumption	0.1449636m	0.1462685m
3	DC gain	52.8868dB	52.77dB
	f-3dB	279.375k	310.75k
	Unity Gain frequency	111.517M	115.072M
	Phase margin	72.21	69.3
4	Closed Loop Gain	16.1252mdB	15.9738mdB
	f-3dB	148.309M	155.027M
	Input referred offset (DC analysis)	-2.011m	-1.847m
5	Common-mode gain	-24.3365dB	-21.2934dB
	CMRR	16.51	11.626
6	Output Swing (Vpk-pk)	624.6m	624.8m
7	Slew rate	60.2266M	60.595M
	Settling Time (1% accuracy)	21.0781n	19.2398n
8	Input referred spot noise (at 0.1 MHz)	60.8216n	60.7691n
	Input referred spot noise (at 10 MHz)	15.6132n	15.4195n
	Total Summarized noise	50.717n	50.3659n
	Total Input Referred Noise	103.788n	100.629n

Figure 44: Summary Comparison of specifications met by layout vs schematic

## 2.3 Summary of Results Obtained

## 2.4 Observations

- The spot noise at 0.1MHz and 10MHz is higher in the layout when compared to the schematic since the layout considers the process variations that can occur during fabrication which can potentially change the width and length of the transistor. This changes the parameters of the transistor and hence, can lead to an increase in the noise. As a result, we observe an increase in the spot and integrated noise.
- The decrease in the power consumption might be due to the reduction in the currents( $I_{ss}$  and  $I_{oss}$ ) by a small amount.
- The slew rate has also decreased slightly because it is inversely proportional to the capacitance and the layout considers the interconnect capacitance. This also leads to a decrease in the settling time.
- The input referred offset has also increased because of the slightly mismatched transistor dimensions during fabrication.
- In the layout, we use techniques such as fingers and multipliers which improve matching to some extent. Since I have taken the dimensions of the transistors to be roughly the same and used multipliers and fingers effectively, the common mode rejection ratio(CMRR) has slightly gone up and so has the DC gain.
- The interconnect capacitance also increases the capacitive loading and hence, decreases the unity gain frequency( $f_u$ ) and subsequently, reduces the 3dB cut-off frequency( $f_{3dB}$ ) and increases the phase margin.