EE671 VLSI Assignment-1

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1 Student Details

My roll number ends with 29. So, the value of nn is 29 and thus, the expected rise and fall time is 258 ps.

2 CMOS Inverter Design

A computation file is created using python in order to calculate the area of the drain and source, perimeter of the drain and source everytime the width of the pmos and nmos is changed and accordingly measured the rise and fall times. The rise time depends only on the pmos transistor width(W_p) and the fall time depends only on the nmos transistor width(W_n). The values of W_p and W_n are varied via hit and trial using the fact that there is a linear dependence between them.

2.1 NGSPICE Simulation

2.1.1 Code Snippet

```
* CMOS Inverter Design
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=1.559U AD = 0.56124P AS = 0.56124P PD = 3.838U PS = 3.838U
MN1 Output Inp 0      0      cmosn
+ L=0.18U W=0.523U AD = 0.18828P AS = 0.18828P PD = 1.766U PS = 1.766U
.ends

vdd supply 0 dc 1.8
*  Device under test
x3  supply Ck dutout inv
* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm

*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

2.1.2 Results Obtained

The expected and the obtained rise and fall times are tabulated below:

Expected Rise Time	Obtained Rise Time
258ps	258.096ps

Expected Fall Time	Obtained Fall Time
258ps	258.299ps

3 Inverter Static Transfer Characteristics

3.1 Methodology

A DC sweep of V(Ck) from 0 to 1.8V is performed and V(dutout) is plotted as a function of the sweep voltage. A variable der is defined to store the derivative of the output voltage(V(dutout) with respect to the sweep voltage(V(Ck)). The noise margins are calculated using the meas command when der = -1. We obtain the values of V_{IL},V_{OH},V_{IH} and V_{OL} using this approach and proceeded to print out the values of high noise margin and low noise margin.

3.2 NGSPICE Simulation

3.2.1 Code Snippet

```
*Code to measure the high and low noise margins
* Minimum Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=1.559U AD = 0.56124P AS = 0.56124P PD = 3.838U PS = 3.838U
MN1 Output Inp 0      0      cmosn
+ L=0.18U W=0.523U AD = 0.18828P AS = 0.18828P PD = 1.766U PS = 1.766U
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF

* Input voltage
VCk Ck 0 dc
.include models-180nm

*TRANSIENT ANALYSIS with pulse inputs
*VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
*.tran 1pS 35nS 0nS
.dc VCk 0 1.8 0.001
.control
run
*plot 4.0+V(Ck) V(dutout)
plot V(dutout) vs V(Ck)
let der = deriv(V(dutout))
```

```
meas dc VIL find V(Ck) when der = -1
meas dc VIH find V(Ck) when der = -1 rise = last
meas dc VOL find V(dutout) when V(CK) = VIH
meas dc VOH find V(dutout) when V(Ck) = VIL
let highnoisemargin = VOH - VIH
let lownoisemargin = VIL - VOL
print highnoisemargin
print lownoisemargin

.endc
.end
```

3.2.2 Results obtained

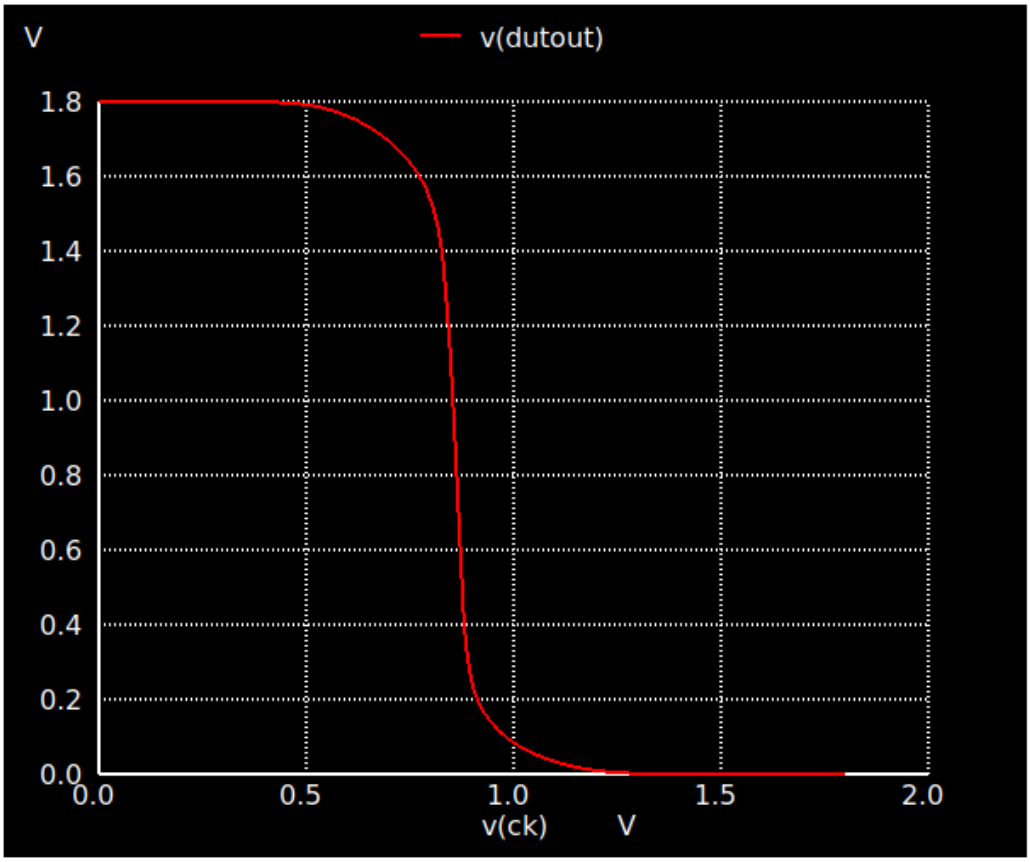

Figure 1: Static Transfer Characteristics

Parameter	Value Obtained(in V)
V_{IL}	0.709
V_{IH}	0.968
V_{OL}	0.112
V_{OH}	1.684
Low Noise Margin	0.597
High Noise Margin	0.715

Table 1: Noise Margins

4 Other Logics from Inverter

4.1 Methodology

To design any logic using inverters, the logic needs to be expressed in the sum of products form followed by inversion. Subsequently, series, parallel rules are followed while arranging the PMOS and NMOS transistors. Lastly, the transistor widths are scaled for the transistors connected in series in order to match the rise and fall times. The circuit diagram is created using Xcircuit is attached below:
Note the widths and lengths of the transistor are not the same as those used for NgSpice simulations.

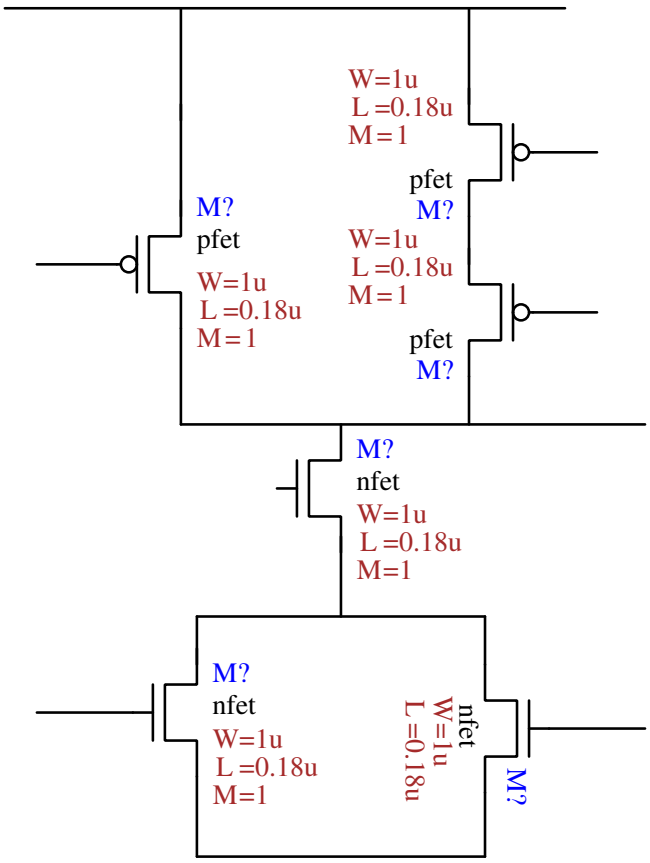

Figure 2: Logic from Inverter Circuit

4.2 Code Snippet

The following code contains 3 cases. Uncomment one of them in order to run the particular case.

```
* Implementation of the given logic using inverters
* Name: G Kamalesh
* Roll: 20D070029
* n : 29
.param Wp = 1.559U
.param Lp = 0.18U
.param Adp = 0.56124P
.param Asp1 = 0.56124P
.param Asp2 = 1.12248P
```

```
.param Psp1 = 3.838U
.param Psp2 = 6.956U
.param Wn = 0.523U
.param Ln = 0.18U
.param Adn = 0.37656P

.param Psn = 2.812U
.subckt function supply A B C Y
MP1 Y A Supply Supply cmosp
+ L=0.18U W=1.559U AD = 0.56124P AS = 0.56124P PD = 3.838U PS = 3.838U
MP2 P1 B Supply Supply cmosp
+ L=0.18U W=3.118U AD = 1.12248P AS = 1.12248P PD = 6.956U PS = 6.956U
MP3 Y C P1 P1 cmosp
+ L=0.18U W=3.118U AD = 1.12248P AS = 1.12248P PD = 6.956U PS = 6.956U
MN1 Y A N1 N1 cmosn
+ L=0.18U W=1.046U AD = 0.37656P AS = 0.37656P PD = 2.812U PS = 2.812U
MN2 N1 B 0 0 cmosn
+ L=0.18U W=1.046U AD = 0.37656P AS = 0.37656P PD = 2.812U PS = 2.812U
MN3 N1 C 0 0 cmosn
+ L=0.18U W=1.046U AD = 0.37656P AS = 0.37656P PD = 2.812U PS = 2.812U
.ends

vdd supply 0 dc 1.8

* Load Capacitor
C3 dutout 0 0.05pF

*device under test
x3 supply A B C dutout function

.include models-180nm

* Transient analysis with pulse inputs
* Case (a):
* A = '1', B = '0', C = 0 → 1 and C = 1 → 0.
*Va A 0 DC 1.8
*Vb B 0 DC 0
*Vc C 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)

* Case (b):
*A = '1', C = '0', B = 0 → 1 and B = 1 → 0.
Va A 0 DC 1.8
Vb B 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
Vc C 0 DC 0

* Case (c):
*B = '0', C = '1', A = 0 → 1 and A = 1 → 0.
*Vb B 0 DC 0
*Vc C 0 DC 1.8
*Va A 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS
.control

run
plot 4.0+V(A) 8+V(B) 12+V(C) V(dutout)
meas tran inrise TRIG v(B) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
```

```
meas tran infall TRIG v(B) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

4.3 Results Obtained

4.3.1 Case (a)

A = '1', B = '0', C = 0 → 1 and C = 1 → 0.

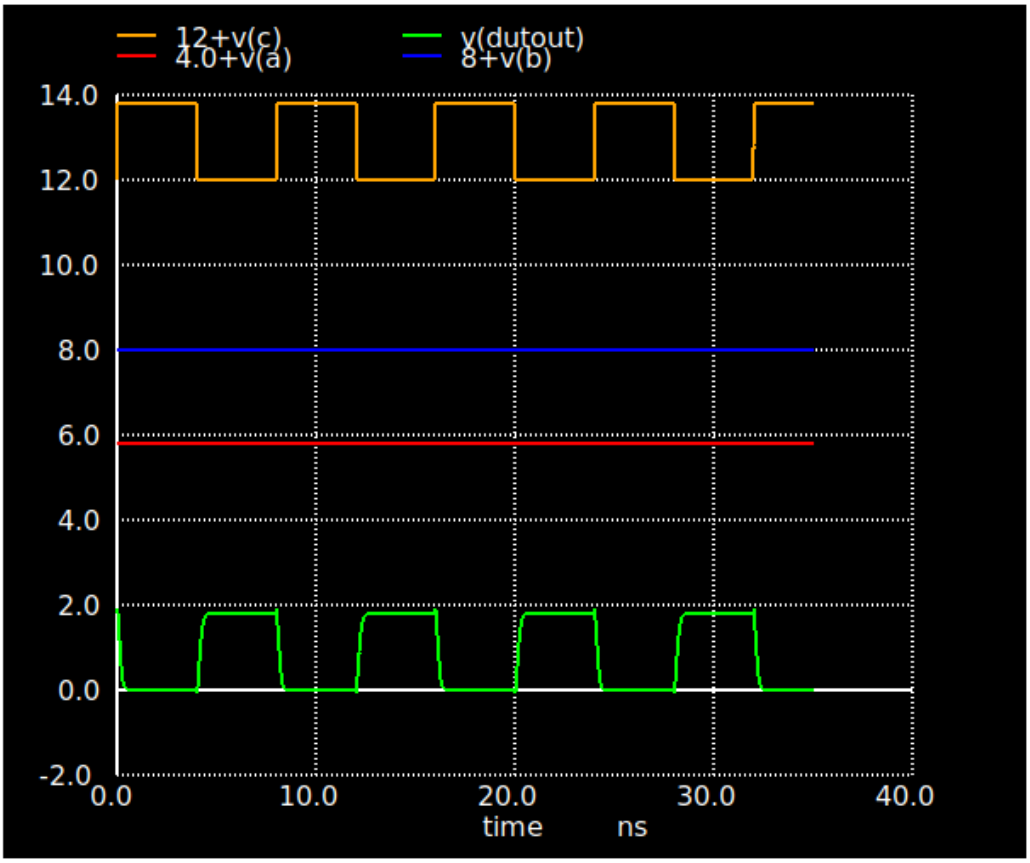

Figure 3: Case a

We can verify that the output is just the inversion of C.

4.3.2 Case (b)

A = '1', C = '0', B = 0 → 1 and B = 1 → 0.

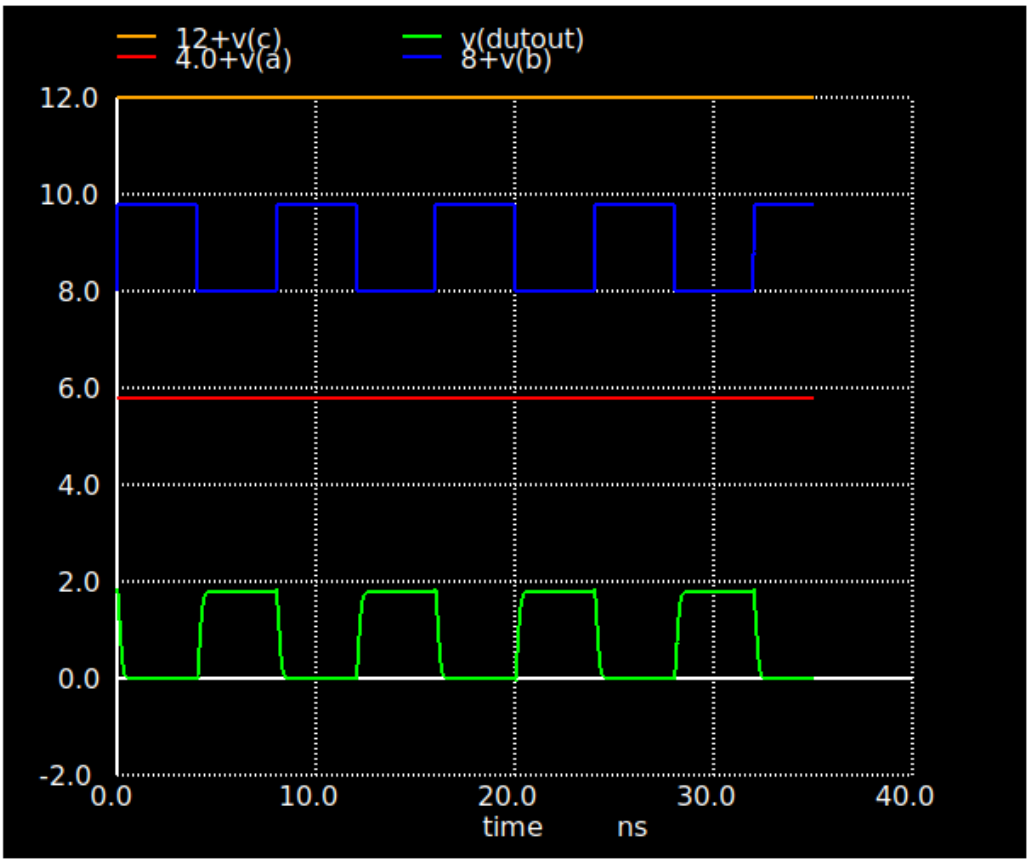

Figure 4: Case (b)

We can verify that the output is just the inversion of B.

4.3.3 Case (c)

B = '0', C = '1', A = 0 → 1 and A = 1 → 0.
We can verify that the output is indeed the inverted version of A.

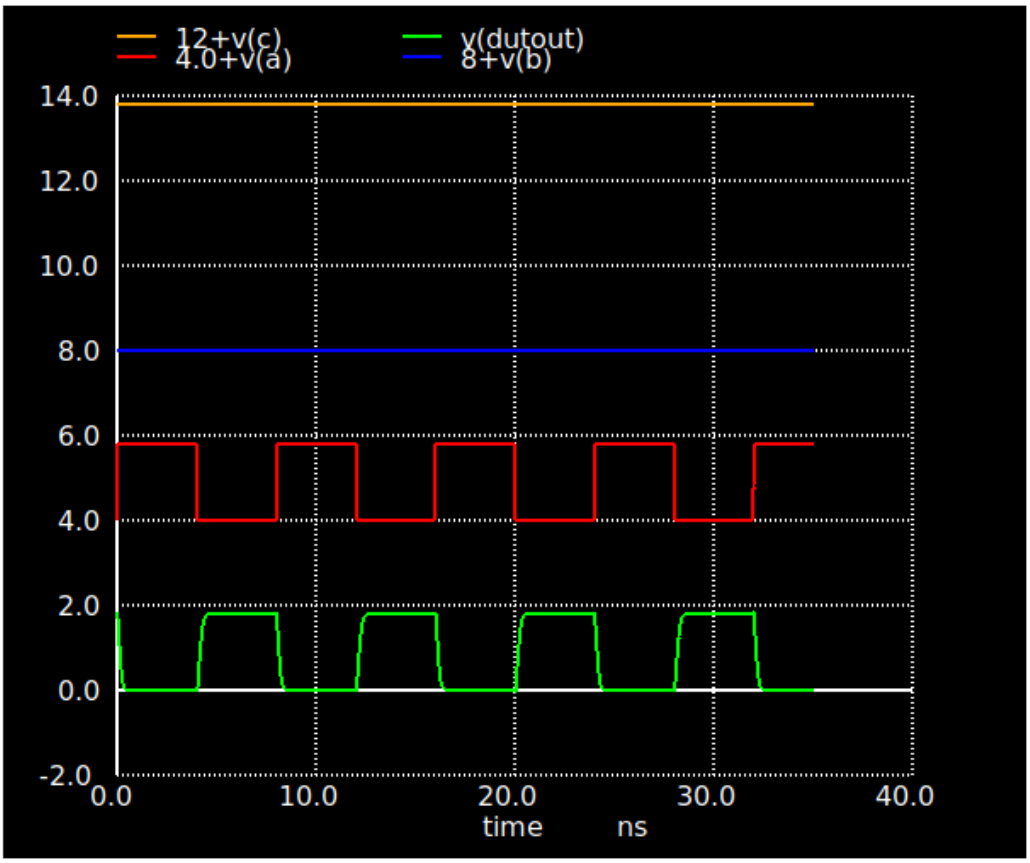

Figure 5: Case (c)

4.3.4 Timing Characteristics

Logic transition	Rise Time(in ps)	Fall Time(in ps)
A=1, B=0, C varying	280.01	246.537
A=1, C=0, B varying	280.10	265.064
B=0,C=1, A varying	285.45	246.54

Table 2: Timing Characteristics