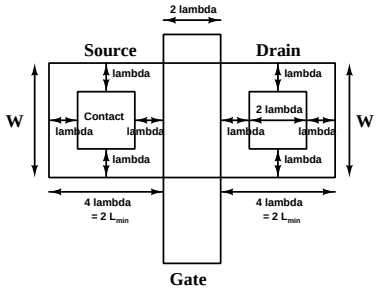
Monday	EE 671: VLSI Design	Due on
Aug. 14, 2023	Assignment 1	Aug. 21, 2023

We want to design a CMOS inverter using a 180 nm CMOS process. The n and p channel transistors in this process have a channel length of 0.18μm and a minimum channel width of 0.24μm. The supply voltage for logic design is 1.8V. Transistor models for this process are attached in a separate file called models-180nm.

Design an inverter in this process with a load capacitance of 0.05pF. In addition to this capacitance, the capacitances associated with the inverter tranistors themselves should be included in the design. For this, the source/drain area and perimeter values (which depend on transistor geometry) should be given to the simulator. These parameters can be calculated as shown in the figure below.

Width of either diffused region is W while its length is 4λ. Since $\lambda = L_{min}/2, 4\lambda = 2L_{min}$, the Source/Drain area is given by as = ad $= W \times 2L_{min}$.
Source/Drain perimeter is given by:
ps = pd $= 2 \times (W + 2L_{min})$.
Thus the capacitances contributed by transistors can be accounted for if we know transistor width and length.



When *as*, *ad*, *ps* and *pd* are specified, the capacitance contributed by these diffused regions is incorporated by the transistor models (and need not be specified separately as a circuit component).

A template file to simulate the inverter is given below. It uses minimum widths for n as well as p channel transistors. Your solution should replace these with appropriate values to meet the delay specification. Notice that the values of area and perimeter of source and drain regions will have to be recalculated when you change the widths.

The .include statement in the template input file given below imports the models from the file models-180nm.

```
* Unit Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
MN1 Output Inp 0      0      cmosn
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv
```

```
* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm

*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS

.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

Q–1 Design a CMOS inverter which gets a rail to rail square wave as the input with rise/fall times of 20 ps. Your inverter should have equal rise/fall times of $200 + 2 \times nn$ ps, where nn represents the last two digits of your roll number.
The design involves the choice of appropriate widths for n and p channel transistors such that it meets the rise/fall time requirements with the given load. Measure the rise/fall times of the output by finding the time taken by the output to traverse between 10% of V_{DD} and 90% of V_{DD}.

Q–2 Use ng-spice to plot the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to V_{DD}. Determine the static noise margins for it by drawing tangents with slope = -1.

Q–3 Using the above inverter as the base design, apply series-parallel rules to design a logic gate which produces $\overline{A \cdot (B + C)}$ at its output. Find the rise and fall times of this gate for the following input combinations:

a) A = '1', B = '0', C = $0 \rightarrow 1$ and C = $1 \rightarrow 0$.
b) A = '1', C = '0', B = $0 \rightarrow 1$ and B = $1 \rightarrow 0$.
c) B = '0', C = '1', A = $0 \rightarrow 1$ and A = $1 \rightarrow 0$.

Take a logic '1' to be $0.9V_{DD}$ and a logic '0' to be $0.1V_{DD}$.