Indian Institute of Technology, Bombay

MIXED SIGNAL VLSI DESIGN

EE - 719

9-Bit Hybrid Fully Differential ADC

Name : Roll Number :
Abhijeet 20D070003
G Kamalesh 20D070029

Professor : Maryam Shojaei Baghini

Feb. 20, 2023

1 Bootstrap Switch Design

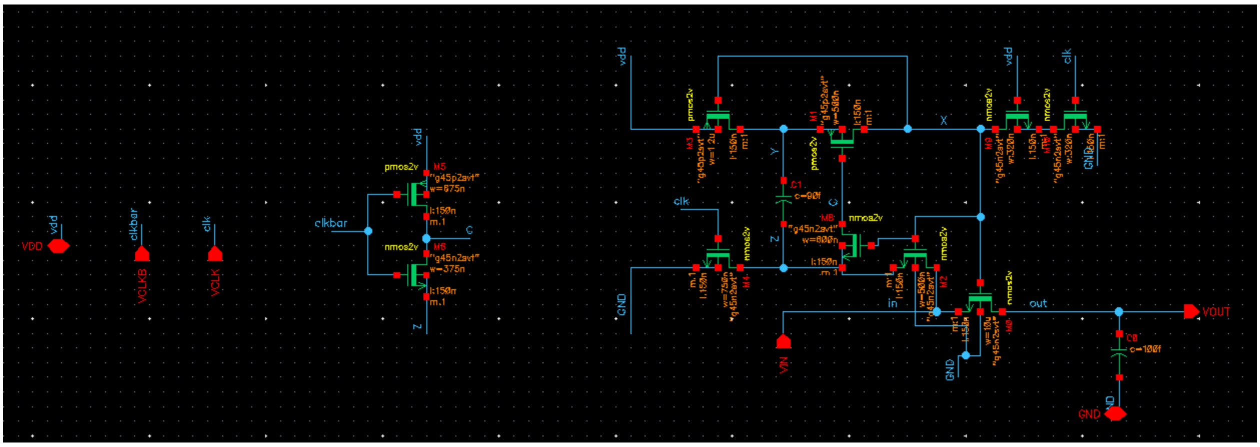

Figure 1: Bootstrap Switch Schematic

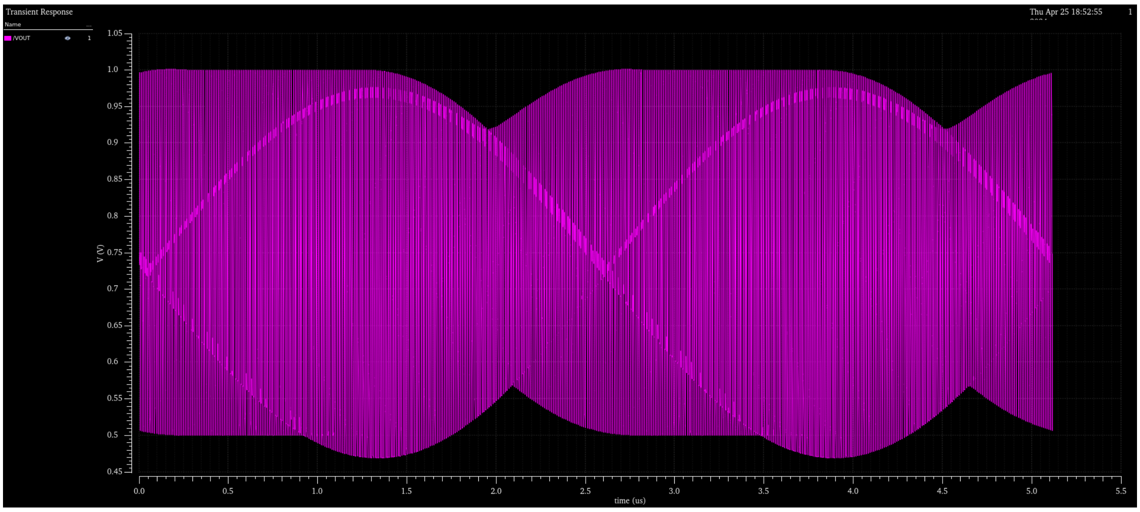

Figure 2: Bootstrap output waveform

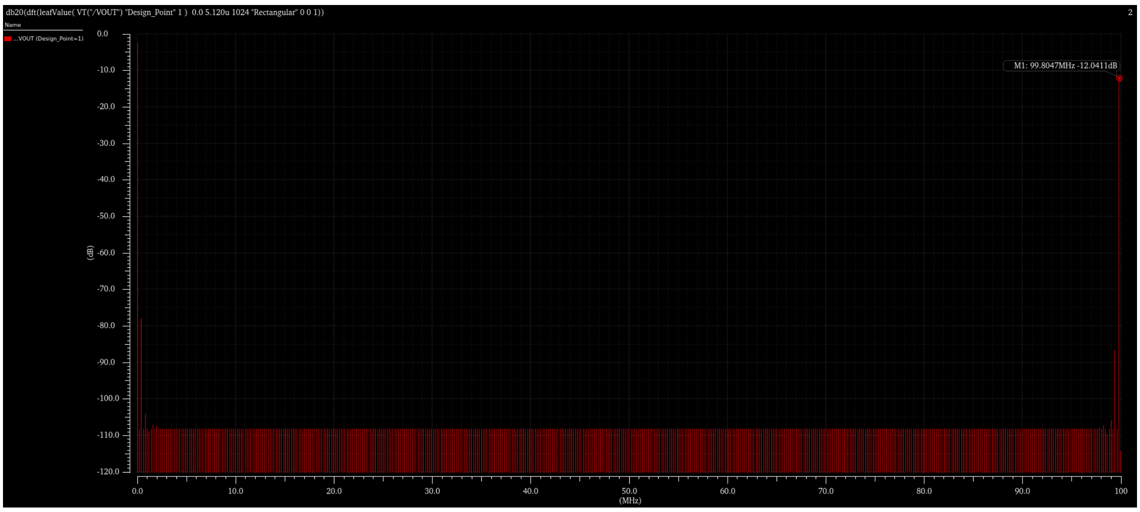

Figure 3: FFT of Bootstrap output waveform

This 9 bit bootstrap switch is giving ENOB 10.28.

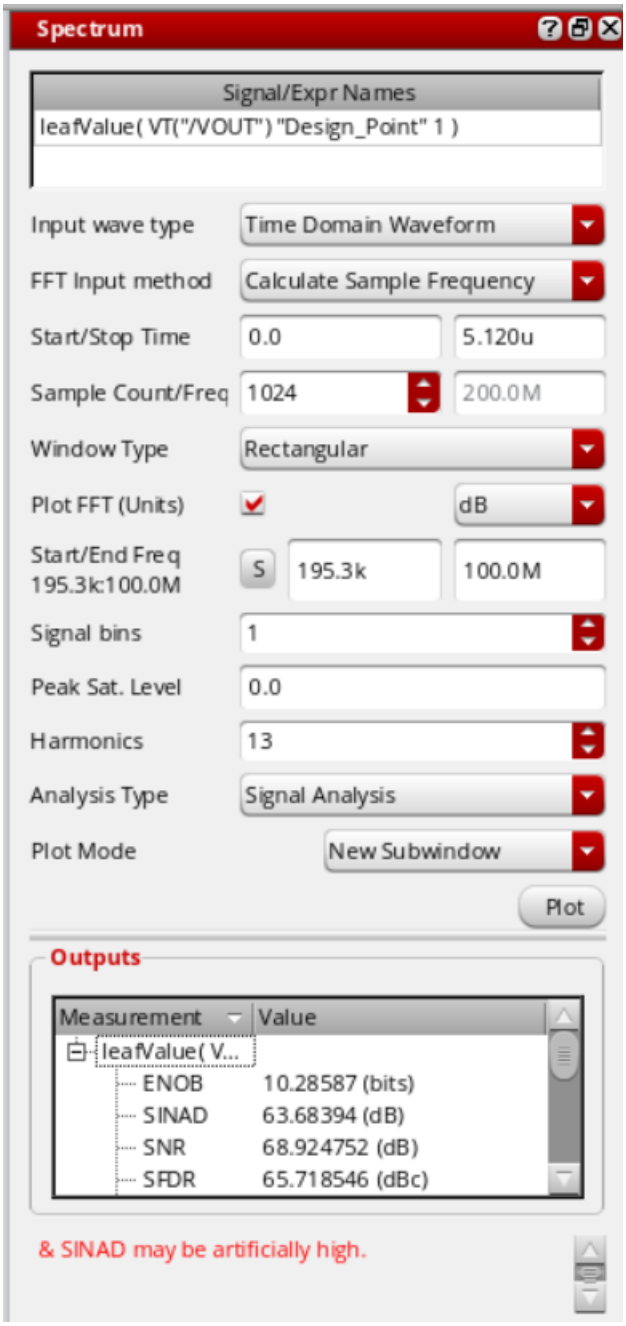

Figure 4: Bootstrap SNR

[1.1] Report the final value of the widths and lengths of all transistors.

Parameter	M_1	M_2	M_3	M_4	M_5	M_6	M_8	M_a	M_b	M_c	C_1	C_B
W(in m)	10 μ	500n	500n	320n	1.2 μ	750n	320n	675n	375n	600n	90 fF	100 fF
L(in nm)	150	150	150	150	150	150	150	150	150	150	X	X

Table 1: Final Parameter Summary of Bootstrap Switch

2 3-bit differential Flash ADC Design

2.1 Preamplifier design

The preamplifier is a fully differential amplifier designed to produce a gain of 2 before the comparator

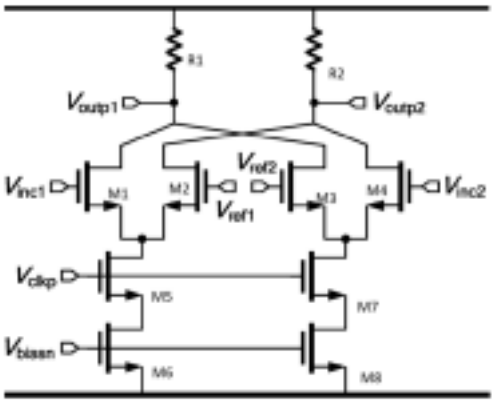

Figure 5: FFT of Bootstrap output waveform

- As a starting point we assumed to flow a 25 uA current in the tail part of the pre-amplifier.
- For that value of current we tried to find the initial value of the biased transistor such that it will come the saturation region.
- At the Width of 1um and bias voltage of 0.6V. the bottommost transistor is in saturation mode.
- Now we increasd the current by increasing widths and of the differential pair and the biased transistors. So that differential pired transistors will be in saturation mode.
- Now our final task is to increase the gain for the worst case more than 2.
- That we achieved be increasing the bias voltage from 0.6V to 0.8 V and slight increments in the widths of the transistor.

Initial parameters

Design Variable	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	R_1	R_2
Width	5um	5um	5um	5um	1um	1m	1um	1um	1KΩ	1KΩ
Length (nm)	150	150	150	150	150	150	150	150		

Table 2: Initial parameters for Preamplfier

Final parameters

Design Variable	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	R_1	R_2
Width	40u	40u	20u	20u	10u	10u	10u	10u	-	-
Length	150n	150n	150n	150n	150n	150n	150n	150n	1k	1k

Table 3: Final parameters for Preamplifier

Please note that the transistor numberings are reversed in the table and the schematic

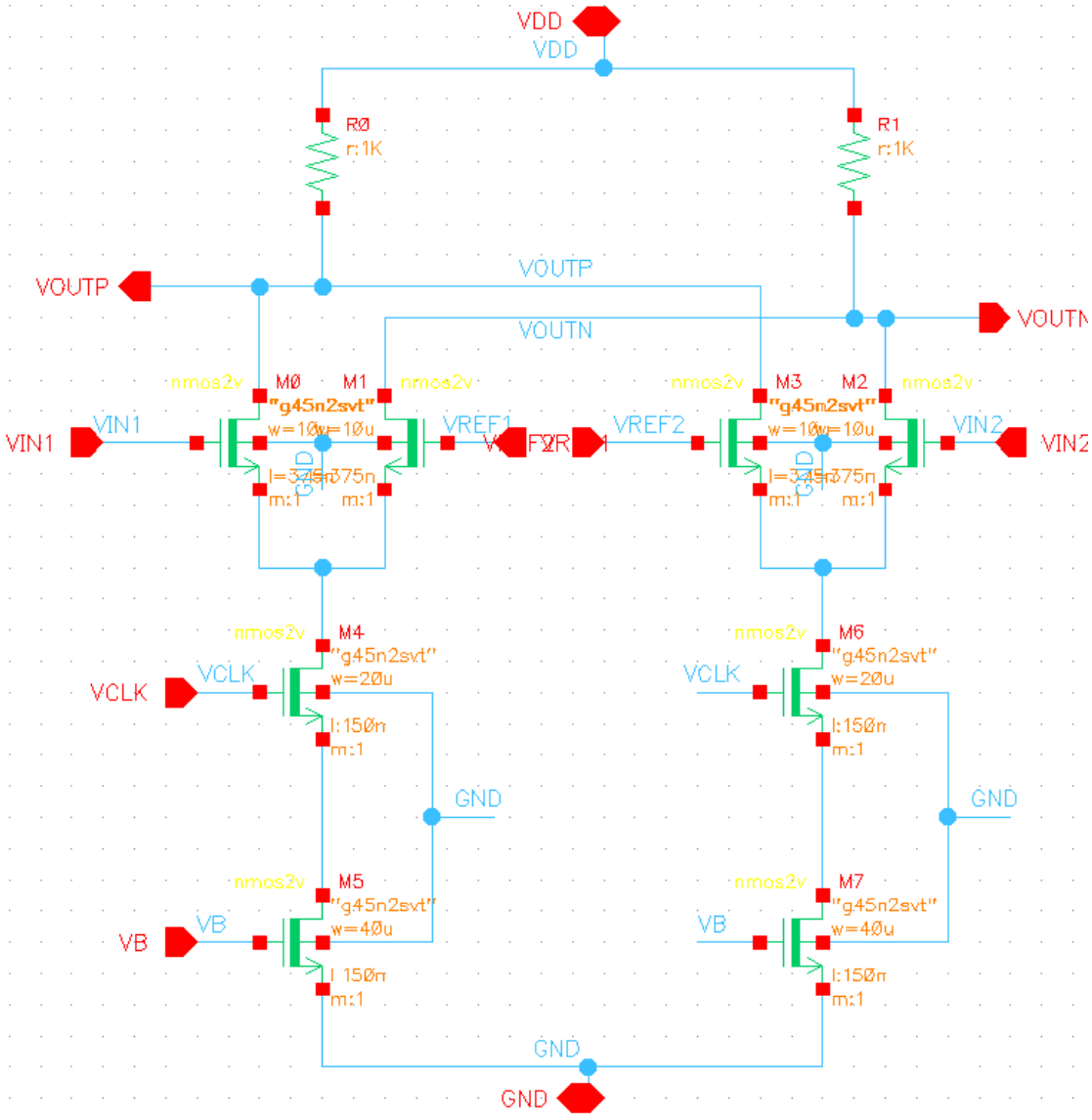

Figure 6: Preamplifier schematic

2.2 Testing of Preamplifier

1. Take Vref1 = 0.9375 V and Vref2 = 0.5625 V (worst case reference inputs in the flash ADC) and Vinc1 = Vcm + 0.25 Sin(2fint) and Vinc2 = Vcm 0.25 Sin(2fint) and plot the transient output for fin = 50 MHz.

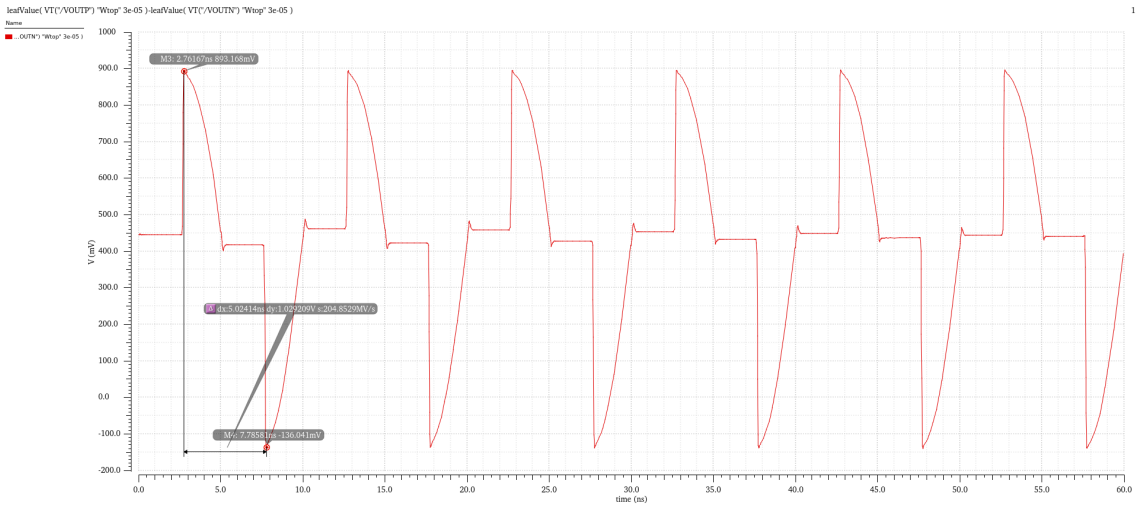

Figure 7: Preamplifier output waveform

2. Take Vref1 = 0.75 V and Vref2 = 0.75 V and Vinc1 = Vcm + 0.25 Sin(2fint) and Vinc2 = Vcm 0.25 Sin(2fint) and plot the transient output for fin = 50 MHz.

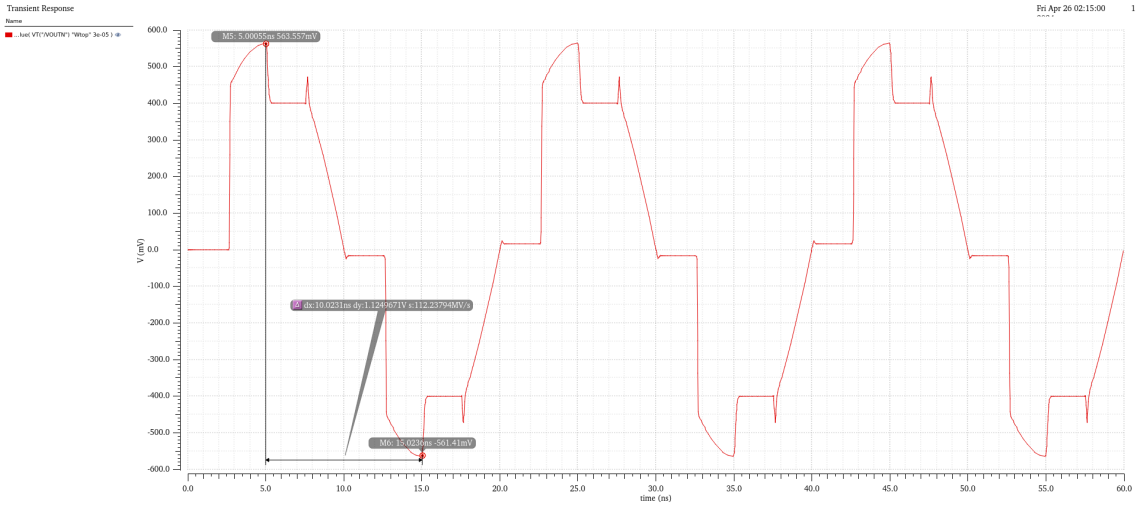

Figure 8: Preamplifier output waveform

2.3 Reuse of the comparator designed in assignment 5 + RS Latch

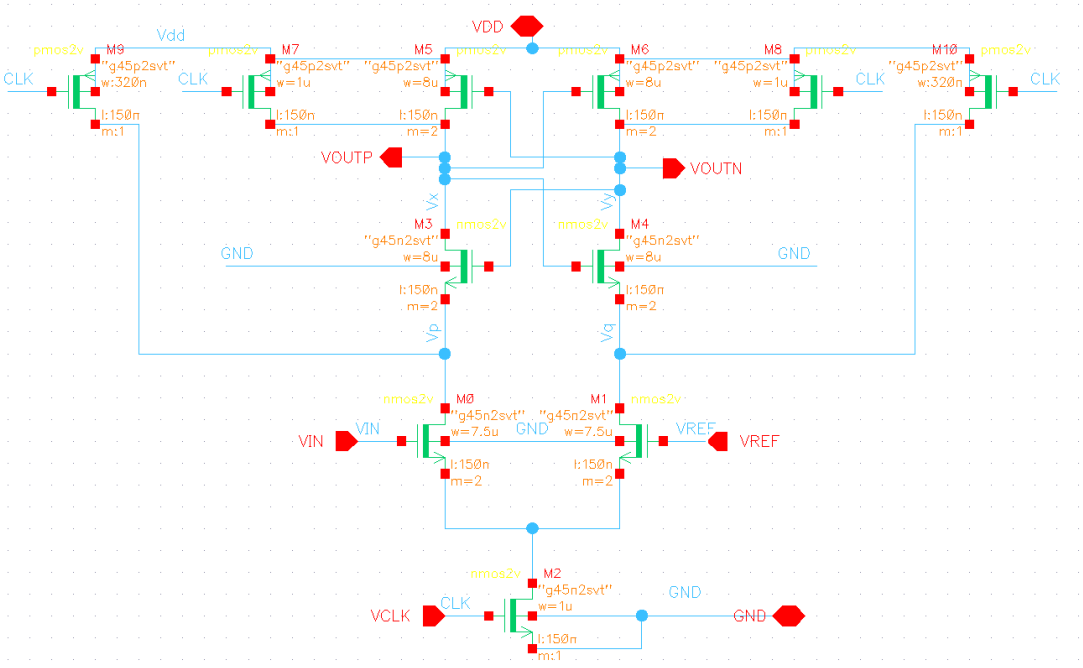

Figure 9: Strong arm Latch Comparator schematic

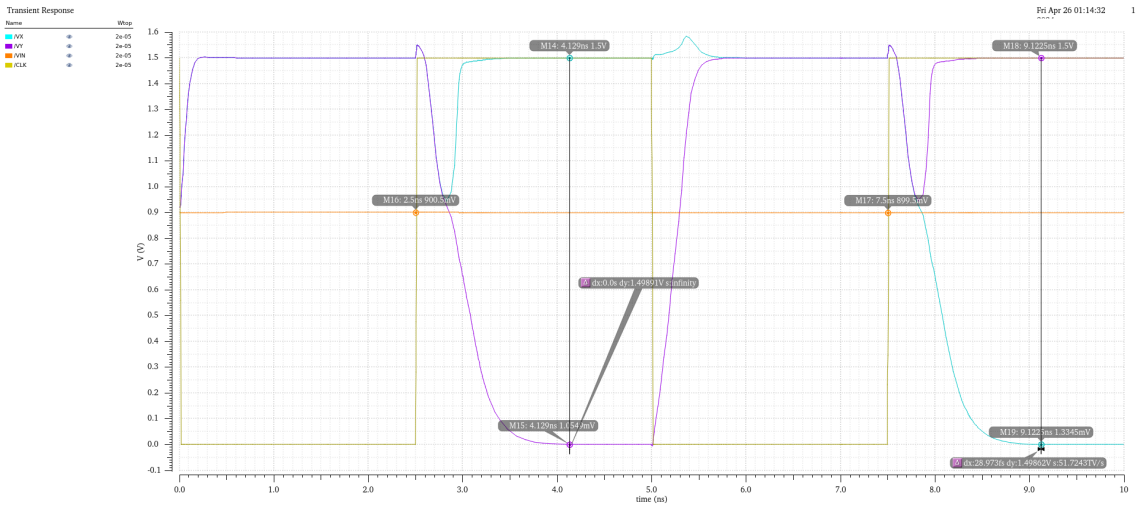

Figure 10: Strong arm Latch Comparator schematic

Design Variable	M_0	M_1	M_2	M_3	M_{P1}	M_{N1}	M_{P2}	M_{N2}
Width	5u	5u	10u	10u	640nmu	320nm	640nm	320nm
Length	150n	150n	150n	150n	150n	150n	150n	150

Table 4: Initial parameters for Preamplifier

Design Variable	M_0	M_1	M_2	M_3	M_{P1}	M_{N1}	M_{P2}	M_{N2}
Width	20u	20u	25u	25u	640nm	320nm	640nm	320nm
Length	150n	150n	150n	150n	150n	150n	150n	150

Table 5: Final parameters for Preamplifier

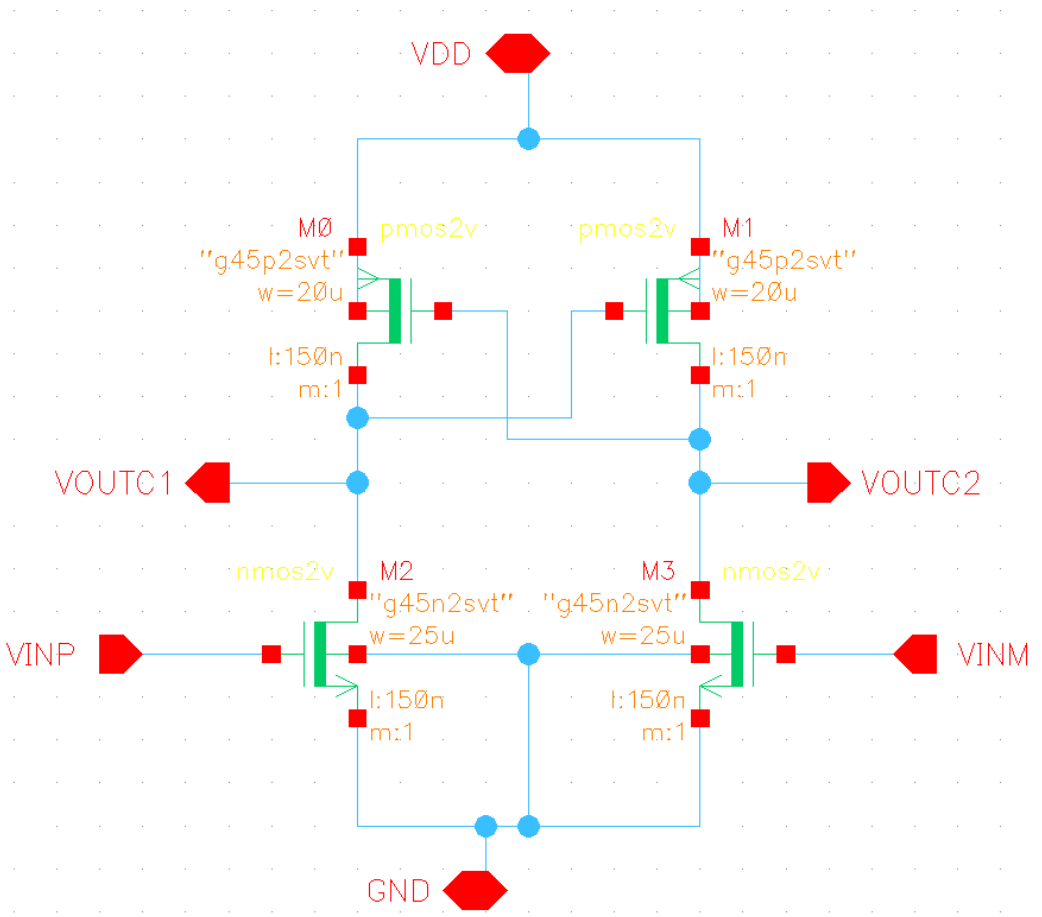

Figure 11: RS Latch schematic

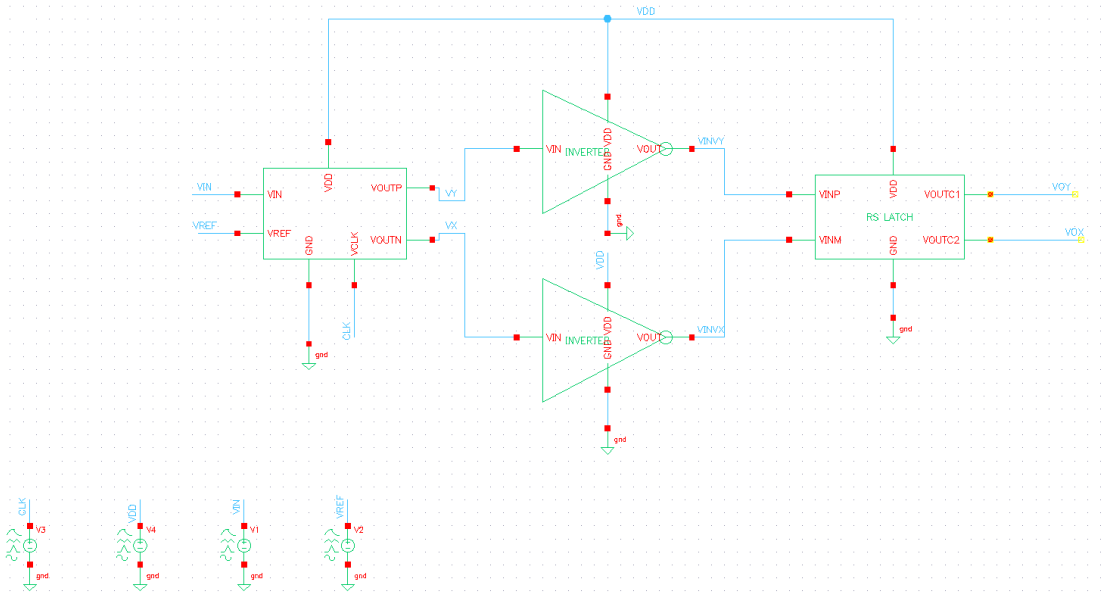

Figure 12: Strong arm Latch Comparator followed by RS Latch Testbench

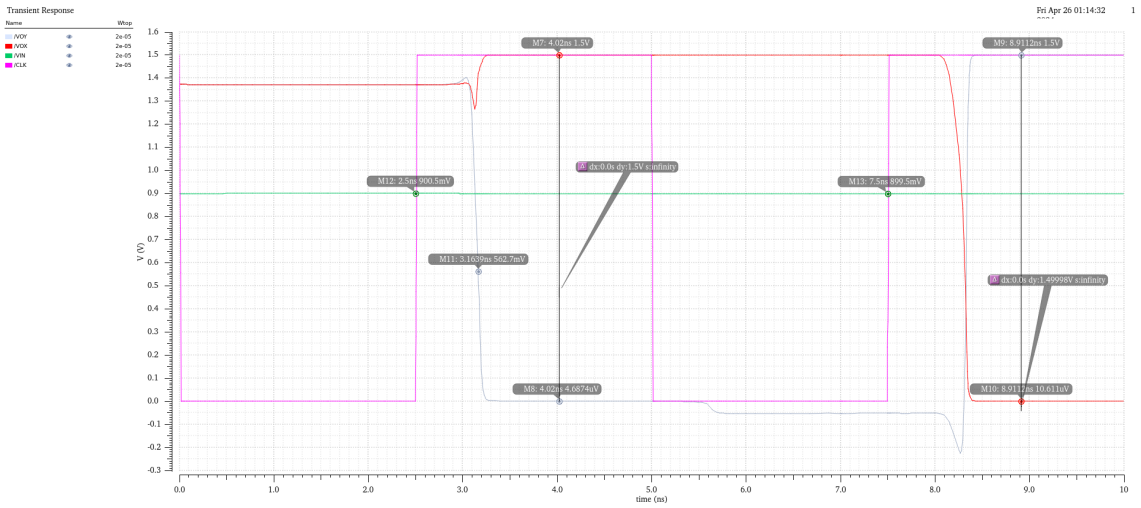

Figure 13: Strong arm Latch followed by RS Latch output waveform

2.4 Differential Flash ADC

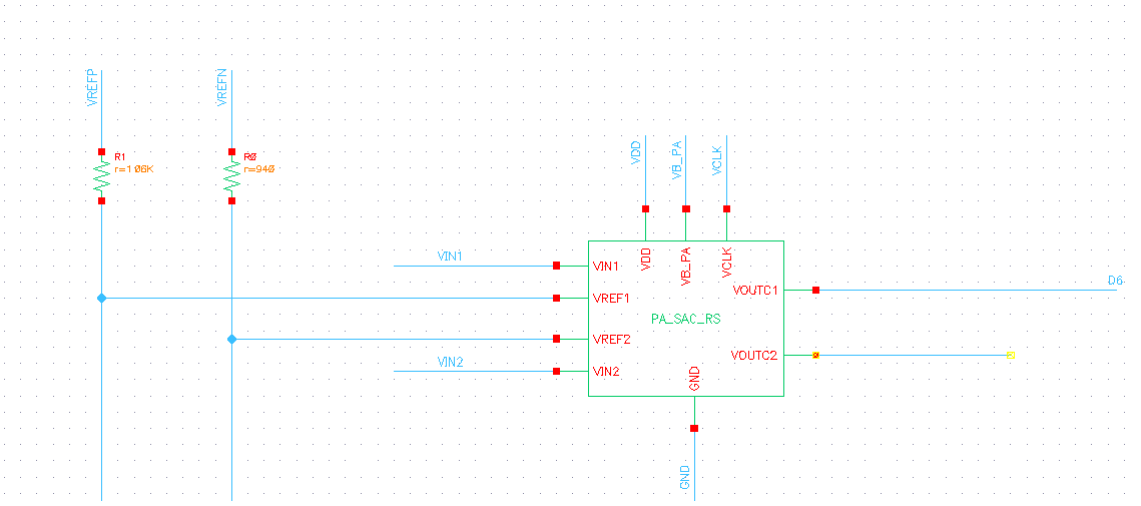

Figure 14: Temperature code generator

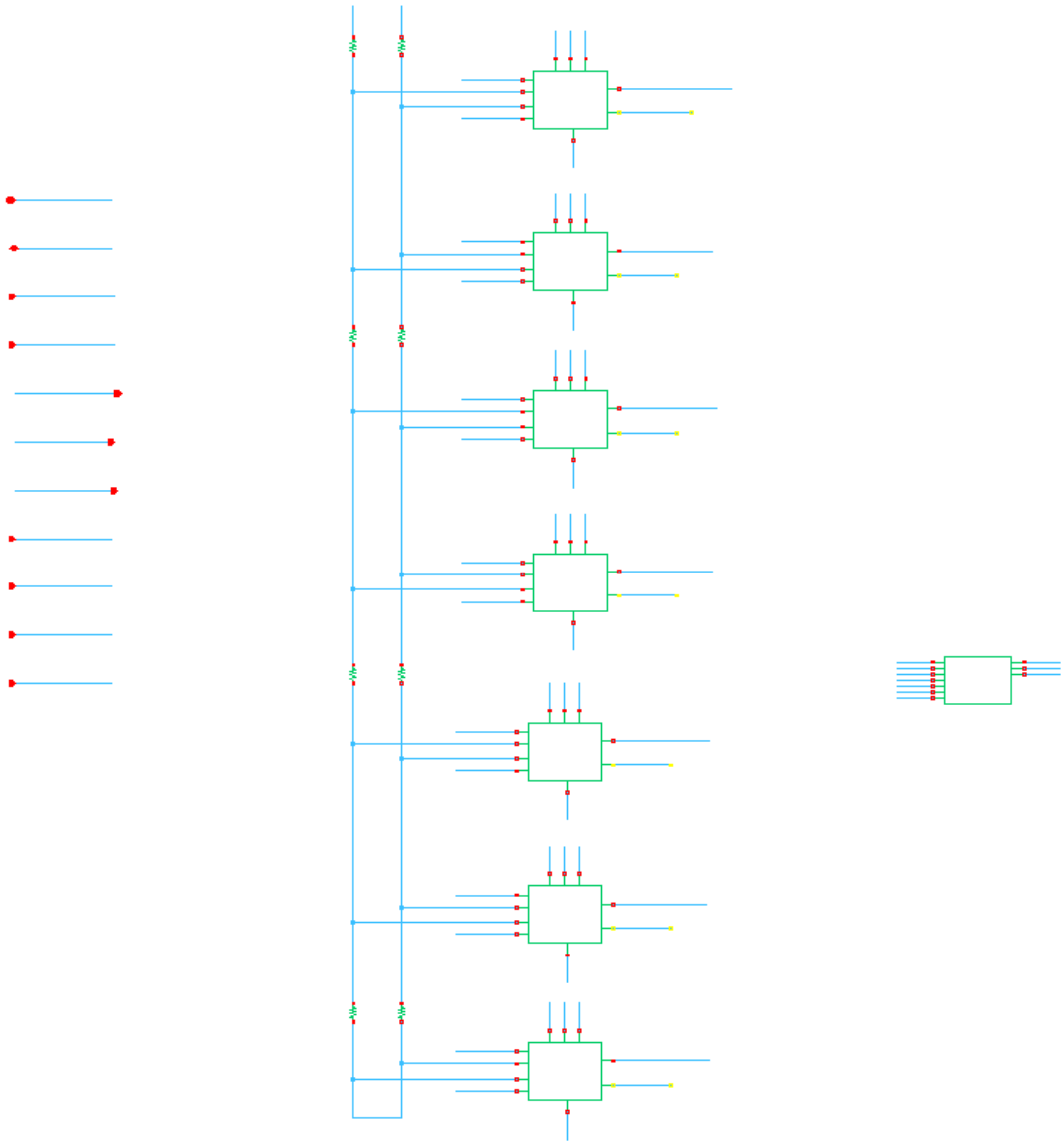

Figure 15: 3 Bit Fully differential Flash ADC

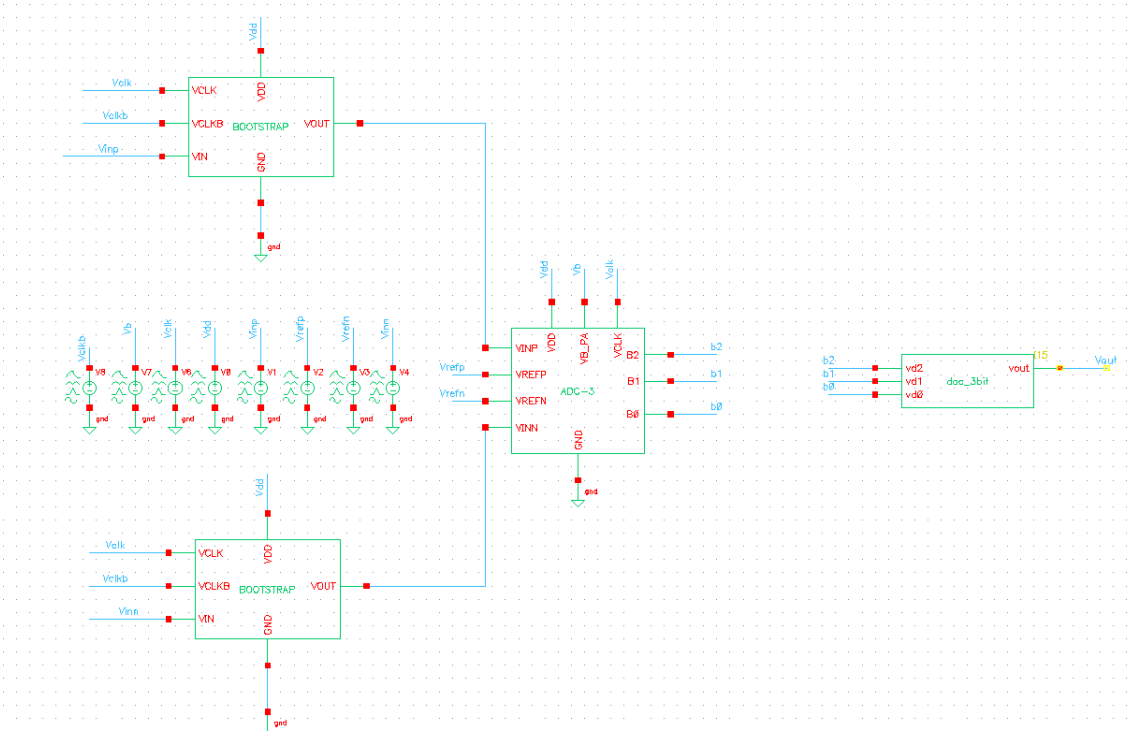

Figure 16: Flash ADC Testbench

2.5 FFT with ADC + ideal DAC topology

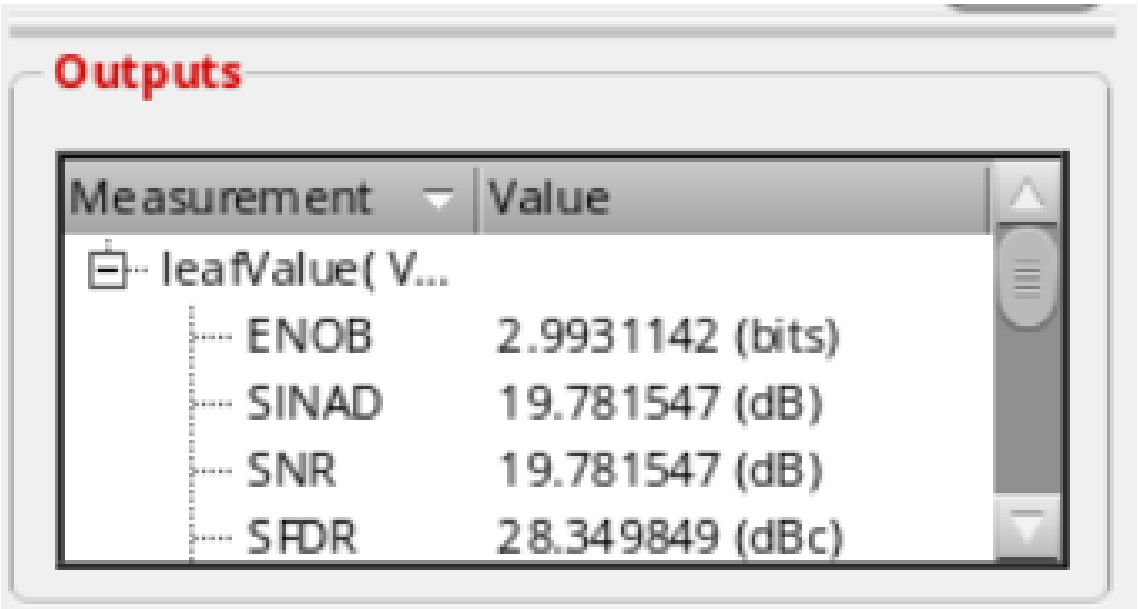

Figure 17: SNR of Flash ADC

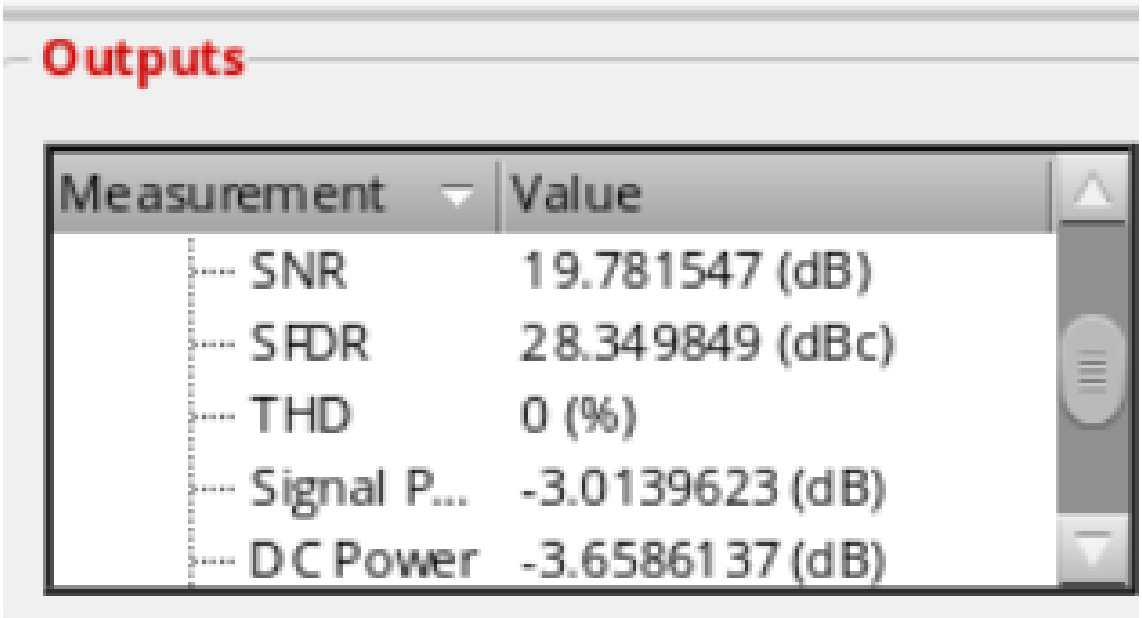

Figure 18: THD of Flash ADC

2.6 INL DNL - non-linearities in the resistor

The value of R is 1k Ω and hence, Δ R = 20 Ω. The plots obtained by providing a ramp signal at the input are attached below:

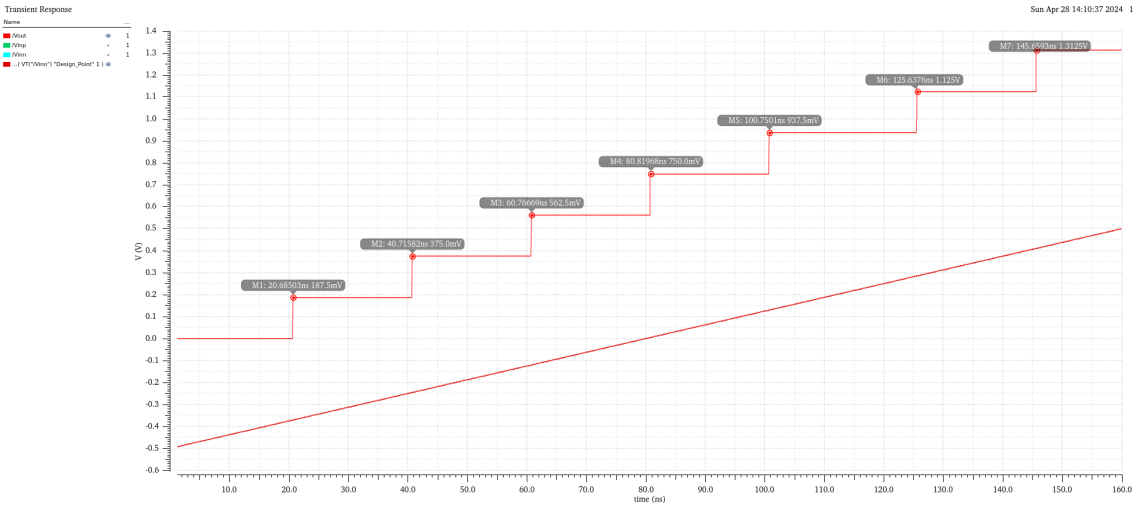

Figure 19: DAC Output vs Input characteristics

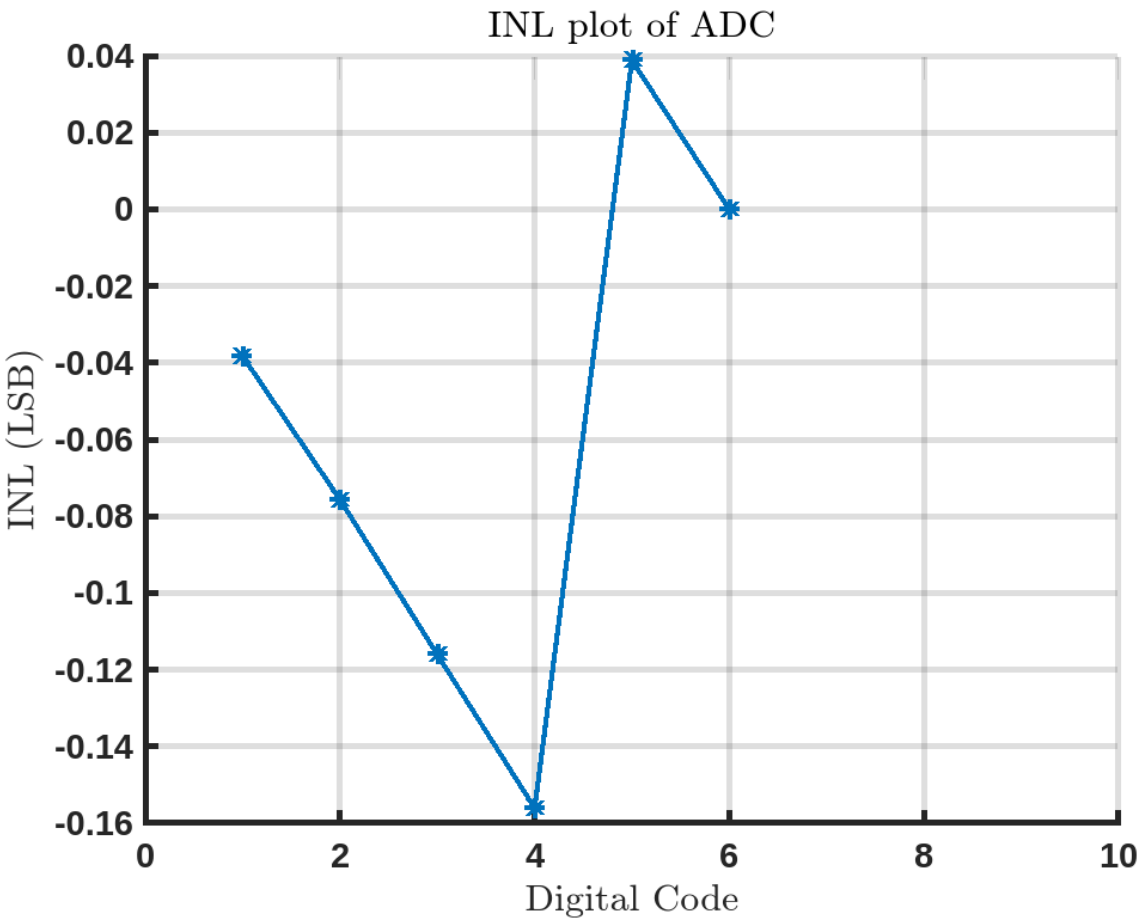

Figure 20: INL

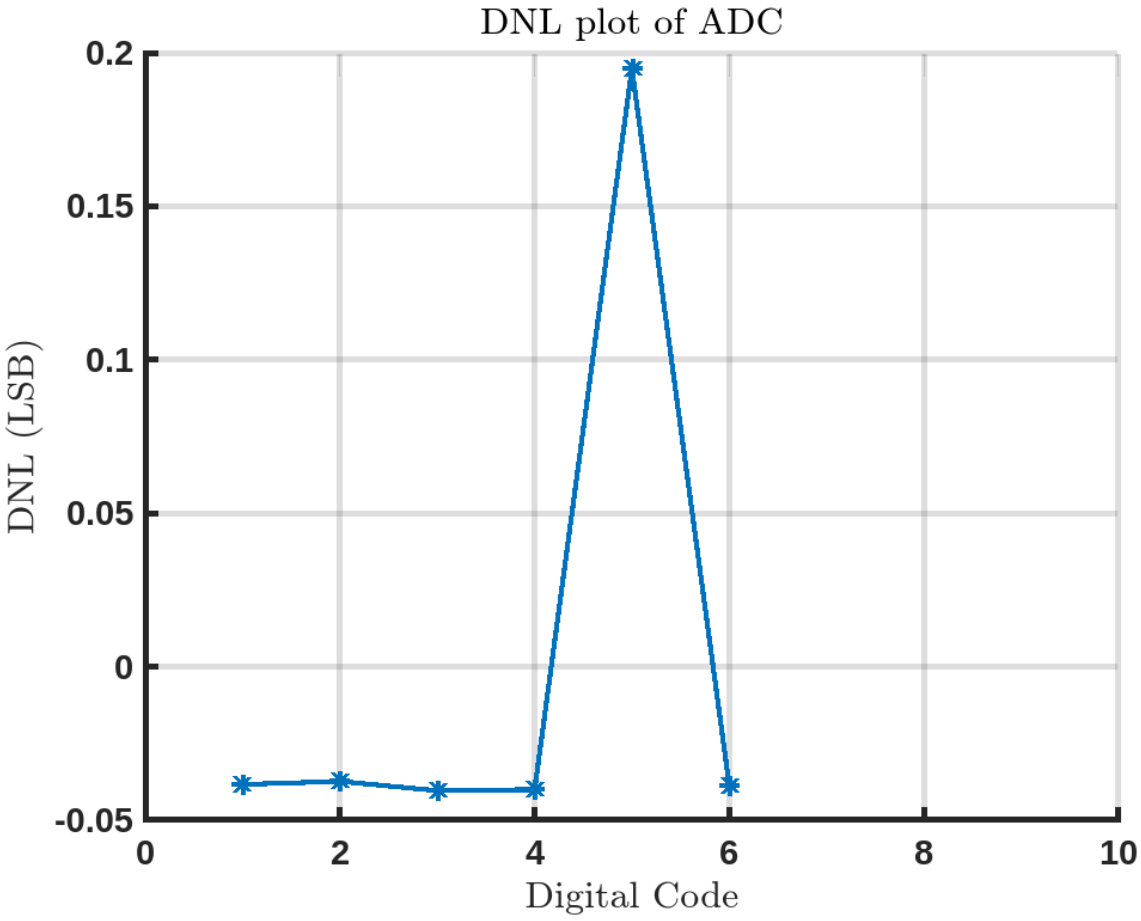

Figure 21: DNL

Parameters	Values
Supply Voltage (V_{DD})	$1.5\,V$
Input Voltage Swing (V_{FS})	$0.5 - 1.0\,V$
Number of Bits (N)	3
Sampling Frequency	$200\,MHz$
Temperature	$27°C$
Clock rise, fall time	$20\,ps$

Figure 22: Specifications of SAR ADC

3 Design of 6-bit Differential SAR ADC

3.1 Comparator + RS Latch

In this section, you need to design a latched comparator for the fine ADC. The Report the design procedure followed and tabulates the initial and final dimensions of all the transistors. Ensure that the comparator's outputs are settling within a half-clock cycle.

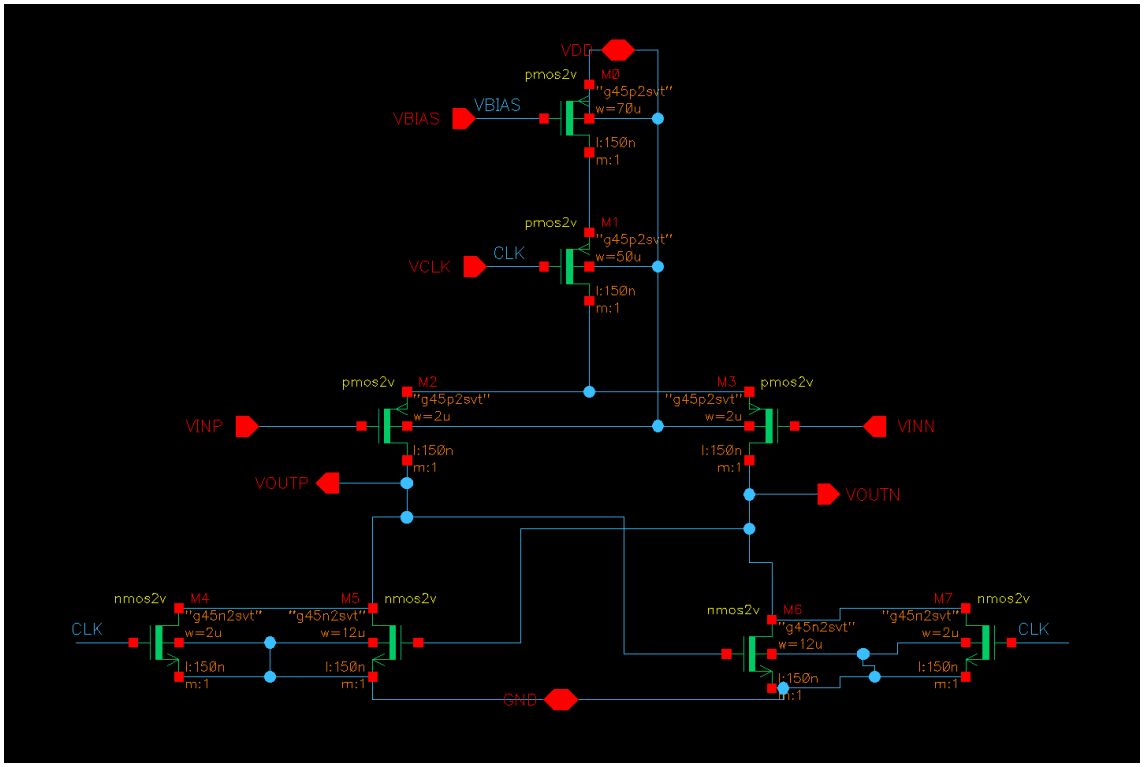

Figure 23: PMOS Strong Arm Latch Comparator Schematic

Design Variable	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
Width	70u	50u	2u	2u	2u	12u	12u	2u
Length	150n	150n	150n	150n	150n	150n	150n	150n

Table 6: Final parameter summary of PMOS Strong ARM latch comparator

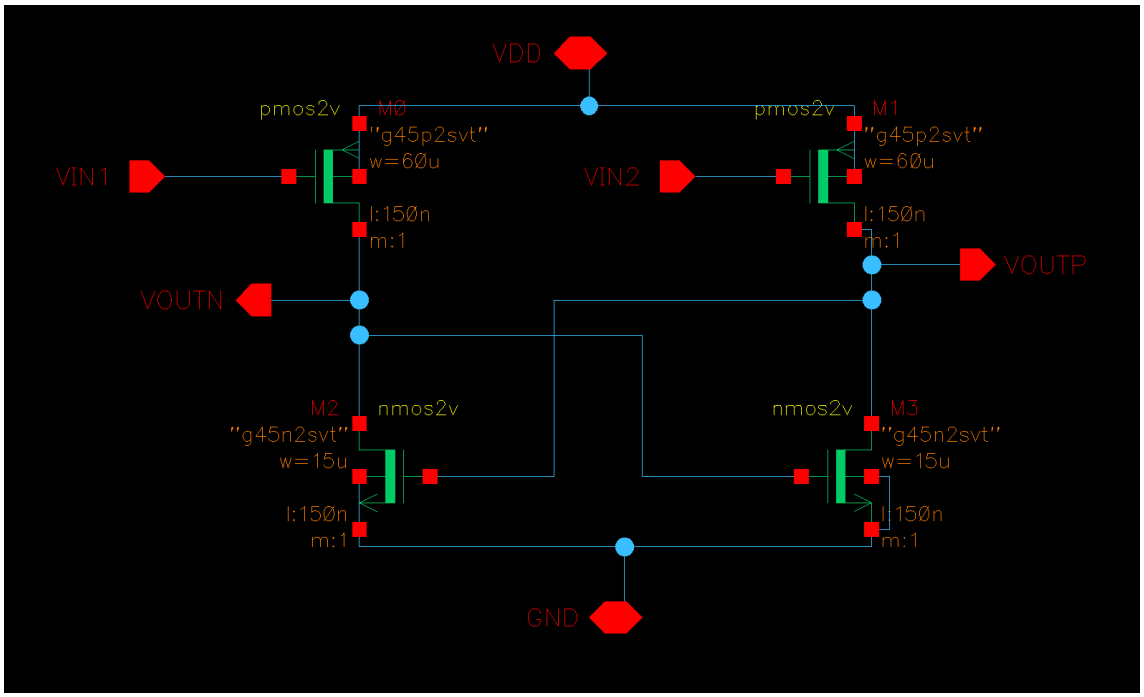

Figure 24: RS Latch Schematic

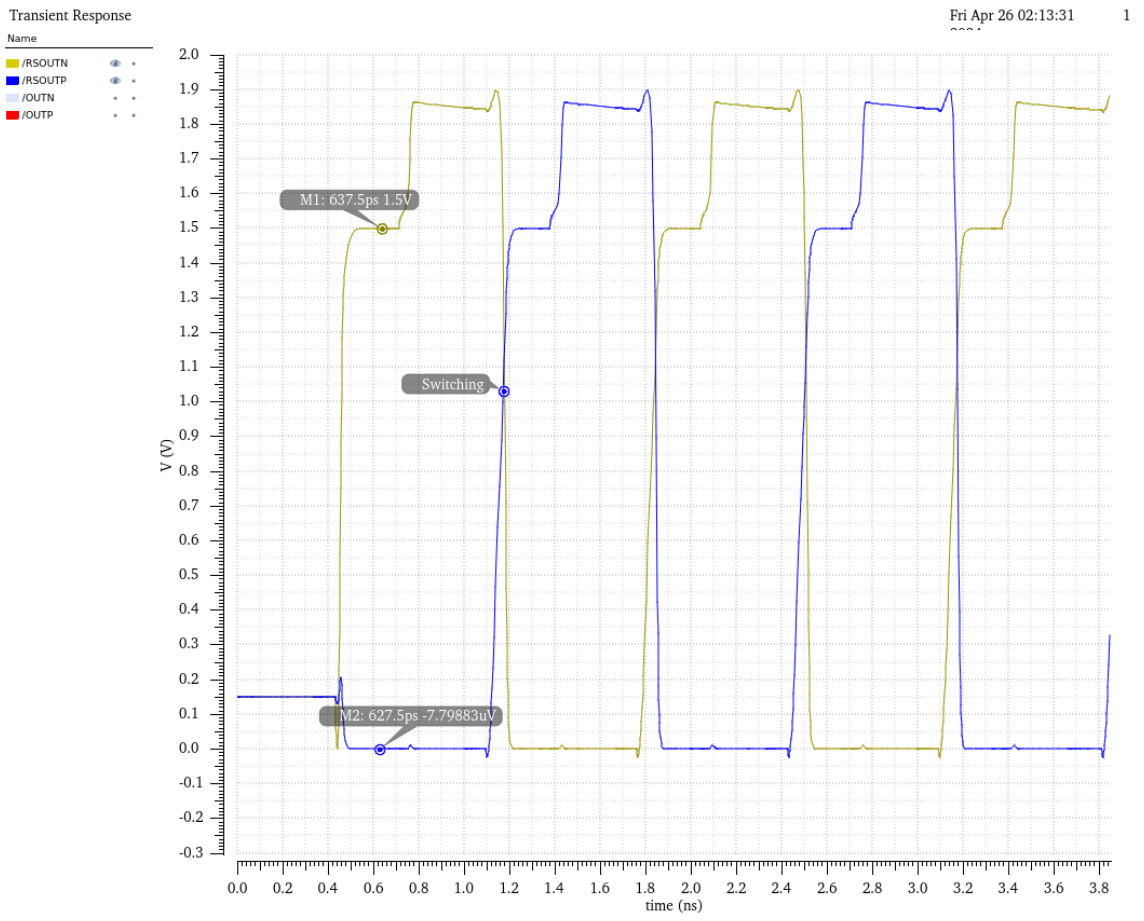

Figure 25: RS Latch output waveform

Design Variable	M_{P1}	M_{N1}	M_{P2}
M_{N2}			
Width	60u	15u	60u
15u			
Length	150n	150n	150n
150n			

Table 7: Final parameters for Preamplifier

3.2 Binary weighted charge redistribution capacitive DAC

1. Choose an appropriate unit capacitance value for the C-DAC considering the SNR requirements. Justify the capacitance value chosen in the report.
   SNR of the Sampler-ADC cascade is,

$$SNR = \frac{\frac{A^2}{2}}{\frac{\Delta^2}{2} + \frac{KT}{C_1}} \tag{1}$$

   Ideal SNR = 56 dB = $10 \log\left(\frac{\frac{A^2}{2}}{\frac{\Delta^2}{2}}\right) \implies \frac{\Delta^2}{A^2} = 10^{-6.2}$

   Degraded SNR = 56 - 2 = 54 dB.

$$SNR = 54dB = 10 \times log\left(\frac{\frac{A^2}{2}}{\frac{\Delta^2}{2} + \frac{KT}{C_1}}\right) \tag{2}$$

$$C_1 = 90 \times 10^{-15} \tag{3}$$

   Since the SAR ADC is fully differential, the capacitance C1 would be twice C1. Therefore, C1 = 180 fF. We took C_1 = **217 fF**.

2. To introduce nonideality in the capacitor values, use the MATLAB script provided to generate the values of the 5 capacitances to be used. You need to input your group number and the chosen value of the unit capacitance. Use the same capacitances for C-DACs on both sides of SAR ADC (e.g. C1p = C1n).
   We had assumed the mean value of unit capacitance to be 7 fF and our group number is 5. The corresponding capacitance values(in fF) are 6.9760, 14.2333, 27.7853, 57.4759, and 111.9812.

3.3 SAR Logic

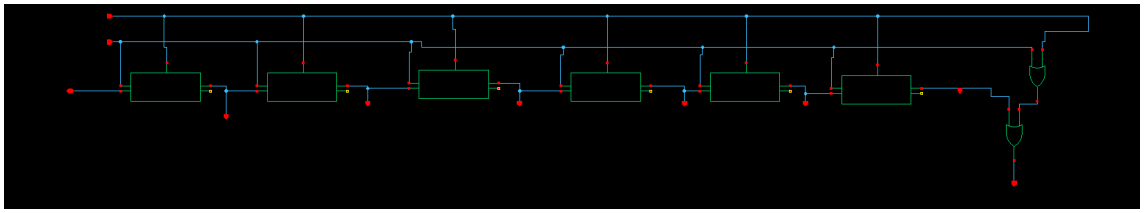

Figure 26: SAR Logic Schematic

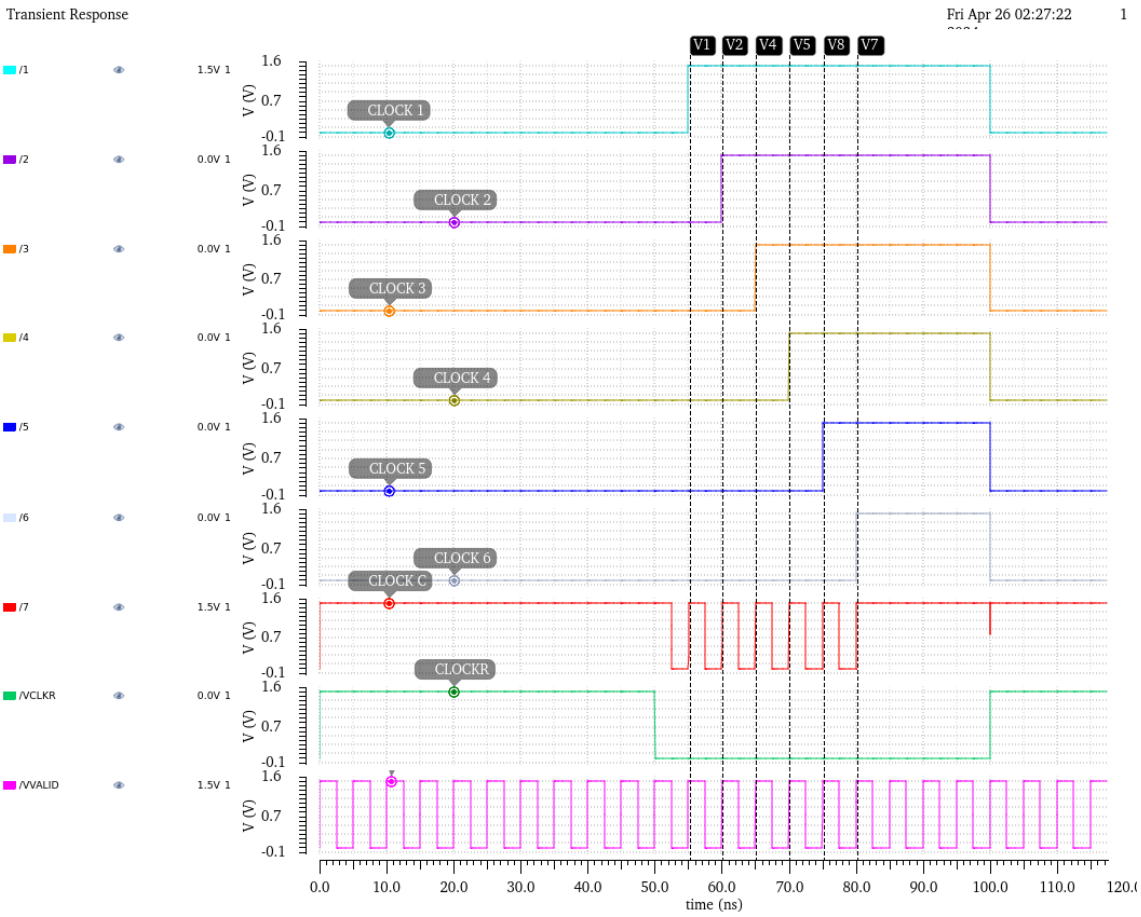

Figure 27: SAR Logic

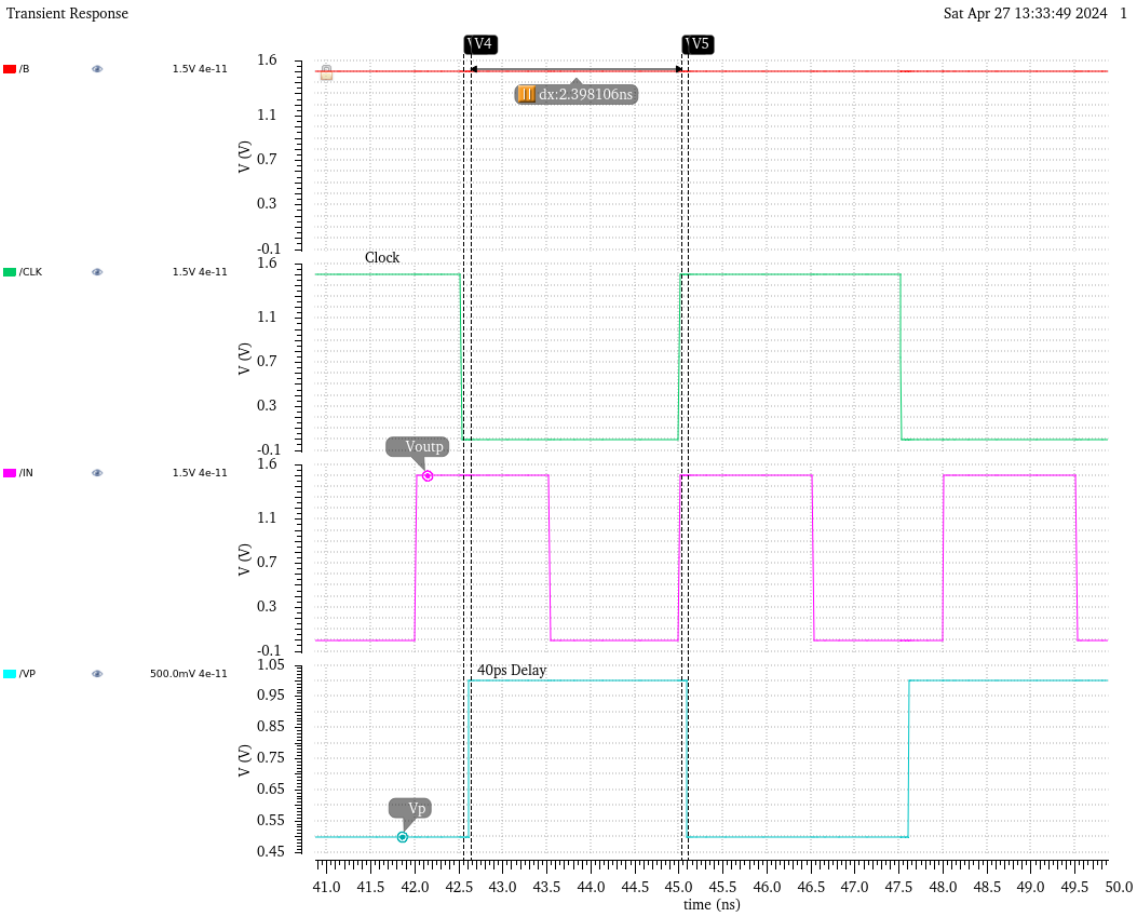

Figure 28: SAR Logic

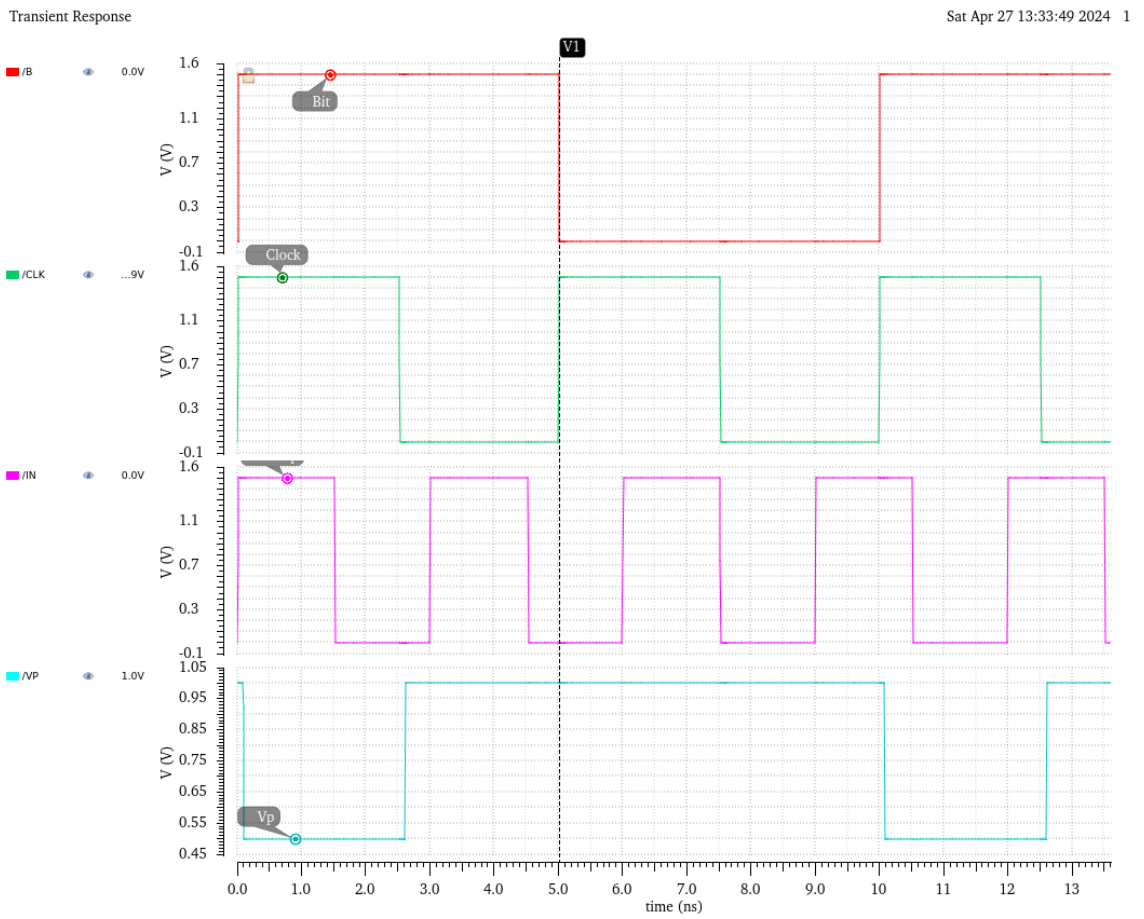

Figure 29: SAR Logic

(a) **Monotonic Switching:**
Plot the waveforms of Vinp and Vinn (inputs to the comparator of SAR ADC), showing the reduction in range due to the monotonic switching scheme for the complete SAR conversion cycle (6 clock cycles), for inputs - 0.64V (V_{inp}) and 0.72V (V_{inn}).

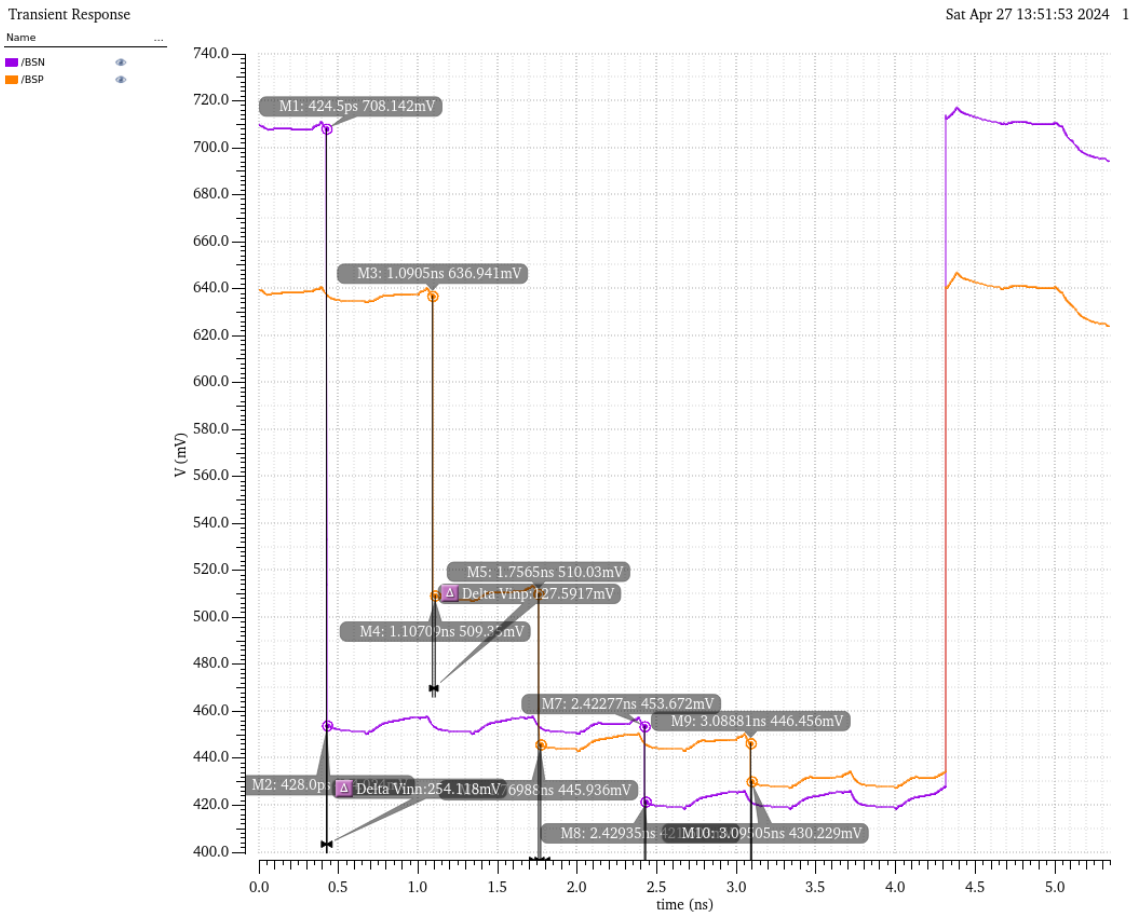

Figure 30: Input waveform monotonic switching

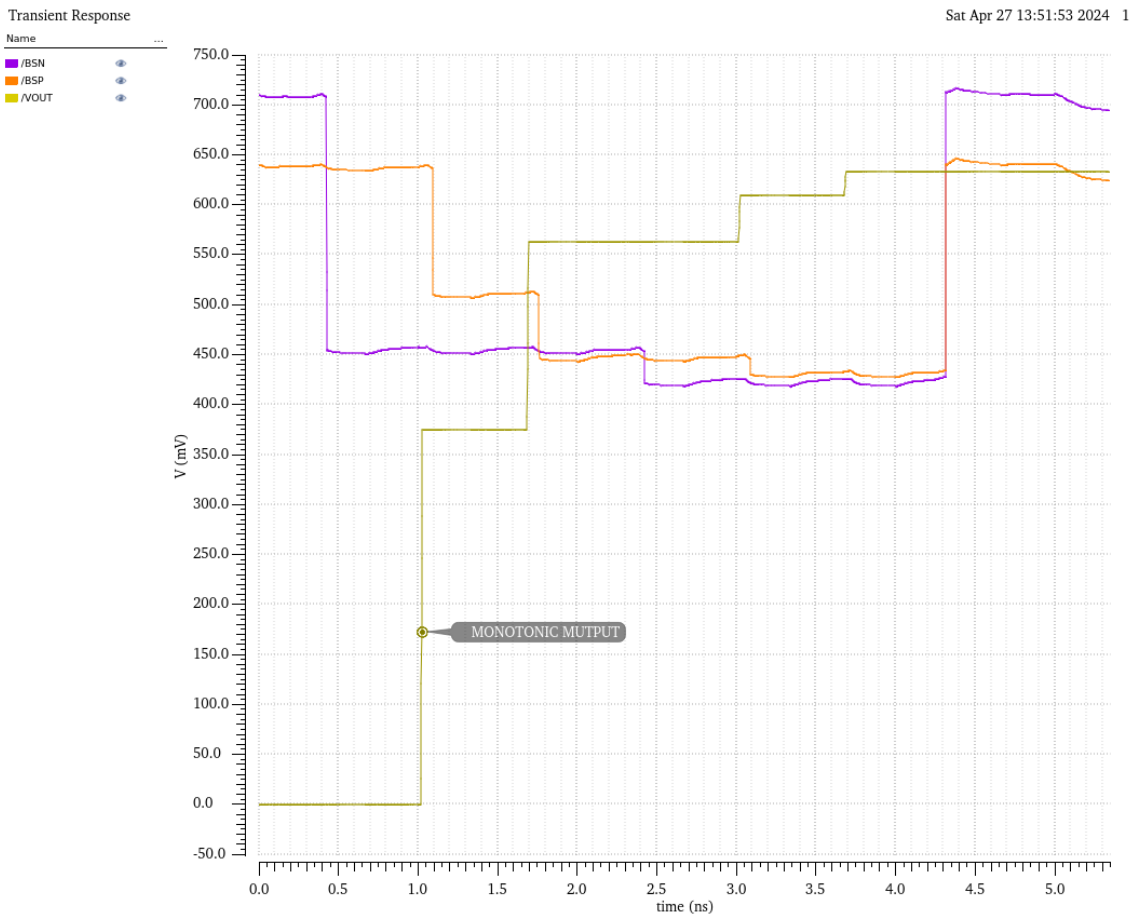

Figure 31: Output waveform monotonic switching

(b) **Output waveform:**
Use the provided ideal 6-bit DAC at the outputs of the SAR ADC. Apply a differential input ramp as shown in Fig. 6 (b)for 800 clock cycles. Plot Output (after DAC) versus Input (differential ramp) characteristics of the ADC.

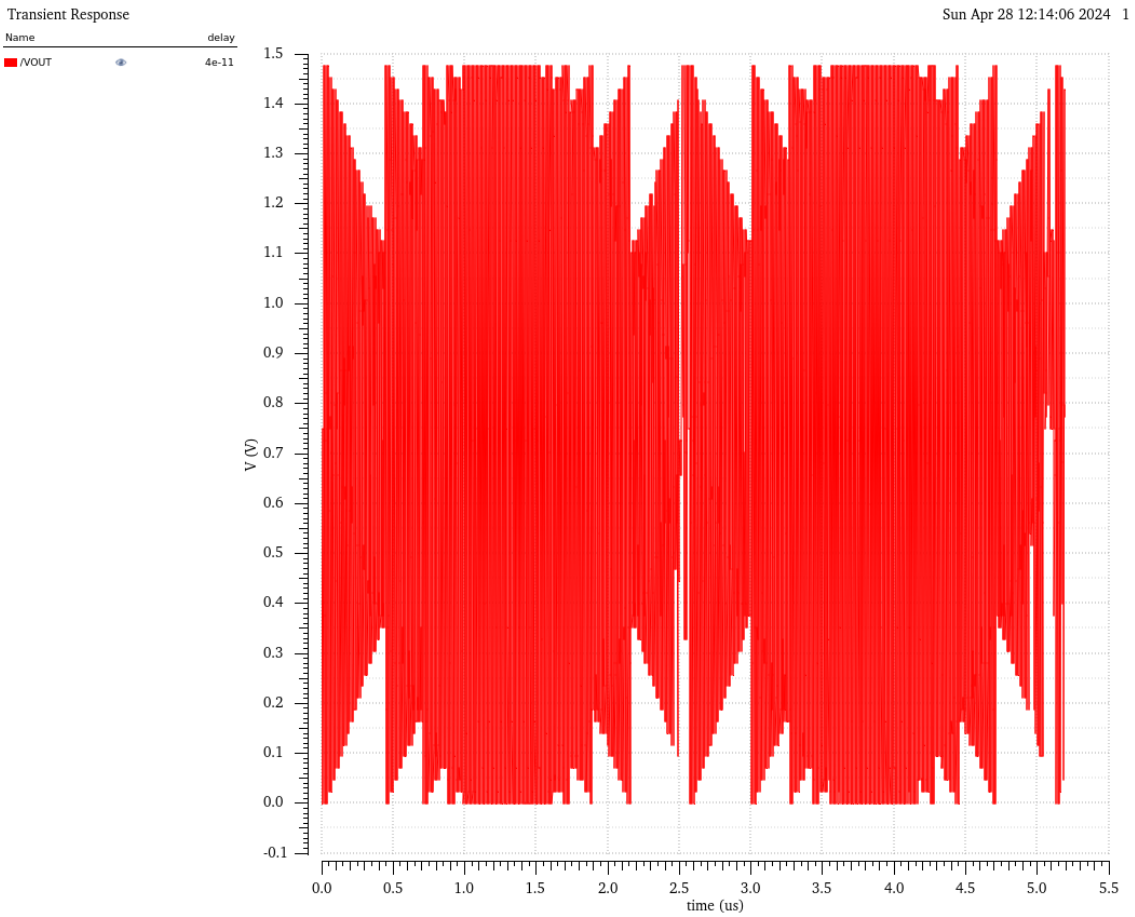

Figure 32: DAC output waveform characteristics of SAR ADC

(c) **INL DNL** Using the same applied inputs in part (b), for the obtained output characteristics, plot the INL and DNL of the ADC versus code using the MATLAB code provided.

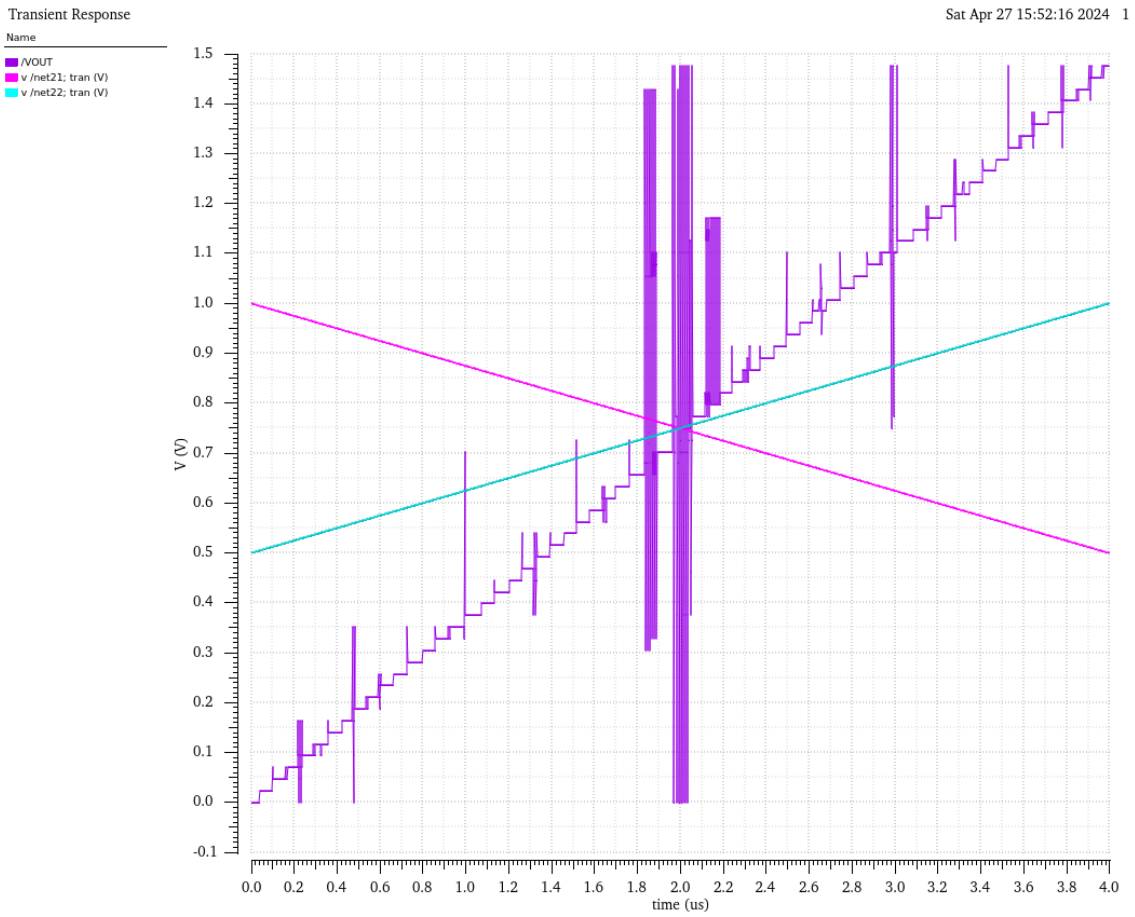

Figure 33: Output characteristics of Ramp input

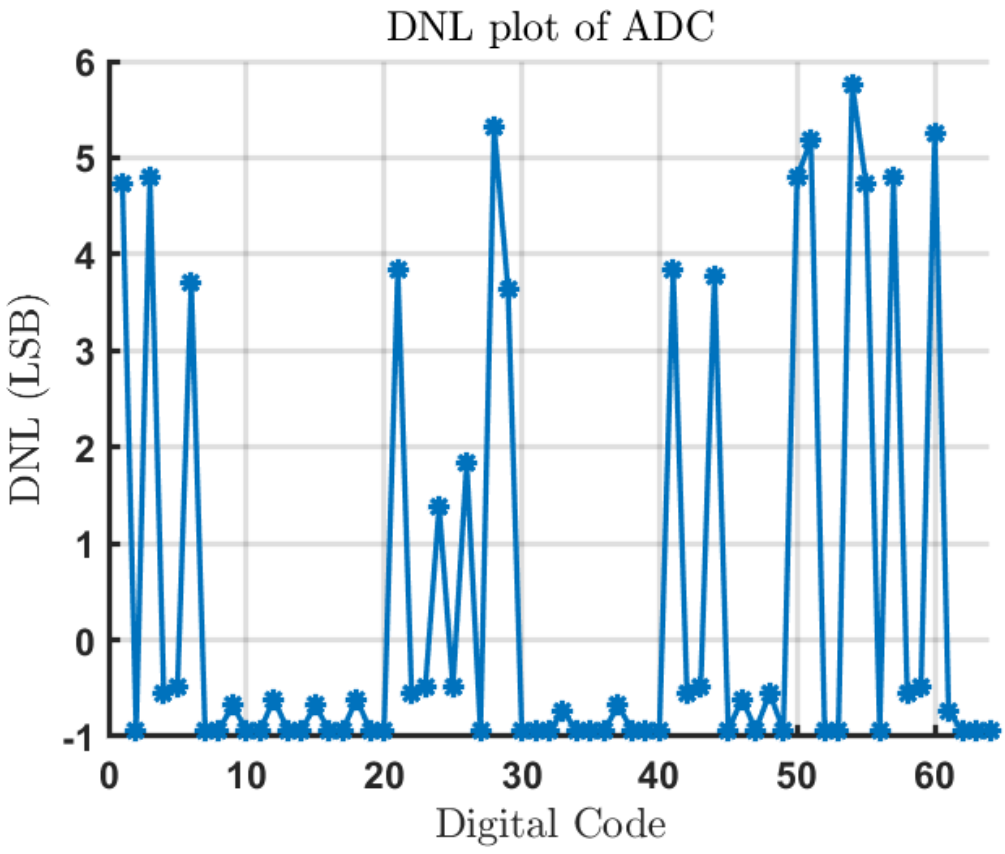

Figure 34: DNL plot of SAR ADC

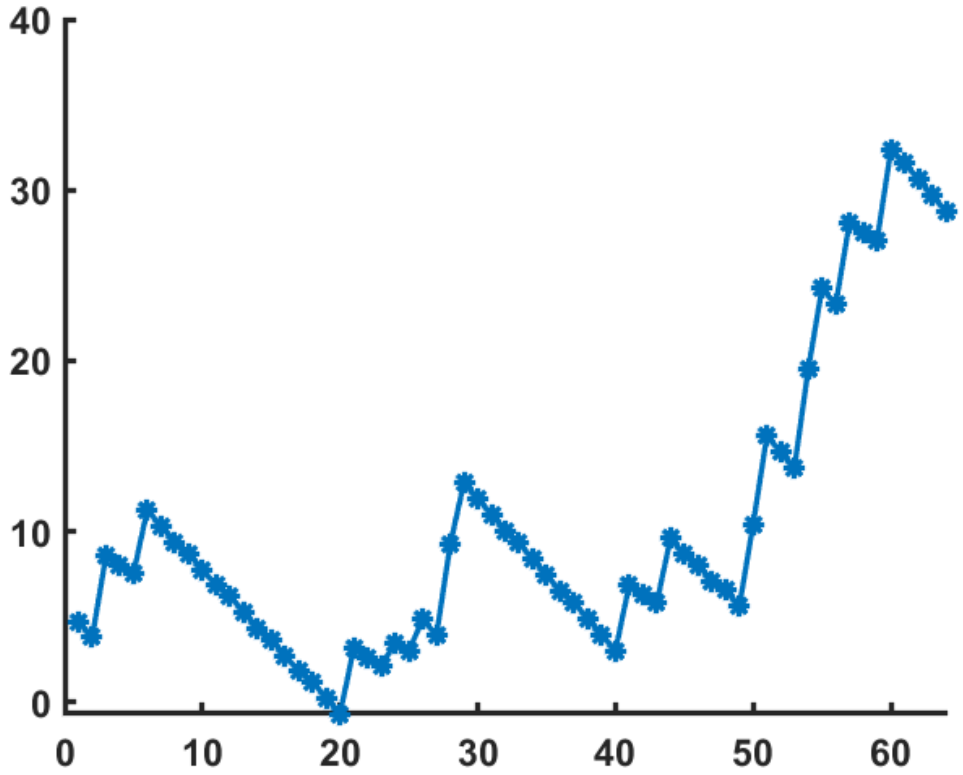

Figure 35: INL plot of SAR ADC

(d) **FFT, SNR ENOB:** To the circuit shown in Fig. 11, apply Vin1 = 0.75+0.25 Sin(2fint) and Vin2 = 0.750.25 Sin(2fint) with fin = m · fs/N, m = 511, N = 1024 and plot FFT of the Vout. Annotate the fundamental, 2nd and 3rd harmonic components and calculate ENOB, SNR.

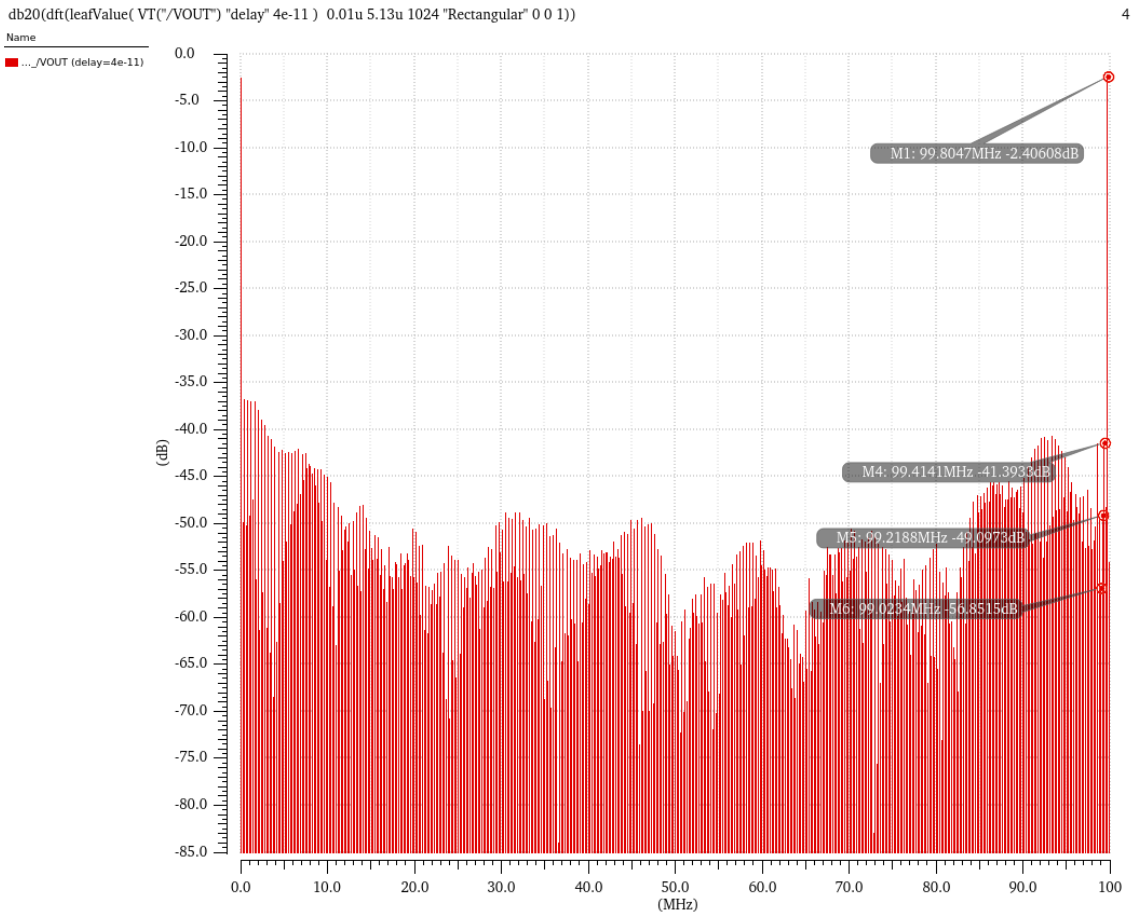

Figure 36: FFT of output waveform for SAR ADC

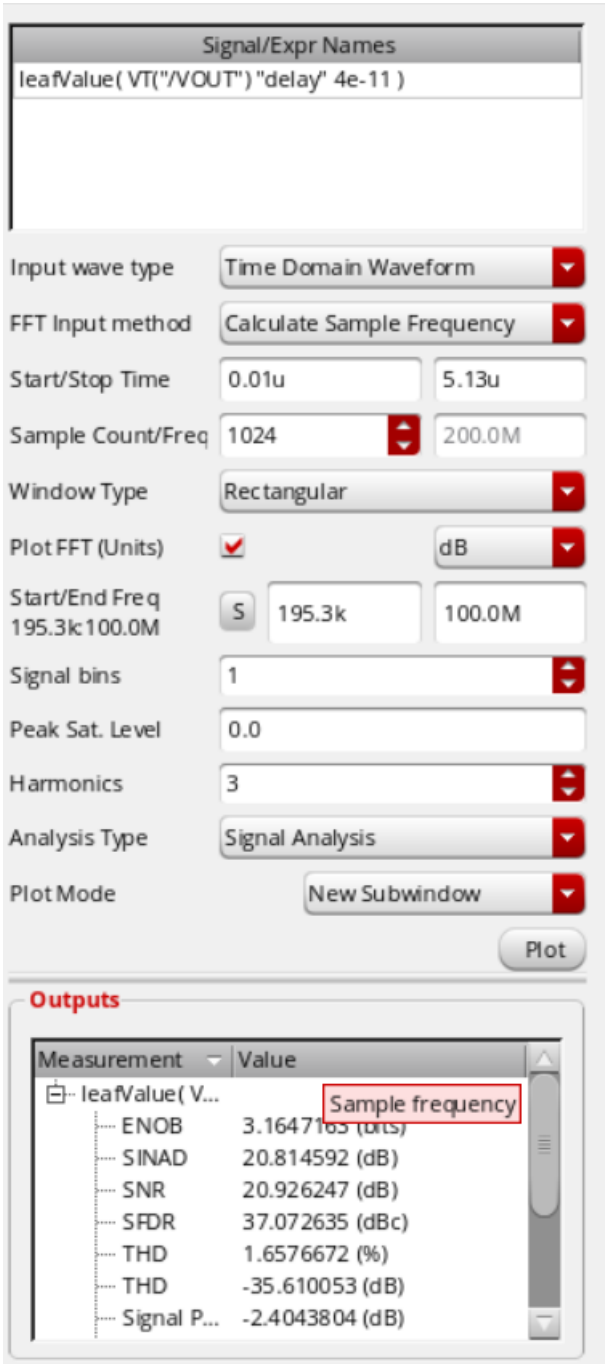

Figure 37: FFT of output waveform for SAR ADC

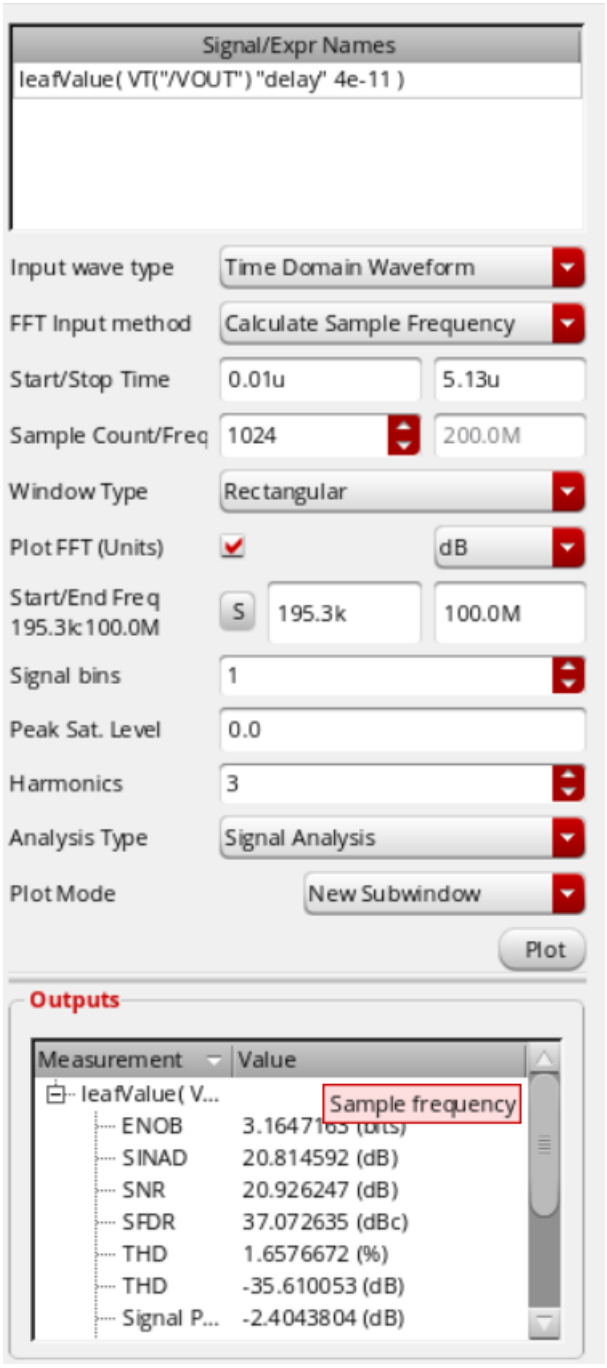

Figure 38: FFT of output waveform for SAR ADC