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Lab 1 Remarks:

Each of the parts of this lab use an insignificant amount of resources on the FPGA, with the exception of IO pins (due to IO requiring physical space on the board). The first part used only pins, since it was simple mapping of the switches to LEDs with no combinatorial logic involved. The second part used a single logic element to implement a NAND gate, a NOR gate, and an AND gate. The third part used 7 logic elements because it needed a multiplexer for each hex output bit.

Since modern FPGAs have such a large amount of logic elements, larger (and even multiple) designs can be loaded onto the chip for testing. Since modern ASICs are growing larger and larger due to the shrinking size of transistors, having larger FPGAs allows designs to be prototyped and tested with hardware rather than pure simulation.

lab1.vhd

Total logic elements	0 / 114,480 (0 %)
Total combinational functions	0 / 114,480 (0 %)
Dedicated logic registers	0 / 114,480 (0 %)
Total registers	0
Total pins	36 / 529 (7 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

part1.vhd

Total logic elements	1 / 114,480 (< 1 %)
Total combinational functions	1 / 114,480 (< 1 %)
Dedicated logic registers	0 / 114,480 (0 %)
Total registers	0
Total pins	36 / 529 (7 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

part2.vhd

Total logic elements	7 / 114,480 (< 1 %)
Total combinational functions	7 / 114,480 (< 1 %)
Dedicated logic registers	0 / 114,480 (0 %)
Total registers	0
Total pins	60 / 529 (11 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)