Combinational Logic

Part II: Arithmetic Circuits

- Binary Adder and Subtractor
- Decimal Adder
- Binary Multiplier
- Magnitude Comparator

Adders

- A combinational circuit that performs the addition of two bits is called a **half-adder**. One that performs the addition of three bits (two significant bits and a previous carry) is a **full-adder**. The name of the former stems from the fact that two half-adders can be employed to implement a full-adder.

Half-Adder

- The input variables designate the **augend** (first bit) and **addend** (second bit); the output variables produce the **sum** and **carry**. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols x and y to the two inputs and S (for sum) and C (for carry) to the outputs.

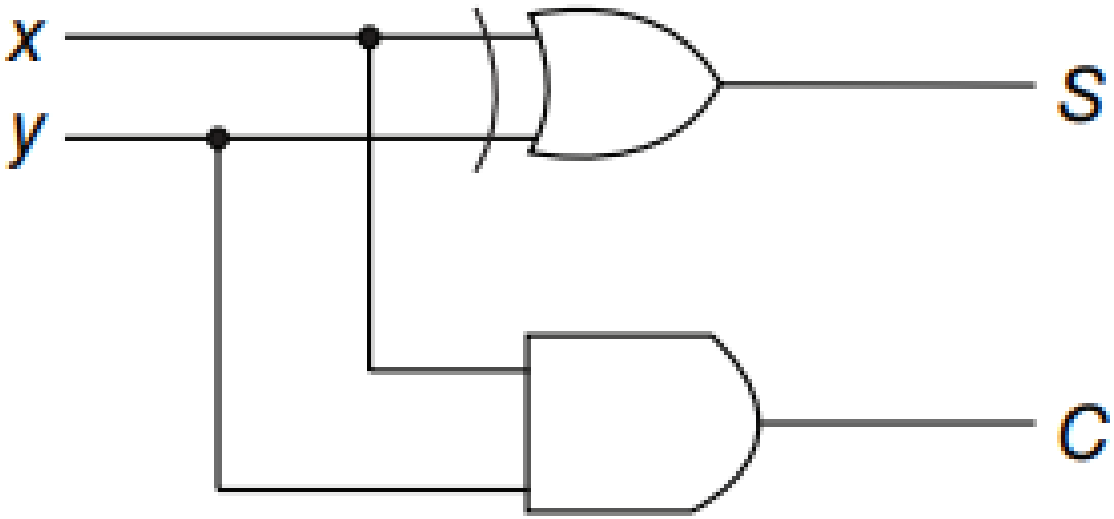
Truth table for Half-Adder:

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = x'y + xy'$$

$$C = xy$$

Logic Diagram:



$S = X \oplus Y$

$C = XY$

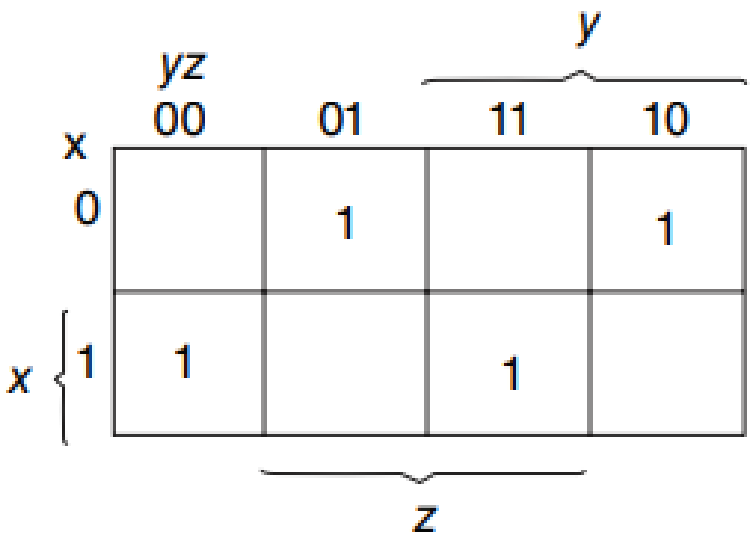
Full Adder

- Design a combinational circuit that adds 3 input bits (x,y,z) to generate a Sum (S) bit and a carry-out (C) bit.

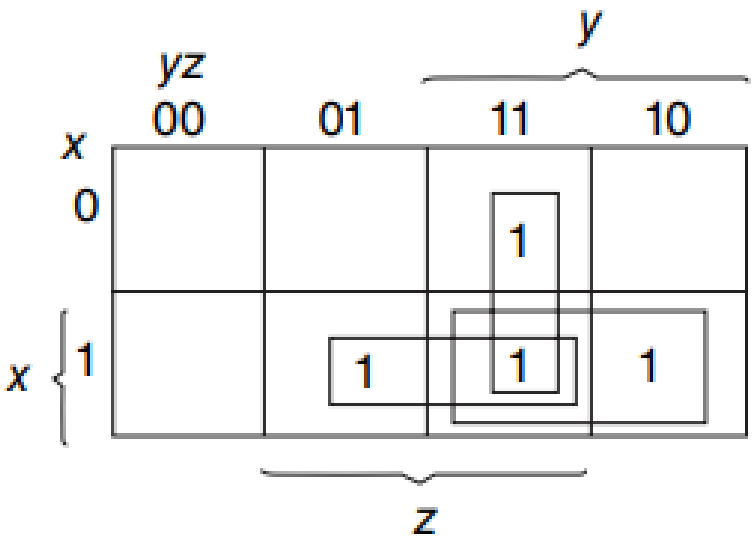
Truth Table

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Simplification using K-map:



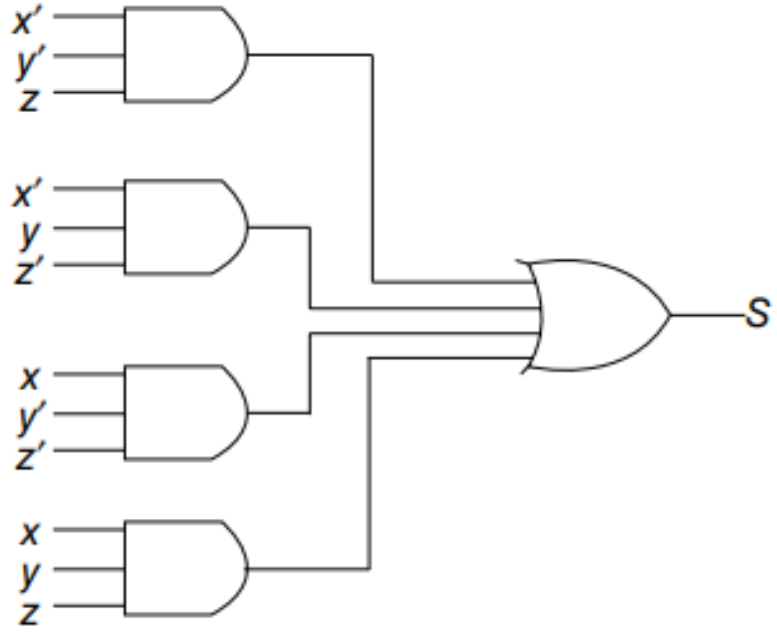
$$S = x'y'z + x'yz' + xy'z' + xyz$$



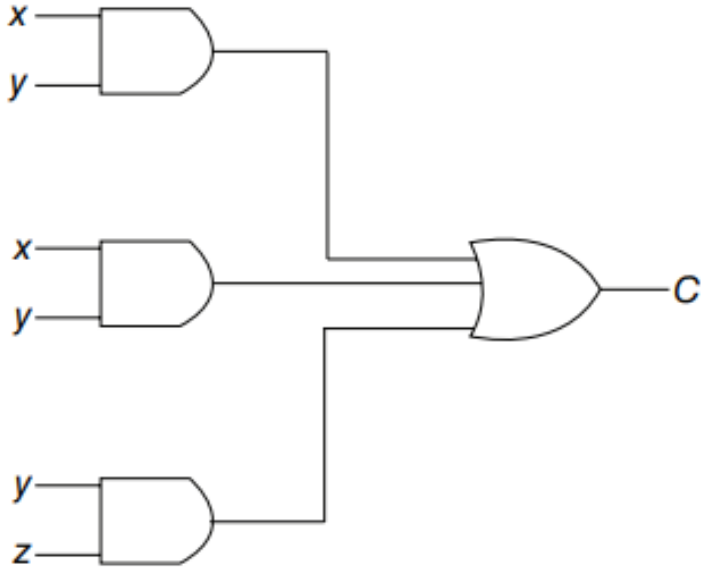
$$C = xy + xz + yz$$

Logic diagram (SOP)

$$S = x'y'z + x'yz' + xy'z' + xyz$$



$$C = xy + xz + yz$$



Full Adder using two half-adders and an OR gate

$S = x'y'z + x'yz' + xy'z' + xyz$

$= z'(x'y+xy') + z(xy+x'y') \rightarrow$ XNOR

$= z'(x'y+xy') + z(x'y+xy')' \rightarrow$ complement of XNOR is XOR

$= z'(x \oplus y) + z(x \oplus y)'$ let $x \oplus y = w$

$= z'w + zw'$

$= z \oplus w$

Therefore:

$S = z \oplus (x \oplus y)$

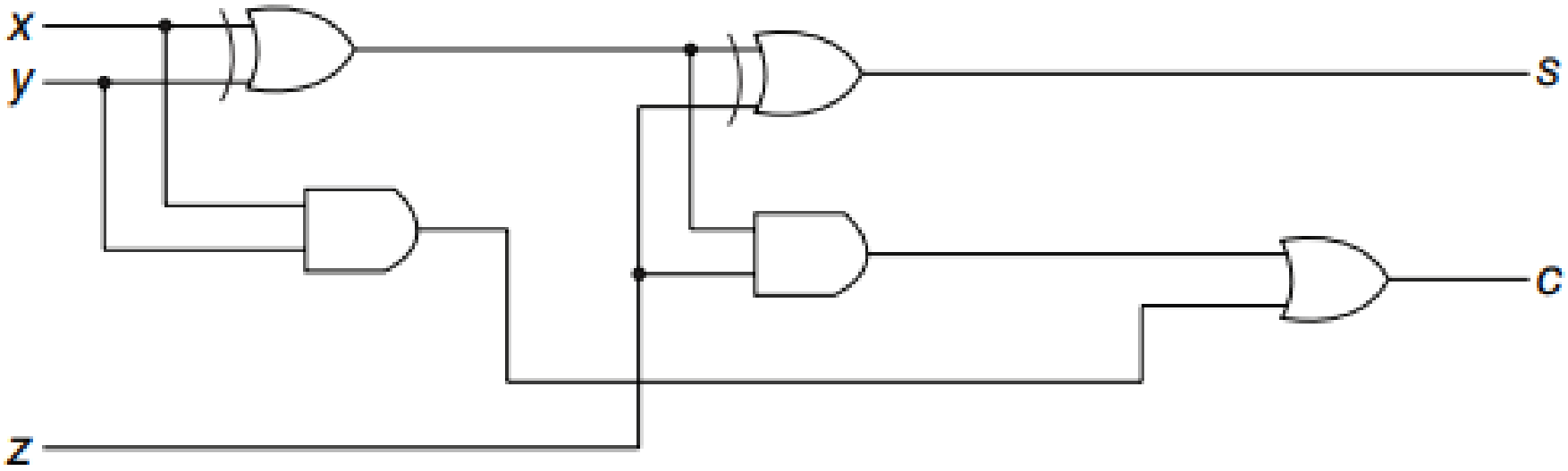
$C = xy'z + x'yz + xy = z(xy'+x'y) + xy$

$C = z(x \oplus y) + xy$

Implementation of full-adder with two half-adders and an OR gate

$S = z \oplus (x \oplus y)$

$C = z(x \oplus y) + xy$



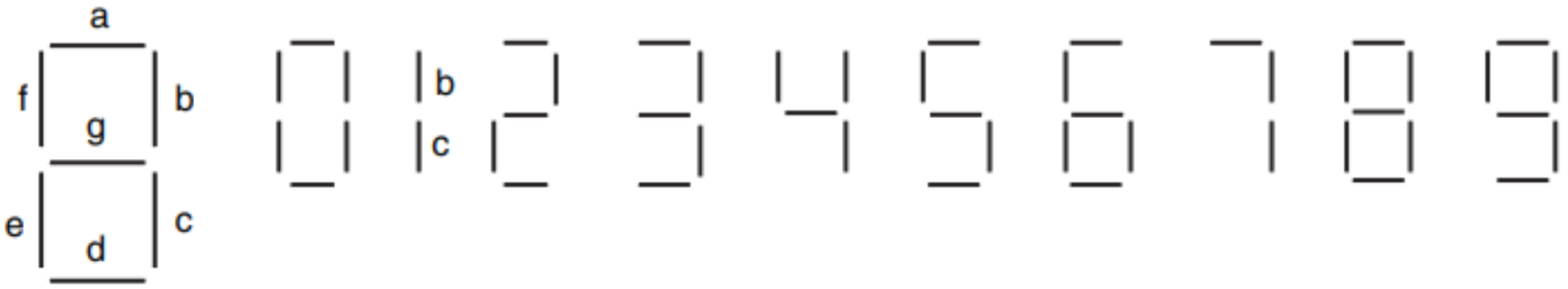
Seatwork#2:

1. Show that $A \oplus B \oplus C \oplus D = \Sigma(0, 3, 5, 6, 9, 10, 12, 15)$
2. Design a combinational circuit to check for even parity of four bits. A logic-1 output is required when the four bits do not constitute an even parity.

Assignment #2:

- A BCD-to-seven-segment decoder is a combinational circuit that accepts a decimal digit in BCD and generates the appropriate outputs for selection of segments in a display indicator used for displaying the decimal digit. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display as shown in (a). The numeric designation chosen to represent the decimal digit is shown in (b) in the next slide.

Assignment #2:



(a) Segment designation

(b) Numerical designation for display