Combinational Logic

Part III: Decoders and Encoders

DECODERS

Decoders

- A binary decoder is a **digital logic device that translates a binary input code into a single output**, allowing it to be easily understood and utilized by other devices. It plays a crucial role in simplifying complex binary data, making it an essential component in modern digital systems.
- Converts an n-bit code to a single active output.
- Can be developed using AND/OR gates
- Can be used to implement logic circuits.
- Extensively used in digital systems.

Binary Decoders

- Figure 1(a) shows the block diagram with n input lines and 2^n possible output lines.
- Only one output is a 1 for any given input.

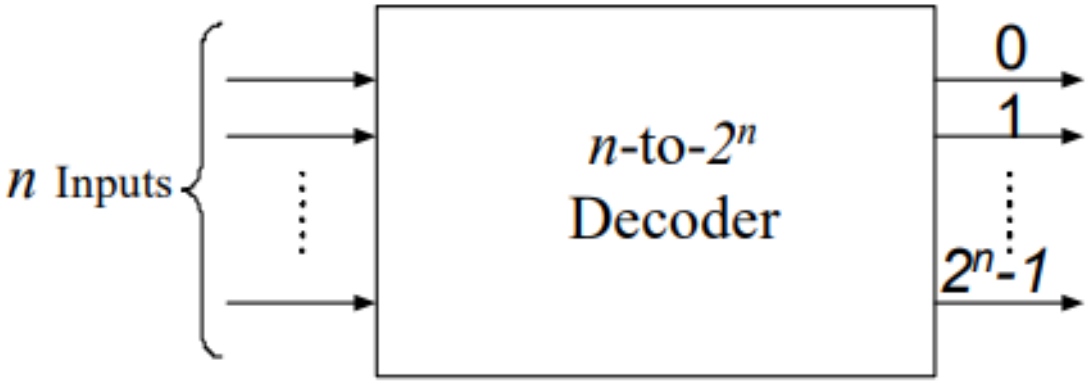


Figure 1(a): A typical decoder

- Thus, a decoder has n inputs and 2^n outputs. Each of the 2^n outputs corresponds to one of the possible 2^n input combinations.

Example: 2-to-4 decoders

- It contains two inputs denoted by A_1 and A_0 and four outputs denoted by D_0, D_1, D_2, and D_3. Also note that A_1 is the most significant bit (MSB) while A_0 is the least significant bit (LSB).

Decimal #	Input		Output			
	A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	1	0	0	0
1	0	1	0	1	0	0
2	1	0	0	0	1	0
3	1	1	0	0	0	1

Table 1: Truth table for 2-to-4 decoder

Example: 2-to-4 decoders

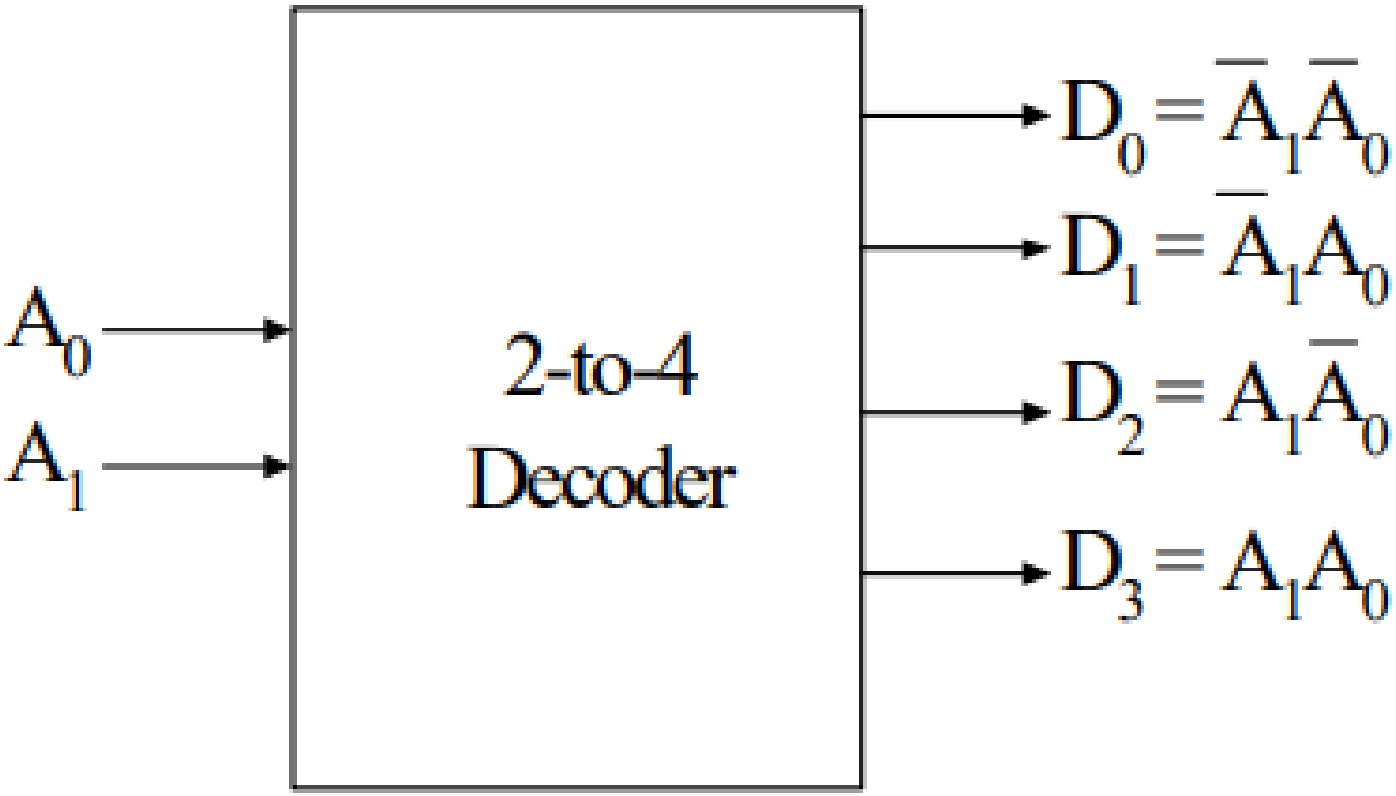


Figure 2: A 2-to-4 decoder without enable

Example: 2-to-4 decoders

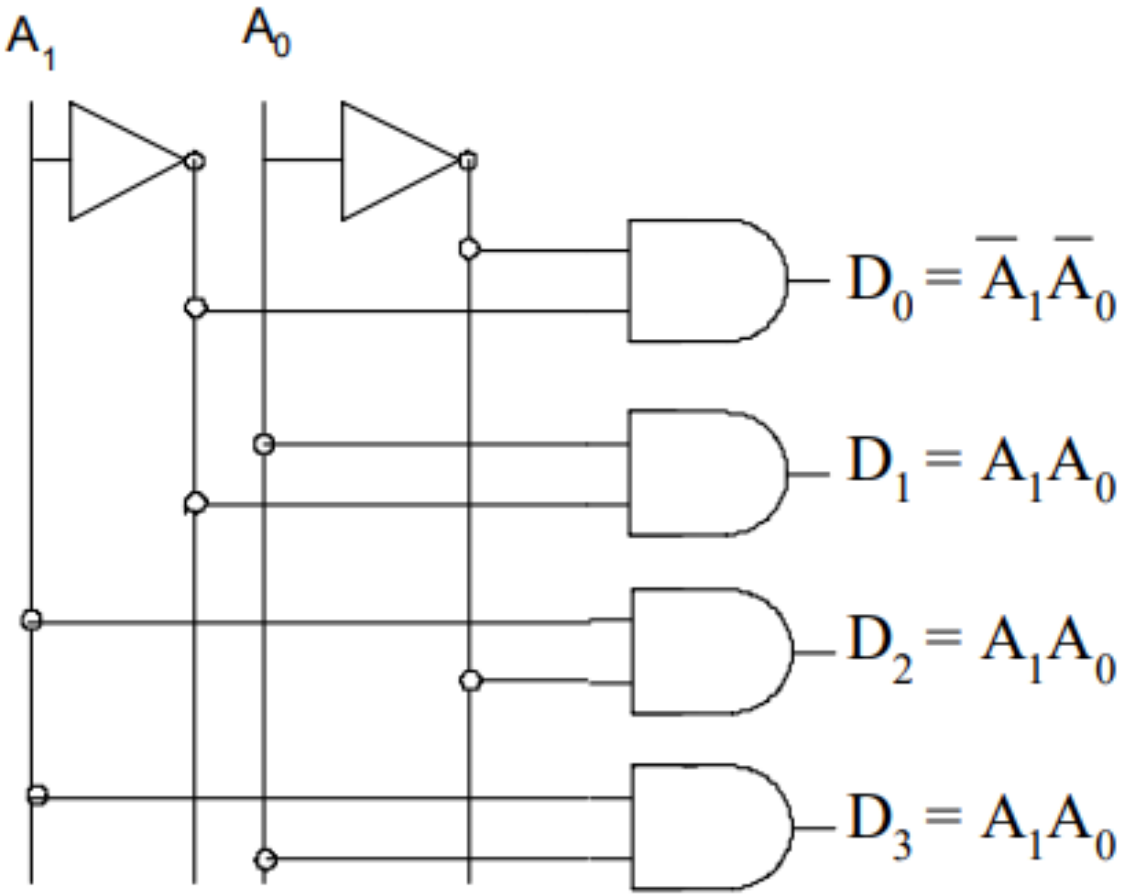


Figure 3: Implementation 2-to-4 decoder

Decoders with “enable” input

- Generally, decoders have the “enable” input. The enable input performs no logical operation, but is only responsible for making the decoder ACTIVE or INACTIVE.
- If the enable “E” o is zero, then all outputs are zero regardless of the input values.
- If the enable “E” is one, then the decoder performs its normal operation.

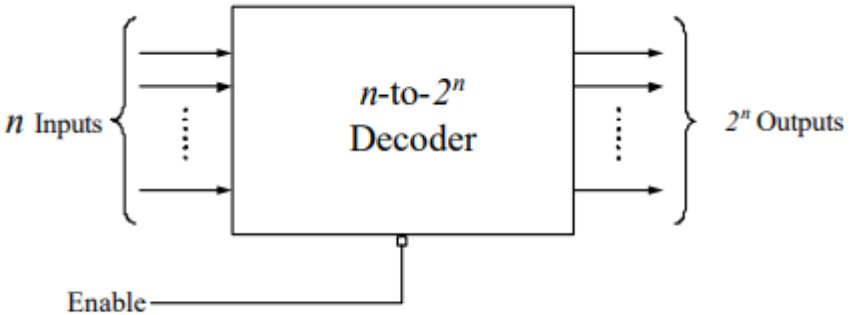


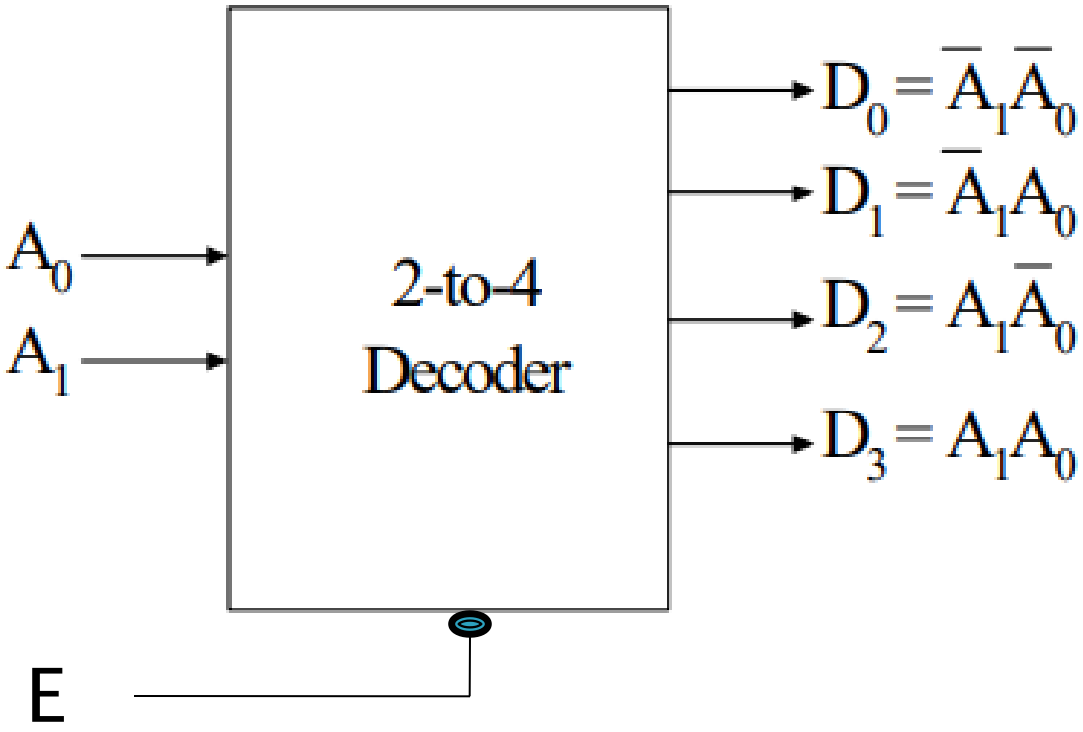
Figure 1(b): A typical decoder

2-to-4 Decoders with enable

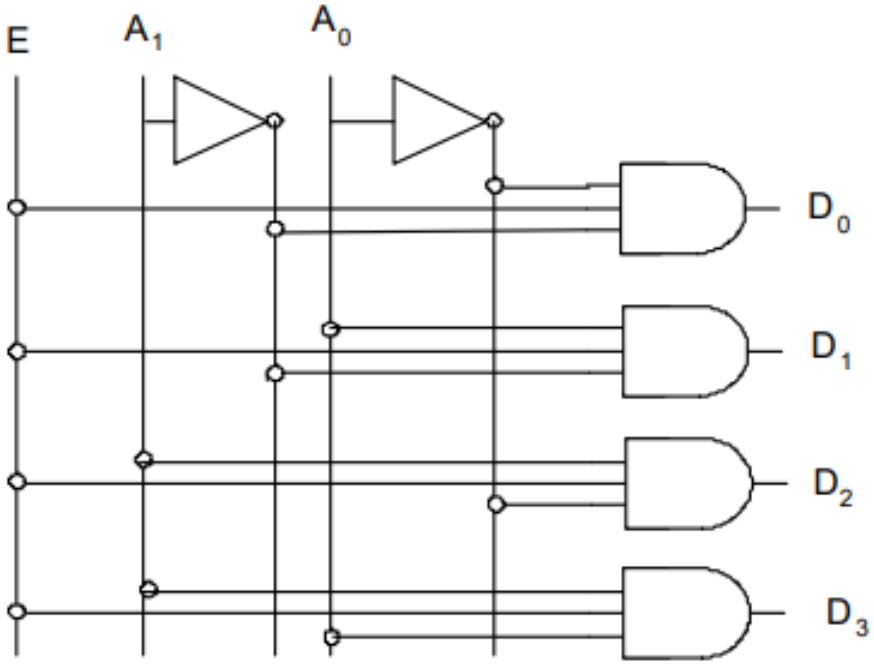
Decimal value	Enable	Inputs		Outputs			
	E	A_1	A_0	D_0	D_1	D_2	D_3
	0	X	X	0	0	0	0
0	1	0	0	1	0	0	0
1	1	0	1	0	1	0	0
2	1	1	0	0	0	1	0
3	1	1	1	0	0	0	1

Truth table of 2-to-4 decoder with enable

2-to-4 Decoders with enable



2-to-4 Decoders with enable



Implementation of 2-to-4 decoder with enable

Decoder Expansion

- It is possible to build larger decoders using two or more smaller ones.
- Example: Construct a 3-to-8 decoder using two 2-to-4 decoders with enable inputs.

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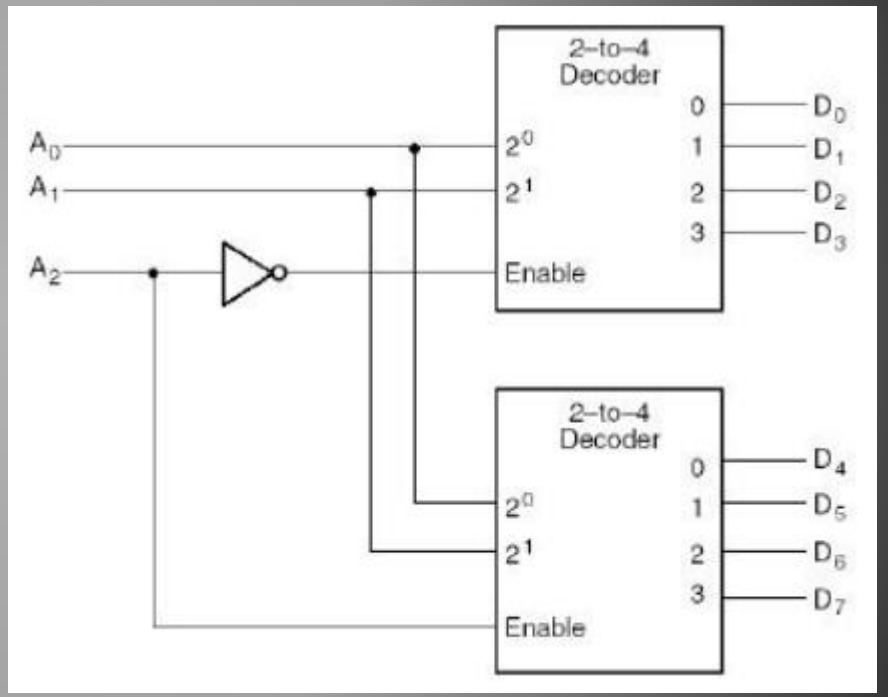

Assignment #4: (50 pts)

1. Make a 3-to-8 decoder with 3 inputs A_0, A_1, A_2 and 8 outputs (D_0 to D_7). Show the truth table. (15 pts)
2. Construct a 4x16 decoder using two 3x8 decoders. (20 pts)
3. Decoder implementation of a full adder. Refer to the truth table below. (15 pts)

Decimal value	Input			Output	
	X	Y	Z	S	C
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1