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Assignment

Chapter # 3

Problems

3.3

(a)

- Remaining bits usable = 24 bits
- No. of distinct addresses = 2^{24}
- Since each address refers to byte
  Capacity 2^{24} = 16,777,216 (16MB)

(b)

(i)

- Address bus width (32 bits) → can address upto 2^{32} locations.

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Address space large enough, but 16-bit data bus forces multi-cycle transfers for 32-bit words → halved bandwidth and increased instruction fetch time.

(b)

Smaller address bus severely limits addressable memory. Data bus halves throughput compared to 32-bit data bus.

(c)

IR → must hold entire instruction = 32 bits.

PC → we can directly access 24-bit addresses for this processor. so 24-bits required.

PC = 24, IR = 32 bits.

3.4

(a)

No. of addresses = 2^{16} words

Each word = 16 bits = 2 bytes

Total bytes = $2^{16} \times 2 = 2^{17}$ bytes

= 131,072 = 128 KB.

(b)

- Address lines = 16 → 2^{16} addresses
- if memory is 8-bit (byte) wide each address access 1 byte.
- Total bytes = 2^{16} bytes = 64 kB.

(c)

- Isolated I/O (Port-mapped I/O)
- Memory-mapped I/O
- Dedicated control signal / buses.

Use either port-mapped I/O or memory-mapped I/O; port-mapped I/O requires dedicated I/O instructions and decoding.

(d)

If 8-bit port numbers and 16-bit ports occupy two consecutive 8-bit port addresses, then 128 distinct 16-bit I/O ports.

3.5

(a)

- External data bus width = 16 bits = 2 bytes per bus transfer.
- Input clock = 8 MHz → clock

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period $T_{clk} = 1/8 \times 10^6 = 125ns$

- Bus cycle duration = 4 clock cycles
  $= 4 \times 125ns = 500ns.$
- Per bus cycle bytes transferred (assuming one data transfer per bus cycle) = 2 bytes.

$$\text{Rate} = \frac{2 \text{ bytes}}{500 \times 10^{-9}} = \frac{2}{5 \times 10^{-7}}$$

$$= 4 \times 10^6 \text{ bytes} = 4MBs.$$

(b)

Both give same theoretical bandwidth ie.

i) Double clock frequency to 16MHz
ii) Double data bus width ie. 32 bits. (8MB/s) under the assumption bus cycle remains 4 clocks; practical choice depends on cost/power/timing tradeoffs.

3.6

(a)

Input sequence (polling):

i) CPU polls FGI. if FGI == 0, no data available -, keep polling or do other work.

ii) When FGI == 1, CPU reads INPR (read 8-bit character).

iii) Reading INPR typically causes devices I/O module to clear FGI.

iv) CPU process the character.

Output sequence (polling):

i) CPU polls FGO. if FGO == 0, transmitter busy, keep polling.

ii) When FGO == 1, CPU writes character into OUTR.

iii) Writing OUTR starts transmission, FGO is cleared until transmitter is ready again.

iv) When transmitter finishes sending device sets FGO = 1 to indicate ready for next char.

This is simple but CPU wastes cycle polling.

(b)

Using IEN:

- CPU sets IEN = 1 to enable interrupts from I/O module.
- For input: when a character arrives, I/O module sets FGI = 1 and asserts a interrupt request if IEN = 1, CPU is interrupted runs ISR:
  - ISR reads INPR
  - ISR clear the flag or let device clear it.
  - ISR returns - CPU can resume otherwork without busy polling.
- For output when FGI = 1 and CPU has data to send it can write OUTR or CPU can be interrupted when FGO becomes 1 and service routine writes the next char.

3-7

(a)

- 16-bit bus: Transfer 2 bytes per bus cycle
- 8-bit bus: transfer 1 byte per bus cycle

Data transfer rate differs by a factor of 2 (16-bit bus twice as fast).

(b)

- 16-bit bus : 2 bytes/cycle. Avg. cycle per instruction = 3.0/2 = 1.5 cycles.
- 8-bit bus : 1 byte/cycle. Avg. cycle per instruction = 3.0/1 = 3.0 cycles.
- Ratio 3.0/1.5 = 2. Again factor of 2.

(3.10)

On the VAX SBI, the priority 16 device usually has the lowest average wait time because the bus uses a rotating priority scheme, giving all devices fair access. This would not hold if higher-priority devices continously requested the bus, causing heavy contention.
