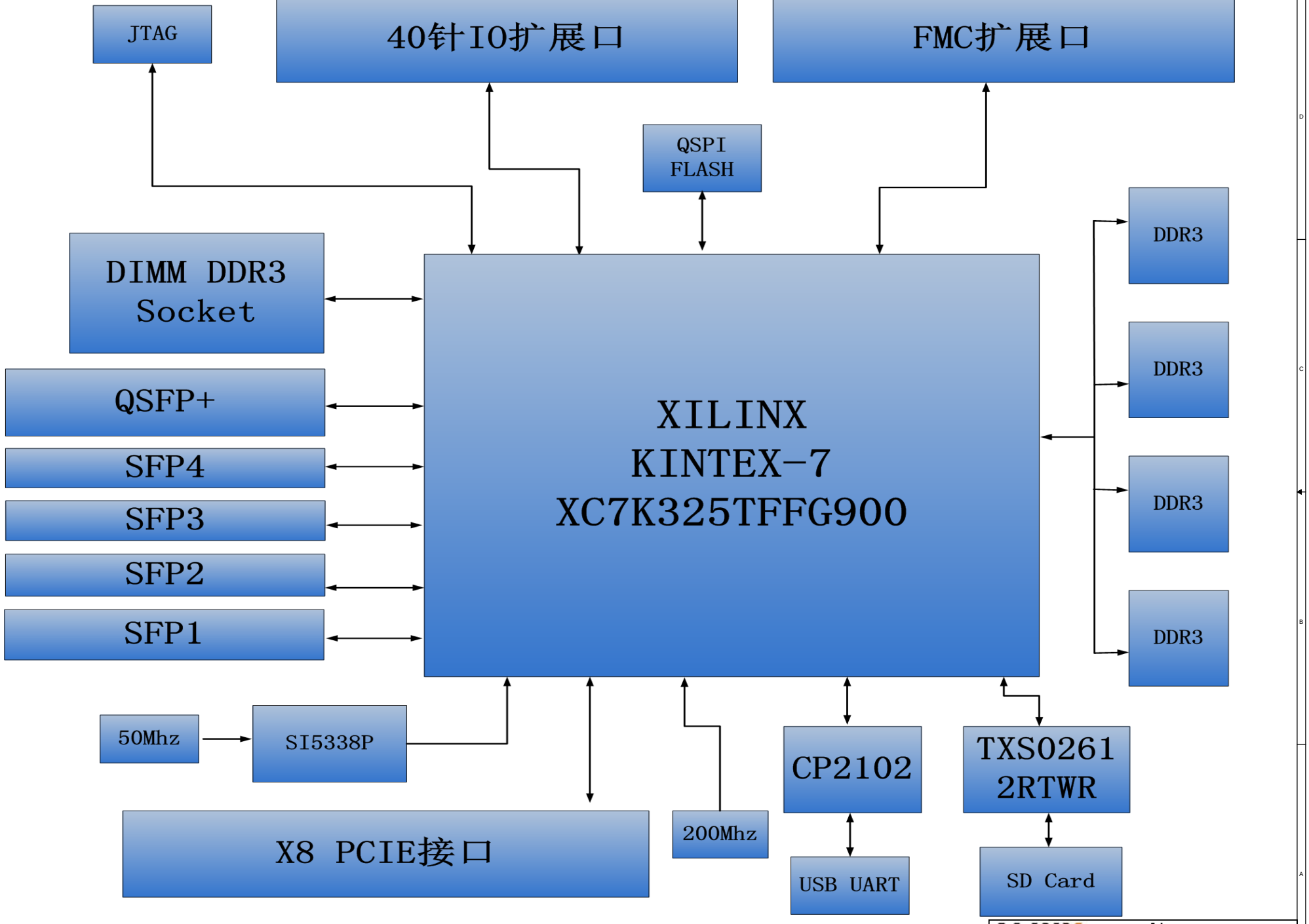

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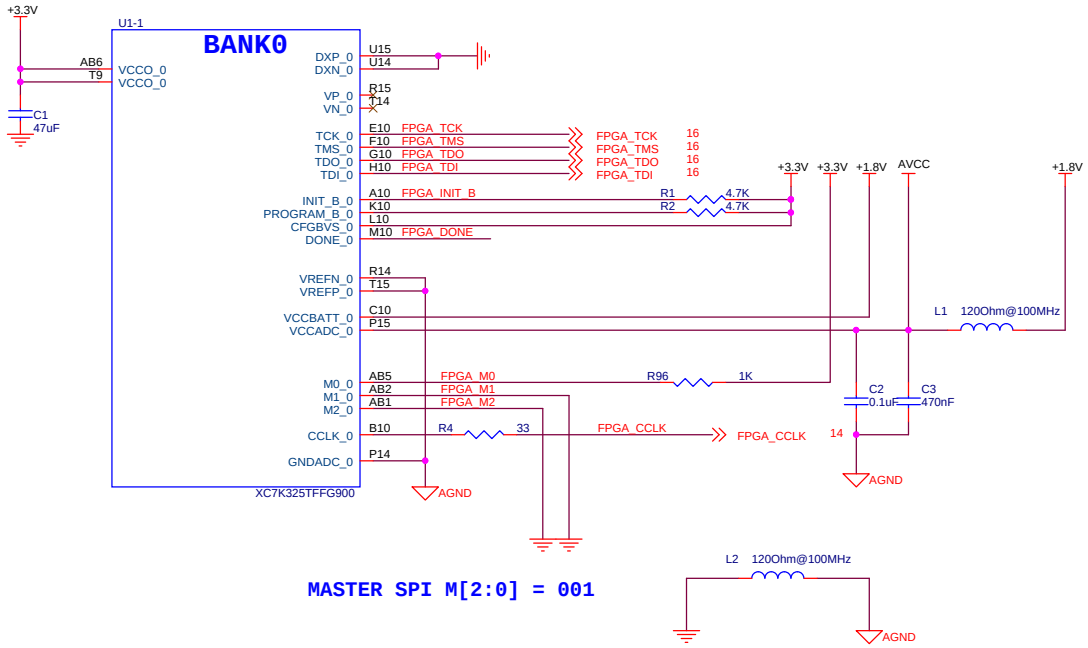
Title: PAGE01 BLOCK DIAGRAM

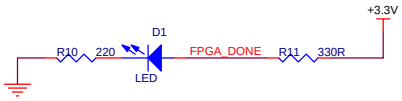
Size | Document Number: Kintex-7开发板 Schematics | Rev: 1.0

Date: Wednesday, August 29, 2018 | Sheet 1 of 20

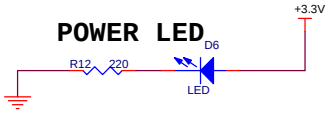


MASTER SPI M[2:0] = 001

FPGA DONE LED



POWER LED



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Title	PAGE02 FPGA BANK0
Size	
Document Number	Kintex-7开发板 Schematics
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Date:	Wednesday, August 29, 2018
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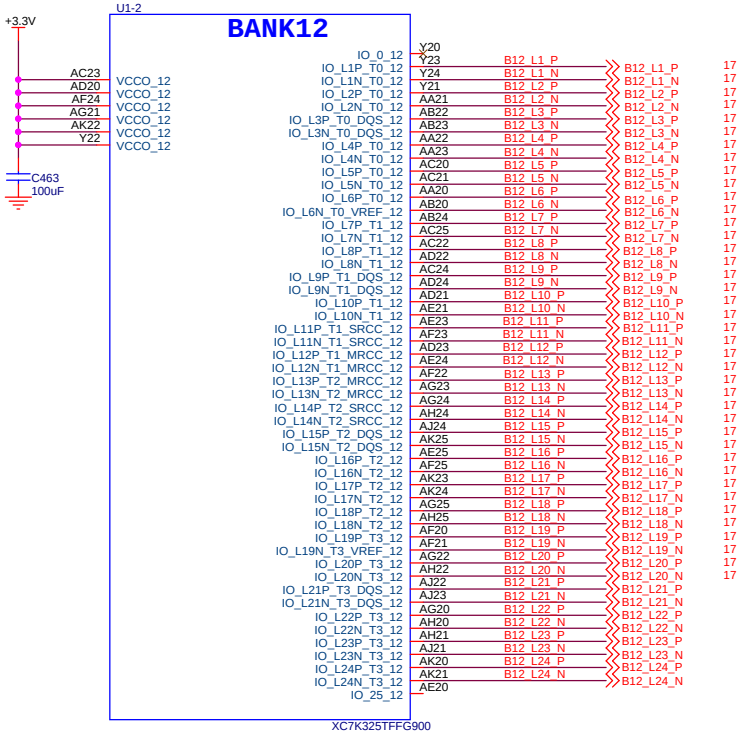

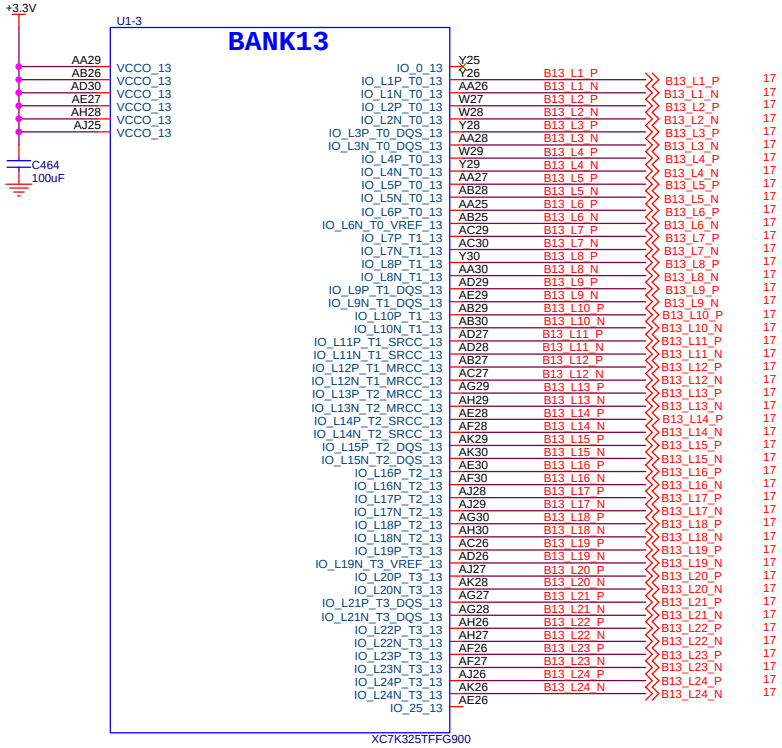

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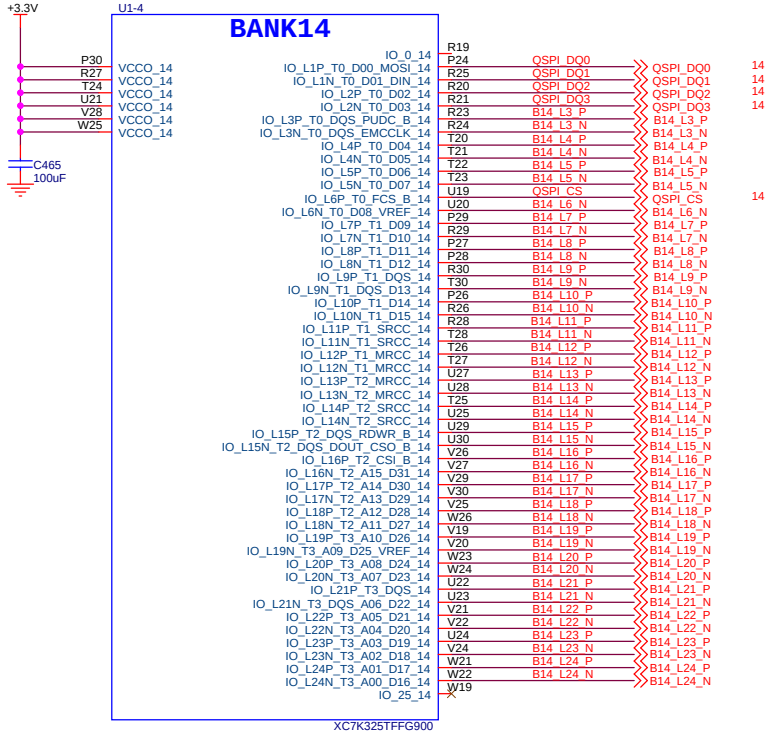
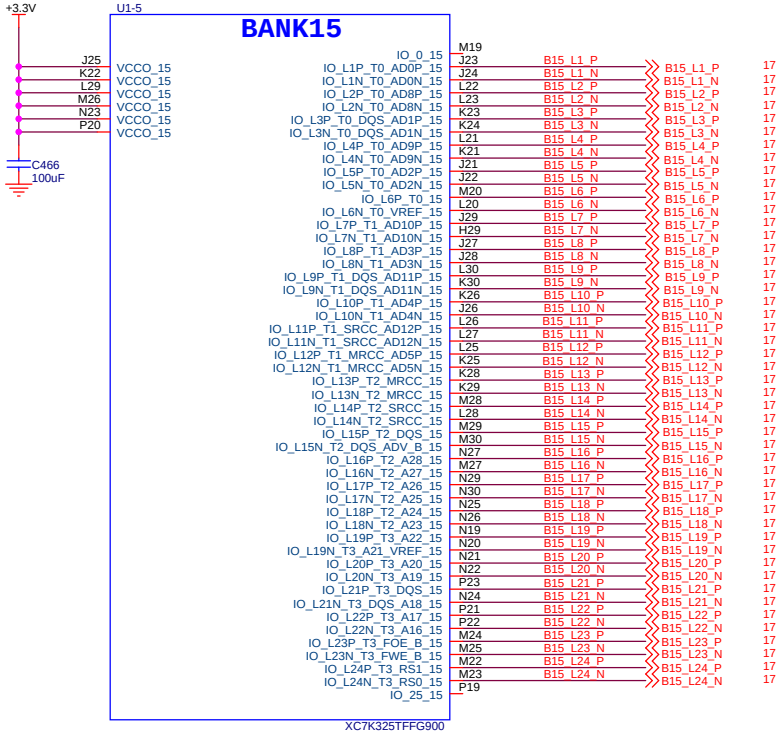
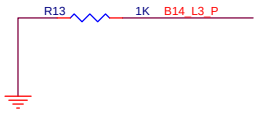
Title: PAGE03 FPGA BANK12/13		
Size	Document Number: Kintex-7开发板 Schematics	Rev: 1.0
Date: Wednesday, August 29, 2018	Sheet 3 of 20	





PUDC_B=1: Deactive internal Pull up Resister



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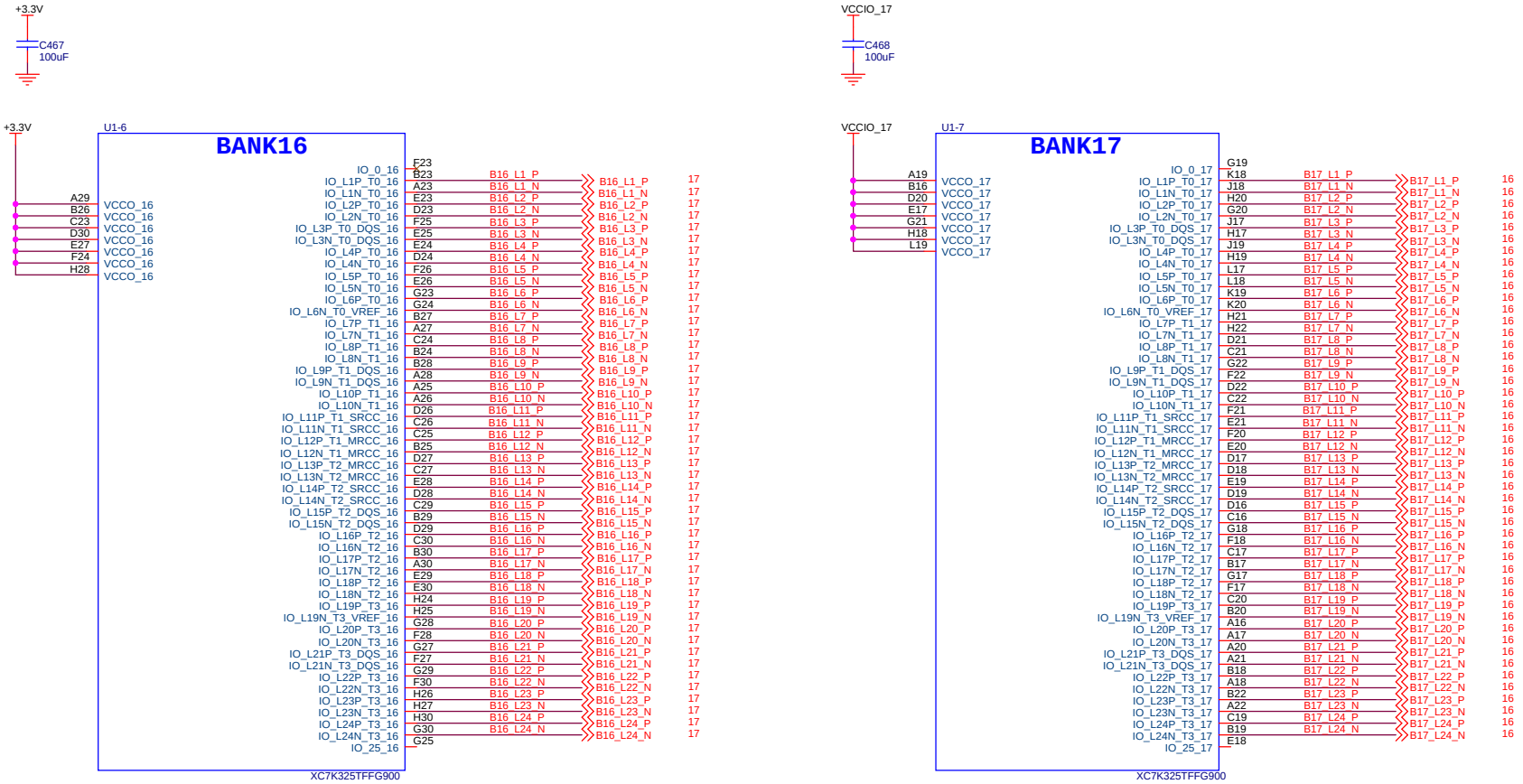
Title: PAGE04 FPGA BANK14/15

Size | Document Number: Kintex-7开发板 Schematics | Rev: 1.0

Date: Wednesday, August 29, 2018 | Sheet 4 of 20



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Title: PAGE05 FPGA BANK16/17

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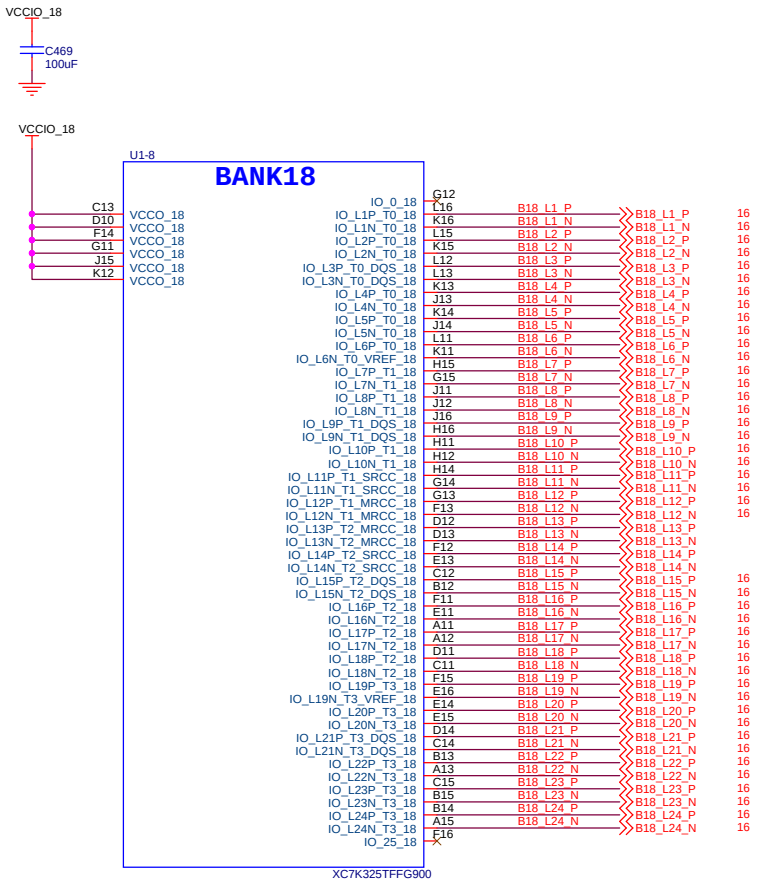
Date: Wednesday, August 29, 2018 | Sheet 5 of 20



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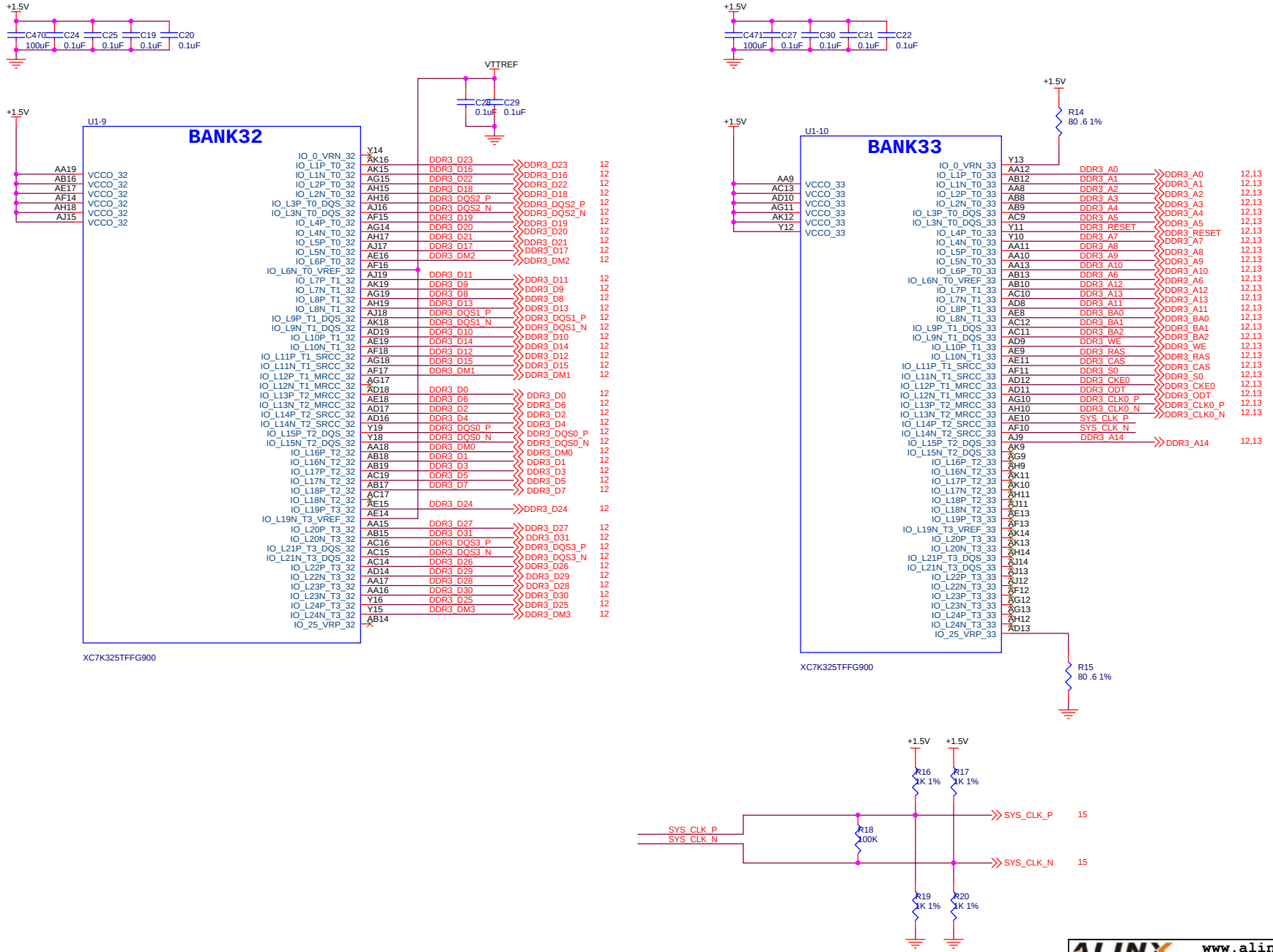
Title: PAGE06 FPGA BANK18

Size | Document Number: Kintex-7开发板 Schematics | Rev: 1.0

Date: Wednesday, August 29, 2018 | Sheet 6 of 20



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Title	PAGE07 FPGA BANK32/33	
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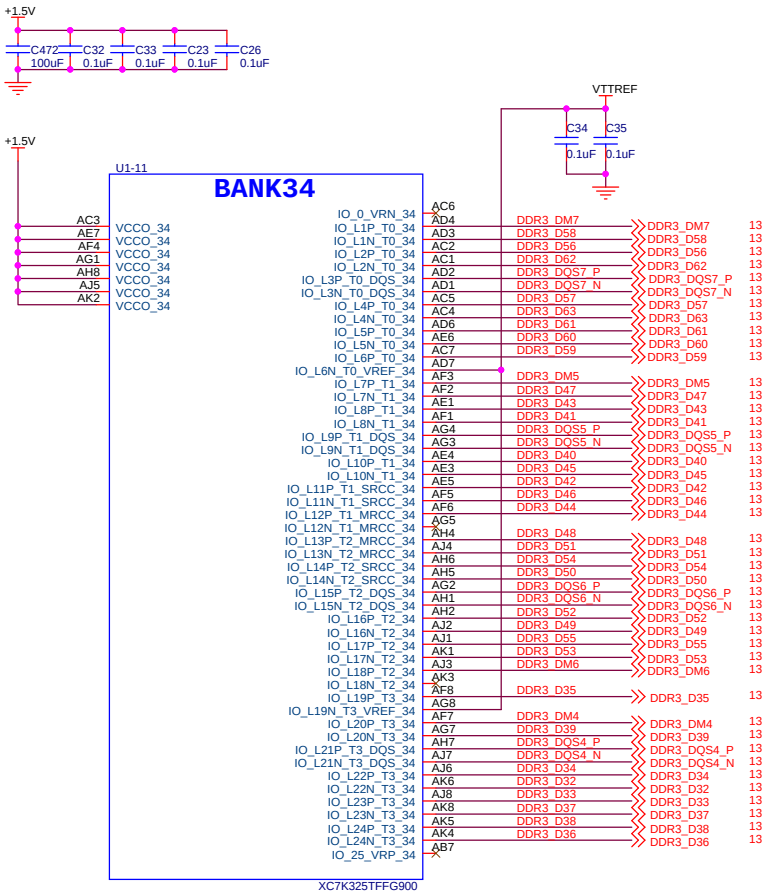
Date: Wednesday, August 29, 2018	Sheet 7 of 20	



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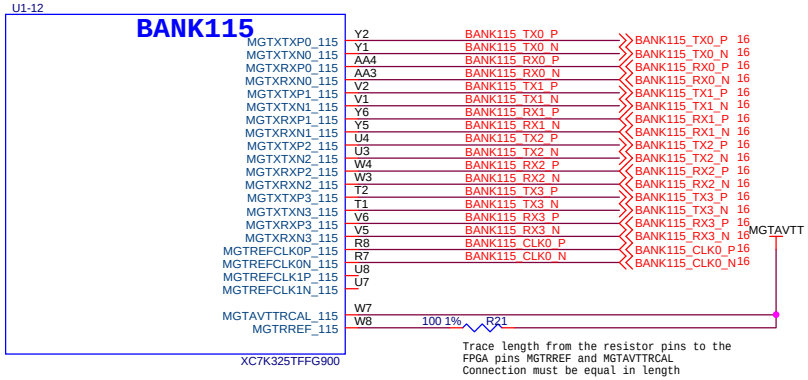
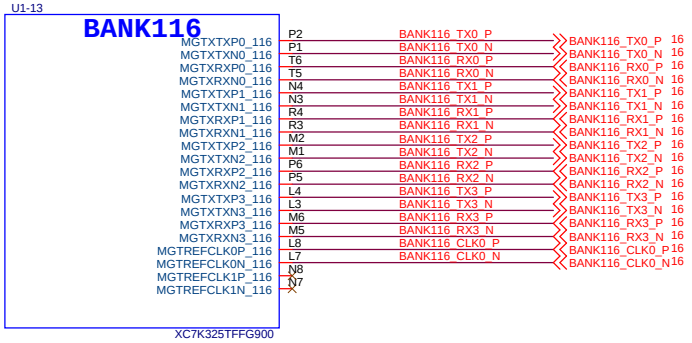
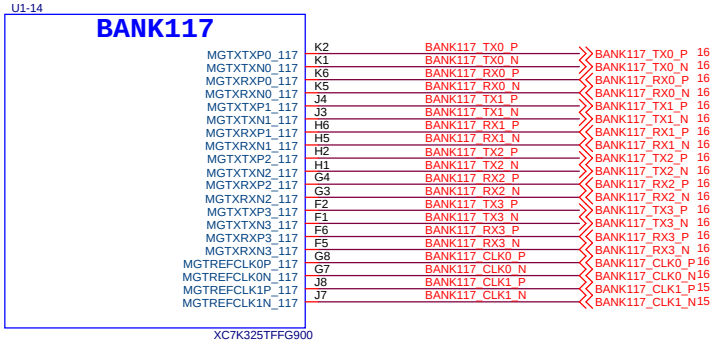
Title: PAGE08 FPGA BANK34

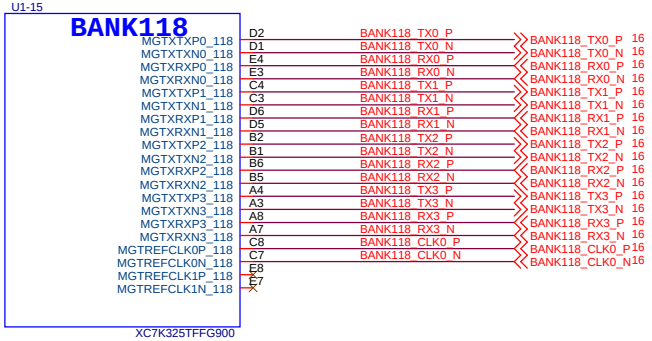
Size | Document Number: Kintex-7开发板 Schematics | Rev: 1.0

Date: Wednesday, August 29, 2018 | Sheet 8 of 20









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Title: PAGE09 FPGA BAN115/116/117/118

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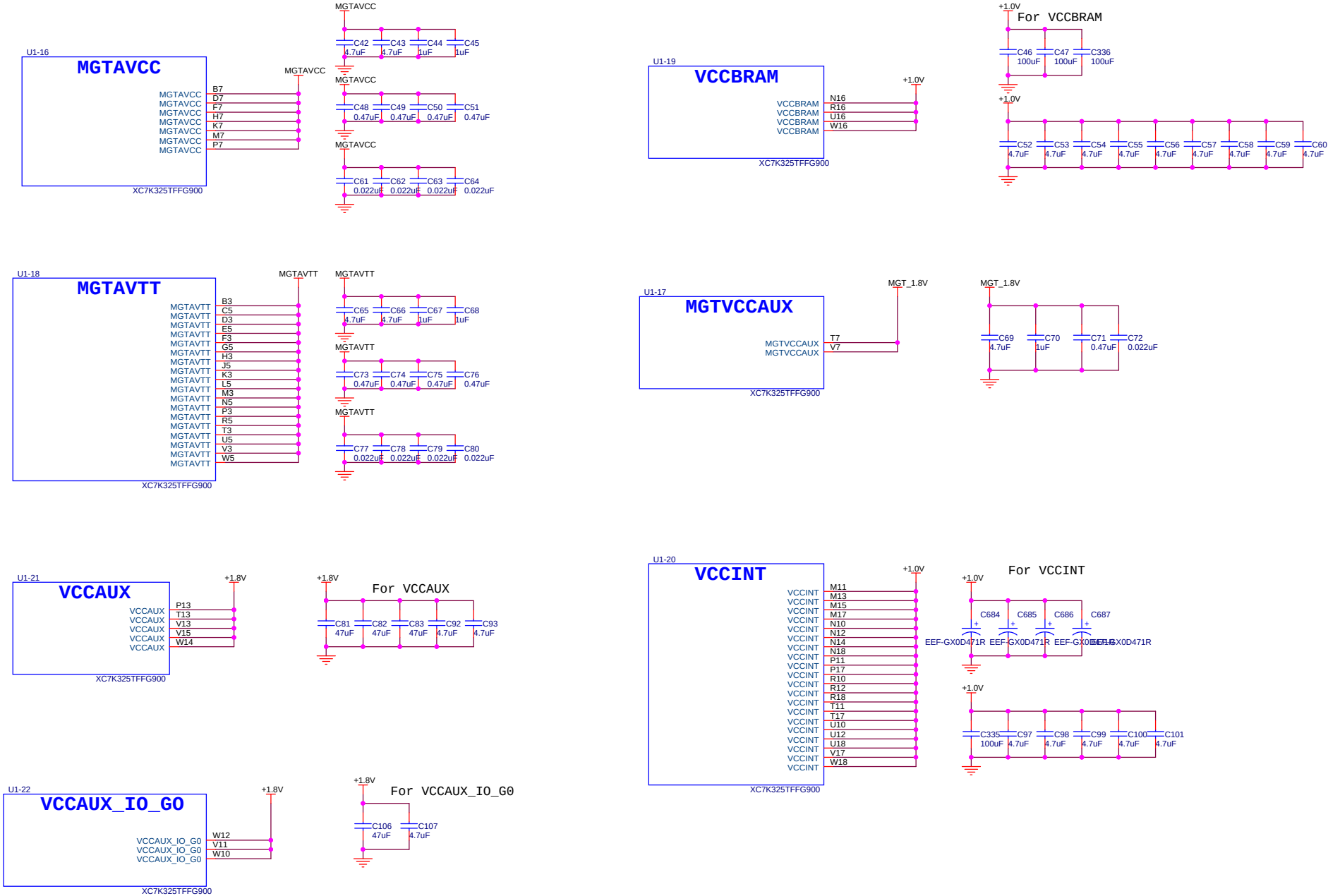
Date: Wednesday, August 29, 2018 | Sheet 9 of 20



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Title: PAGE10 FPGA Power		
Size	Document Number: Kintex-7开发板 Schematics	Rev: 1.0
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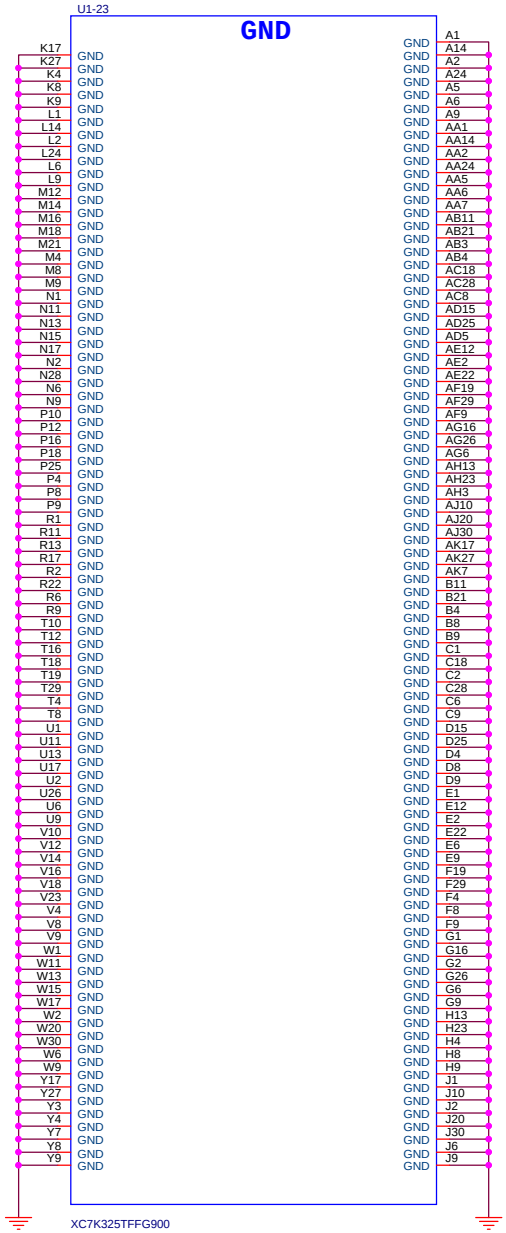

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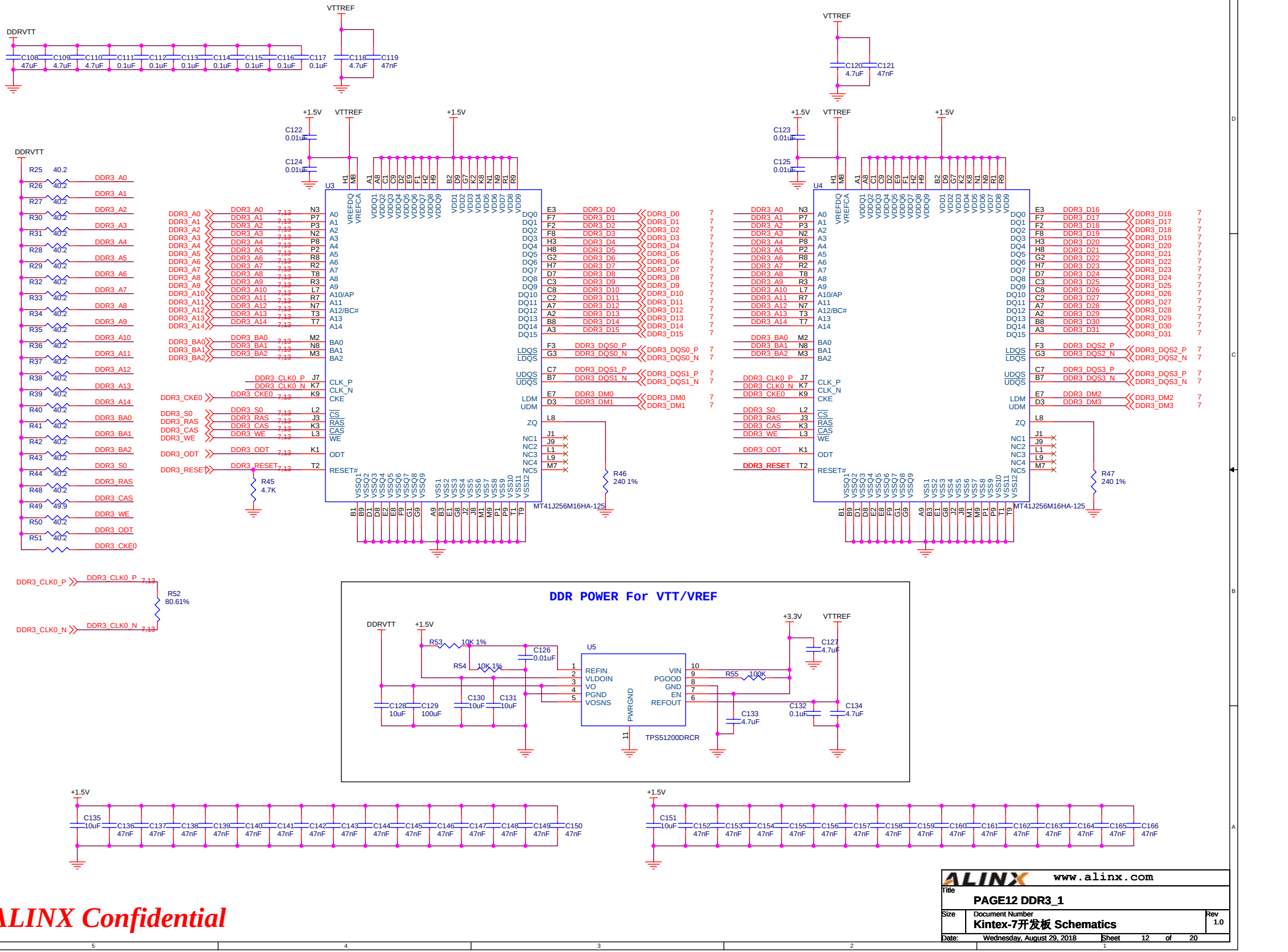
Title: PAGE11 FPGA GND

Size | Document Number: Kintex-7开发板 Schematics | Rev: 1.0

Date: Wednesday, August 29, 2018 | Sheet 11 of 20


DDRVTT
VTTREF
+1.5V
+3.3V
U3
U4
U5
MT41J256M16HA-125
TPS51200DRCR
DDR POWER For VTT/VREF
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PAGE12 DDR3_1
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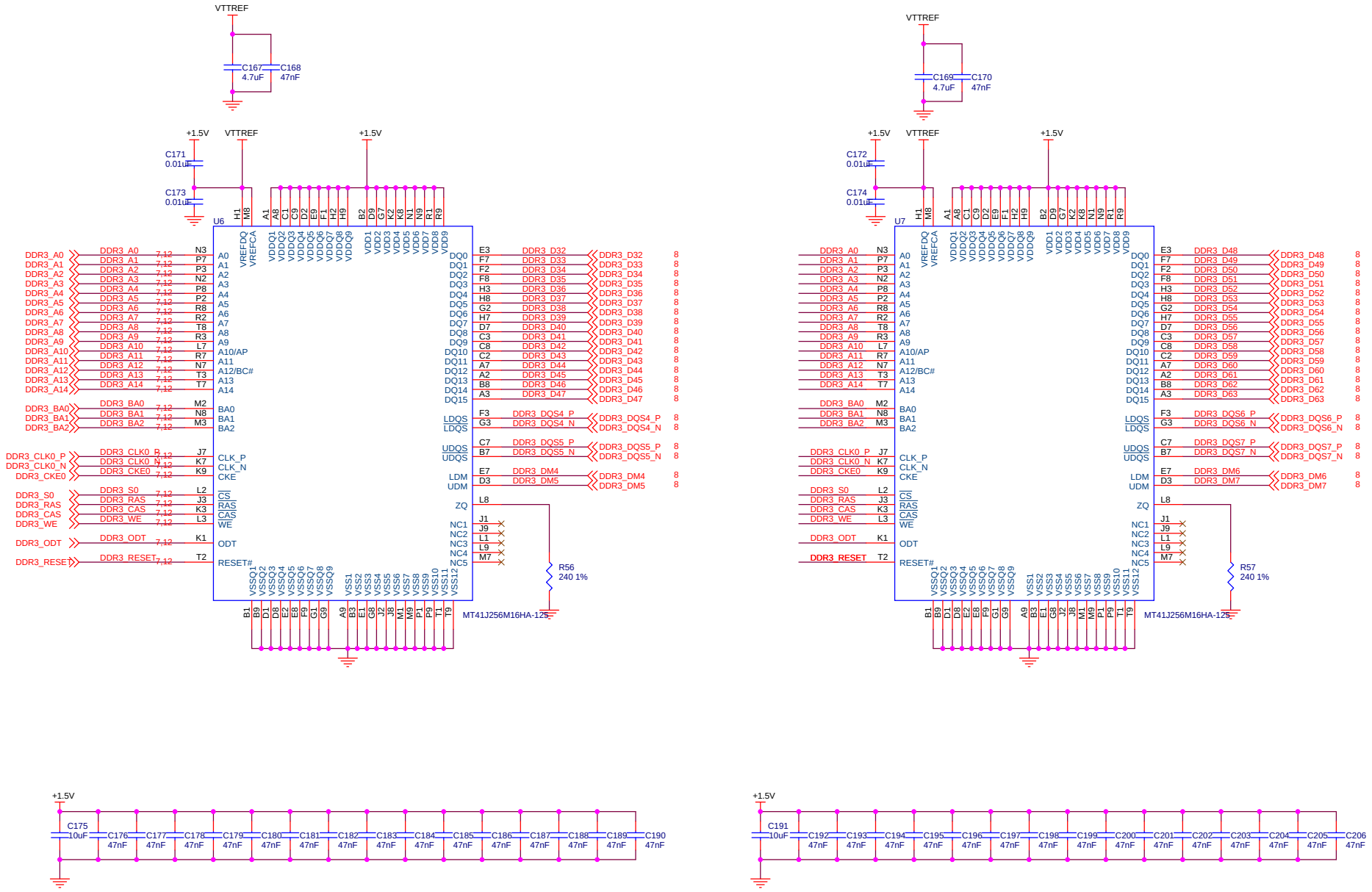

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Title	PAGE13 DDR3_2	
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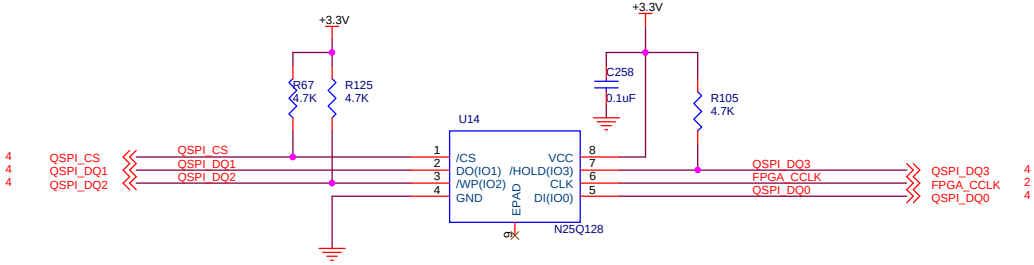
FPGA CONFIG SPI



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Title: PAGE14 FLASH		
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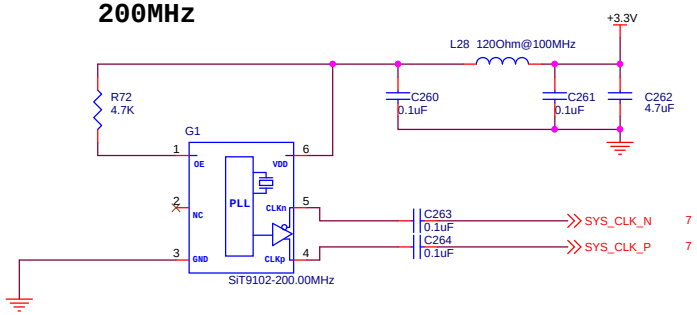
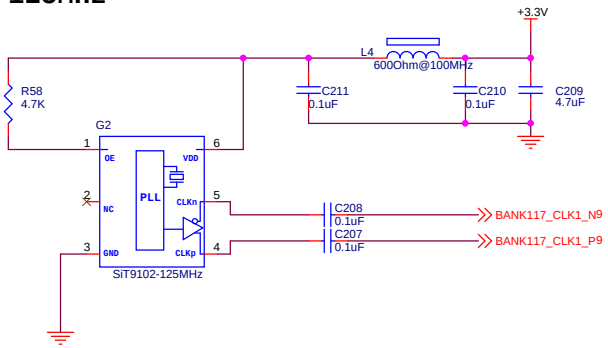
SYSTEM CLOCK

200MHz



GTX CLOCK

125MHz



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Title: PAGE15 CLOCK		
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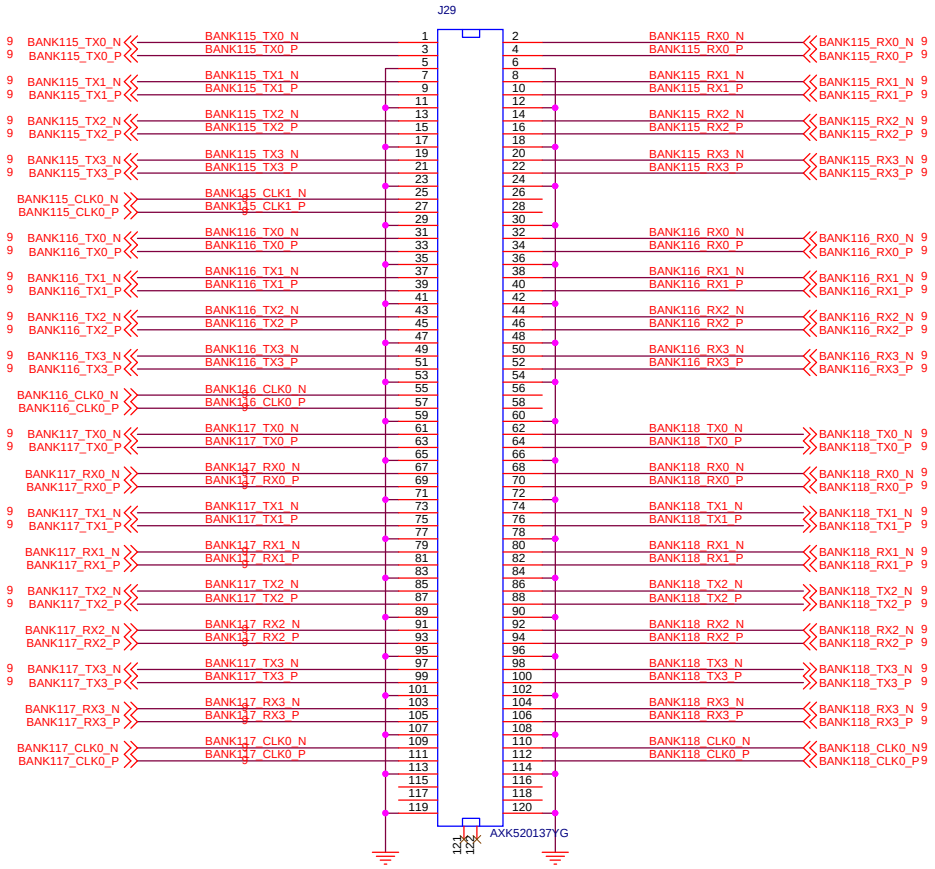

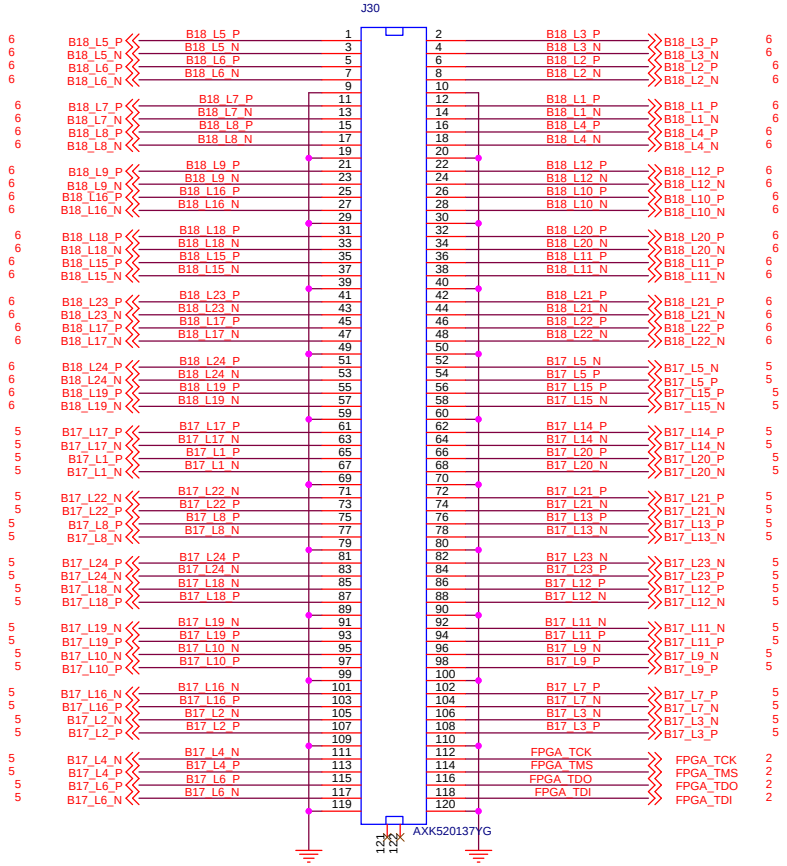

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Title: PAGE16 Connector_1

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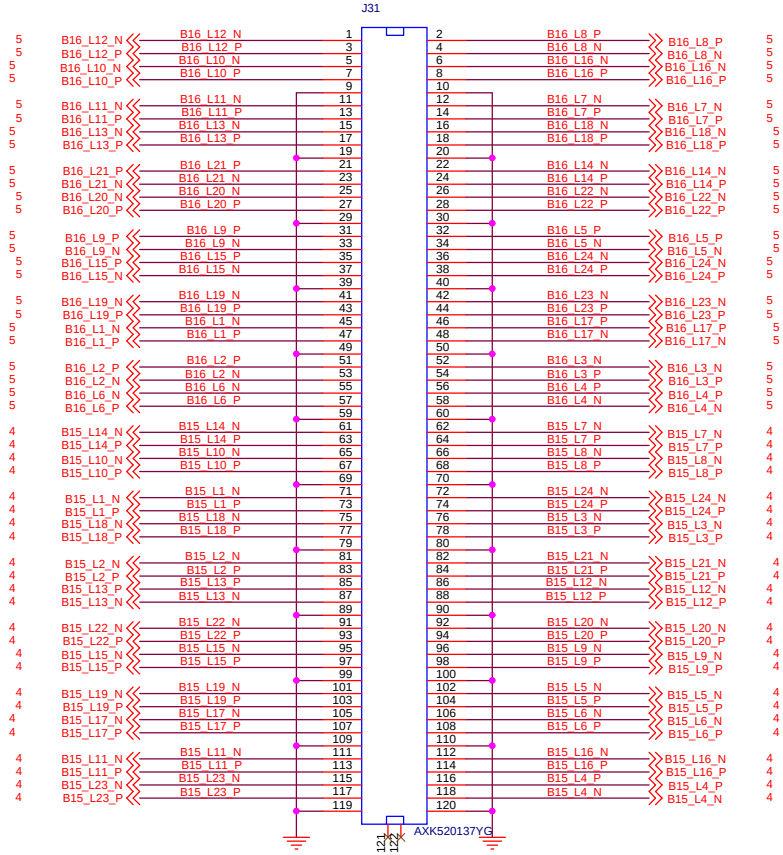

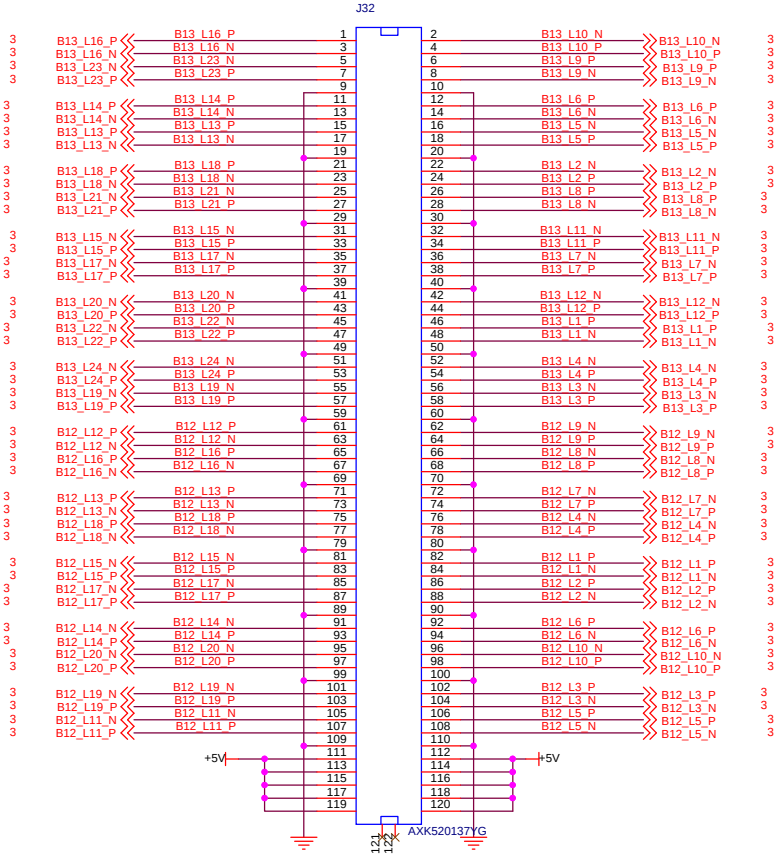

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Title: PAGE17 Connector_2		
Size	Document Number: Kintex-7开发板 Schematics	Rev: 1.0
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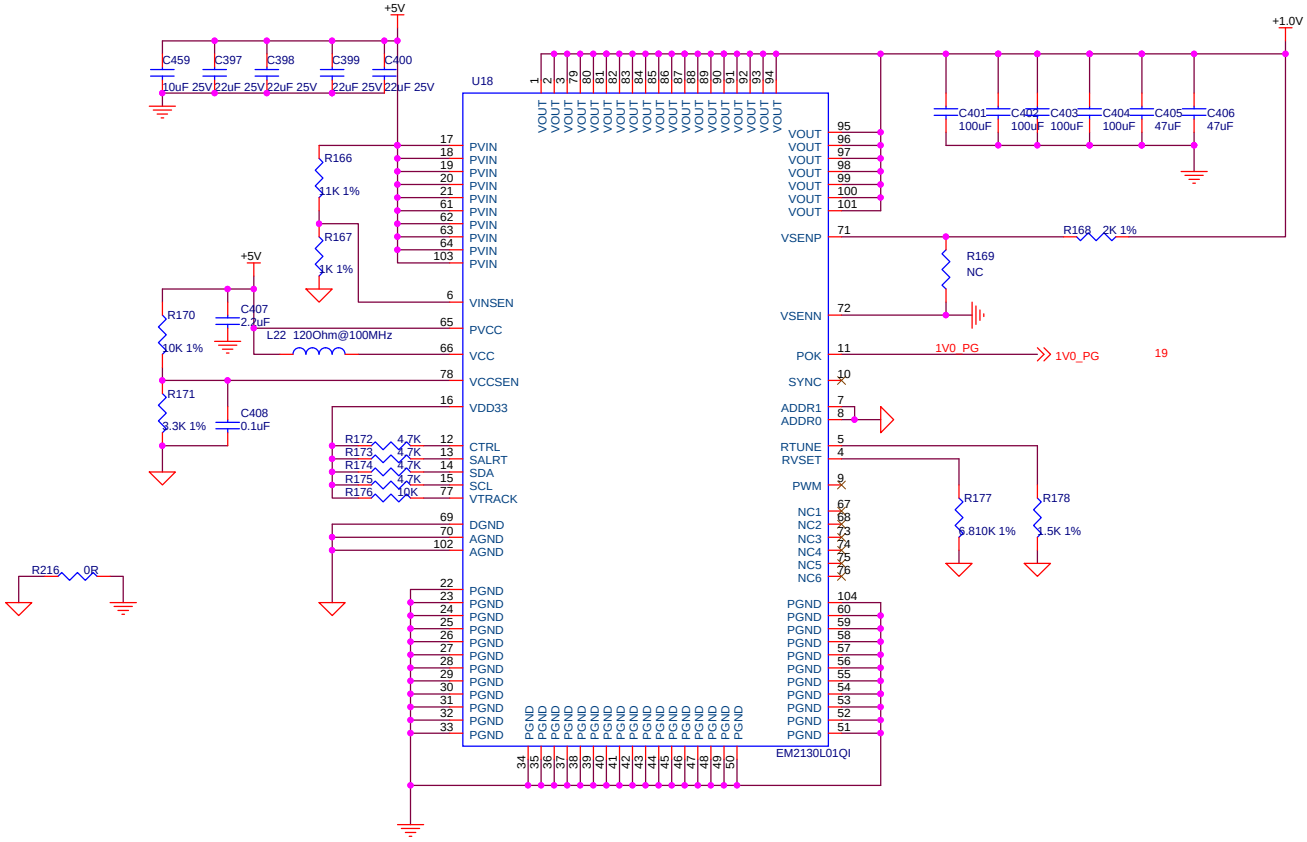

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Title	PAGE18 POWER +1.0V	
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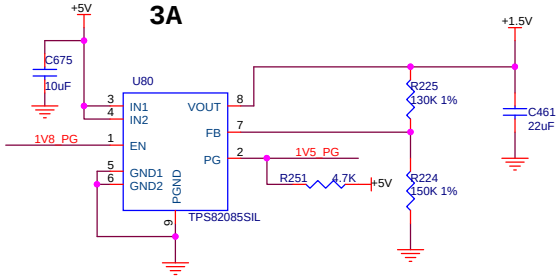

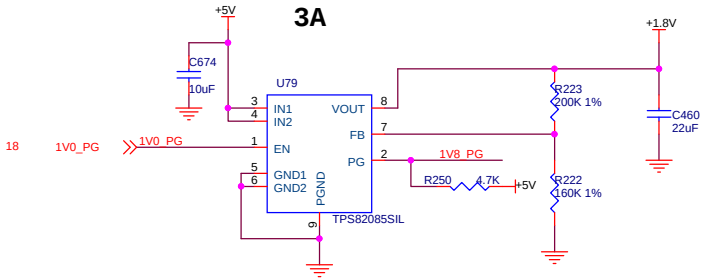

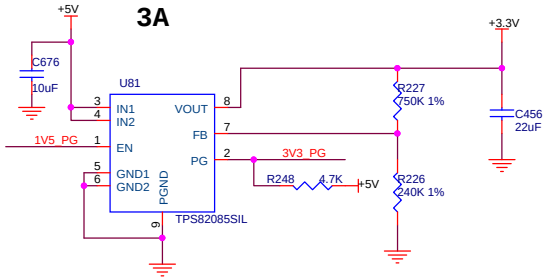

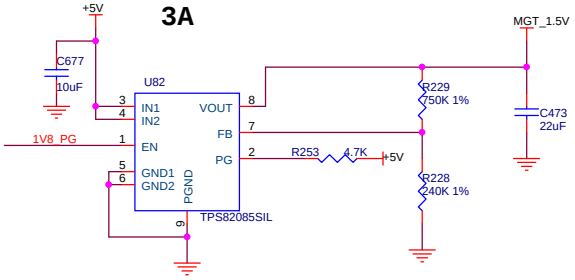

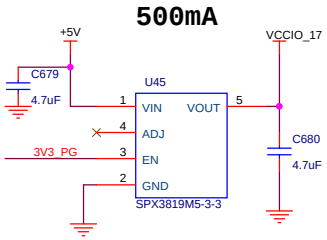

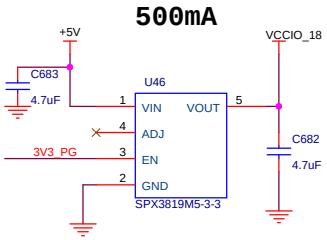

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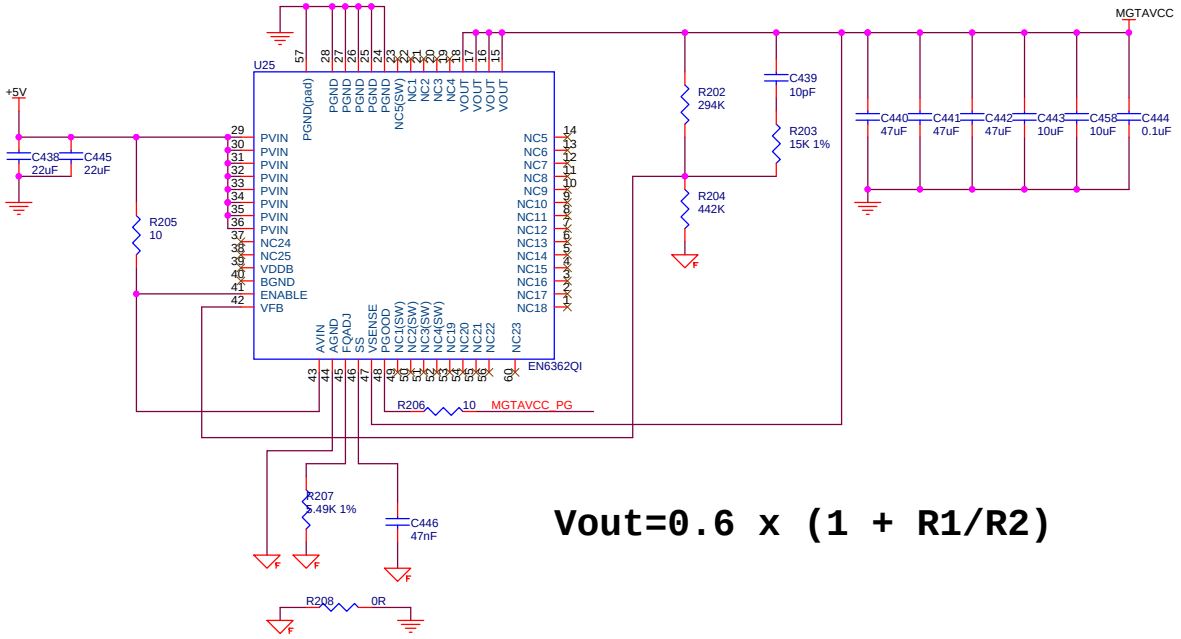
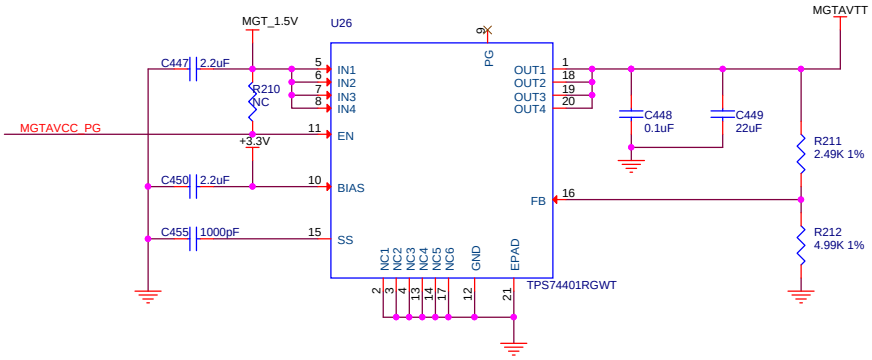
+1.0V 6A

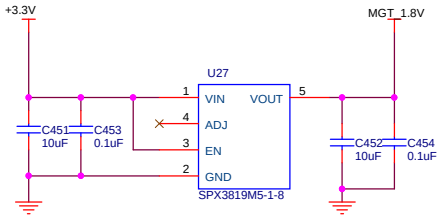


Vout=0.6 x (1 + R1/R2)

+1.2V 3A



Vout=0.8 x (1 + R1/R2)



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Title	PAGE20 POWER MGT	
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