IBIS/HSPICE Model Quality Report

Design ID: V00H
Description: 4Gb 1.5V DDR3 SDRAM
Marketing device name(s): MT41J1G4DA, MT41J512M8DA, MT41J256M16TW, MT41J1G4V00H, MT41J512M8V00H, MT41J256M16V00H
Valid speed grades: DDR3-1066, DDR3-1333, DDR3-1600, DDR3-1866, DDR3-2133[1]
Zip filename: v00h_ibis.zip
IBIS filename: v00h_v5p0.ibs, v00h_it_v5p0.ibs　　**File rev:** 2.0
HSpice filename: v00h_hspice.zip　　**File rev:** 2.0
EBD filename (if applicable):　　　　**File rev:**
Die rev: P
Date: August 25, 2015
Datasheet Link (from micron.com):

E-mail modelsupport@micron.com for questions regarding Quality Report.

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Device Parameters

VDDQ – Slow: 1.425V　**Typical:** 1. 5V　**Fast:** 1.575V
VDD – Slow: 1.425V　**Typical:** 1.5V　**Fast:** 1.575V
Junction Temperature (Commercial) - Slow: 110C　**Typical:** 50C　**Fast:** 0C
Junction Temperature (Industrial) - Slow: 110C　**Typical:** 50C　**Fast:** -40C
VDDQ/VSSQ Decoupling Capacitance: 6.6nF
　　Included in HSPICE DQ/DQS models? Yes　**Amount per DQ/DQS model:** 300pF/600pF
　　Included in IBIS DQ/DQS/DM models? No, must be included with separate Spice subcircuit.
VDDQ/VSSQ Decoupling Capacitance Series Resistance: 0.01Ohms

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IBIS Quality Summary

1. ☐ Include the IBIS Quality Specification 2.0 Overall IBIS Quality level. For details on IBIS Quality, reference the quality specification and quality checklist on IBIS quality webpage http://www.eda.org/pub/ibis/quality_wip/.

   Overall IBIS Quality Level: IQ3MS
   Exceptions: NA

2. ☒ Include the filename of the IBIS Quality Checklist that accompanies this report.

   Filename for Version 4.2 file: v00h_ibis_quality_checklist.xls
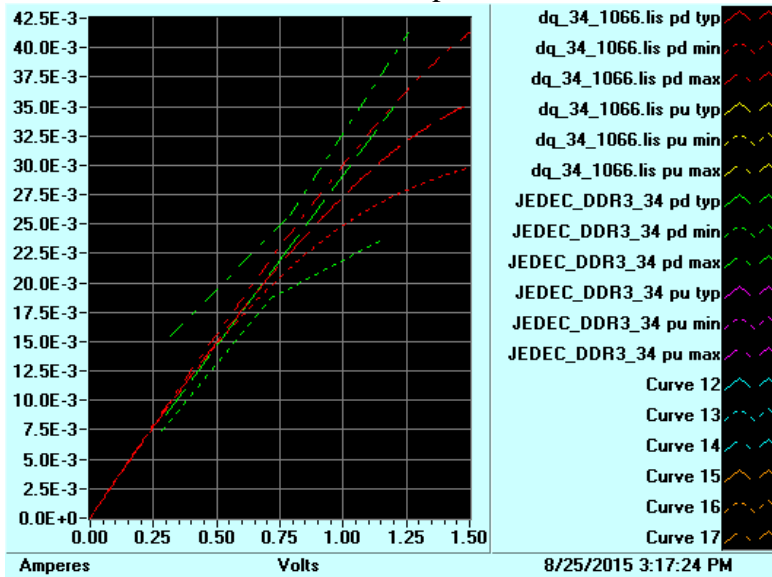   **Filename for Version 5.0 file:** v00h_v5p0_ibis_quality_checklist.xls

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IBIS MODEL Correlation
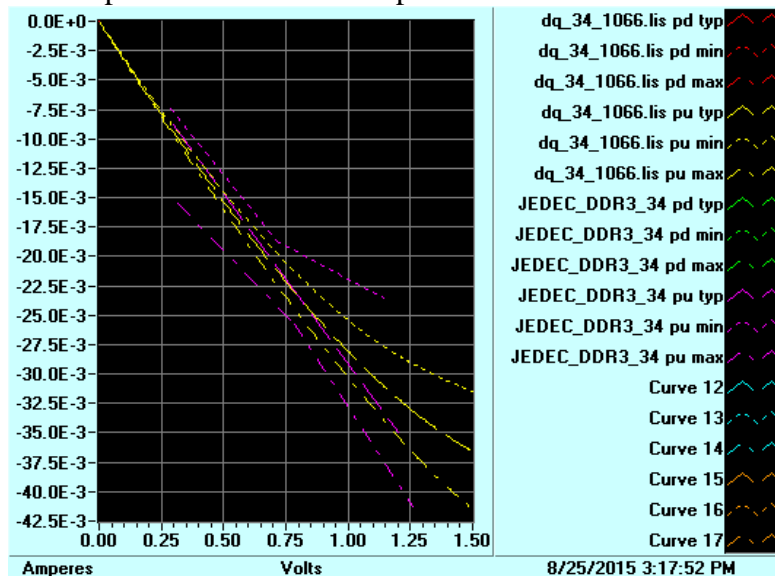
Datasheet Correlation

1. ☒ For Output or I/O model compare datasheet IOH/IOL data with IBIS pullup/pulldown data.

   a. Model name: **DQ_34_*[2]**
      i. Pulldown I-V versus **JEDEC** specification
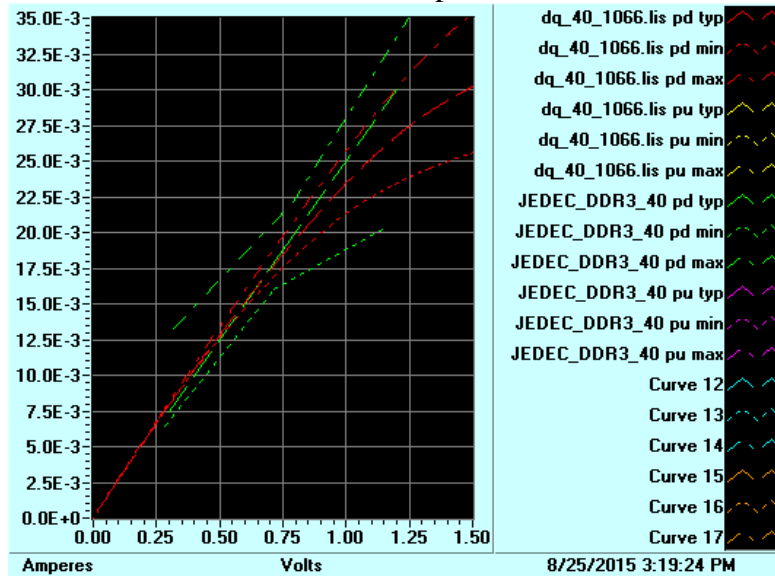

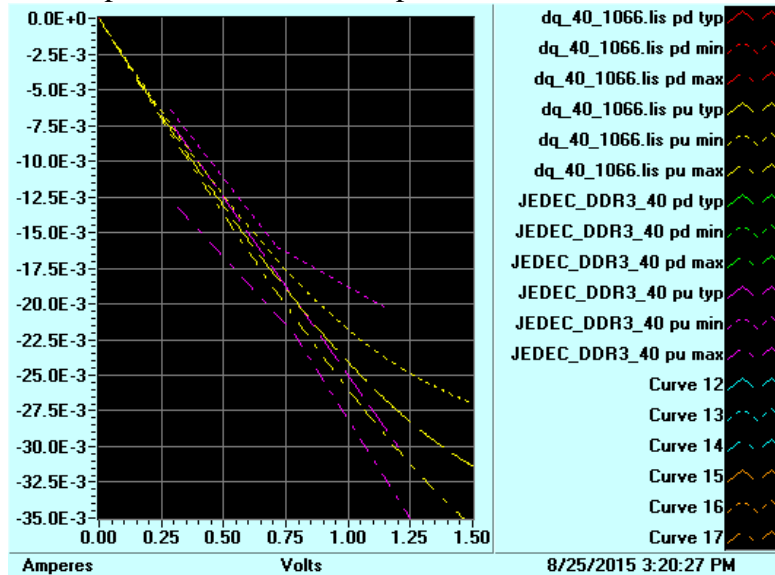   ii. Pullup I-V versus **JEDEC** specification

b. Model name: **DQ_40_***[2]

    i.   Pulldown I-V versus **JEDEC** specification

    ii.   Pullup I-V versus **JEDEC** specification

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2. ☒ Compare C_comp with datasheet Input C. Provide C_comp comparison table for all models and for all package combinations (i.e. x4, x8 and x16).

Component name: **MT41K1G4DA, MT41K512M8DA (78b x4, x8)**[3]

		IBIS (pF)		Datasheet (pF)	
		min	max	min	max
DQ	C_comp	1.03	1.18	NA	NA
	C package	0.40	0.57	NA	NA
	C_total	1.42	1.75	1.40	2.10
INPUT1	C_comp	0.38	0.53	NA	NA
	C package	0.35	0.52	NA	NA
	C_total	0.73	1.04	0.75	1.20
INPUT2	C_comp	0.45	0.60	NA	NA
	C package	0.33	0.41	NA	NA
	C_total	0.78	1.01	0.75	1.20
CLK	C_comp	0.43	0.58	NA	NA
	C package	0.37	0.40	NA	NA
	C_total	0.80	0.98	0.80	1.30
RST	C_comp	0.58	0.73	NA	NA
	C package	0.49	0.49	NA	NA
	C_total	1.07	1.22	NA	3.00

Component name: **MT41K256M16TW (96b x16)**

		IBIS (pF)		Datasheet (pF)	
		min	max	min	max
DQ	C_comp	1.03	1.18	NA	NA
	C package	0.38	0.61	NA	NA
	C_total	1.40	1.79	1.40	2.10
INPUT1	C_comp	0.38	0.53	NA	NA
	C package	0.45	0.58	NA	NA
	C_total	0.82	1.10	0.75	1.20
INPUT2	C_comp	0.45	0.60	NA	NA
	C package	0.38	0.47	NA	NA
	C_total	0.83	1.07	0.75	1.20
CLK	C_comp	0.43	0.58	NA	NA
	C package	0.38	0.43	NA	NA
	C_total	0.81	1.02	0.80	1.30
RST	C_comp	0.58	0.73	NA	NA
	C package	0.57	0.57	NA	NA
	C_total	1.14	1.29	NA	3.00

3. ☒ If slew rate specifications (rise/fall slew) are available from the datasheet, complete Spice simulations to generate slew rate data and provide a comparison table.

Model	Slew Rate (V/ns)	IBIS			Datasheet	
		min	typ	max	min	max
DQ_34_1600	Rising	3.76	4.91	6.80	2.50	6.00
	Falling	4.39	5.91	7.85	2.50	6.00
DQ_40_1600	Rising	3.29	4.49	6.01	2.50	6.00
	Falling	3.63	5.21	6.95	2.50	6.00
DQ_34_1866	Rising	3.49	5.12	6.63	2.50	6.00
	Falling	4.17	6.16	7.73	2.50	6.00
DQ_40_1866	Rising	3.11	4.53	6.03	2.50	6.00
	Falling	3.46	5.30	6.84	2.50	6.00
DQ_34_2133	Rising	4.17	5.32	6.65	2.50	6.00
	Falling	4.98	6.38	8.05	2.50	6.00
DQ_40_2133	Rising	3.65	4.66	5.94	2.50	6.00
	Falling	4.20	5.46	7.05	2.50	6.00

4. ☒ Compare ODT data with datasheet.

ODT calculated using the formula $RTT = (V_{IH(ac)} - V_{IL(ac)})/|(I (V_{IH(ac)}) - I(V_{IL(ac)})|$

ODT20	TYP	MIN	MAX
Vil (V)	0.575	0.5375	0.6125
Vih (V)	0.925	0.8875	0.9625
Ivil (A)	-8.06E-03	-6.62E-03	-8.86E-03
Ivih (A)	7.07E-03	6.51E-03	8.22E-03
	TYP	MAX	MIN
Rtt (Model)	23.14	26.65	20.49
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	20	32	18

ODT30	TYP	MIN	MAX
Vil (V)	0.575	0.5375	0.6125
Vih (V)	0.925	0.8875	0.9625
Ivil (A)	-5.36E-03	-4.41E-03	-5.89E-03
Ivih (A)	4.73E-03	4.35E-03	5.50E-03
	TYP	MAX	MIN
Rtt (Model)	34.70	39.97	30.73
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	30	48	27

ODT40	TYP	MIN	MAX
Vil (V)	0.575	0.5375	0.6125
Vih (V)	0.925	0.8875	0.9625
Ivil (A)	-4.03E-03	-3.31E-03	-4.43E-03
Ivih (A)	3.54E-03	3.26E-03	4.11E-03
	TYP	MAX	MIN
Rtt (Model)	46.28	53.30	40.99
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	40	64	36

ODT60	TYP	MIN	MAX
Vil (V)	0.575	0.5375	0.6125
Vih (V)	0.925	0.8875	0.9625
Ivil (A)	-2.70E-03	-2.21E-03	-2.97E-03
Ivih (A)	2.34E-03	2.16E-03	2.73E-03
	TYP	MAX	MIN
Rtt (Model)	69.44	79.96	61.50
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	60	96	54

ODT120	TYP	MIN	MAX
Vil (V)	0.575	0.5375	0.6125
Vih (V)	0.925	0.8875	0.9625
Ivil (A)	-1.33E-03	-1.09E-03	-1.46E-03
Ivih (A)	1.19E-03	1.10E-03	1.39E-03
	TYP	MAX	MIN
Rtt (Model)	138.81	159.90	122.91
Rtt (datasheet-in units of ZQ/12)	1.0	1.6	0.9
Rtt (datasheet)	120	192	108

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Measurement Correlation

1. ☒ For Output or I/O models compare measured IOH/IOL data with IBIS pullup/pulldown data. If the measurement conditions are different than the IBIS conditions, run Spice simulations using the same measurement conditions such as VCC, temperature, and process. Include measurement conditions in the image labels.

    a. Model name: **DQ_34_1066**
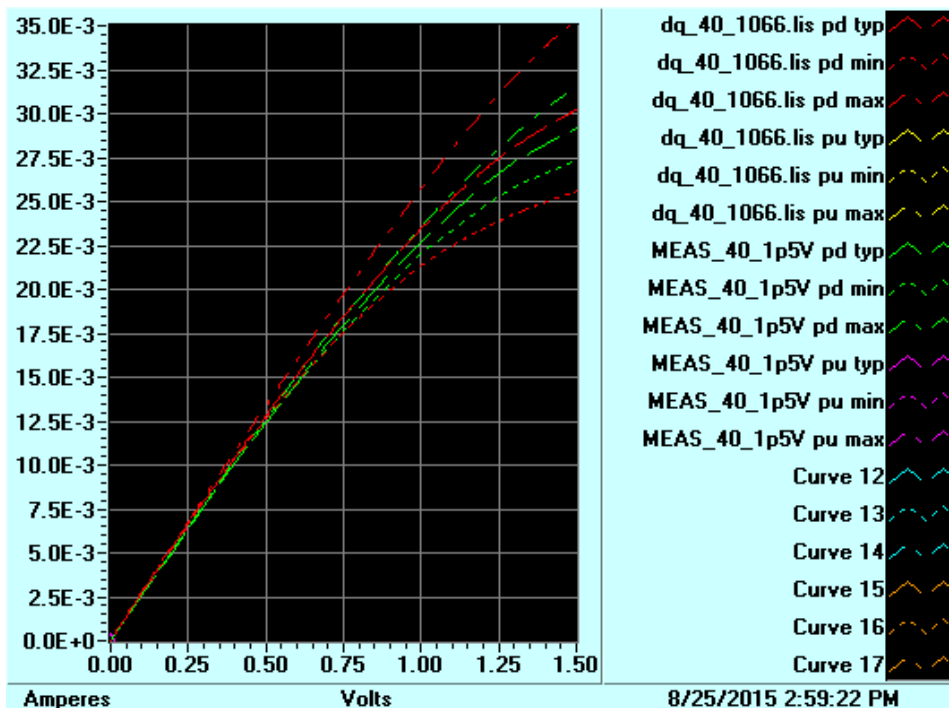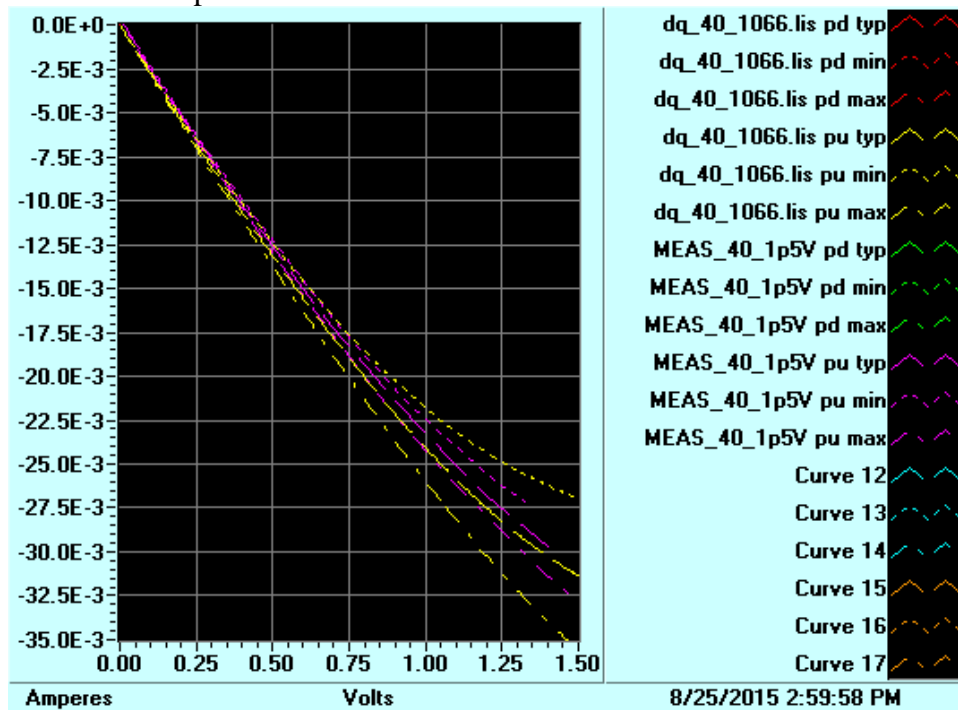   i. Pulldown I-V versus Measurement
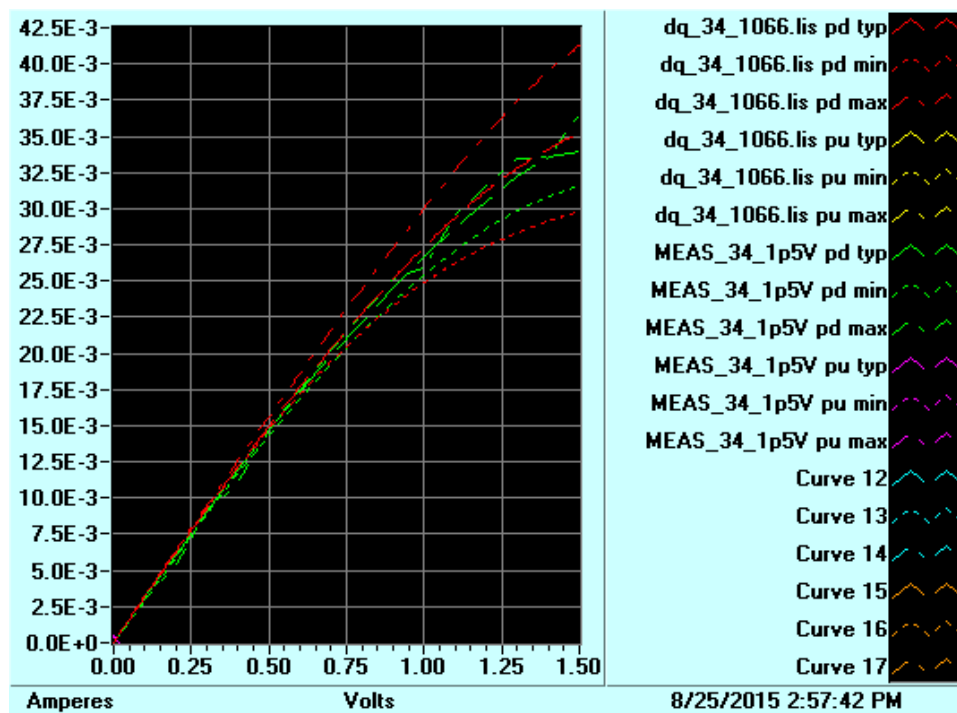
ii.   Pullup I-V versus Measurement
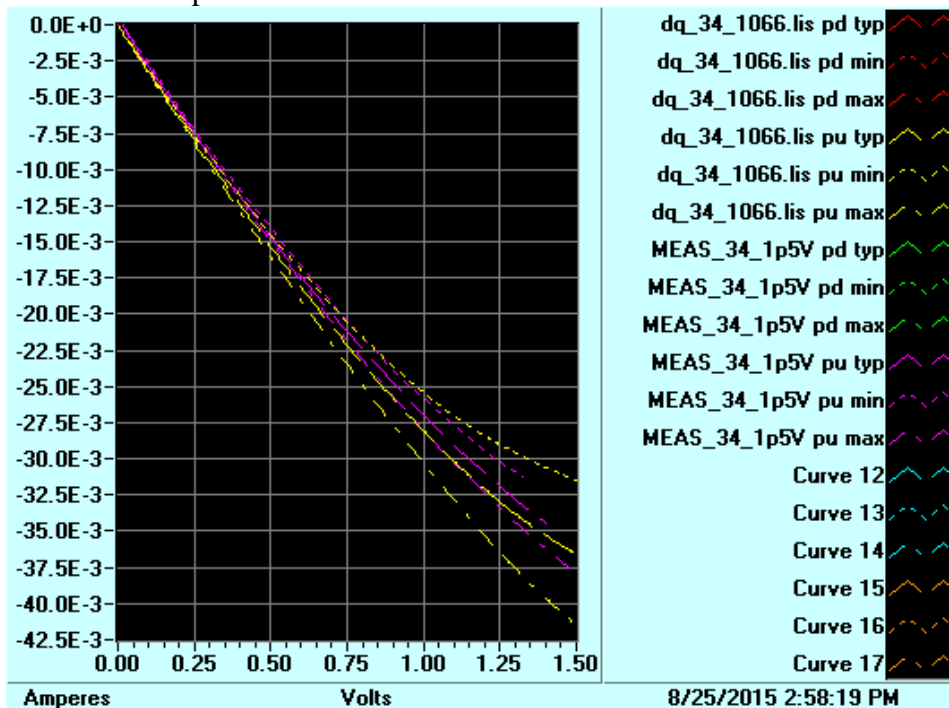
b.   Model name: **DQ_40_1066**

i.   Pulldown I-V versus Measurement

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ii.   Pullup I-V versus Measurement

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2. ⊠ Compare C_comp with measured C_comp. Provide C_comp comparison table for all models and for all package combinations (i.e x4, x8 and x16).

Component name: **MT41K1G4DA, MT41K512M8DA (78b x4, x8)**

		IBIS (pF)			Measured (pF)		
		min	typ	max	min	typ	max
DQ	C_comp	1.03	1.10	1.18	NA	NA	NA
	C package	0.40	0.47	0.57	NA	NA	NA
	C_total	1.42	1.57	1.75	1.45	1.57	1.75
INPUT1	C_comp	0.38	0.45	0.53	NA	NA	NA
	C package	0.35	0.43	0.52	NA	NA	NA
	C_total	0.73	0.88	1.04	0.73	0.86	1.02
INPUT2	C_comp	0.45	0.53	0.60	NA	NA	NA
	C package	0.33	0.37	0.41	NA	NA	NA
	C_total	0.78	0.89	1.01	0.75	0.86	0.99
CLK	C_comp	0.43	0.51	0.58	NA	NA	NA
	C package	0.37	0.38	0.40	NA	NA	NA
	C_total	0.80	0.89	0.98	0.87	0.90	0.94
RST	C_comp	0.58	0.65	0.73	NA	NA	NA
	C package	0.49	0.49	0.49	NA	NA	NA
	C_total	1.07	1.14	1.22	1.06	1.10	1.15

Component name: **MT41K256M16TW (96b x16)**

		IBIS (pF)			Measured (pF)		
		min	typ	max	min	typ	max
DQ	C_comp	1.03	1.10	1.18	NA	NA	NA
	C package	0.38	0.46	0.61	NA	NA	NA
	C_total	1.40	1.56	1.79	1.46	1.57	1.75
INPUT1	C_comp	0.38	0.45	0.53	NA	NA	NA
	C package	0.45	0.51	0.58	NA	NA	NA
	C_total	0.82	0.96	1.10	0.91	1.01	1.11
INPUT2	C_comp	0.45	0.53	0.60	NA	NA	NA
	C package	0.38	0.43	0.47	NA	NA	NA
	C_total	0.83	0.95	1.07	0.89	0.96	1.04
CLK	C_comp	0.43	0.51	0.58	NA	NA	NA
	C package	0.38	0.41	0.43	NA	NA	NA
	C_total	0.81	0.91	1.02	0.91	0.94	1.00
RST	C_comp	0.58	0.65	0.73	NA	NA	NA
	C package	0.57	0.57	0.57	NA	NA	NA
	C_total	1.14	1.22	1.29	1.23	1.24	1.24

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3. ☐ If measured clamp current data is available, provide an IBIS versus measurement comparison for all models. Include measurement conditions in the image labels.

   Not available

4. ☐ If slew rate data (rise/fall slew) is available from measurements, complete Spice simulations to generate slew rate data and provide a comparison table.

   Not available

IBIS vs Spice Correlation

1. ☒ For all Output or I/O models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element).
   a. ☒ Use the setup and node naming conventions shown below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2012.06**
   b. ☒ Run simulations for all corners cases and at fastest speed grades, testing ODT models as loads when applicable.

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i. **DQ_34_1600 driving DQ_34_1600**
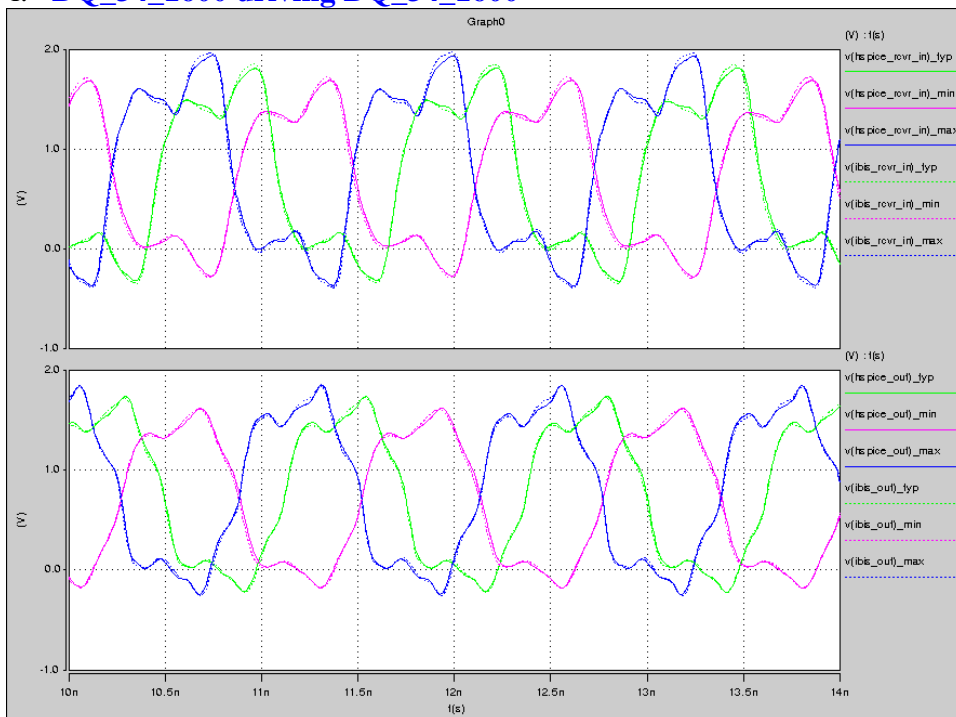
ii. **DQ_34_1600 driving DQ_34_ODT20_1600**

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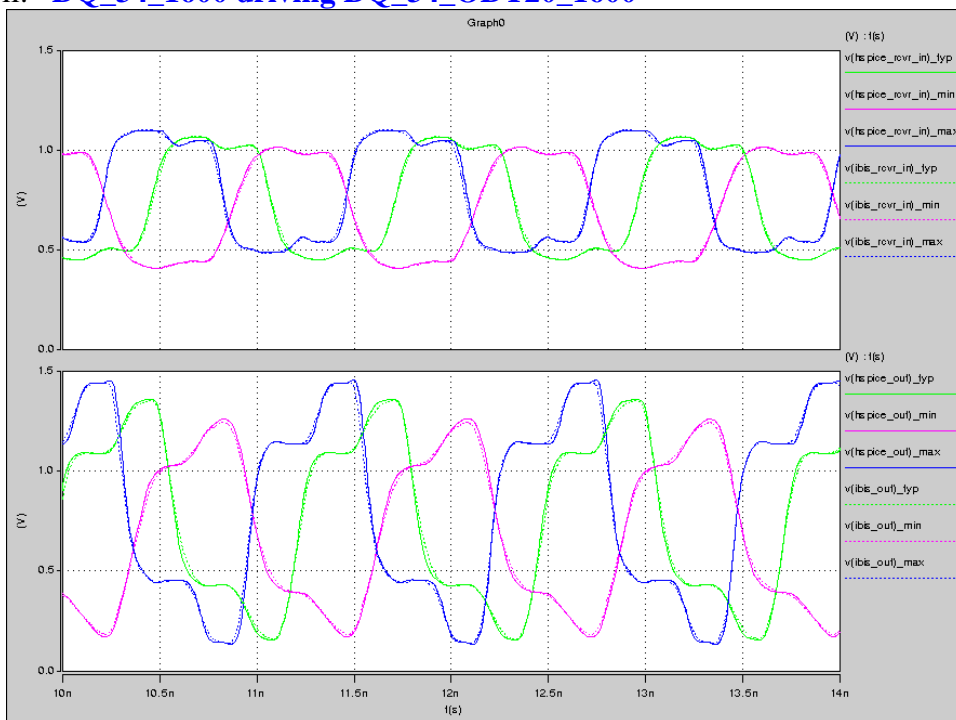
iii. DQ_34_1600 driving DQ_34_ODT30_1600
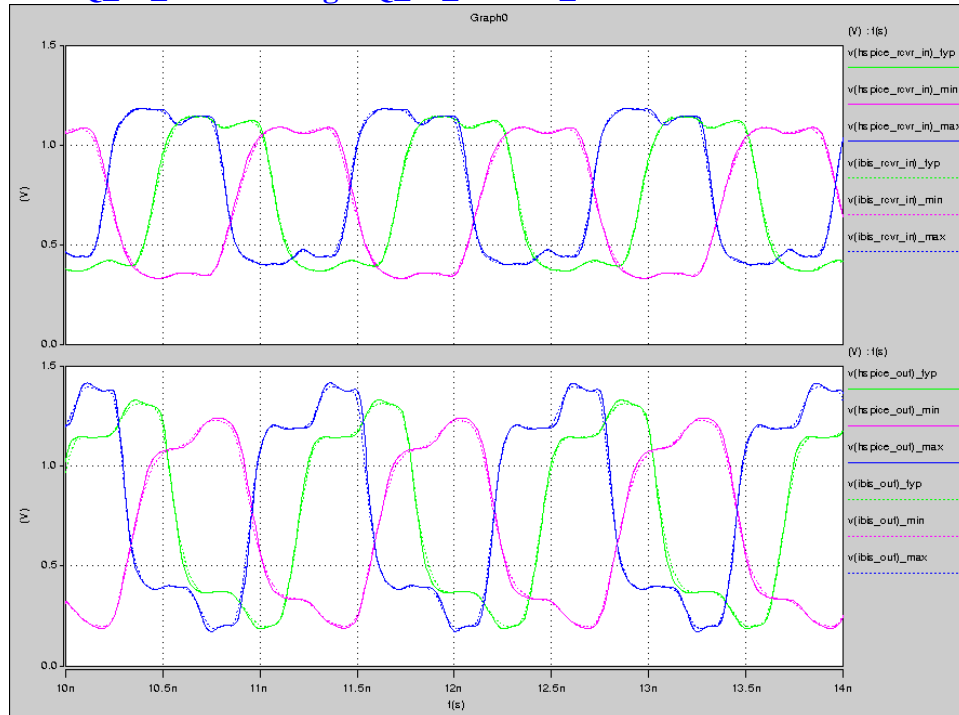
iv. DQ_34_1600 driving DQ_34_ODT40_1600

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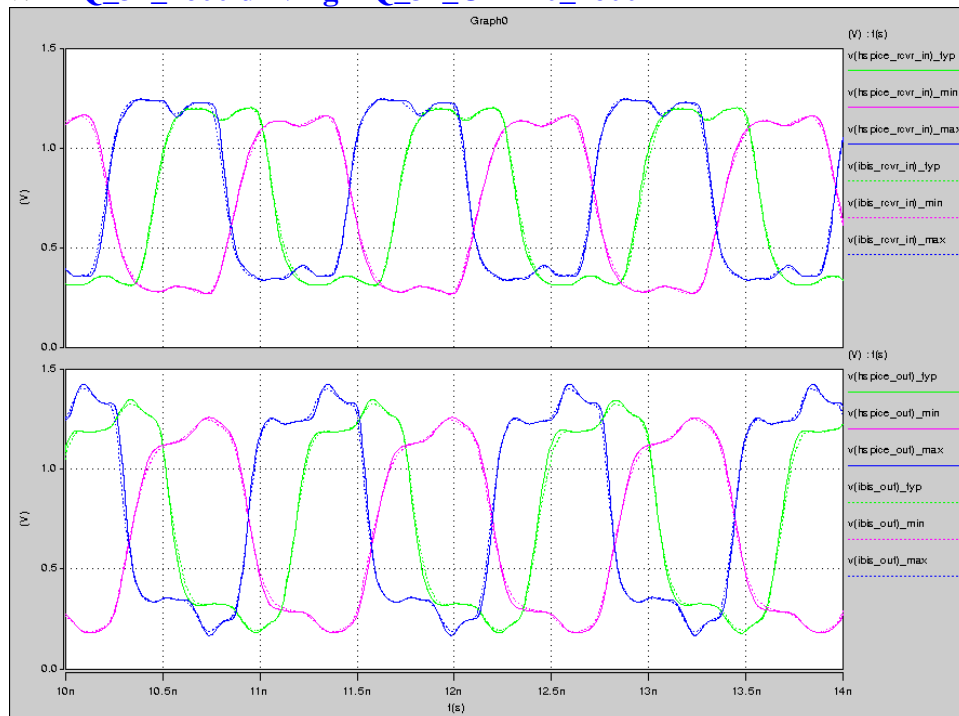
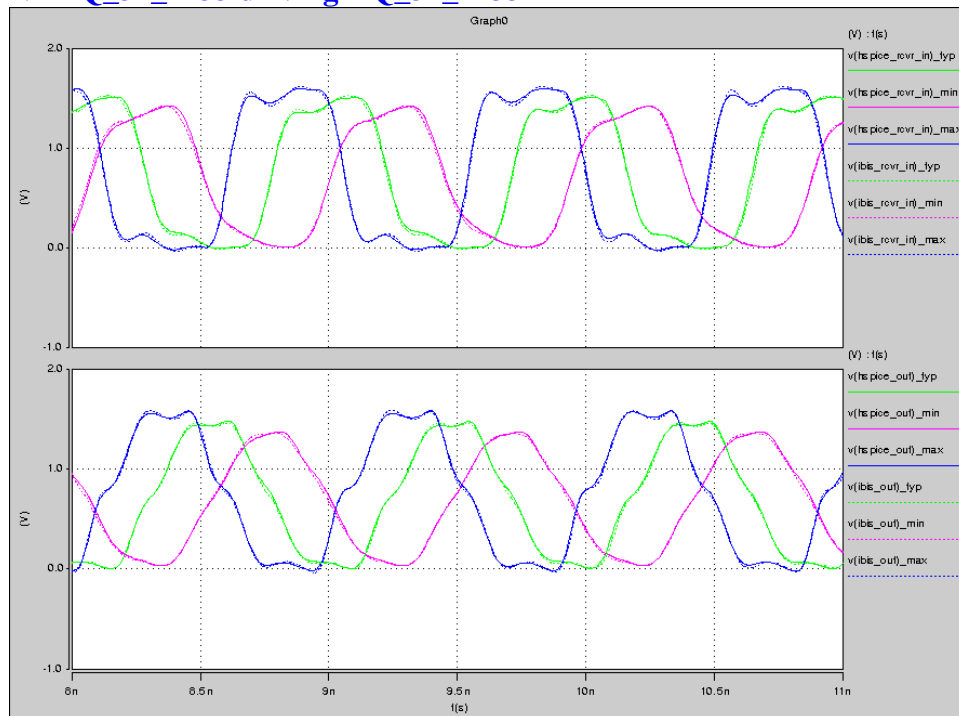v.   **DQ_34_1600 driving DQ_34_ODT60_1600**
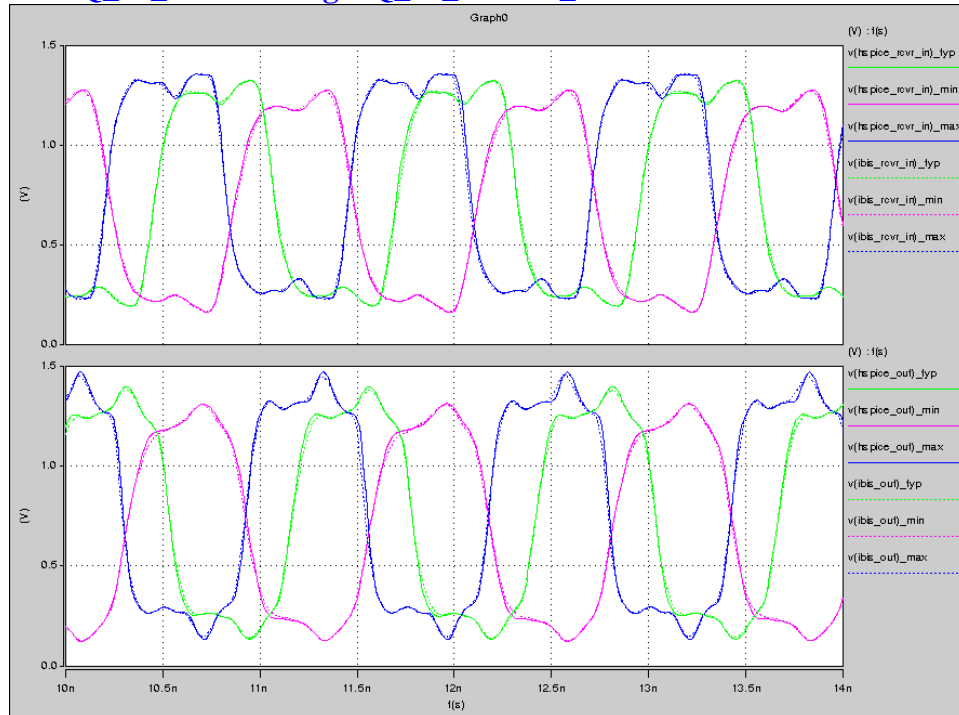
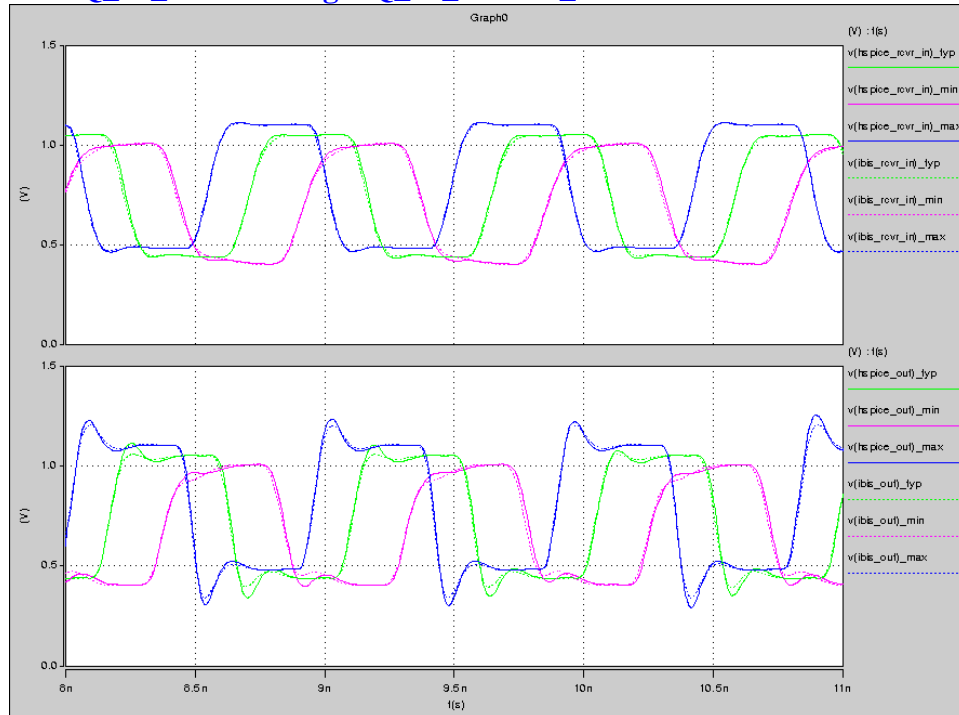vi.   **DQ_34_1600 driving DQ_34_ODT120_1600**
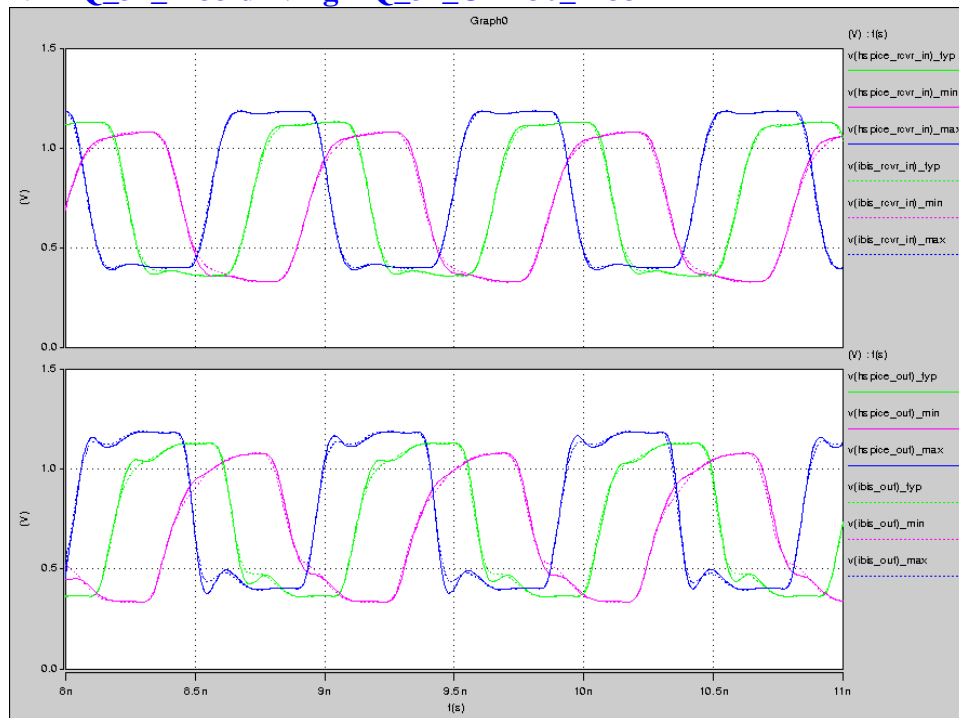
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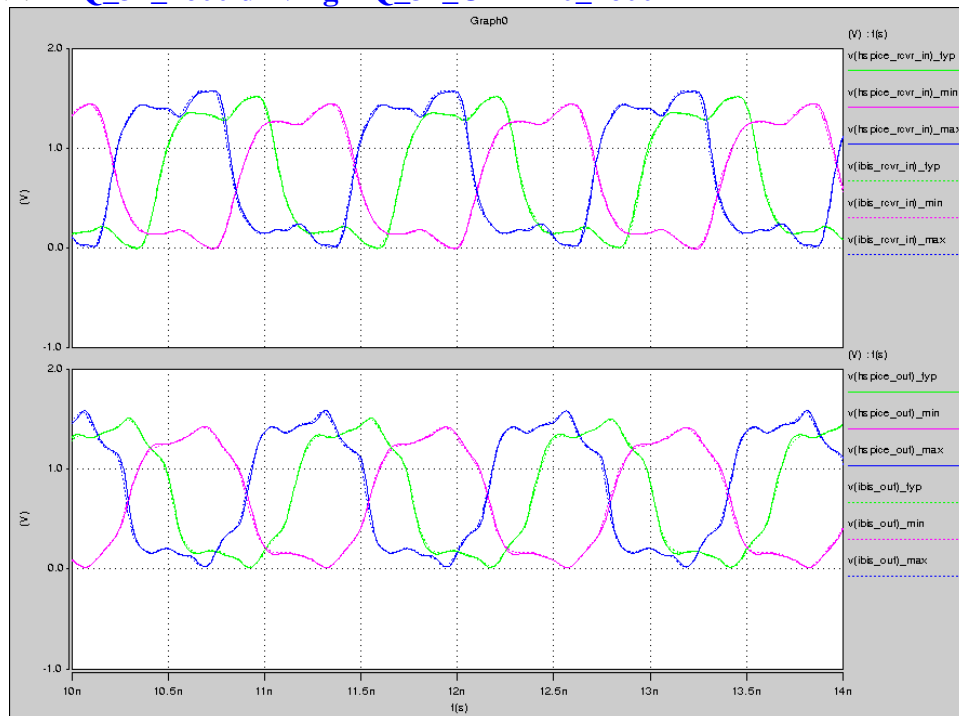
vii. DQ_40_1600 driving DQ_40_ODT60_1600
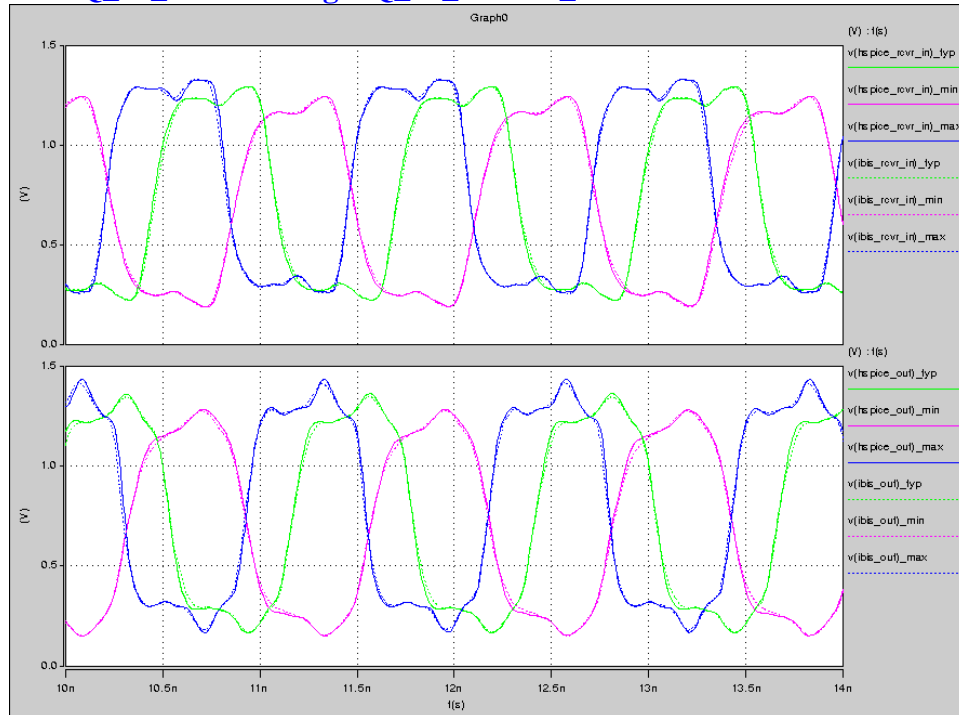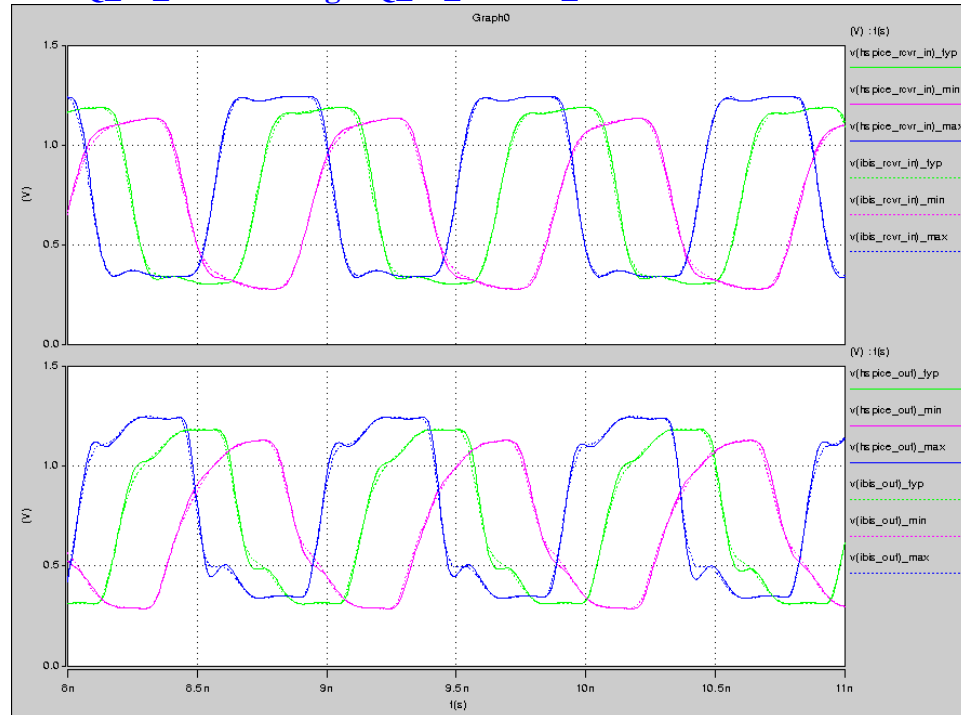

viii. DQ_34_2133 driving DQ_34_2133

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ix. **DQ_34_2133 driving DQ_34_ODT20_2133**

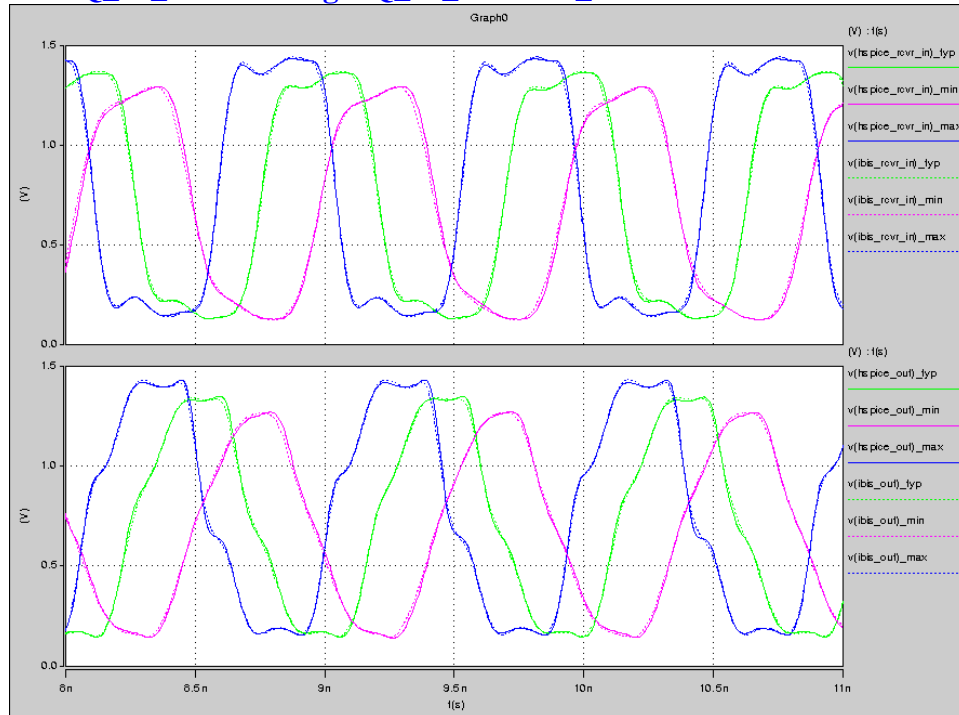x. **DQ_34_2133 driving DQ_34_ODT30_2133**

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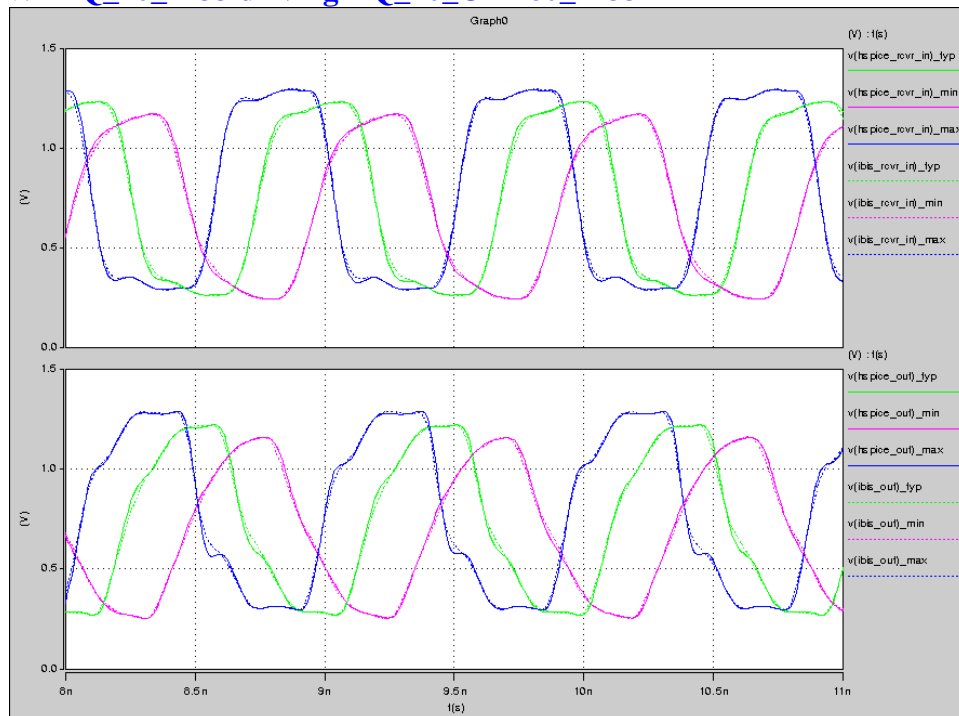## xi. DQ_34_2133 driving DQ_34_ODT40_2133

xii. DQ_34_2133 driving DQ_34_ODT60_2133

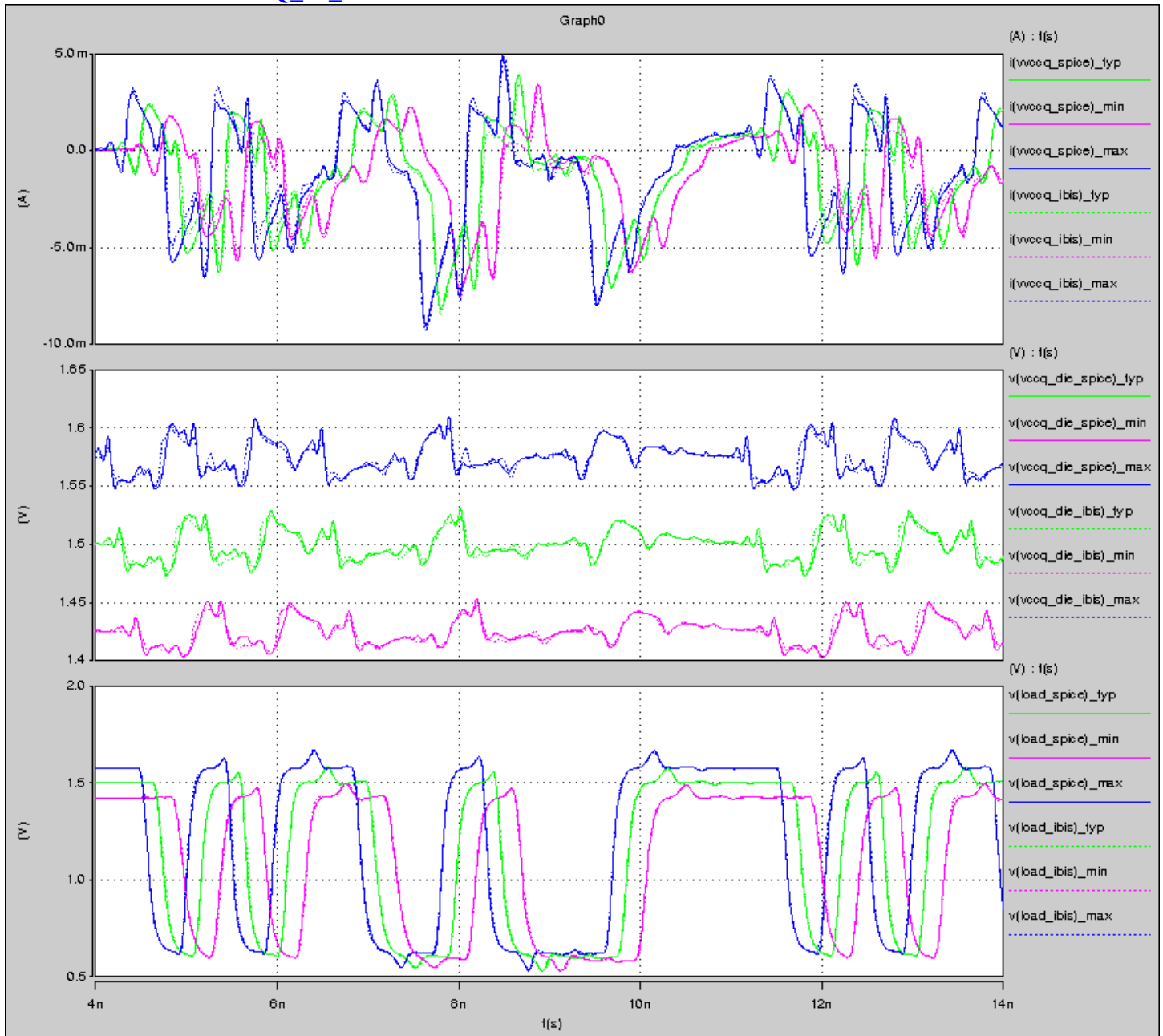_____
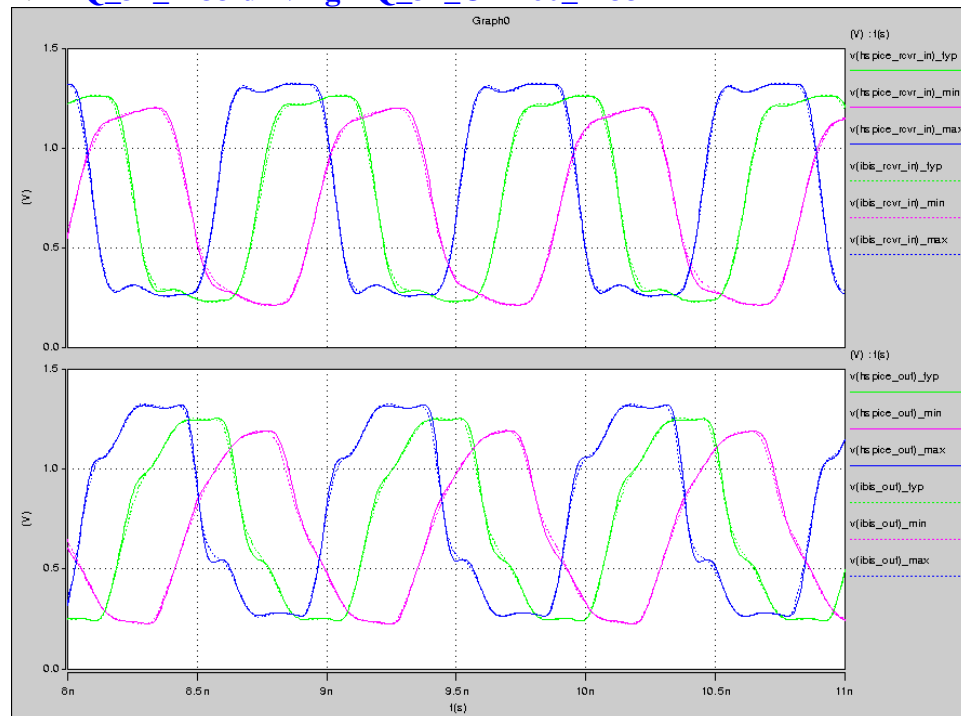
xiii.   **DQ_34_2133 driving DQ_34_ODT120_2133**
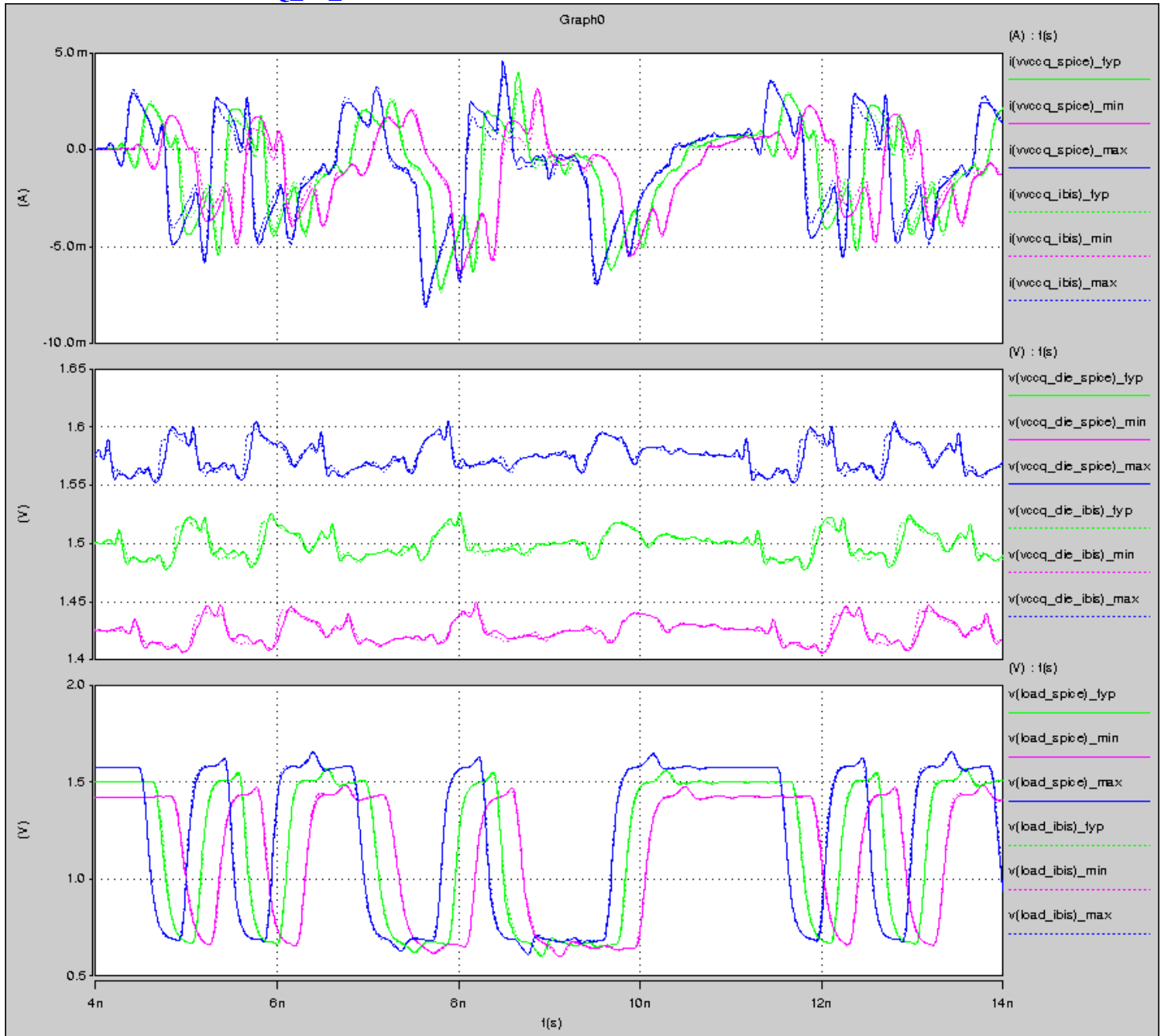

xiv.   **DQ_40_2133 driving DQ_40_ODT60_2133**

2. ☒ For all Output or I/O IBIS Version 5.0 power-aware models, run Spice transient simulations using encrypted netlists and the IBIS model (b-element) with a non-ideal power supply connection.

    a. ☒ Use the setup and node naming conventions shown in Setup B below for the IBIS and Spice files. Update the setup diagram if it is different. Indicate the version of Spice simulator used for simulations: **HSPICE 2015.06**

    b. ☒ Run simulations for all corner cases and at fastest speed grades.
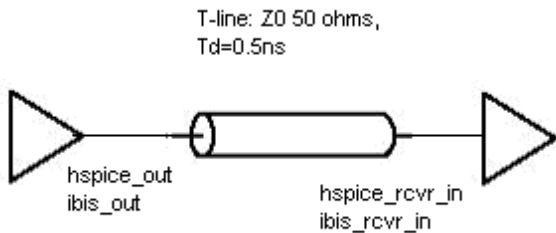
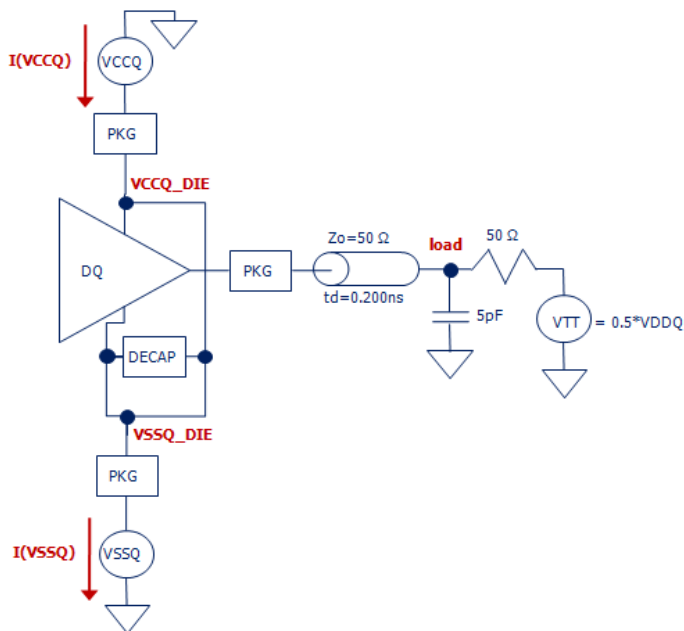i.   **DQ_34_2133**

ii. **DQ_40_2133**

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Setup

A:

T-line: Z0 50 ohms,
Td=0.5ns

hspice_out
ibis_out

hspice_rcvr_in
ibis_rcvr_in

B:

I(VCCQ)   VCCQ

PKG

VCCQ_DIE

DQ   PKG   Zo=50 Ω   load   50 Ω
td=0.200ns
5pF   VTT = 0.5*VDDQ

DECAP

VSSQ_DIE

PKG

I(VSSQ)   VSSQ

* Package Model used for correlation
lpkg PAD BALL 1.25e-9 R=0.25
lpkg_vccq vccq_die vccq_ball 1.25e-9 R=0.25
lpkg_vssq vssq_die vssq_ball 0.10e-9 R=0.05
k1 lpkg_vccq lpkg_vssq 0.20
k2 lpkg lpkg_vccq 0.40
k3 lpkg lpkg_vssq 0.20
cpkg_vccq BALL vccq_ball 0.20e-12
cpkg_vssq BALL vssq_ball 0.20e-12
cpkg_vccq_vssq vccq_ball vssq_ball 0.400e-12

Comments:

1. IBIS model may not reflect speed grade availability.
2. IV correlation shown for DDR3-1866 and below only.
3. C_comp is compared with the DDR3-2133 specification only.
4. Slew rate is based on HSPICE simulation with a 25ohm load to Vtt. This includes simple package parasitics.

Document Revision History

Rev **1.0** - Date **10/23/2014**
      a. IBIS revision (Version 4.2) **1.0**
      b. IBIS revision (Version 5.0) **1.0**
      c. HSpice revision **1.0**

Rev **2.0** - Date **08/25/2015**
      d. IBIS revision (Version 4.2) **2.0**
      e. IBIS revision (Version 5.0) **2.0**
      f. HSpice revision **2.0**