

Cologne Chip GateMate FPGA Module: GMM-7550 for CCGM1A 1/2/4 (BGA320, 15x15 mm)

Revision	Date	Notes
0.5	2020-07-08	Initial release of the schematic
1.0	2020-10-01	Schematic freeze, preliminary placement is done. (I/O and BoM changes back ported from PCB)

Sheet: GPIO

File: io.sch

Sheet: Power Converter

File: power.sch

Sheet: Clock and SERDES

File: clk_serdes.sch

Sheet: Configuration and Control

Sheet: IO Connectors

Fide: File: Fil

File: connectors.sch

File: cfg_spi.sch

You may redistribute and modify this documentation and make products using it under the terms of the CERN-OHL-P v2 (https://cern.ch/cern-ohl).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

Please see the CERN-OHL-P v2 for applicable conditions



Copyright (c) 2020 Anton Kuzmin Licensed under CERN-OHL-P v2 https://github.com/ak-fau/gmm7550.git

Sheet: / File: gmm.sch

Title: GateMate FPGA Module: GMM-7550

Size: A4	Date: 2020-10-01	Rev: 1.0		
KiCad E.D.A. kid	cad 5.1.6	ld: 1/7		











