DATA SHEET

# GPL95101UA

## High-end 16-bit Interactive LCD Toy & Game Controller

Jan. 16, 2019

Version 1.0

# Table of Contents

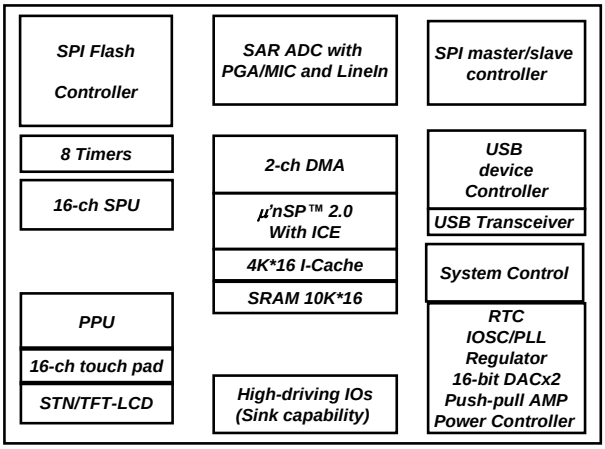
**PAGE**

# High-end 16-bit Interactive LCD Toy & Game Controller with μ'nSP® 2.0

## 1. GENERAL DESCRIPTION

GPL95101UA, a highly integrated System-on-a-Chip (SoC), is a cost-effective and high performance micro-controller solution for game, education and interactive learning applications. It equips a μ'nSP® 2.0 CPU with 8KB I-cache, picture process unit (PPU), 16-channel sound process unit (SPU), SPI Flash controller, two channels of DMA controller, USB device, mono STN-LCD and TFT-LCD interface, interrupt controller, and many other advanced features. Providing a complete set of common system peripherals, GPL95101UA minimizes overall system costs and eliminates many additional components that other microcontrollers may require. Its development system integrates several powerful tools such as system with C language capability, assembly compiler, linker, source debugger, and project management tools to manage a project from start to the end.

## 2. BLOCK DIAGRAM




## 3. FEATURES

- ***Built-in 16-bit μ'nSP® 2.0 microprocessor***
  - Running up to 96MHz
  - Operating from 2.9V to 5.5V
- **Memory**
  - 4K*16-bit I-cache
  - 10K*16-bit RAM, stack area included
  - Linear mapping and executing program on the external SPI FLASH. Both 2-IO mode and 4-IO mode are supported.
- **I/O**
  - Max. 37 General Programmable I/O ports (GPIO).
  - Each incorporates with pull-up resistor, pull-down resistor or floating input based on programmer's settings via the corresponding registers
  - 13 high driving I/O ports with LED driving capability and 40mA current sink
- **Clock Management**
  - Internal oscillator: 8MHz ±1.5%(typ), @ 2.7V~3.6V
  - 32768Hz Crystal input @ 1.62V~1.98V
  - PLL (Phase-Lock Loop): 8MHz~96MHz, step=4MHz @ 2.7V~3.6V
- **Flexible Power Management (Operating/ Power down/ Wait/ Halt Mode)**
  - Operating mode: High performance@96MHz high speed
  - Deep Halt mode: 3.3V/1.8V off with only RTC on and approximately 5uA current
  - Wait mode: CPU clock off and system clocks are all on
  - Halt mode: CPU and system clocks are all off. Only RTC, 32768Hz-XTAL, and LDOs modules are active
- **Picture Process Unit (PPU)**
  - 3 Text layers + 256 Sprites
  - QVGA output
  - Line-base operation
  - Up to 1024 x 1024 Text Size
- **TFT-LCD controller**
  - UPS051 (serial RGB)
  - UPS052 (serial RGB dummy),
  - Parallel RGB
  - I80 (8-bit/16-bit system bus) I/F type
  - CCIR601/CCIR656
  - **Supports various LCD resolutions: 160x128, 220x176, and 320x240**
- **Mono and 16-gray STN-LCD controller interface**
- **Sound Process Unit (SPU)**
  - 16 hardware PCM/ADPCM channels
  - Cache supporting for directly accessing 16-channel wave table on external SPI Flash, 2-channel A1800 playback
- 16-channel capacitive touch detection
- Two-channel DMA controller
- 29 interrupt sources.
- Universal Serial Bus (USB) 2.0 full speed compliant device with built-in transceiver
- Watchdog timer
- Independent power real-time clock

- 11-output x 8-input matrix key scan controller
- Eight 16-bit timers
- Six re-loadable timers/counters support comparison, PWM, capture and BAM (4-bit angle modulation)
- SPI master/slave controller.
- Power controller with on power-on key and one system power enable output pad.
- Built-in 5.5V to 3.3V regulator, 3.3V to 1.8V regulator, Regulator for touch pad macro and regulator for ADC
  –
- Low voltage reset(LVR)(2.4V trigger/2.6V release for 3.3V)
- IOSC, 96MHz PLL
- **DAC/Amplifier:** 16-bit stereo L and R DAC output that can be added external amplifier. Or mix L_R internally then through a push pull amplifier output, which can driver external speaker directly.
- **ADC: Two 12-bit ADCs**
  – One for MIC in with PGA and digital AGC
  – One for 1-channel line-in

## 4. SIGNAL DESCRIPTION

Left Side

| Package No | Name | Group | Type | Normal Function Description |
|---|---|---|---|---|
| 1 | IOE5 | ADC | I/O | IOE5 or ADC line in 5 |
| 2 | IOE6 | ADC | I/O | IOE6 or MIC input or UART_RX |
| 3 | IOE7 | ADC | I/O | IOE7 or ADC voltage reference output or UART_TX |
| 4 | VSS_ADC | ADC | G | ADC ground |
| 5 | V33_ADC | ADC | P | 3.3V ADC power. This power can be provided by internal regulator out and then connect capacitor to ADC ground only. |
| 6 | RESETB | SYS | I | Reset pin, low active. |
| 7 | ICECK | ICE | I | ICE clock input. Default is input pull low. |
| 8 | ICEDA | ICE | I/O | ICE data. Default is input pull low. |
| 9 | IOD0 | SPI FLASH I/F | I/O | Default is SPI FLASH DATA0 |
| 10 | IOD1 | SPI FLASH I/F | I/O | Default is SPI FLASH CLOCK |
| 11 | DVSS | Digital Ground | G | Digital ground |
| 12 | IOD2 | SPI FLASH I/F | I/O | Default is SPI FLASH DATA3 |
| 13 | IOD3 | SPI FLASH I/F | I/O | Default is SPI FLASH CSB |
| 14 | IOD4 | SPI FLASH I/F | I/O | Default is SPI FLASH DATA1 |
| 15 | IOD5 | SPI FLASH I/F | I/O | Default is SPI FLASH DATA2 |
| 16 | V33_DVCC | Digital 3.3V | P | 3.3V I/O power input for PortD |

Bottom Side

| Package No | Name | Group | Type | Normal Function Description |
|---|---|---|---|---|
| 17 | V18_DVCC | Digital 1.8V | P | 1.8V digital power |
| 18 | IOA0 | High driving IO | I/O | IOA0 or TFT TE input(i-80) or external input interrupt(EXT0_INT) |
| 19 | IOA1 | High driving IO | I/O | IOA1 or TFT OEB(i-80) or TFT DE or SPI1 DO |
| 20 | IOA2 | High driving IO | I/O | IOA2 or TFT R/S(i-80) or TFT HSYNC or SPI1 CSB |
| 21 | IOA3 | High driving IO | I/O | IOA3 or TFT CSB(i-80) or TFT VSYNC or SPI1 CLK |
| 22 | IOA4 | High driving IO | I/O | IOA4 or TFT WEB(i-80) or TFT clock or SPI1 DI |
| 23 | IOB0 | High driving IO | I/O | IOB0 or TimerA CCP or TFT D0(CCIR) |
| 24 | IOB1 | High driving IO | I/O | IOB1 or TimerB CCP or TFT D1(CCIR) |
| 25 | V50_IOAB | IO power | P | PortA /B power input |
| 26 | IOB2 | High driving IO | I/O | IOB2 or TimerC CCP or TFT D2(CCIR) |
| 27 | IOB3 | High driving IO | I/O | IOB3 or TimerD CCP or TFT D3(CCIR) |
| 28 | IOB4 | High driving IO | I/O | IOB4 or Timer PWM0 or TFT D4(CCIR) or SPI1 DO |
| 29 | IOB5 | High driving IO | I/O | IOB5 or Timer PWM1 or TFT D5(CCIR) or SPI1 CSB |
| 30 | IOB6 | High driving IO | I/O | IOB6 or Timer PWM2 or TFT D6(CCIR) or SPI1 CLK |
| 31 | IOB7 | High driving IO | I/O | IOB7 or Timer PWM3 or TFT D7(CCIR) or SPI1 DI |
| 32 | IOF0 | Touch | IO | IOF0 or Touch pad 0 or TFT B3(CCIR) or TFTD0(CCIR) or SPI1 DO |

Right Side

| Package No | Name | Group | Type | Normal Function Description |
|---|---|---|---|---|
| 33 | IOF1 | Touch | IO | IOF1 or Touch pad 1 or TFT B4(CCIR) or TFTD1(CCIR) or SPI1 CSB |
| 34 | IOF2 | Touch | IO | IOF2 or Touch pad 2 or TFT B5(CCIR) or TFTD2(CCIR) or SPI1 CLK |
| 35 | IOF3 | Touch | IO | IOF3 or Touch pad 3 or TFT B6(CCIR) or TFTD3(CCIR) or SPI1 DO |
| 36 | IOF4 | Touch | IO | IOF4 or Touch pad 4 or TFT B7(CCIR) or TFTD4(CCIR) or SPI0 DO |
| 37 | IOF5 | Touch | IO | IOF5 or Touch pad 5 or TFT G2(CCIR) or TFTD5(CCIR) or SPI0 CSB |

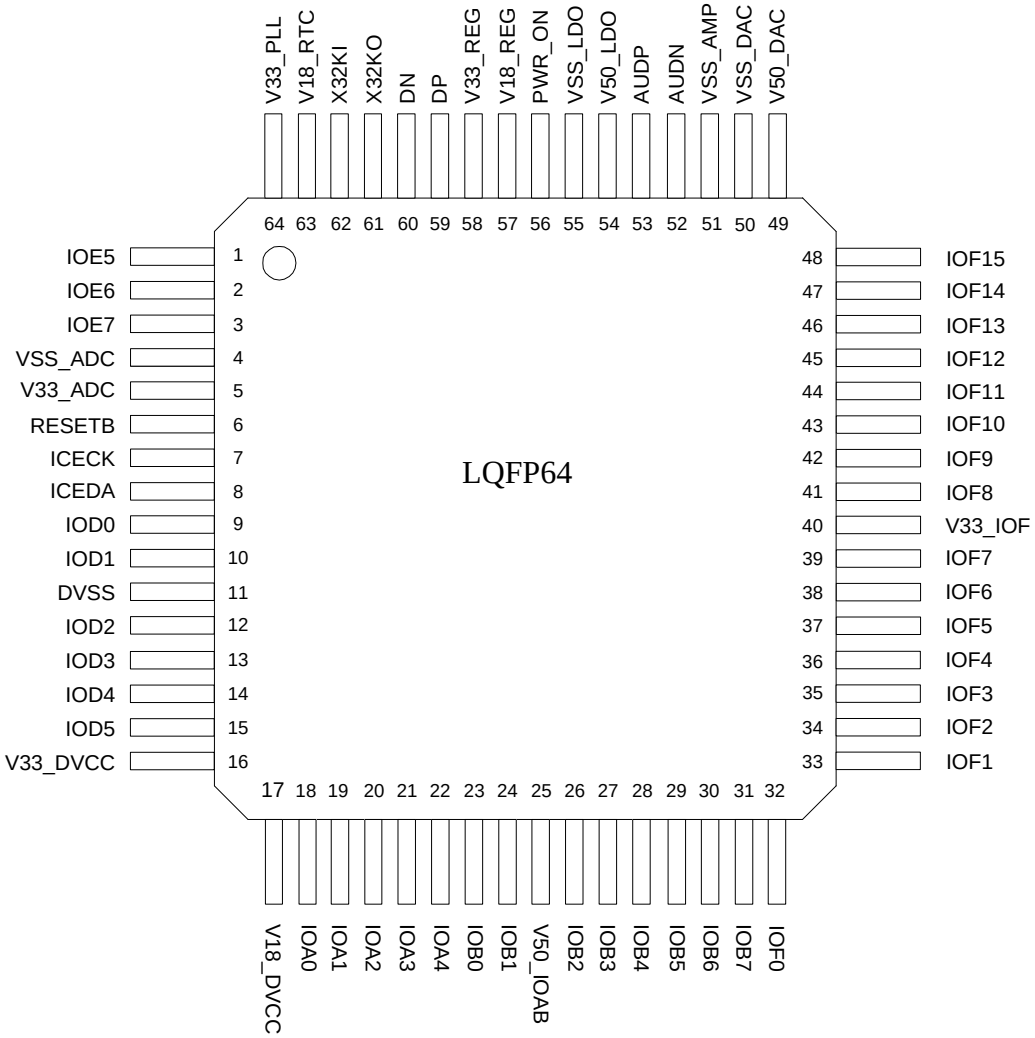
| Package No | Name | Group | Type | Normal Function Description |
|---|---|---|---|---|
| 38 | IOF6 | Touch | IO | IOF6 or Touch pad 6 or TFT G3(CCIR) or TFTD6(CCIR) or SPI0 CLK |
| 39 | IOF7 | Touch | IO | IOF7 or Touch pad 7 or TFT G4(CCIR) or TFTD7(CCIR) or SPI0 DI |
| 40 | V33_IOF | Touch | P | 3.3V power input for PortF. |
| 41 | IOF8 | Touch | IO | IOF8 or Touch pad 8 or TFT G5(CCIR) or TFT TE input(i-80) |
| 42 | IOF9 | Touch | IO | IOF9 or Touch pad 9 or TFT G6(CCIR) or TFT OEB(i-80) or TFT DE(CCIR) |
| 43 | IOF10 | Touch | IO | IOF10 or Touch pad 10 or TFT G7(CCIR) or TFT R/S(i-80) or TFT HSYNC(CCIR) |
| 44 | IOF11 | Touch | IO | IOF11 or Touch pad 11 or TFT R3(CCIR) or TFT CSB(i-80) or TFT VSHYNC(CCIR) or UART TX |
| 45 | IOF12 | Touch | IO | IOF12 or Touch pad 12 or TFT R4(CCIR) or TFT WEB(i-80) or TFT CLK(CCIR) or UART RX |
| 46 | IOF13 | Touch | IO | IOF13 or Touch pad 13 or TFT R5(CCIR) or I2C CLK |
| 47 | IOF14 | Touch | IO | IOF14 or Touch pad 14 or TFT R6(CCIR) or I2C SDA |
| 48 | IOF15 | Touch | IO | IOF15 or Touch pad 15 or TFT R7(CCIR) or external input interrupt(EXT1_INT) |

Top Side

| Package No | Name | Group | Type | Normal Function Description |
|---|---|---|---|---|
| 49 | V50_DAC | DAC_AMP | P | DAC power (up to 5.5V) input |
| 50 | VSS_DAC | DAC_AMP | G | DAC ground |
| 51 | VSS_AMP | DAC_AMP | G | Audio AMP ground |
| 52 | AUDN | DAC_AMP | AO | Audio AMP output N/DAC output channel L |
| 53 | AUDP | DAC_AMP | AO | Audio AMP output P/DAC output channel R |
| 54 | V50_LDO | LDO | P | DC 5V power input |
| 55 | VSS_LDO | LDO | G | LDO ground |
| 56 | PWR_ON | LDO | AI | Power-on key, high active. Default is input pull low |
| 57 | V18_REG | LDO | P | Internal V1.8 LDO regulator output |
| 58 | V33_REG | LDO | P | Internal V3.3 regulator output |
| 59 | DP | USB | I/O | DP pin of USB PHY |
| 60 | DN | USB | I/O | DN pin of USB PHY |
| 61 | X32KO | RTC | AO | 32768Hz X'TAL output |
| 62 | X32KI | RTC | AI | 32768Hz X'TAL input |
| 63 | V18_RTC | RTC | P | RTC power output if V50_LDO is provided.<br>RTC power input if V50_LDO is not provided. |
| 64 | V33_PLL | PLL | P | 3.3V PLL power input |

### 4.1. Pin Map

Package Pin Sequence – LQFP64 Package Top View



# 5. FUNCTIONAL DESCRIPTIONS

## 5.1. CPU

GPL95101UA equips a 16-bit *μ'nSP*™ 2.0 CPU with sixteen registers: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose registers). The interrupt includes three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. GPL95101UA is also built-in an 8K bytes I-cache which can increase the performance significantly.

## 5.2. Memory

### 5.2.1. Internal SRAM

The amount of SRAM is 10K-word (including stack), ranged from 0x0000 through 0x27FF with access speed of one CPU clock. Since this SRAM is located in CPU's local bus, the system bus will not be occupied when the SRAM is accessed by CPU. It can be accessed by CPU/PPU/DMA /LCD.

### 5.2.2. SPI FLASH memory

The memory space of SPI FLASH is from 0x9000 and it is linear mapping, the range is dependent on the density of the external SPI FLASH. Other bus masters such as PPU, SPU and DMA can access SPI FLASH directly. Both 2-IO and 4-IO mode are supported to enhance system performance. The controller is configurable for various SPI FLASH providers with different timing formats. The maximum SPI FLASH clock is up to 96MHz (PCB dependent).

## 5.3. PLL, Clock, Power Mode

### 5.3.1. PLL (Phase Lock Loop)

An internal 8MHz oscillator and a 96MHz PLL are embedded in GPL95101UA.

### 5.3.2. System clock

Several system clock options are available via registers settings: 32768Hz, 8MHz, or 96MHz. (determined by fast PLL's output frequency). Furthermore, a clock divider which can divide clock up to 1/128 is provided to reduce the power consumption.

## 5.4. Power Savings Mode

The GPL95101UA has four power management modes: Operating, Deep Halt, Wait, and Halt.

| Mode | CPU | System | RTC | POWEREN | After wakeup |
|---|---|---|---|---|---|
| Operating | ON | ON | ON | ON | - |
| Deep Halt | OFF* | OFF* | ON | OFF* | Reset System |
| Wait | OFF | ON | ON | ON | Next Instruction |
| Halt | OFF | OFF | ON | ON | Next Instruction |

*OFF: In Deep Halt mode, OFF is power off; in other modes, OFF means clock off.

Entering Deep Halt/Wait/Halt mode is implemented by writing a specific value to a designated port. The wakeup source can be a key-change or RTC wakeup.

## 5.5. Picture Process Unit

GPL95101UA also outfits a powerful processing engine, PPU, which has the following features.

| Item | Features |
|---|---|
| Text Layer | 1. Maximum of three text layers at the same time<br>2. Supports text size up to 1024x1024.<br>3. Supports Text scale effect.<br>4. Text1 and text2 support horizontal/ vertical compression effect.<br>5. Supports horizontal movement effect.<br>6. Supports 64-level alpha blending. |
| Sprite | 1. Maximum 256 sprites at the same time<br>2. Each sprite supports 64-level rotate function.<br>3. Each sprite supports 64-level zoom in/ zoom out function from 1/32 to 8.75 times.<br>4. Each sprite supports 64-level alpha blending effect.<br>5. Each sprite supports three types of mosaic effect.<br>6. All above functions can involve at the same time. |
| Color | 1. Text layer and sprites support 4/16/64/256-color palette and RGB1555/ RGB565/ YUYV/ RGBG bitmap mode.<br>2. 1024 palette entrances for text layers and sprites.<br>3. Supports 16-bit level of palette index color. |
| Other Features | Supports sprite DMA function. |

## 5.6. Sound Process Unit

GPL95101UA equips a 16-channel SPU. Each channel of SPU supports PCM8/ PCM16/ ADPCM36. For software application, GPL95101UA also supports wide-band (sample rate >= 16KHz) low bit rate algorithm.

### 5.7. Video Output Interface

#### 5.7.1. STN-LCD Interface

The STN-LCD driver interface supports LCD resolution up to 320 x 240 and 1/4-bit data bus for monochrome/gray-scale STN. Memory interface type CSTN is also supported.

#### 5.7.2. TFT-LCD Interface

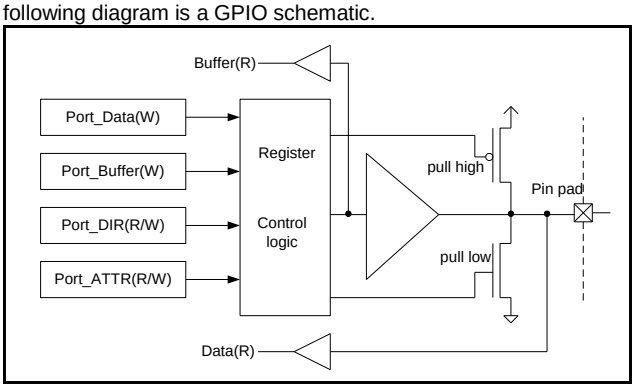
GPL95101UA supports TFT-LCD controller. The LCM interface includes parallel RGB (5-6-5), serial delta RGB, serial stripe RGB, CPU (MPU) type, and CCIR601/CCIR656. The horizontal resolution of TFT controller can reach 320 pixels, and the vertical resolution of TFT controller is up to 240 pixels. The TFT controller mainly provides four timing control pins and 8 or 16 data pins to control external TFT panel. Those are VSYNC, HSYNC, DE, DCLK, and DATA.

### 5.8. Interrupt

GPL95101UA has 29 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt and IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt source can be programmed as FIQ or IRQ by register settings.

### 5.9. GPIO

Five I/O ports are available in GPL95101UA: IOA, IOB, IOD, IOE, and IOF. IOA and IOB provide high current sink capability for LED applications. IOE shares with ADC, and IOF shares with touch pads. Each I/O pin has its normal function and is described in the signal description section. When an I/O's normal function is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.




### 5.10. Timer / Counter

GPL95101UA provides eight 16-bit timers/counters, TimerA to TimerH. The clock source of each timer can be set individually. For TimerA to TimerH, an INT will be sent to CPU when timer overflows. Besides, BAM, Capture, Comparison and PWM functions are also provided by TimerA ~ TimerF.

| Clock Source A | Clock Source B |
|---|---|
| Fosc/2 | 2048Hz |
| Fosc/256 | 1024Hz |
| 32768Hz | 256Hz |
| 8192Hz | Time Base B |
| 4096Hz | Time Base A |
| 1 | 0 |
| Another Timer | 1 |
| INT1 | INT2 |

The GPL95101UA features a time base controller which is used to generate a slow and precise interrupt from 32768Hz crystal. The following table shows available timebases.

| TimeBase A | TimeBase B | TimeBase C |
|---|---|---|
| -- | 8Hz | 128Hz |
| 1Hz | 16Hz | 256Hz |
| 2Hz | 32Hz | 512Hz |
| 4Hz | 64Hz | 1024Hz |

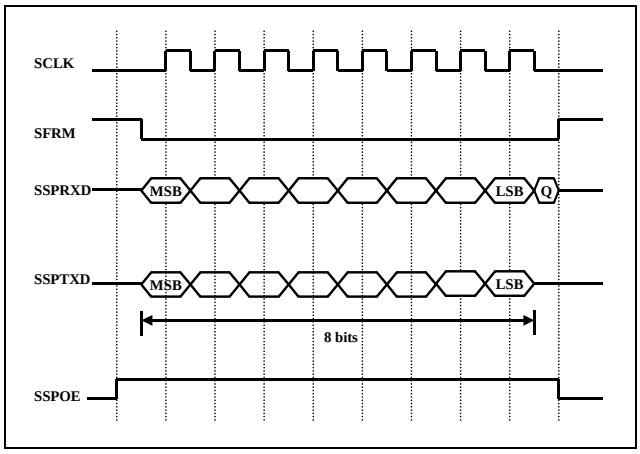
### 5.11. Watchdog

The purpose of watchdog is to monitor whether the system operates normally. Within a specific period, watchdog must be cleared. If not, CPU assumes program has been running into an abnormal condition. As a result, CPU will reset the system to the initial state and start running the program all over again. In GPL95101UA, the clearance period is software programmable. If watchdog is cleared before expiration, the system will not be reset.

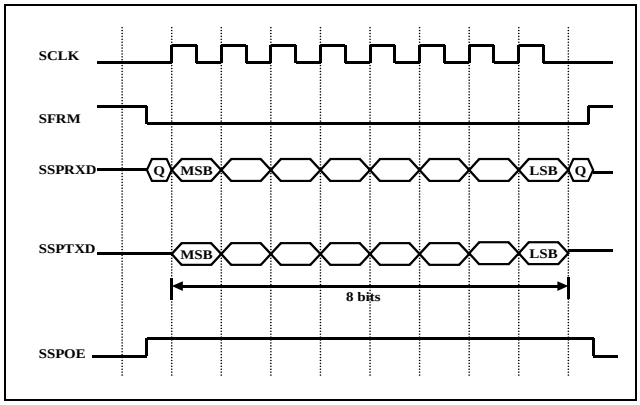
### 5.12. Serial Interface

#### 5.12.1. Serial Peripheral Interface (SPI)

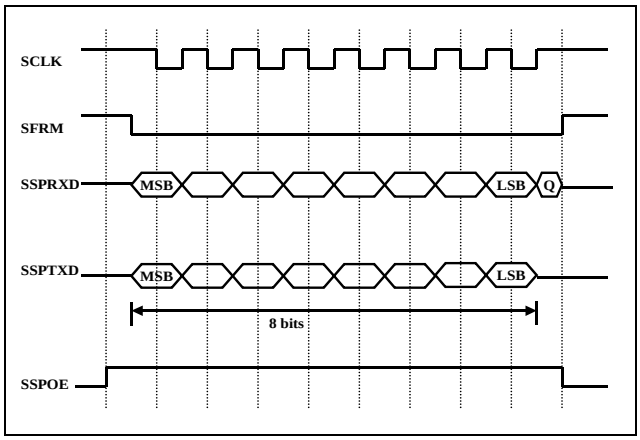
The SPI interface is a master interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timing waveforms are supported and shown in the following diagram.



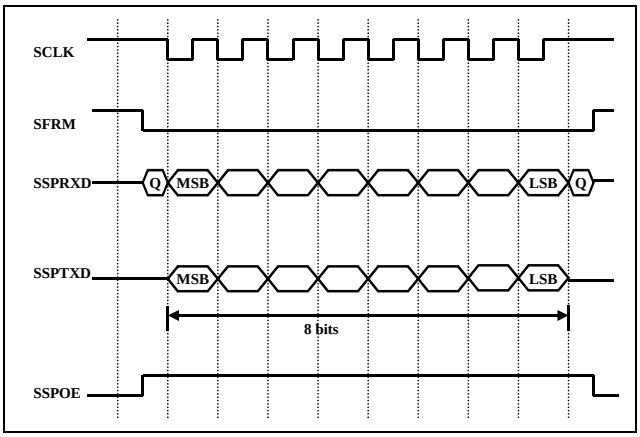

SPO = 0, SPH = 0




SPO = 0, SPH = 1




SPO = 1, SPH = 0




SPO = 1, SPH = 1

### 5.12.2. USB Device Function

GPL95101UA also features USB function which is compatible with USB 1.1 and USB 2.0 full speed standard. A FIFO with size of 128x8 is used for bulk-in and bulk-out transmission and an 8-byte FIFO is used for pipe transmission control. Interrupt IN/OUT pipes are also supported. The DMA transferring is enabled for bulk-in/out to maximize the transmission performance.

## 5.13. IDE Tools Function

The IDE includes the following functions:

1) C compiler, Assembler, and Linker
2) Single step trace
3) Break point (break point for debug)
4) Run (execution)

## 5.14. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

## 5.15. Analog Control

### 5.15.1. DAC/AMP control

A 16-bit stereo DAC (2ch) is embedded in GPL95101UA. For both left and right channels, a 16x16 FIFO is used to avoid sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can use the stereo playback and a push-pull AMP is built in for speaker applications.

## 6. ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Rating

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage 1 | V33_DVCC<br>V33_IOF<br>V33_PLL<br>V33_ADC<br>V33_USB | -0.3 to 4.0 | V |
| Supply Voltage 2 | V18_DVCC<br>V18_RTC | -0.3 to 2.16 | V |
| Supply Voltage 3 | V50_IOAB<br>V50_DAC<br>V50_AMP<br>V50_LDO | -0.3 to 5.5 | V |
| Input Voltage | $V_{IN}$ | -0.3 to 4.0 | V |
| Operating Temperature | $T_A$ | 0 to 70 | ℃ |
| Storage Temperature | $T_{STG}$ | -40 to +150 | ℃ |

### 6.2. DC Characteristics

| Characteristic | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage 1 | V33_DVCC<br>V33_IOF<br>V33_PLL<br>V33_ADC<br>V33_USB | 2.7<br>3.0[1] | 3.3 | 3.6 | V | - |
| Operating Voltage 2 | V18_DVCC<br>V18_RTC | 1.62 | 1.8 | 1.98 | V | - |
| Operating Voltage 3 | V50_IOAB<br>V50_DAC<br>V50_AMP<br>V50_LDO | 2.9<br>3.3 | 3.6 | 5.5 | V | - |
| Operating Current | $I_{OP}$ | - | 55[2] | - | mA | @96MHz, 3.3V, all clocks on |
| Deep Halt mode Current | $I_{PD}$ | - | 5 | 25 | μA | All power off except RTC |
| Halt mode Current | $I_{HALT}$ | - | 40 | 85 | μA | 3.3V, system clock off, Internal Power on, RTC ON |
| High Input Voltage | $V_{IH}$ | 0.7*Vsource[3] | - | Vsource[3] | V | - |
| Low Input Voltage | $V_{IL}$ | VSS | - | 0.8 | V | - |
| Output High/Low Current (I/O) | $I_{OH}$ | - | 4[4] | - | mA | IO is 3.3V, VOH=0.7*VDDIO and IO driving set as 4mA. |
| | $I_{OL}$ | - | 7[4] | - | mA | IO is 3.3V, VOL=0.3*VDDIO and IO driving set as 4mA. |
| IO Input Pull-Low Resistor | $R_{PL}$ | - | 95K | - | OHM | IO 3.3V on PA/PB/PD/PE/PF<br>IO 4.5V on PD/PE/PF |
| | $R_{PL}$ | - | 70K | - | OHM | IO 4.5V on PA/PB |
| IO Input Pull-High | $R_{PH}$ | - | 95K | - | OHM | IO 3.3V on PA/PB/PD/PE/PF |

| Characteristic | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resistor | | | | | | IO 4.5V on PD/PE/PF |
| | $R_{PH}$ | - | 70K | - | - | IO 4.5V on PA/PB |
| Crystal Frequency | - | - | 32768 | - | Hz | - |
| System Clock | $F_{SYS}$ | 256Hz | 48 | 96 | MHz | - |

**Note1:** When USB function is enabled, the minimum voltage of operation voltage 1 is 3.0V, and 3.3V for operating voltage 3.

**Note2:** Operating current depends on software code. In this test case, all clocks are on and system is in idle mode.

**Note3:** Vsource may be V33_DVCC, V33_IOF, V33_ADC or V50_IOAB.

**Note4:** IO driving can be setup by program. There are 4mA/8mA/12mA/16mA can be setup and default driving is 4mA.

### 6.3. Audio DAC Characteristics

| Characteristic | Limits | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Resolution | - | 16 | - | Bit | - |
| Full Scale Output Voltage | - | 0.6*VDDDA | - | Vp-p | - |
| THD+N (f = 1kHz) | - | 0.1 | - | % | - |
| Noise at No Signal | - | 90 | - | dBrA | - |
| Frequency Response | 20 | - | 19200 | Hz | - |

### 6.4. SAR ADC Characteristics

| Characteristics | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SAR ADC Input Voltage Range | VIN_RANGE | 2.7 | - | 3.6 | V |
| Resolution of ADC | RESO | 12 | 12 | 12 | bit |
| Signal-to-Noise Plus Distortion of ADC from Line in | SINAD (Note 1) | 58 | 60 | 62 | dB |
| Effective Number of Bit | ENOB (Note 2) | 9.0 | 9.66 | 10 | bit |
| Integral Non-Linearity of ADC | INL | - | +/-3 | - | LSB (Note 3) |
| Differential Non-Linearity of ADC | DNL | - | +/-2 | - | LSB |
| No Missing Code | | 10 | 11 | 12 | bit |
| AD Conversion Rate=ADCCLK/16 | $F_{CONV}$ | - | - | 125K | Hz |

**Note1:** The SINAD testing condition at VINLp-p = 0.8 * V33_AD, $F_{CONV}$ = 62.5KHz, Fin = 1.0KHz Sine waves at V33_AD = 3.0V from ADC input.

**Note2:** ENOB = (SINAD - 1.76) / 6.02.

**Note3:** LSB means Least Significant Bit (at 12-bit resolution).

### 6.5. LDO18 Characteristics

| Characteristics | Symbol | Unit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Input Voltage | VREGI | 2.7 | 3.3 | 3.6 | V |
| Maximum Current Output | IREGO | - | 140 | 280 | mA |
| Output Voltage | VREGO | 1.33[1] | 1.8 | 1.995 | V |
| Standby Current | IREGS | - | 3 | - | uA |

**Note1:** To save more power, it is recommended switching to 1.4V before entering the halt mode and switching to 1.8V in normal operation mode.

### 6.6. LDO33 Characteristics

| Characteristics | Symbol | Unit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Input Voltage | VREGI | 2.9 | 3.6 | 5.5 | V |
| Maximum Current Output | IREGO | - | 350 | 700 | mA |
| Output Voltage | VREGO | 2.85 | 3.3 | 3.465 | V |
| Standby Current | IREGS | - | 3 | - | uA |

## 7. RECOMMENDED BOARD LAYOUT

### 7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin as the following diagram. The power of analog parts should be connected from power source with high quality.

### 7.2. Analog Section

A specific AGND ground plane, connected by a single trace to the GND ground, should be provided. No digital signal should cross the AGND plane. AVREF_ADC should be connected to a 1μF capacitor.

## 8. ORDERING INFORMATION

### 8.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPL95101UA - NnnV – QL24x | Halogen Free Package |

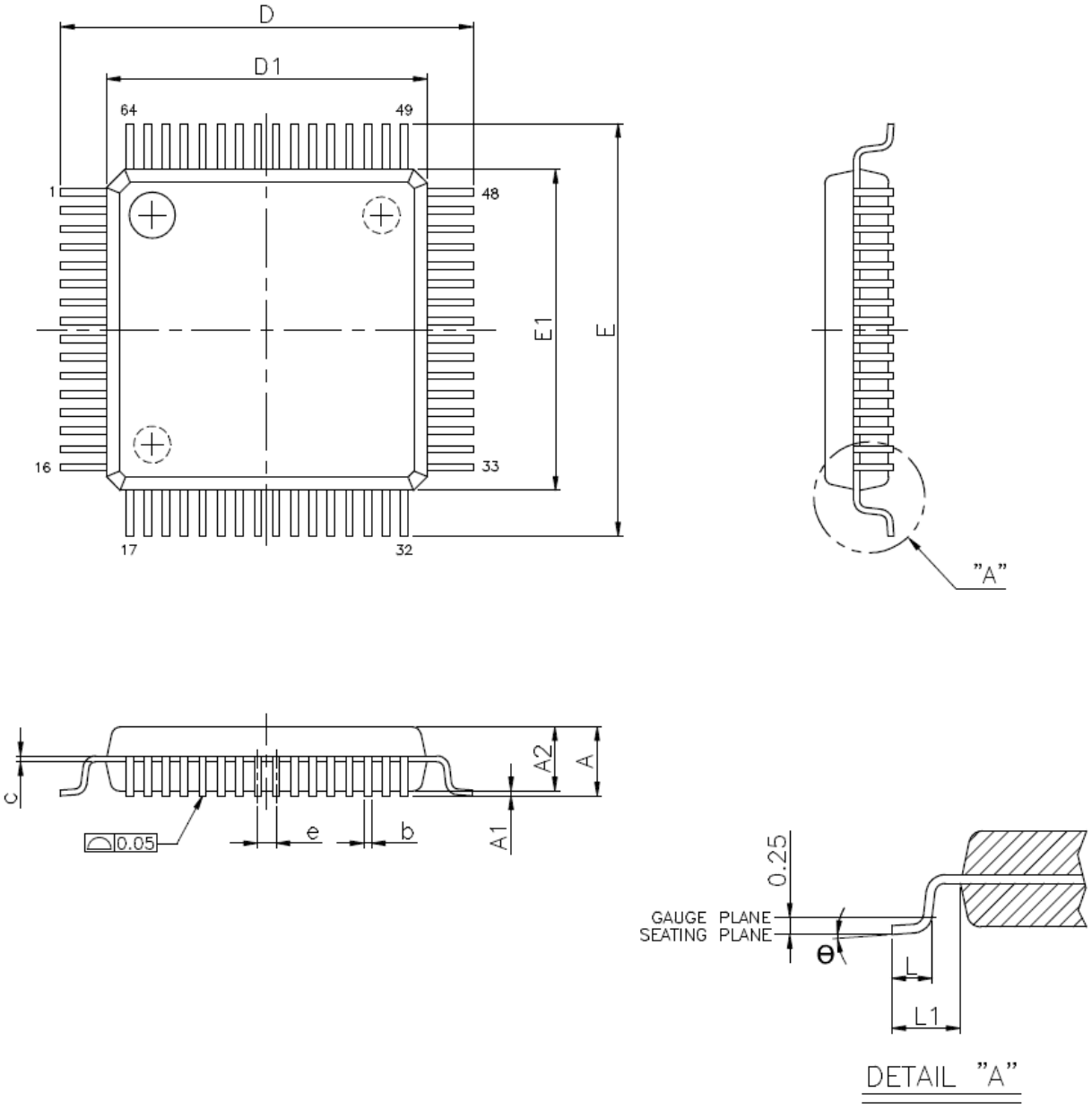
**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

**Note3:** Package form number (x = 1 - 9, serial number).

### 8.2. Package Information

LQFP 64




| Symbols | Min. | Nom. | Max. |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |

| Symbols | Min. | Nom. | Max. |
|---|---|---|---|
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.13 | 0.18 | 0.23 |
| c | 0.09 | - | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| e | 0.40 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| $\theta$ | 0° | 3.5° | 7° |

**Notes:**

1. JEDEC Outline: MS-026 BCD
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

## 9. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

## 10. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| Jan. 16, 2019 | 1.0 | 1. Modify DAC descriptions | 4 |
| | | 2. Modify 8 timers for PWM to 6 timers for PWM | 4 |
| | | 3. Modify PWR_ON descriptions in “SIGNAL DESCRIPTION” | 5 |
| | | 4. Modify Audio DAC Characteristics | 13 |
| | | 5. Add SAR ADC Characteristics | 13 |
| Oct. 05, 2016 | 0.1 | Preliminary version. | 18 |