

# Gabriel McTeer & Shaelynn Nixon

## Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

### Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

### Lab Summary

Summarize your learnings from the lab here.

### Lab Questions

#### 1 - Describe the stages of building a Verilog project in Vivado.

In the Verilog software, choose the create project option in the Quick Start section. Give a name for the project and save it on your pc. Then select RTL as the project type and add in your files. For this class test.v and top.v were the files to be added. Change the HDL Source For simulation only in test.v as well as synthesis and simulation for top.v. A constraint file can be added before choosing a board for the project. Finally install the board, Basys3 is the one used in this lab, then view the project summary and hit finish.

#### 2 - What is the value in looking at the elaborated design schematic?

The elaborated design schematic in Vivado gives us an image of our circuit as we previously described. However, this is before the FPGA hardware is introduced. It's basically giving us an overview of the wires, constant values, modules, logic, bit widths, etc of the design before

implementing the hardware. The value in this is that it can help us find errors like incorrect connections or signal widths.

### 3 - Why should we simulate our designs frequently? What does the simulation do?

We should simulate our designs frequently to make sure it does what we originally expected it to do. Also, the more simulations we run the easier it is to discover and resolve bugs. If the circuit simulates properly then we can be confident in programming the hardware. The simulation showed us that our switch and LED will turn on at approximately 200 ns.

## Code Submission

Upload a .zip of all your code or a public repository on GitHub.