Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B1	VREFB1N0	IO	ASDO	ASDO	1	1	C3					
B1	VREFB1N0	IO	nCSO	nCSO	2	2	F4					
B1	VREFB1N0	IO	LVDS15p	CRC_ERROR	3	3	C1					
B1	VREFB1N0	IO	LVDS15n	CLKUSR	4	4	C2					
B1	VREFB1N0	IO	LVDS14p				5	D5					
B1	VREFB1N0	IO	LVDS14n				6	E5					
B1	VREFB1N0	VCCIO1			5	7						
B1	VREFB1N0	IO	LVDS13p				8	F5		DQ1L0			
B1	VREFB1N0	GND			6	9						
B1	VREFB1N0	IO	LVDS13n			10			DQ1L1			
B1	VREFB1N0	IO	LVDS12p			11	D3		DQ1L2		DQ0L0	DQ1L0
B1	VREFB1N0	IO	LVDS12n			12	D4		DQ1L3		DQ0L1	DQ1L1
B1	VREFB1N0	VCCIO1										
B1	VREFB1N0	IO	VREFB1N0		7	13	F3					
B1	VREFB1N0	IO	LVDS11p				D2					
B1	VREFB1N0	IO	LVDS11n				D1				DQ0L2	DQ1L2
B1	VREFB1N0	IO	LVDS10p				E3				DQ0L3	DQ1L3
B1	VREFB1N0	IO	LVDS10n				E4				DQ0L4	DQ1L4
B1	VREFB1N0	GND										
B1	VREFB1N0	IO					G4					
B1	VREFB1N0	IO	LVDS9p				J6					
B1	VREFB1N0	IO	LVDS9n				H6					
B1	VREFB1N0	IO	LVDS8p		8	14	E1	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L
B1	VREFB1N0	IO	LVDS8n		9	15	E2				DQ0L5	DQ1L5
B1	VREFB1N0	VCCIO1										
B1	VREFB1N0	TDO		TDO	10	16	G2					
B1	VREFB1N0	TMS		TMS	11	17	G1					
B1	VREFB1N0	TCK		TCK	12	18	F2					
B1	VREFB1N0	TDI		TDI	13	19	H5					
B1	VREFB1N0	DATA0	DATA0	DATA0	14	20	F1					
B1	VREFB1N0	DCLK	DCLK	DCLK	15	21	H4					
B1	VREFB1N0	nCE		nCE	16	22	G5					
B1	VREFB1N0	CLK0	LVDSCLK0p/input(3)		17	23	H2					
B1	VREFB1N0	CLK1	LVDSCLK0n/input(3)		18	24	H1					
B1	VREFB1N0	GND			19	25						
B1	VREFB1N0	nCONFIG		nCONFIG	20	26	J5					
B1	VREFB1N1	CLK2	LVDSCLK1p/input(3)		21	27	J2					
B1	VREFB1N1	CLK3	LVDSCLK1n/input(3)		22	28	J1					
B1	VREFB1N1	VCCIO1			23	29						
B1	VREFB1N1	IO	LVDS7p		24	30	K2	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L

PT-EP2C8-1.5

EP2C8 Pin List

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B1	VREFB1N1	IO	LVDS7n		25	31	K1				DQ0L6	DQ1L6
B1	VREFB1N1	IO	LVDS6p				K4				DQ0L7	DQ1L7
B1	VREFB1N1	VCCINT			26	32						
B1	VREFB1N1	IO	LVDS6n			33	K5		DQ1L4			DQ1L8
B1	VREFB1N1	IO				34			DQ1L5			
B1	VREFB1N1	IO	LVDS5p			35	L1		DQ1L6		DM0L	DM1L0/BWS#1L0
B1	VREFB1N1	GND			27	36						
B1	VREFB1N1	IO	LVDS5n				L2				DQ1L0	DQ1L9
B1	VREFB1N1	GND										
B1	VREFB1N1	IO	VREFB1N1		28	37	J4					
B1	VREFB1N1	VCCIO1										
B1	VREFB1N1	IO	LVDS4p				M1					
B1	VREFB1N1	IO	LVDS4n				M2				DQ1L1	DQ1L10
B1	VREFB1N1	IO	LVDS3p				M3				DQ1L2	DQ1L11
B1	VREFB1N1	GND				38						
B1	VREFB1N1	IO	LVDS3n			39	L3		DQ1L7			
B1	VREFB1N1	IO	LVDS2p			40	N1		DQ1L8		DQ1L3	DQ1L12
B1	VREFB1N1	IO	LVDS2n			41	N2		DM1L/BWS#1L		DQ1L4	DQ1L13
B1	VREFB1N1	IO	LVDS1p				P1				DQ1L5	DQ1L14
B1	VREFB1N1	IO	LVDS1n				P2				DQ1L6	DQ1L15
B1	VREFB1N1	VCCIO1			29	42						
B1	VREFB1N1	IO				43						
B1	VREFB1N1	IO	LVDS0p			44	N3				DQ1L7	DQ1L16
B1	VREFB1N1	IO	LVDS0n			45	N4				DQ1L8	DQ1L17
B1	VREFB1N1	IO			30	46	P3				DM1L/BWS#1L	DM1L1/BWS#1L1
B1	VREFB1N1	IO	PLL1_OUTp		31	47	L4					
B1	VREFB1N1	IO	PLL1_OUTn		32	48	M4					
B1	VREFB1N1	GND			33	49						
B1	VREFB1N1	GND_PLL1			34	50	L5					
B1	VREFB1N1	VCCD_PLL1			35	51	L6					
B1	VREFB1N1	GND_PLL1			36	52	N5					
B4	VREFB4N1	VCCA_PLL1			37	53	M5					
B4	VREFB4N1	GNDA_PLL1			38	54	M6					
B4	VREFB4N1	GND			39	55						
B4	VREFB4N1	IO	LVDS77n	DEV_OE	40	56	R3					
B4	VREFB4N1	IO	LVDS77p		41	57	T3	DM1B/BWS#1B	DM1B/BWS#1B	DM1B1/BWS#1B1	DM1B/BWS#1B	DM1B1/BWS#1B1
B4	VREFB4N1	IO	LVDS76p		42	58	P5	DQ1B8	DQ1B8	DQ1B17	DQ1B8	DQ1B17
B4	VREFB4N1	IO	LVDS76n		43	59	P4	DQ1B7	DQ1B7	DQ1B16	DQ1B7	DQ1B16
B4	VREFB4N1	IO	LVDS75p		44	60	T4	DQ1B6	DQ1B6	DQ1B15	DQ1B6	DQ1B15
B4	VREFB4N1	IO	LVDS75n		45	61	R4	DQ1B5	DQ1B5	DQ1B14	DQ1B5	DQ1B14

PT-EP2C8-1.5

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B4	VREFB4N1	VCCIO4			46	62						
B4	VREFB4N1	IO	LVDS74p		47	63	T5	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B	DPCLK2/DQS1B
B4	VREFB4N1	GND										
B4	VREFB4N1	IO	LVDS74n		48	64	R5				DQ1B4	DQ1B13
B4	VREFB4N1	IO					N7					
B4	VREFB4N1	IO	LVDS73p				K7					
B4	VREFB4N1	IO	LVDS73n				K6					
B4	VREFB4N1	VCCIO4										
B4	VREFB4N1	GND										
B4	VREFB4N1	IO	LVDS72p				T6					
B4	VREFB4N1	GND			49	65						
B4	VREFB4N1	IO	LVDS72n				R6					
B4	VREFB4N1	IO	LVDS71p				P6				DQ1B3	DQ1B12
B4	VREFB4N1	IO	LVDS71n				N6				DQ1B2	DQ1B11
B4	VREFB4N1	VCCINT			50	66						
B4	VREFB4N1	IO	VREFB4N1		51	67	N8					
B4	VREFB4N1	VCCIO4										
B4	VREFB4N1	GND										
B4	VREFB4N1	IO	LVDS70p		52	68	T7	DQ1B4	DQ1B4	DQ1B13	DQ1B1	DQ1B10
B4	VREFB4N1	IO	LVDS70n			69	R7		DQ1B3	DQ1B12	DQ1B0	DQ1B9
B4	VREFB4N1	IO	LVDS69p				L7					
B4	VREFB4N1	IO	LVDS69n				L8					
B4	VREFB4N1	IO	LVDS68p		53	70	T8	DQ1B3	DQ1B2	DQ1B11		
B4	VREFB4N1	VCCIO4			54	71						
B4	VREFB4N1	IO	LVDS68n		55	72	R8	DQ1B2	DQ1B1	DQ1B10		DM1B0/BWS#1B0
B4	VREFB4N1	GND			56	73						
B4	VREFB4N1	IO	LVDS67p		57	74	T9	DQ1B1	DQ1B0	DQ1B9		
B4	VREFB4N1	IO	LVDS67n		58	75	R9	DQ1B0				
B4	VREFB4N0	IO	LVDS66p		59	76	N9					
B4	VREFB4N0	IO	LVDS66n		60	77	N10					
B4	VREFB4N0	GND			61	78						
B4	VREFB4N0	IO	LVDS65p				T11					
B4	VREFB4N0	VCCINT			62	79						
B4	VREFB4N0	IO	LVDS65n				R11				DM0B	DQ1B8
B4	VREFB4N0	VCCIO4										
B4	VREFB4N0	IO				80	P11					
B4	VREFB4N0	GND										
B4	VREFB4N0	IO	LVDS64p			81	L9					
B4	VREFB4N0	IO	LVDS64n			82	L10					
B4	VREFB4N0	VCCIO4				83						

PT-EP2C8-1.5

EP2C8 Pin List

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B4	VREFB4N0	IO	LVDS63p			84	R10		DM0B	DM1B0/BWS#1B0		
B4	VREFB4N0	GND				85						
B4	VREFB4N0	IO	LVDS63n			86	T10			DQ1B8	DQ0B7	DQ1B7
B4	VREFB4N0	IO	LVDS62p			87	K11		DQ0B7	DQ1B7		
B4	VREFB4N0	IO	LVDS62n			88	K10		DQ0B6	DQ1B6		
B4	VREFB4N0	IO	VREFB4N0		63	89	N11					
B4	VREFB4N0	IO	LVDS61p			90	P12		DQ0B5	DQ1B5	DQ0B6	DQ1B6
B4	VREFB4N0	VCCIO4				91						
B4	VREFB4N0	IO	LVDS61n			92	P13		DQ0B4	DQ1B4	DQ0B5	DQ1B5
B4	VREFB4N0	GND				93						
B4	VREFB4N0	IO	LVDS60p		64	94	T12	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B	DPCLK4/DQS0B
B4	VREFB4N0	IO	LVDS60n		65	95	R12				DQ0B4	DQ1B4
B4	VREFB4N0	IO				96			DQ0B3	DQ1B3		
B4	VREFB4N0	IO	LVDS59p			97	T13		DQ0B2	DQ1B2	DQ0B3	DQ1B3
B4	VREFB4N0	VCCIO4			66	98						
B4	VREFB4N0	IO	LVDS59n		67	99	R13		DQ0B1	DQ1B1	DQ0B2	DQ1B2
B4	VREFB4N0	GND			68	100						
B4	VREFB4N0	IO	LVDS58p		69	101	T14		DQ0B0	DQ1B0	DQ0B1	DQ1B1
B4	VREFB4N0	IO	LVDS58n		70	102	R14				DQ0B0	DQ1B0
B4	VREFB4N0	IO	LVDS57p		71	103	M11					
B4	VREFB4N0	IO	LVDS57n		72	104	L11					
B3	VREFB3N1	IO	LVDS56n		73	105	N12	DM1R/BWS#1R				
B3	VREFB3N1	IO	LVDS56p		74	106	M12	DQ1R8	DM1R/BWS#1R	DM1R1/BWS#1R1		
B3	VREFB3N1	IO	LVDS55n				L12					
B3	VREFB3N1	IO	LVDS55p				K13					
B3	VREFB3N1	IO	LVDS54n	INIT_DONE	75	107	N13					
B3	VREFB3N1	IO	LVDS54p	nCEO	76	108	N14					
B3	VREFB3N1	VCCIO3			77	109						
B3	VREFB3N1	IO	LVDS53n			110	P15		DQ1R8	DQ1R17	DM1R/BWS#1R	DM1R1/BWS#1R1
B3	VREFB3N1	GND			78	111						
B3	VREFB3N1	IO	LVDS53p			112	P16		DQ1R7	DQ1R16	DQ1R8	DQ1R17
B3	VREFB3N1	IO	LVDS52n			113	N15		DQ1R6	DQ1R15	DQ1R7	DQ1R16
B3	VREFB3N1	IO	LVDS52p			114	N16		DQ1R5	DQ1R14	DQ1R6	DQ1R15
B3	VREFB3N1	IO					P14				DQ1R5	DQ1R14
B3	VREFB3N1	IO	LVDS51n			115			DQ1R4	DQ1R13		
B3	VREFB3N1	IO	LVDS51p			116			DQ1R3	DQ1R12		
B3	VREFB3N1	IO	VREFB3N1		79	117	M14					
B3	VREFB3N1	IO	LVDS50n				M15				DQ1R4	DQ1R13
B3	VREFB3N1	VCCIO3										
B3	VREFB3N1	IO	LVDS50p				M16					

PT-EP2C8-1.5

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B3	VREFB3N1	GND										
B3	VREFB3N1	IO				118			DQ1R2	DQ1R11		
B3	VREFB3N1	GND			80	119						
B3	VREFB3N1	IO					L14					
B3	VREFB3N1	IO	LVDS49n				L15				DQ1R3	DQ1R12
B3	VREFB3N1	IO	LVDS49p				L16				DQ1R2	DQ1R11
B3	VREFB3N1	VCCINT			81	120						
B3	VREFB3N1	nSTATUS		nSTATUS	82	121	M13					
B3	VREFB3N1	VCCIO3				122						
B3	VREFB3N1	CONF_DONE		CONF_DONE	83	123	L13					
B3	VREFB3N1	GND				124						
B3	VREFB3N1	MSEL1		MSEL1	84	125	K12					
B3	VREFB3N1	MSEL0		MSEL0	85	126	J13					
B3	VREFB3N1	IO	LVDS48n		86	127	K16	DQ1R7	DQ1R1	DQ1R10	DQ1R1	DQ1R10
B3	VREFB3N1	IO	LVDS48p		87	128	K15	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R
B3	VREFB3N1	CLK7	LVDSCLK3n/input(3)		88	129	J16					
B3	VREFB3N1	CLK6	LVDSCLK3p/input(3)		89	130	J15					
B3	VREFB3N0	CLK5	LVDSCLK2n/input(3)		90	131	H15					
B3	VREFB3N0	CLK4	LVDSCLK2p/input(3)		91	132	H16					
B3	VREFB3N0	IO	LVDS47n		92	133	H12	DQ1R6	DQ1R0	DQ1R9	DQ1R0	DQ1R9
B3	VREFB3N0	IO	LVDS47p		93	134	J12	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R
B3	VREFB3N0	IO	LVDS46n		94	135	G16	DQ1R5	DM0R	DM1R0/BWS#1R0	DM0R	DM1R0/BWS#1R0
B3	VREFB3N0	VCCIO3			95	136						
B3	VREFB3N0	IO	LVDS46p		96	137	G15	DQ1R4		DQ1R8		DQ1R8
B3	VREFB3N0	IO	LVDS45n		97	138	F15	DQ1R3	DQ0R7	DQ1R7	DQ0R7	DQ1R7
B3	VREFB3N0	IO	LVDS45p			139	F16		DQ0R6	DQ1R6	DQ0R6	DQ1R6
B3	VREFB3N0	GND			98	140						
B3	VREFB3N0	IO	LVDS44n			141	J11		DQ0R5	DQ1R5		
B3	VREFB3N0	IO	LVDS44p			142	H11		DQ0R4	DQ1R4		
B3	VREFB3N0	IO	LVDS43n				G12				DQ0R5	DQ1R5
B3	VREFB3N0	IO	LVDS43p				G13				DQ0R4	DQ1R4
B3	VREFB3N0	IO	LVDS42n			143	E13		DQ0R3	DQ1R3	DQ0R3	DQ1R3
B3	VREFB3N0	IO	LVDS42p			144	F13		DQ0R2	DQ1R2	DQ0R2	DQ1R2
B3	VREFB3N0	IO	VREFB3N0		99	145	H13					
B3	VREFB3N0	VCCIO3										
B3	VREFB3N0	IO	LVDS41n				D15					
B3	VREFB3N0	IO	LVDS41p				D16					
B3	VREFB3N0	IO	LVDS40n				E15				DQ0R1	DQ1R1
B3	VREFB3N0	GND										
B3	VREFB3N0	IO	LVDS40p				E16				DQ0R0	DQ1R0

PT-EP2C8-1.5

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B3	VREFB3N0	IO					F14					
B3	VREFB3N0	IO	LVDS39n		100	146	C15	DQ1R2	DQ0R1	DQ1R1		
B3	VREFB3N0	IO	LVDS39p		101	147	C16	DQ1R1	DQ0R0	DQ1R0		
B3	VREFB3N0	VCCIO3			102	148						
B3	VREFB3N0	IO	LVDS38n			149	C14					
B3	VREFB3N0	IO	LVDS38p			150	D13					
B3	VREFB3N0	IO	PLL2_OUTp		103	151	E14	DQ1R0				
B3	VREFB3N0	IO	PLL2_OUTn		104	152	D14					
B3	VREFB3N0	GND			105	153						
B3	VREFB3N0	GND_PLL2			106	154	F12					
B3	VREFB3N0	VCCD_PLL2			107	155	F11					
B3	VREFB3N0	GND_PLL2			108	156	D12					
B2	VREFB2N0	VCCA_PLL2			109	157	E12					
B2	VREFB2N0	GNDA_PLL2			110	158	E11					
B2	VREFB2N0	GND			111	159						
B2	VREFB2N0	IO	LVDS37n		112	160	B14					
B2	VREFB2N0	IO	LVDS37p		113	161	A14		DQ0T0	DQ1T0	DQ0T0	DQ1T0
B2	VREFB2N0	IO	LVDS36n		114	162	C13		DQ0T1	DQ1T1	DQ0T1	DQ1T1
B2	VREFB2N0	IO	LVDS36p		115	163	C12		DQ0T2	DQ1T2	DQ0T2	DQ1T2
B2	VREFB2N0	IO	LVDS35n			164	B13		DQ0T3	DQ1T3	DQ0T3	DQ1T3
B2	VREFB2N0	IO	LVDS35p			165	A13		DQ0T4	DQ1T4	DQ0T4	DQ1T4
B2	VREFB2N0	VCCIO2			116	166						
B2	VREFB2N0	GND			117	167						
B2	VREFB2N0	IO	LVDS34n		118	168	B12				DQ0T5	DQ1T5
B2	VREFB2N0	IO	LVDS34p		119	169	A12	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T	DPCLK8/DQS0T
B2	VREFB2N0	IO	VREFB2N0		120	170	C11					
B2	VREFB2N0	IO	LVDS33n		121	171	B11		DQ0T5	DQ1T5	DQ0T6	DQ1T6
B2	VREFB2N0	VCCIO2				172						
B2	VREFB2N0	IO	LVDS33p		122	173	A11		DQ0T6	DQ1T6	DQ0T7	DQ1T7
B2	VREFB2N0	GND				174						
B2	VREFB2N0	IO	LVDS32n				G10					
B2	VREFB2N0	IO	LVDS32p				G11					
B2	VREFB2N0	IO	LVDS31n			175	B10		DQ0T7	DQ1T7		DQ1T8
B2	VREFB2N0	VCCIO2										
B2	VREFB2N0	IO	LVDS31p			176	A10				DQ1T8	
B2	VREFB2N0	GND										
B2	VREFB2N0	IO	LVDS30n				F10					
B2	VREFB2N0	IO	LVDS30p				F9					
B2	VREFB2N0	IO					D9					
B2	VREFB2N0	GND			123	177						

PT-EP2C8-1.5

EP2C8 Pin List

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B2	VREFB2N0	VCCINT			124	178						
B2	VREFB2N0	IO	LVDS29n		125	179	D11	DQ1T0	DM0T	DM1T0/BWS#1T0	DM0T	DM1T0/BWS#1T0
B2	VREFB2N0	VCCIO2										
B2	VREFB2N0	IO	LVDS29p		126	180	D10	DQ1T1				
B2	VREFB2N0	GND										
B2	VREFB2N0	IO				181	A9					
B2	VREFB2N0	IO				182	B9					
B2	VREFB2N1	IO	LVDS27n				A8					
B2	VREFB2N1	IO	LVDS27p				B8					
B2	VREFB2N1	VCCIO2			127	183						
B2	VREFB2N1	IO	LVDS26n				A7				DQ1T0	DQ1T9
B2	VREFB2N1	GND			128	184						
B2	VREFB2N1	IO	LVDS26p		129	185	B7	DQ1T2	DQ1T0	DQ1T9		
B2	VREFB2N1	GND			130	186						
B2	VREFB2N1	IO	LVDS25n			187	F7					
B2	VREFB2N1	IO	LVDS25p			188	F8		DQ1T1	DQ1T10		
B2	VREFB2N1	IO	LVDS24n			189			DQ1T2	DQ1T11		
B2	VREFB2N1	VCCINT			131	190						
B2	VREFB2N1	IO	LVDS24p			191			DQ1T3	DQ1T12		
B2	VREFB2N1	IO	VREFB2N1		132	192	D8					
B2	VREFB2N1	IO	LVDS23n		133	193	B6	DQ1T3	DQ1T4	DQ1T13	DQ1T1	DQ1T10
B2	VREFB2N1	VCCIO2				194						
B2	VREFB2N1	IO	LVDS23p		134	195	A6	DQ1T4	DQ1T5	DQ1T14		
B2	VREFB2N1	GND				196						
B2	VREFB2N1	IO	LVDS22n				G6					
B2	VREFB2N1	IO	LVDS22p				G7					
B2	VREFB2N1	IO					D7				DQ1T2	DQ1T11
B2	VREFB2N1	IO	LVDS21n			197	D6				DQ1T3	DQ1T12
B2	VREFB2N1	VCCIO2										
B2	VREFB2N1	IO	LVDS21p			198	C6				DQ1T4	DQ1T13
B2	VREFB2N1	GND										
B2	VREFB2N1	IO	LVDS20n				C5					
B2	VREFB2N1	IO	LVDS20p				C4				DQ1T5	DQ1T14
B2	VREFB2N1	IO	LVDS19n		135	199	B5	DQ1T5			DQ1T6	DQ1T15
B2	VREFB2N1	IO	LVDS19p		136	200	A5	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T	DPCLK10/DQS1T
B2	VREFB2N1	IO	LVDS18n		137	201	B4	DQ1T6	DQ1T6	DQ1T15	DQ1T7	DQ1T16
B2	VREFB2N1	VCCIO2			138	202						
B2	VREFB2N1	IO	LVDS18p		139	203	A4	DQ1T7	DQ1T7	DQ1T16	DQ1T8	DQ1T17
B2	VREFB2N1	GND			140	204						
B2	VREFB2N1	IO	LVDS17p		141	205	A3	DQ1T8	DQ1T8	DQ1T17	DM1T/BWS#1T	DM1T1/BWS#1T1

PT-EP2C8-1.5

EP2C8 Pin List

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
B2	VREFB2N1	IO	LVDS17n	DEV_CLRn	142	206	B3					
B2	VREFB2N1	IO	LVDS16p		143	207	E6	DM1T/BWS#1T	DM1T/BWS#1T	DM1T1/BWS#1T1		
B2	VREFB2N1	IO	LVDS16n		144	208	F6					
		VCCINT					G9					
		VCCINT					H7					
		VCCINT					H10					
		VCCINT					J7					
		VCCINT					J10					
		VCCINT					K8					
		VCCIO1					B1					
		VCCIO1					G3					
		VCCIO1					K3					
		VCCIO1					R1					
		VCCIO4					M7					
		VCCIO4					M10					
		VCCIO4					P7					
		VCCIO4					P10					
		VCCIO4					T2					
		VCCIO4					T15					
		VCCIO3					B16					
		VCCIO3					G14					
		VCCIO3					K14					
		VCCIO3					R16					
		VCCIO2					A2					
		VCCIO2					A15					
		VCCIO2					C7					
		VCCIO2					C10					
		VCCIO2					E7					
		VCCIO2					E10					
		GND					G8					
		GND					H8					
		GND					H9					
		GND					J8					
		GND					J9					
		GND					K9					
		GND					A1					
		GND					A16					
		GND					B2					
		GND					B15					
		GND					C8					

PT-EP2C8-1.5

EP2C8 Pin List

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	Q208	F256	DQS for x8/x9 in T144	DQS for x8/x9 in Q208	DQS for x16/x18 in Q208	DQS for x8/x9 in F256	DQS for x16/x18 in F256
		GND					C9					
		GND					E8					
		GND					E9					
		GND					H3					
		GND					H14					
		GND					J3					
		GND					J14					
		GND					M8					
		GND					M9					
		GND					P8					
		GND					P9					
		GND					R2					
		GND					R15					
		GND					T1					
		GND					T16					

Notes:

(1) Optional Functions (LVDS, DDR, etc) are not available for some pins in certain packages. E.g. for EP2C8, LVDS70 pair is available for package Q208 and F256 but not for T144.

They do not have support for an I/O register.

(2) DQS0T, DQS1T, DQS0B and DQS1B pin functions are only available in F672 and F896 packages.

(3) If the dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed core logic.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVPECL, LVDS, HSTL and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..4]N[0..1]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..4]	Power	Analog power for PLLs[1..4]. The designer must connect these pins to 1.2 V, even if the PLL is not used. Designer is advised to keep isolated from other VCC for better jitter performance.
VCCD_PLL[1..4]	Power	Digital power for PLLs[1..4]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1..4]	Ground	Analog ground for PLLs[1..4]. The designer can connect this pin to the GND plane on the board.
GND_PLL[1..4]	Ground	Ground for PLLs[1..4]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the Cyclone II device. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. DCLK should not be left floating. Designer should drive it high or low, whichever is more convenient on the board.
DATA0	Input	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active.
MSEL[0..1]	Input	Configuration input pins that set the Cyclone II device configuration scheme. These pins must be hard-wired to VCCPD or GND. The designer should connect MSEL[0..1] to 00 for AS, 10 for PS, 01 for Fast AS and 00 for JTAG-based Configuration.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.

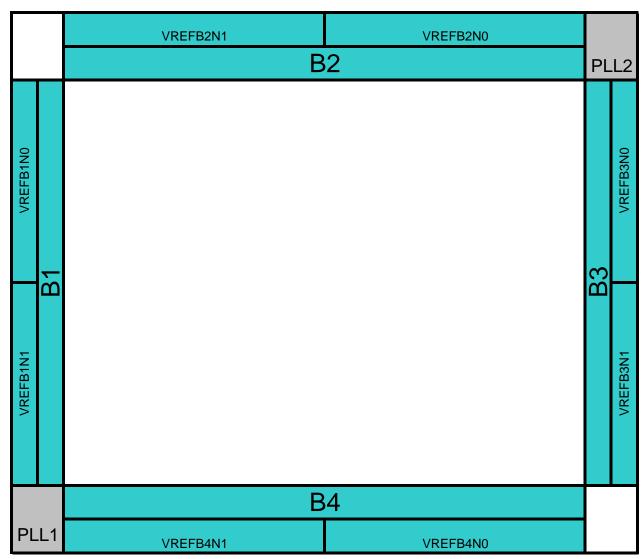| Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the configuration device's nINIT_CONF pin. If JTAG configuration is used, nCONFIG can be tied to VCC.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to Vccio by an external 10k Ω pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be used as an user I/O after configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-kΩ pull-up resistor.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.
Clock and PLL Pins		
CLK[0,2,4,6,8,10,12,14], LVDSCLK[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[1,3,5,7,9,11,13,15], LVDSCLK[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
PLL[1..4]_OUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output
PLL[1..4]_OUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output
Optional/Dual-Purpose Configuration Pins		
nCSO	Output	Output control signal from the Cyclone II FPGA to the nCS pin of the serial configuration device in AS mode that enables the configuration device by driving it low. In AS mode, the nCSO has internal weak pull-up resistor, which is always active.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
ASDO	Output	Output control signal from the Cyclone II FPGA to the serial configuration device in AS mode used to read out configuration data. In AS mode, the ASDO has internal weak pull-up resistor, which is always active.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Dual-Purpose Differential & External Memory Interface Pins		
LVDS[0-77][p,n]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels 0 to 77. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DPCLK[0,1,2,4,6,7,8,10]/ DQS[[0,1]L,[1,0]B,[1,0]R,[0,1]T]	I/O, DPCLK/DQS	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ1[B,L,R,T][0..17]	I/O, DQ	Optional data signal for use in external memory interfacing in the x16 or x18 modes.
DQ[0,1][B,L,R,T][0..8]	I/O, DQ	Optional data signal for use in external memory interfacing in the x8 or x9 modes.
DM1[B,L,R,T][0,1]	I/O, DM	Optional data mask pins for x16/x18 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ & DQS signals requires a DM pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DM[0..1][B,L,R,T]	I/O, DM	Optional data mask pins for x8/x9 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ & DQS signals requires a DM pin.
BWS#1[B,L,R,T][0,1]	I/O, BWS	Byte Write Select is an active LOW pin. When asserted active, BWS will select which byte is written into the device during write operation. Bytes not written remain unchange. Deselecting BWS will cause write data to be ignored and not written into device.
BWS#[0..1][B,L,R,T]	I/O, BWS	Byte Write Select is an active LOW pin. When asserted active, BWS will select which byte is written into the device during write operation. Bytes not written remain unchange. Deselecting BWS will cause write data to be ignored and not written into device.

Notes:

1. This is a top view of the silicon die.

2. This is a pictoral representation only to get an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations.

Version Number	Date	Changes Made
1.0	10/6/2004	Initial revision
1.1	2/24/2005	Modified Pin Definitions for DATA0 pin
1.2	4/27/2005	Added CRC_ERROR pin in Pin List and Pin Definition
		Changed pin name from GNDD_PLL and GNDG_PLL to GND_PLL
		Finalize
1.3	6/2/2005	Modified Pin Type column in Pin Definitions for VREFB[1..8]N[0..1] pins
1.4	2/10/2006	Added footnote for pins that do not support Optional Functions (LVDS, DDR, etc)
		Added footnote for DQS0T, DQS1T, DQS0B and DQS1B pins
		Modified pin definition for NC pins
		Modified Pin Description of VREFB[1..4]N[0..1] pins
		Modified Pin Description of VCCA_PLL[1..4] and VCCD_PLL[1..4] pins
		Added Pin Description for BWS pins
1.5	3/1/2006	Added comment for PLL_OUT pins in Pin Definitions