

# High Performance Software Defined Radio

Open Source Hardware and Software Project Project Description: <a href="http://openhpsdr.org">http://openhpsdr.org</a>



# **Metis**

High Speed PC Ethernet Interface

# **IMPORTANT**

The FPGA and other components on the Metis PCB can be damaged by Electrostatic Discharge (ESD). When handling the PCB do so using ESD precautions e.g. antistatic work bench and grounded wrist strap.

NEVER insert or remove a Metis, or any other HPSDR PCB, from the Atlas bus with power applied to the bus. Doing so my cause serious damage to components on the PCB.

# **Contents**

Introduction	4
What you will need	4
Metis Setup	5
Ethernet connection	5
DB-9 connection	7
RS232 connection	8
Configuration	8
Operation	8
Software	10
SDR Software	10
Updating Metis Firmware	10
Appendix A	14
Setting a static IP Address	14
Reloading the EEPROM on Metis	15
Using Metis to Program other HPSDR Boards	16
Additional information	18

# Introduction

METIS is a high speed PC interface board intended for use with the openHPSDR range of Software Defined Radio circuit boards. Metis is designed to plug into the openHPSDR Atlas bus and is a drop in replacement for an Ozy or Magister USB2 interface board.

Metis provides either a 100T or Gigabit (1000T) interface to the host PC. The board uses a large Altera FPGA (providing some 40,000 logic elements) which provides plenty of room for future code updates and new facilities.

The user input and outputs (e.g. PTT, CW key, relay driver) that are currently available on the Ozy and Magister boards are provided. However, control of the SDR1000 is no longer supported.

All the Ethernet protocol processing is undertaken by the FPGA. Protocols supported include: UDP/IP, DHCP, APR and 'ping'. A unique MAC address is assigned to each board and either a static or automatically assigned IP address can be used.

Future Metis code updates can be achieved via the Ethernet connection eliminating the need for special programming adapters.

Metis may also be used to update the code contained in the flash memory of other openHPSDR boards. For example, the firmware in a Mercury or Penelope board can be updated.

# What you will need

Table 1 and Table 2 below summarize the hardware and software you will require to operate a Metis board

#### Table 1: Hardware Requirements

Atlas board Backplane for all HPSDR boards

Metis board Control data and digital I/Q streams to/from PC

Atlas Power Supply PC ATX type or equivalent \*

Ethernet cable Connection between Metis and PC or Ethernet Switch DB-9 Cable For connection of PTT, CW keys and Open collector

outputs

#### Table 2: Software Requirements

Windows XP or Windows 7 PowerSDR™, KISS Konsole, ghpsdr3

Linux (Ubuntu V10.10) ghpsdr3
MacOS X Heterodyne

<sup>\*</sup>Metis draws 0.4A from 5v at 100T and 0.75A from 5v at 1000T

See <a href="http://openhpsdr.org/wiki/index.php?title=HPSDR\_related\_software">http://openhpsdr.org/wiki/index.php?title=HPSDR\_related\_software</a> for more information on suitable PC software.

# **Metis Setup**

#### **Ethernet Connection**

Metis is connected to a host PC either:

- a) Directly to a dedicated Ethernet port on a host PC; or
- b) To a connection on a full duplex Ethernet switch that is also connected to the host PC.

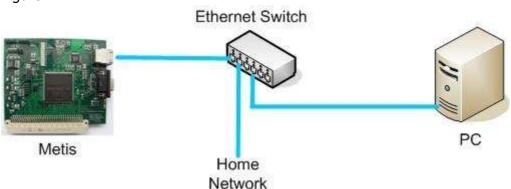
Connection to a dedicated Ethernet port is shown in Figure 1 whilst connection to an Ethernet switch is shown in Figure 2.

Figure 1



For direct connection to a dedicated Ethernet port a CAT 5 Ethernet cable is used. Note that a 'crossover' cable is not necessary but can be used if desired.

Figure 2



For connection to an Ethernet switch a CAT 5 Ethernet cable is used.

**IMPORTANT**: The Ethernet switch must be capable of operating in Full Duplex mode at 100T or 1000T. The initial release of Metis FPGA code will operate at 100T. Future releases will run at 1000T. In which case a 100T Ethernet switch may be used in the interim. If a new purchase is planned then a 100/1000T switch is recommended.

Since Metis operates in full duplex mode it may **NOT** be connected to an Ethernet Hub.

## **Jumper Settings**

Metis uses a number of user configurable jumpers; their location is shown in Figure 3.

Figure 3



Jumper settings are as follows:

Jumper	Inserted	Removed
JP1	Bootloader Mode	Normal operation (Default)
JP2	Force 100T(Default)	Speed select by network connection
JP3	LVDS Rx enabled	LVDS Rx disabled (Default)
JP4	LVDS Tx enabled	LVDS Tx disabled (Default)

JP1 - When inserted this starts the Metis board in Bootloader mode. See Appendix A for details regarding this mode. For normal operation this jumper should not be fitted.

JP2 – When inserted this forces Metis to run at 100T even if it is connected to an Ethernet Switch or PC capable of running at 1000T. When removed Metis will run at the maximum speed available on the Ethernet Switch or adapter it is connected to or as determined by the Metis firmware.

NOTE: for the initial release (V1.0) of Metis FPGA code JP2 should be inserted.

#### **DB-9 Connection**

The DB-9 connector straight through cable on Metis has the same functions and pin out as the original Ozy and Magister boards. The connections are:

Connection
Open Drain user output
Open Drain user output
3.3v TTL user output
3.3v TTL user output
Common/Ground
Dash – connected to 3.3v via 10k pullup
Dot - connected to 3.3v via 10k pullup
PTT - connected to 3.3v via 10k pullup
Flyback diodes, common cathode, for pins 1 and 2

The PTT can be activated by connecting pin 8 to ground (or pin 5).

For use with an Iambic CW Key, connect pin 6 to the dash connection and pin 7 to the dot. The common key connection should be connected to ground (or pin 5).

NOTE: to use a CW key with PowerSDR™ you will need to enable it. To do so, click on Setup and then select the DSP tab followed by the Keyer Sub-tab. In the Connections section select Ozy.

#### **RS232 Connection**

A 3.3v TTL Level RS232 interface is provided at J9. The pin connections are as follows:

```
J9 - 1 Ground
J9 - 2 RS232_out
J9 - 3 RS232 in
```

This connection is intended for advanced users as a means of testing and debugging code. For normal operation no connections are required. A suitable 3.3v to RS232 level converter will be required in order to connect these pins to a PC's serial port or a USB <> RS232 converter.

# **Configuration**

With the jumpers set in their default configuration inset the Metis board into a vacant slot on the Atlas backplane. If Metis is to be used to program other openHPSDR boards, via the Atlas JTAG facility, then Metis should be located farthest from the Atlas power connector and there should be no vacant Atlas bus connectors between any boards.

NOTE: Metis is an alternative to the Ozy and Magister boards and MUST NOT be used in addition to one of these boards. Any other openHPSDR board can be use on the Atlas bus with Metis e.g. Mercury, Penelope, Excalibur etc.

## **Operation**

Revision 1.0

The following LEDs indicate the status of the Metis board. See Figure 3 for a photograph that indicates the location of the various LEDs.

When Metis is powered the following power supply LEDs should be alight:

```
D1 - 3.3v supply OK
D2 - 2.5v supply OK
D3 - 3.3v supply OK
D10 - 3.3v supply OK
```

The meaning of the other LEDs is as follows:

```
    D14 = LED[0] - Displays state of PHY negotiations - fast flash if no Ethernet connection, slow flash if 100T, on if 1000T and swap between fast and slow flash if the connection is not full duplex
    D15 = LED[1] - Lights when Metis receives Ethernet traffic
    D16 = LED[2] - Lights when Metis transmits Ethernet traffic
```

8

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D17 = LED[3] - Lights when an Ethernet broadcast is detected

D22 = LED[4] - Lights when traffic to Metis' MAC address is detected

D12 = LED[5] - Lights when an ARP request is received

D11 = LED[6] - Displays state of DHCP negotiations or static IP - on if DHCP ACK, slow flash if DHCP NAK, fast flash if DHCP time out and long then short flash if static IP. If DHCP NAK, or time out, an IPIPA IP address will be allocated to Metis.

D13 = LED[7] - Lights when a ping request is received

D21 = LED[8] - Lights when a Metis discovery packet is received

D20 = LED[9] - Lights when a Metis discovery packet reply is sent

D19 = LED[10] - Lights when Sync (0x7F7F7F) received from PC

D18 = LED[11] - Lights when a receive sequence error is detected or the EPCS16 flash memory is being erased or programmed.

D23 = LED[12] - HEART\_BEAT - Flashes twice per second

NOTE: The meaning of each LED is under firmware control. Hence this may change in future releases of firmware. Please check the firmware release notes to confirm the meaning of each LED.

When first powered on Metis will attempt to obtain an IP address from a DHCP server (if one in attached to the network). If this is successful then LED[6] will be steadily illuminated. It may take up to 8 seconds for a DHCP IP address to be assigned.

If a DHCP server is not found on the network, or Metis is connected directly to a PC, then an APIPA IP address in the range 169.254.x.x will be assigned.

NOTE: This will be assigned after Metis' attempts to obtain a DHCP IP address has failed so will take 8 seconds from powering on the Metis board. The time that a PC takes to obtain an APIPA address *itself* varies with the particular operating system. Tests using Windows XP indicates this can be up to 20 seconds.

If an APIPA IP address is assigned then LED[6] will flash rapidly.

The user may also set a static IP address (see Appendix A). In which case a DHCP IP address will not be sought and LED[6] will flash short/long.

The PC SDR code may then be started. A Metis board that is ready to communicate with a PC will respond to 'ping' and ARP requests.

# **Software**

#### **SDR Software**

The following describes how to set up PowerSDR<sup>™</sup> to operate with Metis. Please refer to the relevant software documentation for using Metis with other SDR applications.

Run PowerSDR™, Select Setup, click the General tab then Hardware Config. Within Connection Type select Metis (Ethernet) as follows:



Press the Start button on PowerSDR™ whereby the Metis board will automatically be detected. PowerSDR will display the IP address and MAC address of the Metis Board it is connected to. On the Hardware Config form this is displayed within Metis Address as follows:

Metis Address IP: 0.0.0.0 MAC: 00:00:00:00:00

Make a note of the unique MAC address since this is useful for problem solving in the future.

Depending on the processing power of your PC it may be necessary to run PowerSDR™ at a higher priority. If gaps in the receive audio are present when operating at 192kHz sampling rate then try increasing the Process Priority. This can be set by selecting Setup, General, Options and within Process Priority select 'Above Normal' or 'Real Time'. NOTE: There appears to be an issue with selecting 'Real' - please be aware of this.

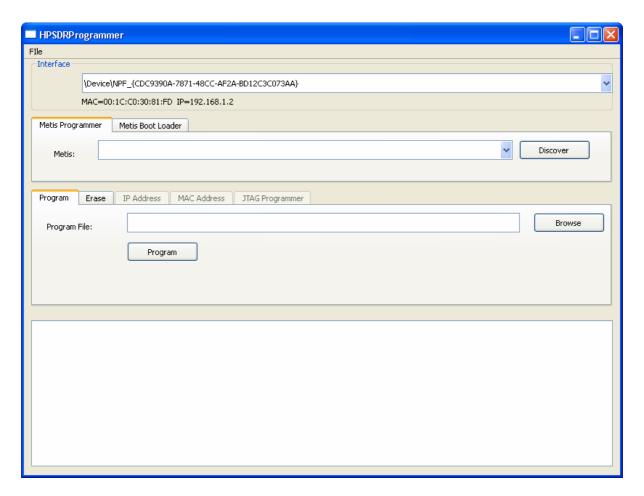
### **Updating Metis Firmware**

The firmware used to control the Metis board is held in an EEPROM on the PCB. The firmware can be updated to the latest version via the Ethernet connection and the HPSDRProgrammer PC software.

To update, install the HPSDRProgrammer software from <a href="http://openhpsdr.org/download.php">http://openhpsdr.org/download.php</a>. Versions of this software are available for Windows, Linux(Ubuntu 10.10, 32 & 64 bit) and MacOS X operating systems.

Before installing new firmware, ensure that all PC SDR software has been stopped and the application closed.

Run the HPSDRProgrammer software which will result in the following screen being displayed (Windows version used for illustration):

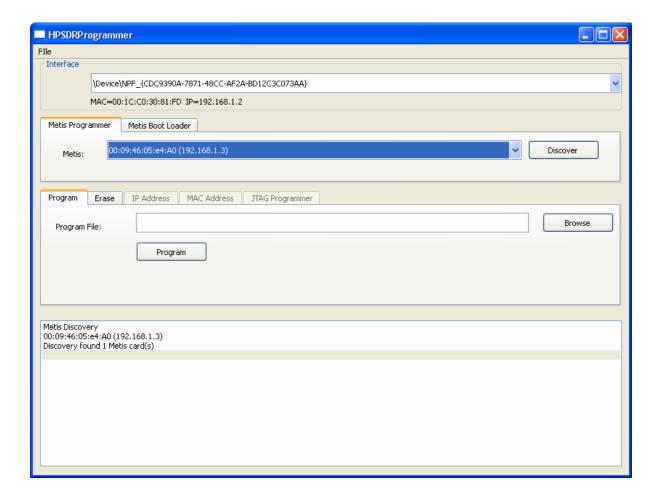


The 'Interface' section will list the Ethernet adapters present on the PC. If there is more than one found then use the drop-down menu to select the adapter that the Metis board is connected to. The IP address that the adapter is using is displayed beneath the entry to assist with selecting the correct one. The Linux version will display available adapters using eth0, eth1 etc. and MacOS X en0, en1, en2, etc.

Check that the 'Metis Programmer' Tab is selected.

Click the 'Discover' button; this will locate any Metis board(s) that the PC is able to access. If more than one Metis board is located then the board to be programmed may be selected using the drop-down menu in the 'Metis Programmer' section.

The successful discovery of a Metis board will be indicated as follows:



To program the selected Metis board check that the 'Program' Tab is selected. Use the 'Browse' button to locate the Metis\_Vx.x.rbf file that is to be loaded into the Metis flash memory. The current Metis\_Vx.x.rbf file can be found at <a href="http://openhpsdr.org/download.php">http://openhpsdr.org/download.php</a>.



Click on the 'Program' button to start the erase and programming cycle. A successful erase and program will be indicated as follows:

```
reading file...
file read successfully
Erasing device ... (takes several seconds)
Device erased successfully
Programming device ...
Programming device 20% written ...
Programming device 40% written ...
Programming device 60% written ...
Programming device 80% written ...
Programming device 80% written ...
Programming device sompleted successfully
```

Once the new firmware has been successfully loaded Metis will automatically load and run the new code.

Should the new firmware not load or operate correctly then please refer to Appendix A for further instructions.

HPSDRProgrammer may also be used to erase the flash memory on a Metis board. In this case select the 'Erase' Tab and click the 'Program' button.

# **Appendix A**

This appendix explains how to set a static IP address and use the Metis Bootloader facility. NOTE: In order to use these facilities you need to be running with Administrator privileges under Windows, root under Linux. The MacOS X version will automatically set the correct privileges.

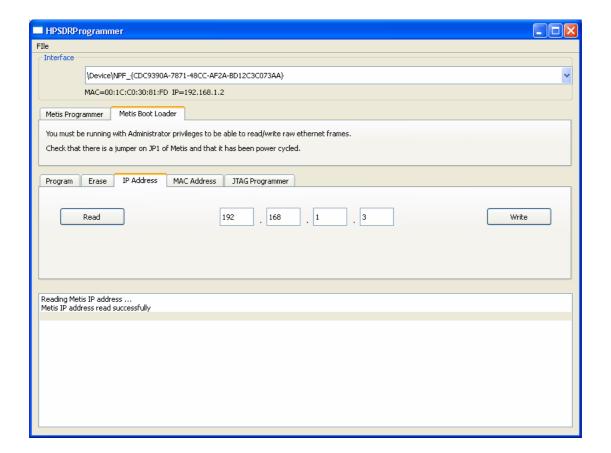
### **Setting a static IP Address**

This section explains how to set a static IP Address on a Metis board. This facility is provided for advanced users who understand the implications of using a static IP Address.

Remove the power from Metis and connect a jumper to JP1, this places Metis into Bootloader mode. Reapply power to Metis.

Ensure that any SDR software has been stopped and terminated. Load the HPSDRProgrammer software, select the appropriate Interface then select the 'Metis Boot Loader' Tab.

Select the 'IP Address' Tab, enter the desired IP address in xxx.xxx.xxx format then click 'Write'. Then click the 'Read' button and check that the information area displays the desired IP address. The result of programming the IP address 192.168.1.3 is shown below.



NOTE: if an IP address of 0.0.0.0 or 255.255.255 is set then Metis will ignore the setting and instead attempt to obtain a DHCP or APIPA IP address.

Remove the power from Metis then remove the jumper on JP1. Reapply power to Metis.

#### **Reloading the EEPROM on Metis**

The normal procedure for updating the EEPROM on Metis is by using the in-line programmer function as described in 'Updating Metis Firmware'. However, should this fail for some reason, or a Metis board is received in an unknown state, then the EEPROM may be updated using the following method.

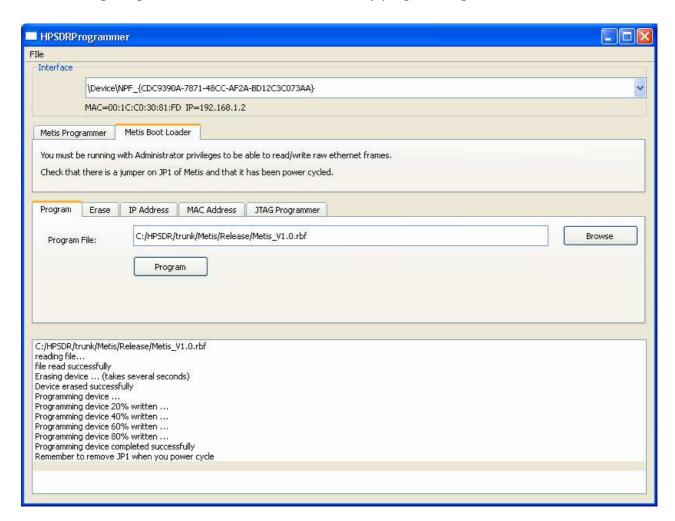
Ensure that any SDR software has been stopped and terminated. Load the HPSDRProgrammer software and select the 'Metis Boot Loader' Tab.

Remove the power from Metis and connect a jumper to JP1, this places Metis into Bootloader mode. Reapply power to Metis.

Ensure that the 'Program' Tab is selected then use the 'Browse' button to select the Metis\_Vx.x.rbf file that you wish to load into the EEPROM. Click 'Program', the EEPROM will be erased and programmed.

Remove the power from Metis then remove the jumper on JP1. Reapply power to Metis to load the new code into the FPGA.

The following image indicates the result of successfully programming Metis.



### **Using Metis to Program other HPSDR Boards**

Metis may be use to update the flash memory on other HPSDR boards e.g. Penelope, Mercury etc. This is referred to as the 'target' in the following description.

Metis uses the JTAG chain on the Atlas bus to access the FPGA on the target board. The JTAG chain is first used to temporarily load code in the target FPGA. This code exposes an interface to the flash memory on the target board which allows Metis to program it.

To update the flash memory on an HPSDR board, close and terminate any running SDR software. Remove power from the Atlas bus then connect a jumper to JP1 on the Metis board; this places the board in Bootloader mode.

Place the 'Last JTAG' jumper on the target board e.g. JP7 for Mercury, Penelope and PennyLane. Remove all other boards from the Atlas bus. Place the target board and Metis in adjacent Atlas slots with Metis farthest from the Power connector.

Reapply power to the Atlas bus.

Run HPSDRProgrammer and select the 'Metis Boot Loader' Tab then Click 'Interrogate'. This checks the integrity of the JTAG chain and reports which HPSDR board it finds on the chain.

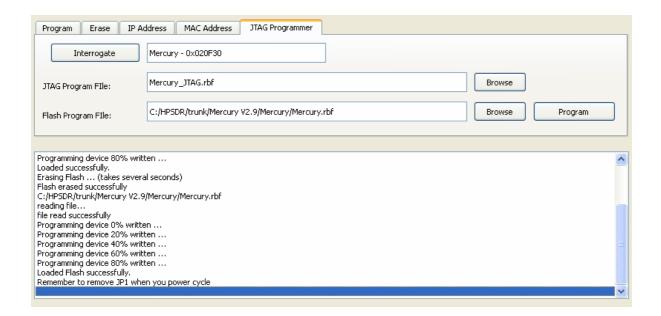
The result of interrogating the JTAG chain with a Mercury board is shown below.



The program will automatically select the default JTAG program file; Mercury\_JTAG.rbf or Penelope\_JTAG.rbf. Should a different file be required then use the 'Browse' button to locate it.

Using the lower 'Browse' button locate the \*.rbf file to be loaded into the targets flash memory. In this example we use V2.9 of the Mercury code. These \*.rbf files can be download from <a href="http://openhpsdr.org/download.php">http://openhpsdr.org/download.php</a>.

Click 'Program', the targets flash memory will be erased and programmed with the selected file. An example of the successful programming of a Mercury board is shown below. Use the right hand scroll bar to see all the text.



Remove power from the Atlas bus and remove the Jumper from JP1 on the Metis board. Reapply power to the Atlas bus and the new code will be loaded into the target board.

#### **Additional information**

A detailed description of the protocol used by Metis can be found in the document 'Metis – how it works.pdf' which can be found here <a href="http://openhpsdr.org/support.html">http://openhpsdr.org/support.html</a>.