Wideband, Ring Demodulator

SD8901

FEATURES

- **High Frequency Operation**
- **Wide Dynamic Range**
- **Low Capacitance**

APPLICATIONS

- **Communications**
- **RF Mixers**

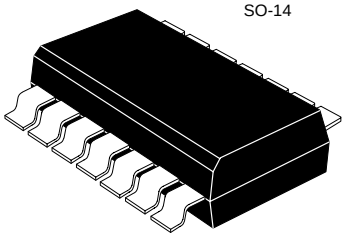
DESCRIPTION

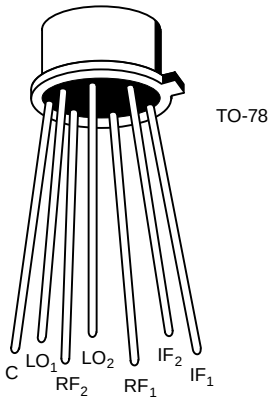
The SD8901 is a ring demodulator/balanced mixer. Designed to utilize Calogic's ultra high speed and low capacitance lateral DMOS process. The SD8901 offers significant performance improvements over JFET and diode balanced mixers when low third order harmonic distortion has been a problem.

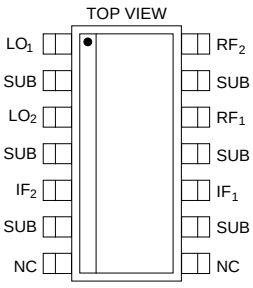
PACKAGE INFORMATION

Part	Package	Temperature Range
SD8901HD	Hermetic TO-78	-55°C to 125°C
SD8901CY	Plastic Surface Mount	-55°C to 125°C
XSD8901	Sorted Chips in Carriers	-55°C to 125°C

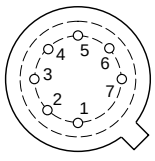
PIN CONFIGURATIONS





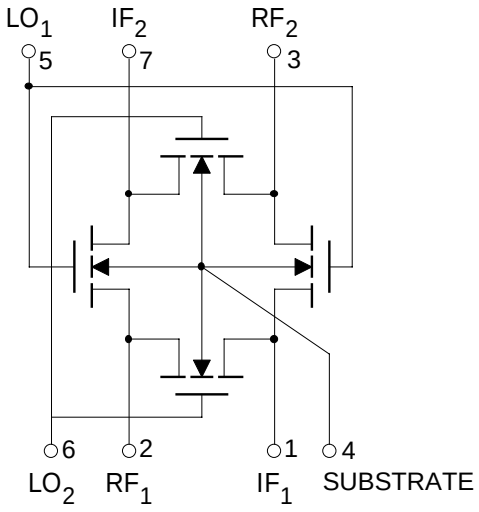


1 IF_1
2 RF_1
3 RF_2
4 CASE
5 LO_1
6 LO_2
7 IF_2



CD4

Functional block diagram



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain to Source . . . . . 15 V
V_{DB} Drain to Substrate . . . . . 22.5 V
V_{SB} Source to Substrate . . . . . 22.5 V
V_{GS} Gate to Source . . . . . -22.5 V to 30 V
V_{GB} Gate to Substrate . . . . . -0.3V to 30 V
V_{GD} Gate to Drain . . . . . -22.5V to 30 V

I_D Drain Current . . . . . 50 mA
Operating Temperature . . . . . -55 to 125°C
Storage Temperature . . . . . -65 to 150°C
Power Dissipation (A Package)* . . . . . 640 mW
* Derate 5 mW/ °C above 25°C

ELECTRICAL CHARACTERISTCIS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
STATIC							
$V_{(BR)DS}$	Drain-Source Breakdown Voltage	15	25		V	$V_{GS} = V_{SB}$ = -5 V Is = 10 nA	
$V_{(BR)SD}$	Source-Drain Breakdown Voltage	15				$V_{GD} = V_{DB}$ = - 5 V I_D = 10 nA	
$V_{(BR)DB}$	Drain-Substrate Breakdown Voltage	22.5				Source Open V_{GB} = 0 V, I_D = 10 nA	
$V_{(BR)SB}$	Source-Substrate Breakdown Voltage	22.5				Drain Open V_{GB} = 0 V, I_D = 10 nA	
V_T	Threshold Voltage	0.1	1	2.0		$V_{DS} = V_{GS} = V_T$ I_S = 1 µA, V_{SB} = 0V	
$r_{DS(ON)}$	Drain-Source "ON" Resistance		50	75	Ω	I_D = 1 mA V_{SB} = 0 V	V_{GS} = 5 V
			30				V_{GS} = 10 V
			23				V_{GS} = 15 V
			19				V_{GS} = 20 V
$\Delta r_{DS(ON)}$	Resistance Matching		3	7			V_{GS} = 5 V
DYNAMIC							
C_{gg}	LO_1 - LO_2 Capacitance		4.4		pF	V_{DS} = 0 V, V_{BS} = -5.5 V V_{GS} = 4 V	
L_c	Conversion Loss		8		dB	See Figure 1, PLO = +17 dBm	
IMD_3	Third Order Intercept		+35				
f_{MAX}	Maximum Operation Frequency		250		MHz		

Note: Guaranteed by design, not subject to production test

PERFORMANCE COMPARISON

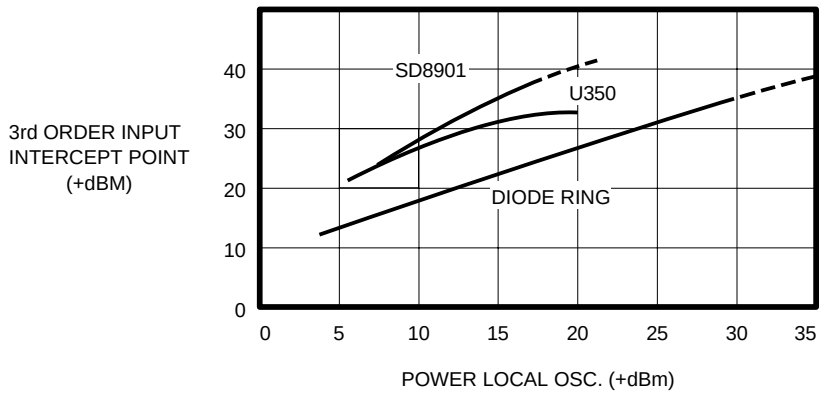


FIGURE 1.

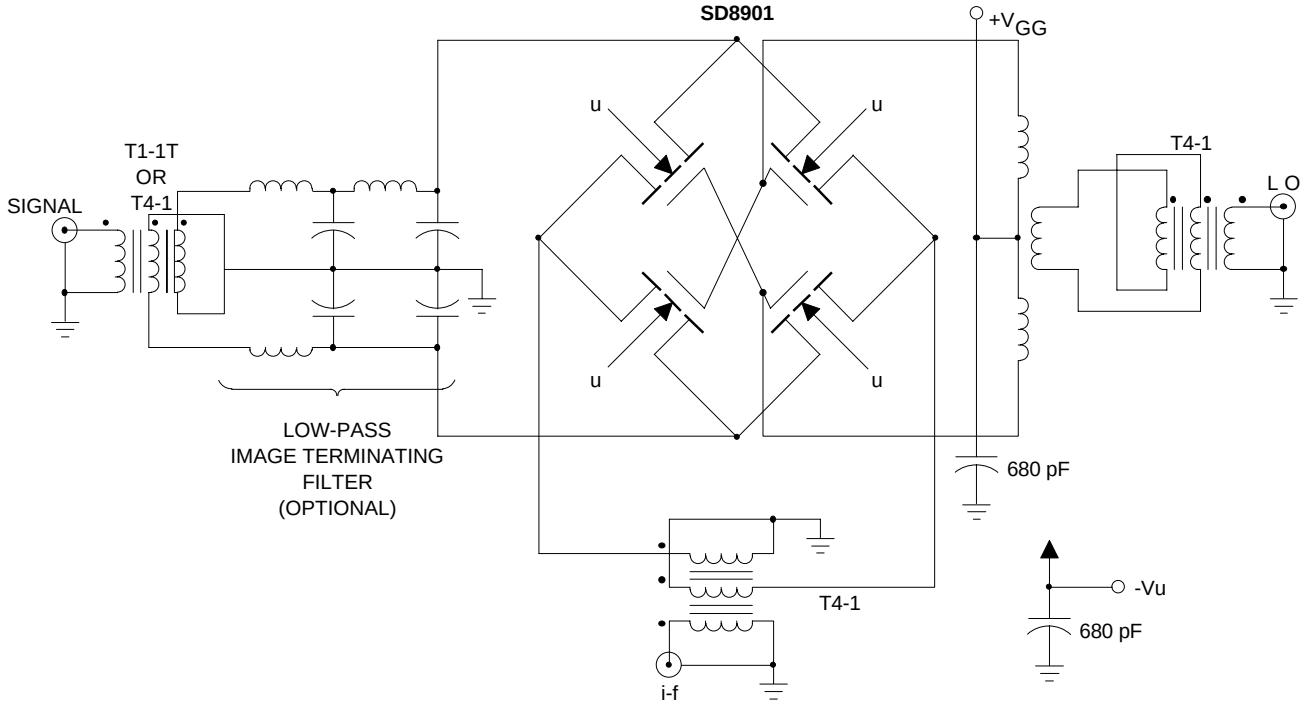


FIGURE 2. First and third Quadrand I-E Characteristic Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion.