TS3A4741
0.9-Ω LOW-VOLTAGE SINGLE-SUPPLY DUAL SPST ANALOG SWITCH

SCDS228B – AUGUST 2006 – REVISED SEPTEMBER 2006

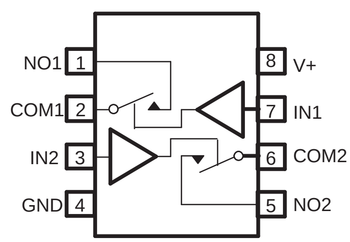
FEATURES

- **Low ON-State Resistance (r_{on})**
  - **– 0.9 Ω Max (3-V Supply)**
  - **– 1.5 Ω Max (1.8-V Supply)**
- **0.4-Ω Max r_{on} Flatness (3-V Supply)**
- **1.6-V to 3.6-V Single-Supply Operation**
- **Available in SOT-23 and MSOP Packages**
- **High Current-Handling Capacity (100 mA Continuous)**
- **1.8-V CMOS Logic Compatible (3-V Supply)**
- **Fast Switching: t_{ON} = 14 ns, t_{OFF} = 9 ns**

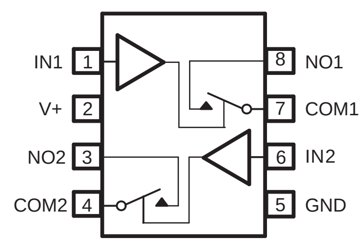
APPLICATIONS

- **Power Routing**
- **Battery-Powered Systems**
- **Audio and Video Signal Routing**
- **Low-Voltage Data-Acquisition Systems**
- **Communications Circuits**
- **PCMCIA Cards**
- **Cellular Phones**
- **Modems**
- **Hard Drives**

DGK PACKAGE (TOP VIEW)



DCN PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS3A4741 is a low ON-state resistance (r_{on}), low-voltage, dual single-pole/single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital logic input is 1.8-V CMOS compatible when using a single 3-V supply.

The TS3A4741 has two normally open (NO) switches that are available in 8-pin SOT-23 and MSOP packages.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	MSOP – DGK	Reel of 2500	TS3A4741DGKR	JYR
	SOT-23 – DCN	Reel of 3000	TS3A4741DCNR	TBD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

Absolute Minimum and Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage reference to GND[2]		–0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range		–0.3	$V_+ + 0.3$	V
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–100	100	mA
I_+ I_{GND}	Continuous current through V_+ or GND			±100	mA
	Peak current pulsed at 1 ms, 10% duty cycle	COM, V_{NO}, V_{COM}		±200	mA
θ_{JA}	Package thermal impedance[3]	DCN package		88	°C/W
		DGK package		88	
T_A	Operating temperature range		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.
(3) The package thermal impedance is measured in accordance with JESD 51-7.

Electrical Characteristics for 3-V Supply(1)(2)

V_+ = 2.7 V to 3.6 V, T_A = –40°C to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP(3)	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.7	0.9	Ω
				Full			1.1	
ON-state resistance match between channels(4)	Δr_{on}	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.03	0.05	Ω
				Full			0.15	
ON-state resistance flatness(5)	$r_{on(flat)}$	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1 V, 1.5 V, 2 V		25°C		0.23	0.4	Ω
				Full			0.5	
NO OFF leakage current(6)	$I_{NO(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
COM OFF leakage current(6)	$I_{COM(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
COM ON leakage current(6)	$I_{COM(ON)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 0.3 V, 3 V, or floating		25°C	–2.5	0.01	2.5	nA
				Full	–5		5	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	14	ns
				Full			15	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		4	9	ns
				Full			10	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		125		MHz
OFF isolation(7)	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–40		dB
			f = 1 MHz			–62		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–73		dB
			f = 1 MHz			–95		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.04		%
			R_L = 600 Ω			0.003		
Digital Control Inputs (IN1, IN2)								
Input logic high	V_{IH}			Full	1.4			V
Input logic low	V_{IL}			Full			0.5	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.5	1	nA
				Full	–20		20	
Supply								
Power-supply range	V_+				1.6		3.6	V
Positive-supply current	I_+	V_+ = 3.6 V, V_{IN} = 0 or V_+		25°C			0.075	µA
				Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at V_+ = 3 V, T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

Electrical Characteristics for 1.8-V Supply[1][2]

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C, V_{IH} = 1 V, V_{IL} = 0.4 V (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP[3]	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		1	1.5	Ω
				Full			2	
ON-state resistance match between channels[4]	Δr_{on}	V_+ = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		0.09	0.15	Ω
				Full			0.25	
ON-state resistance flatness[5]	$r_{on(flat)}$	V_+ = 1.8 V, I_{COM} = –10 mA, $0 \le V_{NO} \le V_+$		25°C		0.7	0.9	Ω
				Full			1.5	
NO OFF leakage current[6]	$I_{NO(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
COM OFF leakage current[6]	$I_{COM(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
COM ON leakage current[6]	$I_{COM(ON)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 0.15 V, 1.65 V, or floating		25°C	–1	0.01	1	nA
				Full	–3		3	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		6	18	ns
				Full			20	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	10	ns
				Full			12	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3.2		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		123		MHz
OFF isolation[7]	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–61		dB
			f = 100 MHz			–36		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–95		dB
			f = 100 MHz			–73		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.14		%
			R_L = 600 Ω			0.013		
Digital Control Inputs (IN1, IN2)								
Input logic high	V_{IH}			Full	1			V
Input logic low	V_{IL}			Full			0.4	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.1	5	nA
				Full	–10		10	
Supply								
Power-supply range	V_+				1.6		1.95	V
Positive-supply current	I_+	V_I = 0 or V_+		25°C			0.05	μA
				Full			0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

TYPICAL PERFORMANCE

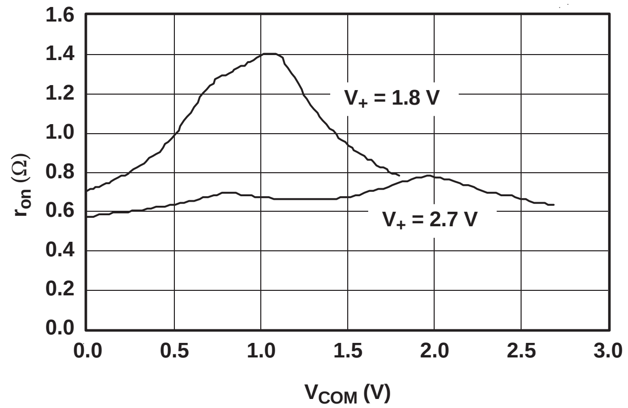


Figure 1. r_{on} vs V_{COM}

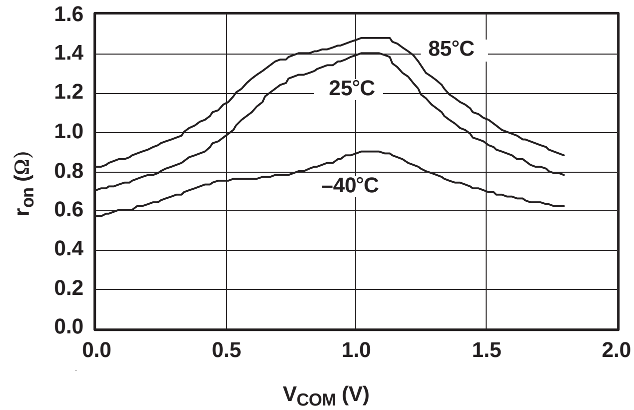


Figure 2. r_{on} vs V_{COM} (V_+ = 1.8 V)

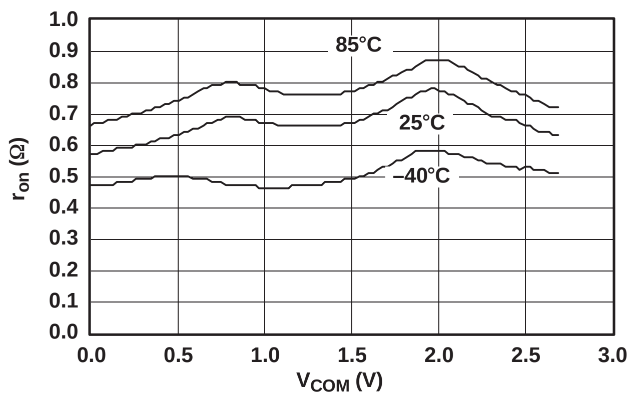


Figure 3. r_{on} vs V_{COM} (V_+ = 2.7 V)

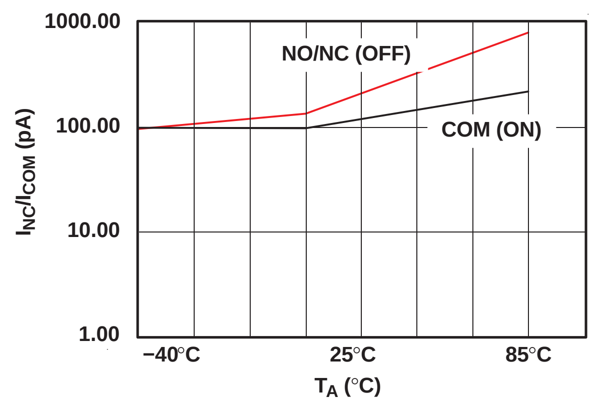


Figure 4. I_{ON} and I_{OFF} vs Temperature (V_+ = 3.6 V)

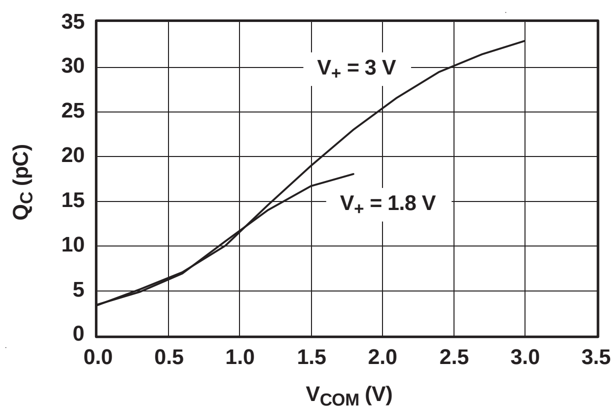


Figure 5. Q_C vs V_{COM}

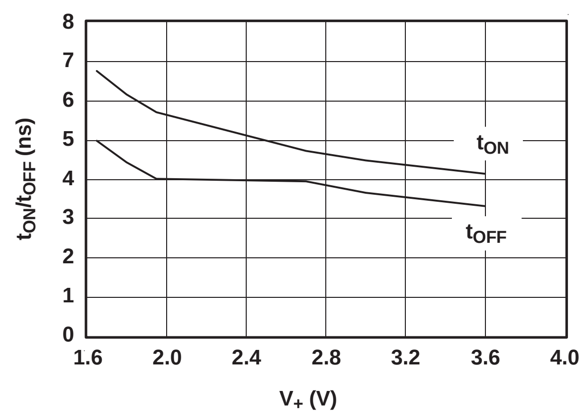


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

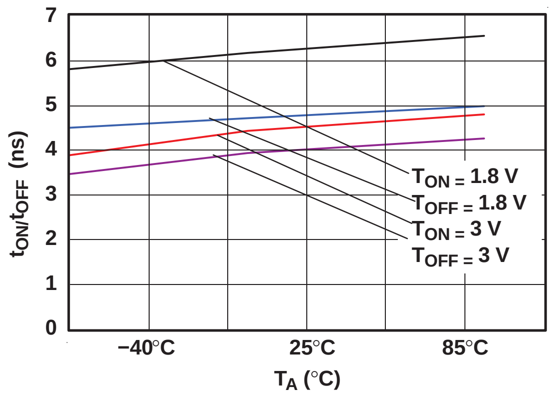


Figure 7. t_{ON} and t_{OFF} vs Temperature

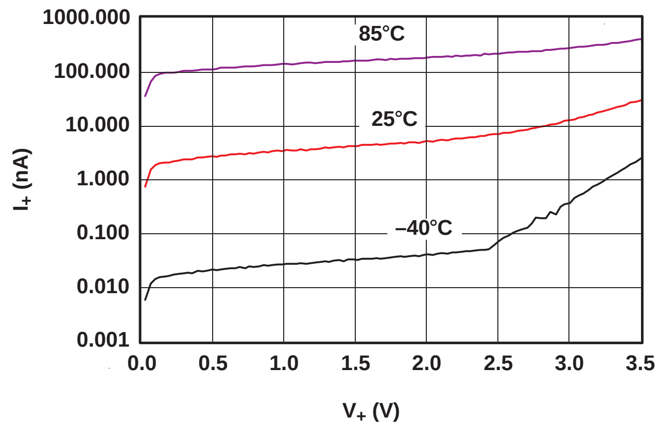


Figure 8. I_+ vs V_+

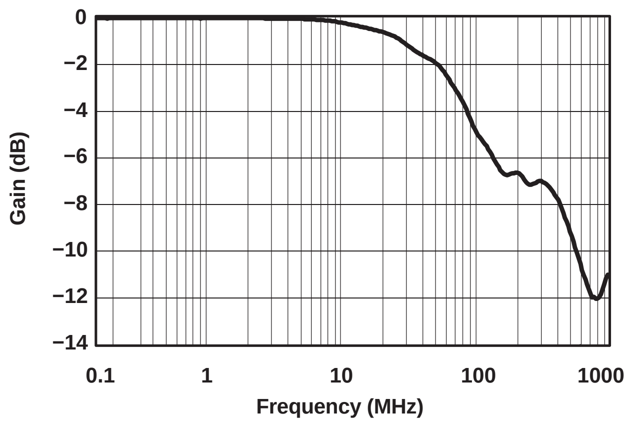


Figure 9. Gain vs Frequency (V_+ = 3 V)

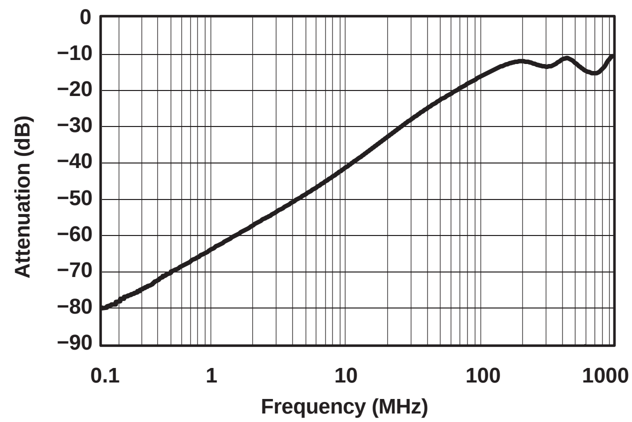


Figure 10. OFF Isolation vs Frequency (V_+ = 3 V)

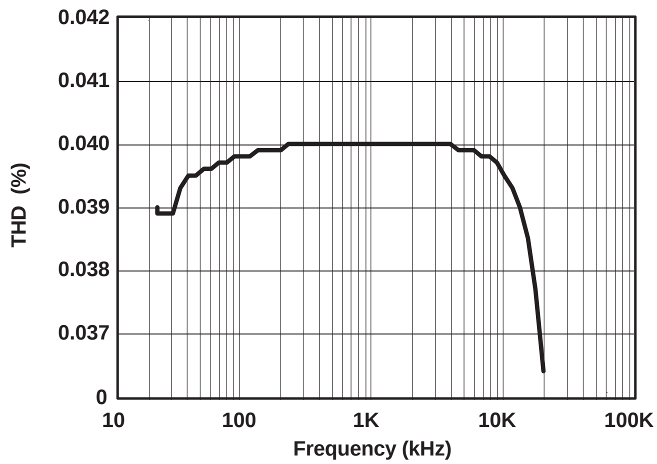


Figure 11. Total Harmonic Distortion vs Frequency (R_L = 32 Ω)

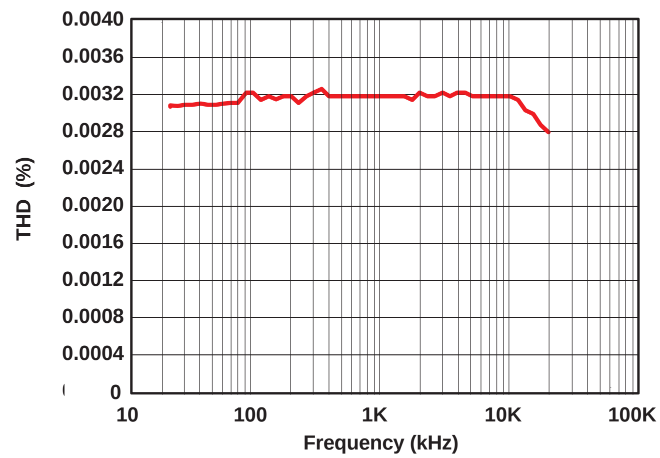


Figure 12. Total Harmonic Distortion vs Frequency (R_L = 600 Ω)

TYPICAL PERFORMANCE (continued)

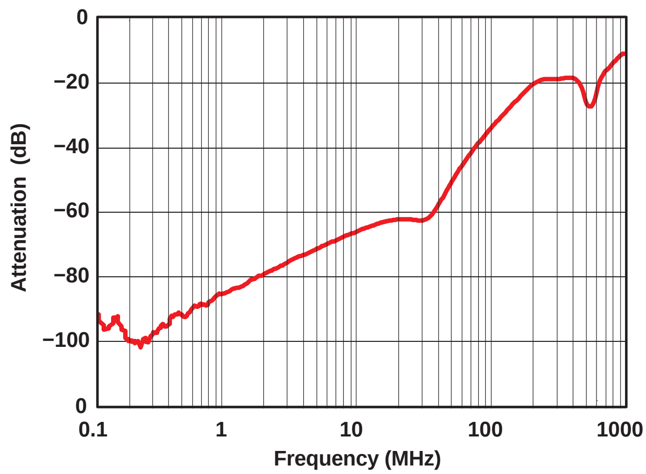


Figure 13. Crosstalk vs Frequency
(V_+ = 3 V)

PIN DESCRIPTION

PIN NO.		NAME	DESCRIPTION
MSOP	SOT-23		
1	8	NO1	Normally open 1
2	7	COM1	Common 1
3	6	IN2	Digital control to connect COM2 to NO2
4	5	GND	Digital ground
5	3	NO2	Normally open 2
6	4	COM2	Common 2
7	1	IN1	Digital control to connect COM1 to NO1
8	2	V_+	Power supply

Application Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_+ on first, followed by NO, NC, or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1-µF capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The TS3A4741 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in r_{on} (see Typical Operating Characteristics). The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

PARAMETER MEASUREMENT INFORMATION

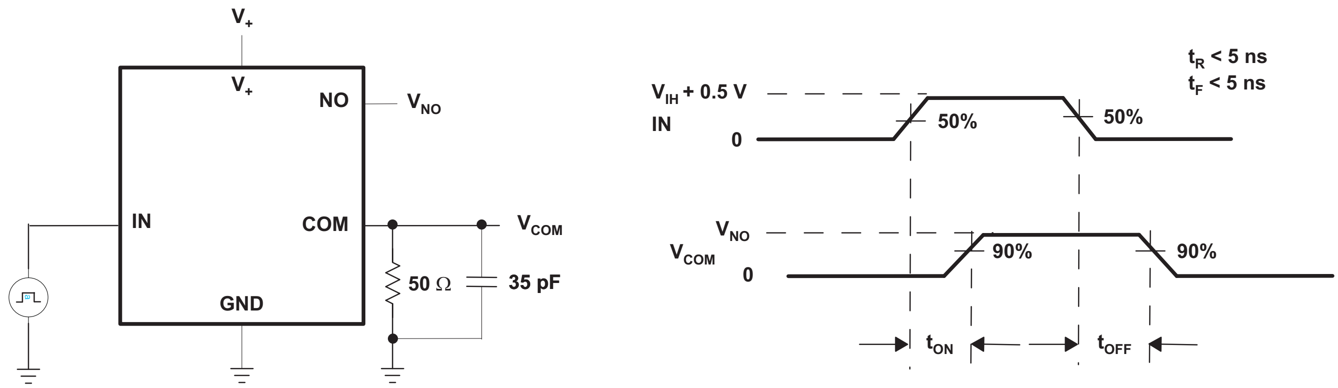


Figure 14. Switching Times

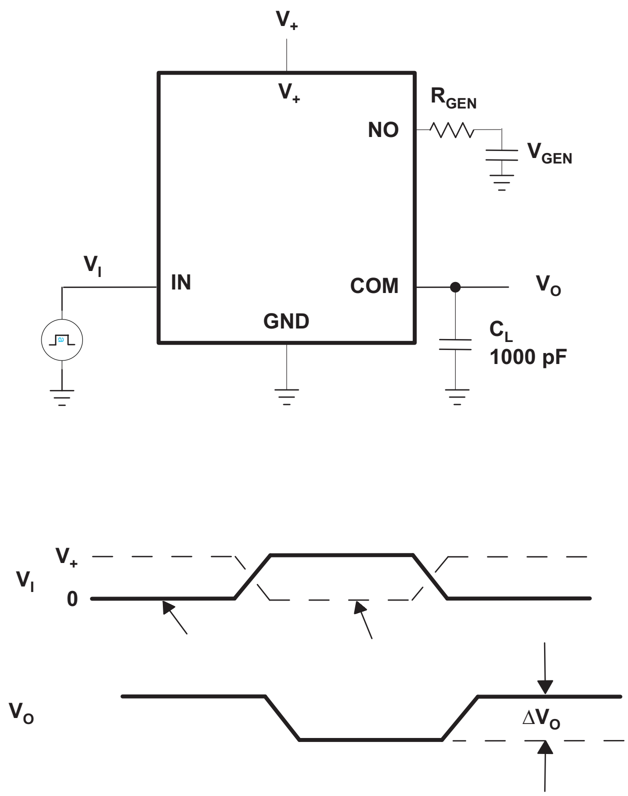


Figure 15. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)

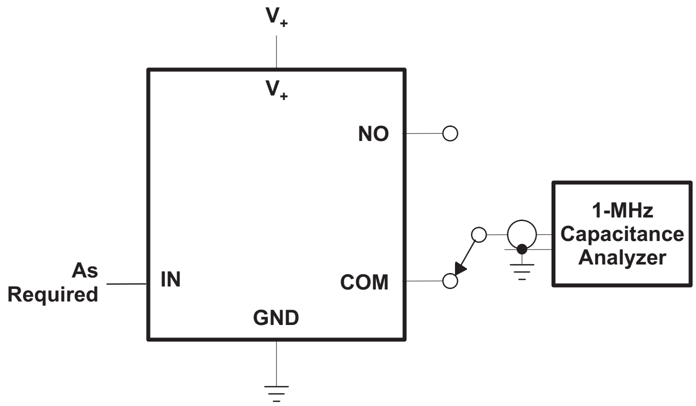
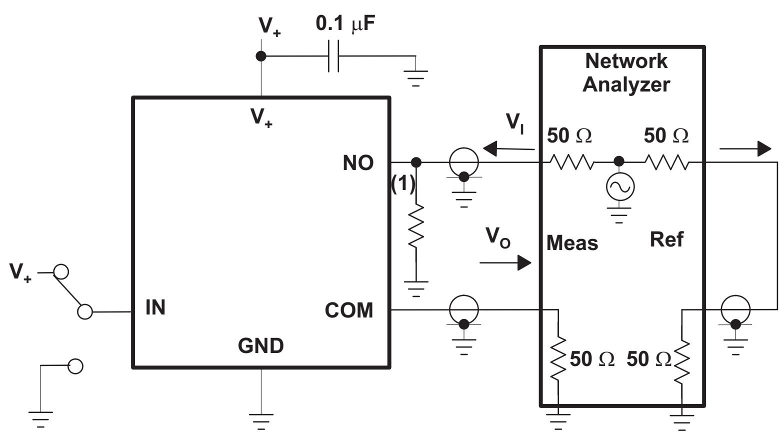


Figure 16. NO and COM Capacitance



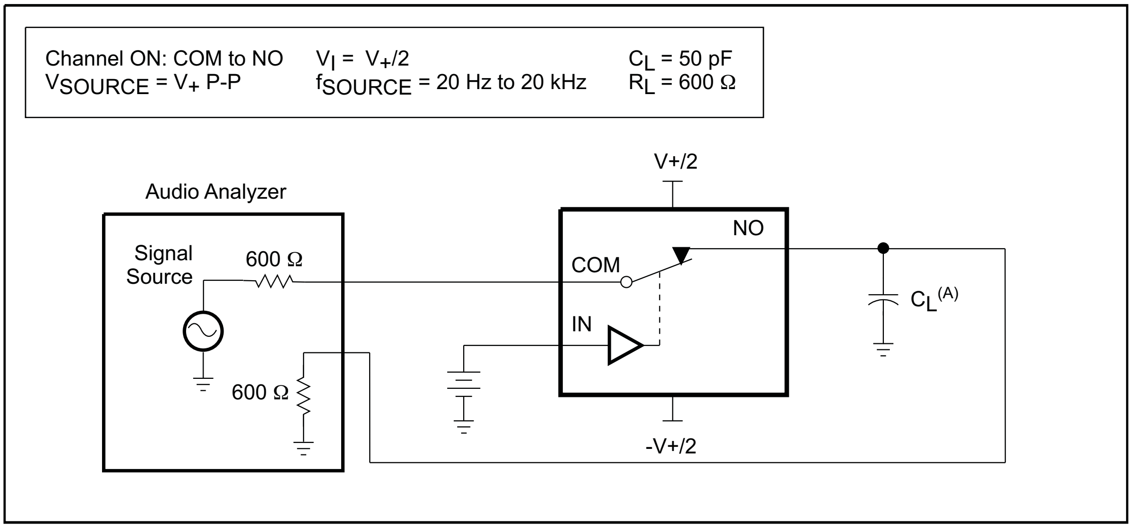
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

OFF isolation = 20 log V_O/V_I

(1) Add 50-Ω termination for OFF isolation

Figure 17. OFF Isolation, Bandwidth, and Crosstalk

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

Figure 18. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TS3A4741DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A4741DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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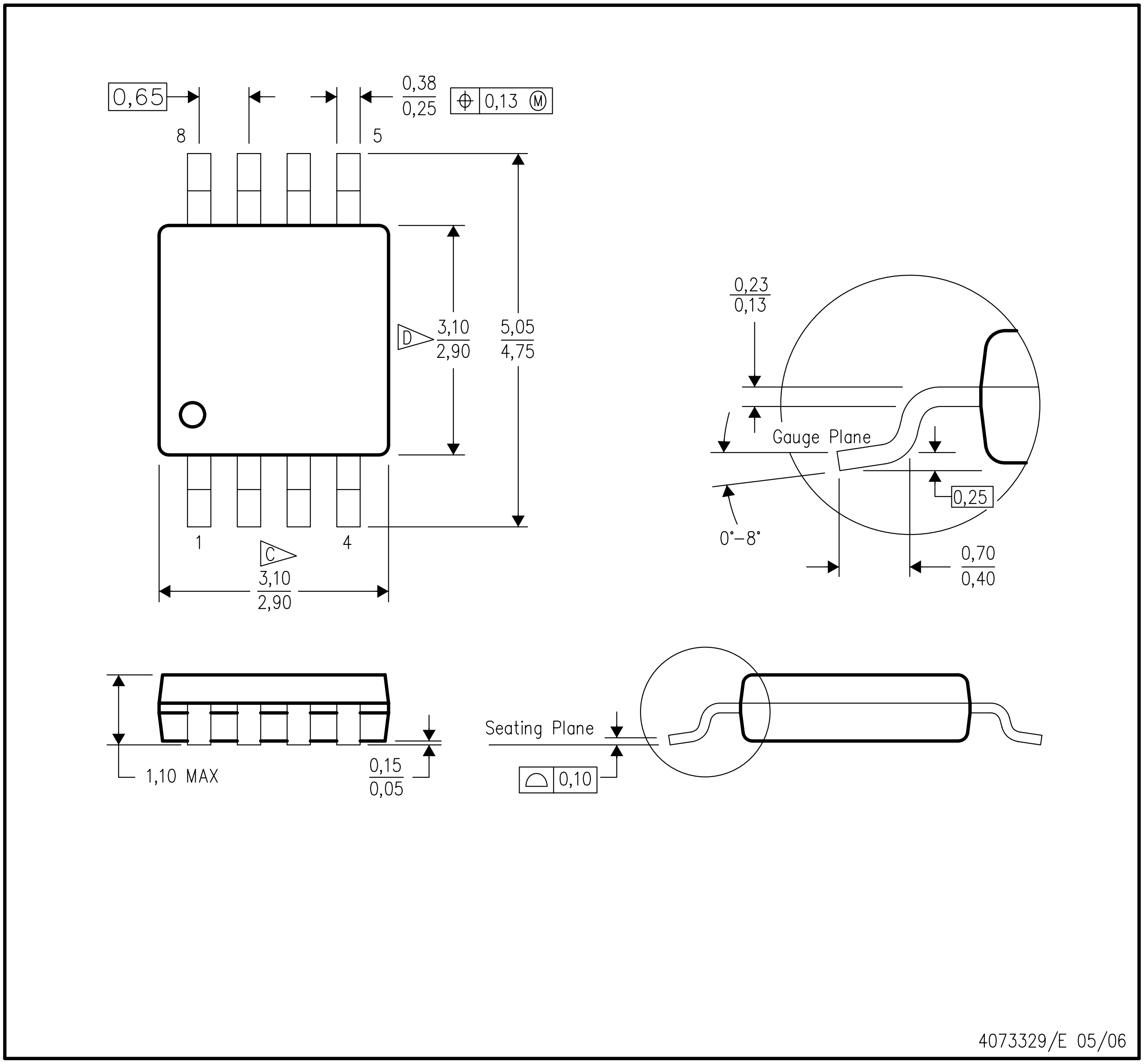
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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