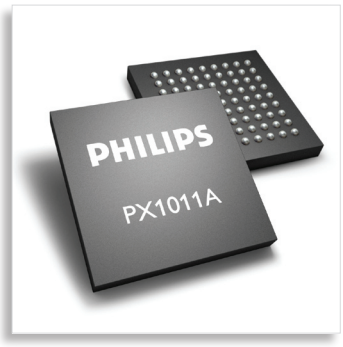


PCI Express PHY

Philips x1 PHY single-lane transceiver PX1011A

This standalone PCI Express transceiver, available in a very small package, is optimized for use with digital ASICs and low-cost FPGAs. It delivers superior performance, faster time-to-market, lower risk, and increased design flexibility.

Features

- One x1 physical lane for PCI Express
- Transmit and receive at 2.5 Gbps
- Complies with PCI Express v1.1a
- Passes PCI Express v1.1 informational jitter tests from PCI-SIG
- Better than $1x10^{-12}$ bit error rate (BER)
- Philips PXPIPE (8-bit, 250-MHz) PHY-MAC interface
  - FPGA-compatible SSTL2 Class 1 signaling
- Suitable for ExpressCard applications
  - < 300 mW power dissipation in L0 mode, including I/O
  - Small, thin 81-pin package
- L0, L0s, L1 power management modes; partial support for L2, L3
- Support for spread-spectrum clocking
- Temperature range: 0 to 70 °C
- Leaded or lead-free LFBGA-81 package (9 x 9 x 1.05 mm)
- Comprehensive support tools
  - Behavioral models for RTL simulation in various tools
  - IBIS model for PCB signal integrity analysis
  - Detailed PCB layout guidelines
  - Multiple third-party design kits available

Design benefits

- Improves digital ASIC designs
  - Quickly add proven mixed-signal functionality and performance
  - Reduce overall cost and risk
- Enables low-cost FPGA PCI Express designs
  - Proven interoperability with multiple FPGAs

Fast, low-risk digital ASIC designs

The PX1011A makes ASIC development faster and less risky. By isolating the mixed-signal PHY functions in an external transceiver, the PX1011A lets the ASIC's digital functions migrate to the latest process technologies without impacting complex PHY operations.

Increased efficiency of low-cost FPGA designs

The PX1011A also improves efficiency in designs that use an FPGA. Low-cost, high-density FPGAs don't typically offer an on-chip PHY or SERDES. The PX1011A lets designers use an FPGA to create inexpensive, flexible PCI Express applications that have customer-specific functions coded into the FPGA. The result is greater differentiation in a format that is easily scalable to high-volume, consumer-oriented applications.

High-performance, low-power operation

The PCI Express standard specifies a maximum transmitter peak-to-peak jitter of 120 ps. The PX1011A delivers excellent transmit jitter and receive performance, with a bit error rate of better than $1x10^{-12}$.

The PX1011A's MAC interface is called the Philips PXPIPE interface, which is an enhanced version of the Intel PIPE standard. The PXPIPE interface improves performance in off-chip applications by using a source synchronous clock for transmit and receive data. The Intel PIPE uses PCLK to synchronize transmit and receive data, but the Philips PXPIPE uses separate clocks, thereby simplifying PCB layout. The 8-bit data interface operates at 250 MHz with SSTL2 signaling that is compatible with popular FPGA I/O interfaces.

To save power at every stage of operation, the PX1011A supports five modes of power management. Low power dissipation and a thin, small package let the PX1011A support new ExpressCard applications, using a sideband WAKE signal as a wakeup mechanism for the L2 power mode.

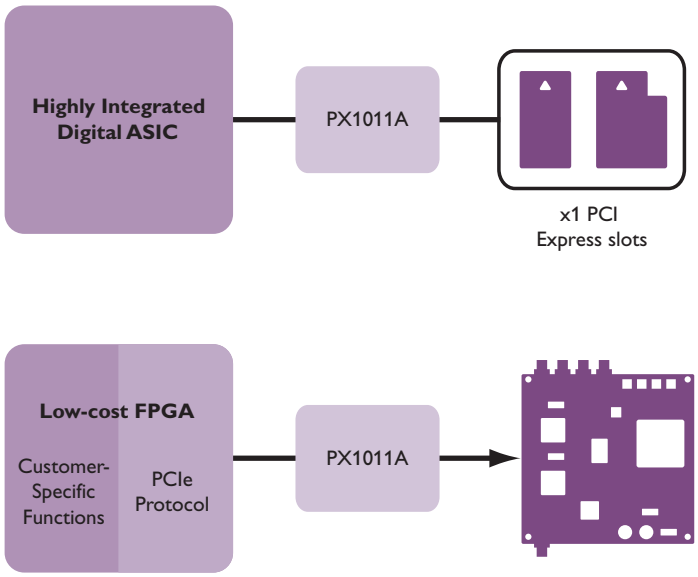
PHILIPS

Receiver operation

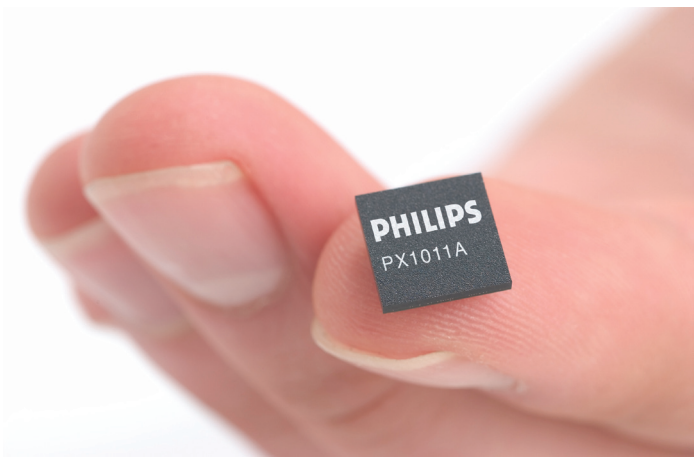
Incoming data enters the PX1011A at the receiver differential input interface and is converted from small-amplitude differential signals into rail-to-rail digital signals before being passed to a deserializer circuit. A Carrier Detect circuit determines whether data is present on the line and passes this information to the SERDES and PCS. The SERDES deserializes data into 10-bit parallel data. The PCS detects a 10-bit comma character (K28.5) from the random data stream, aligning bits into a 10-byte boundary format. The PCS then applies 8b/10b decoding to recover 8-bit data. An elastic buffer brings the resulting data to the right clock domain.

Transmitter operation

During transmission, 8-bit data from the PXPIPE interface is encoded using an 8b/10b encoding algorithm. Comma characters (K28.5) are added for byte synchronization at the receiver end. The redundancy of 8b/10b encoding ensures that serial data will be DC-balanced to avoid baseline wander in AC-coupled systems. It also ensures enough data transition for clock recovery at the receiver end.



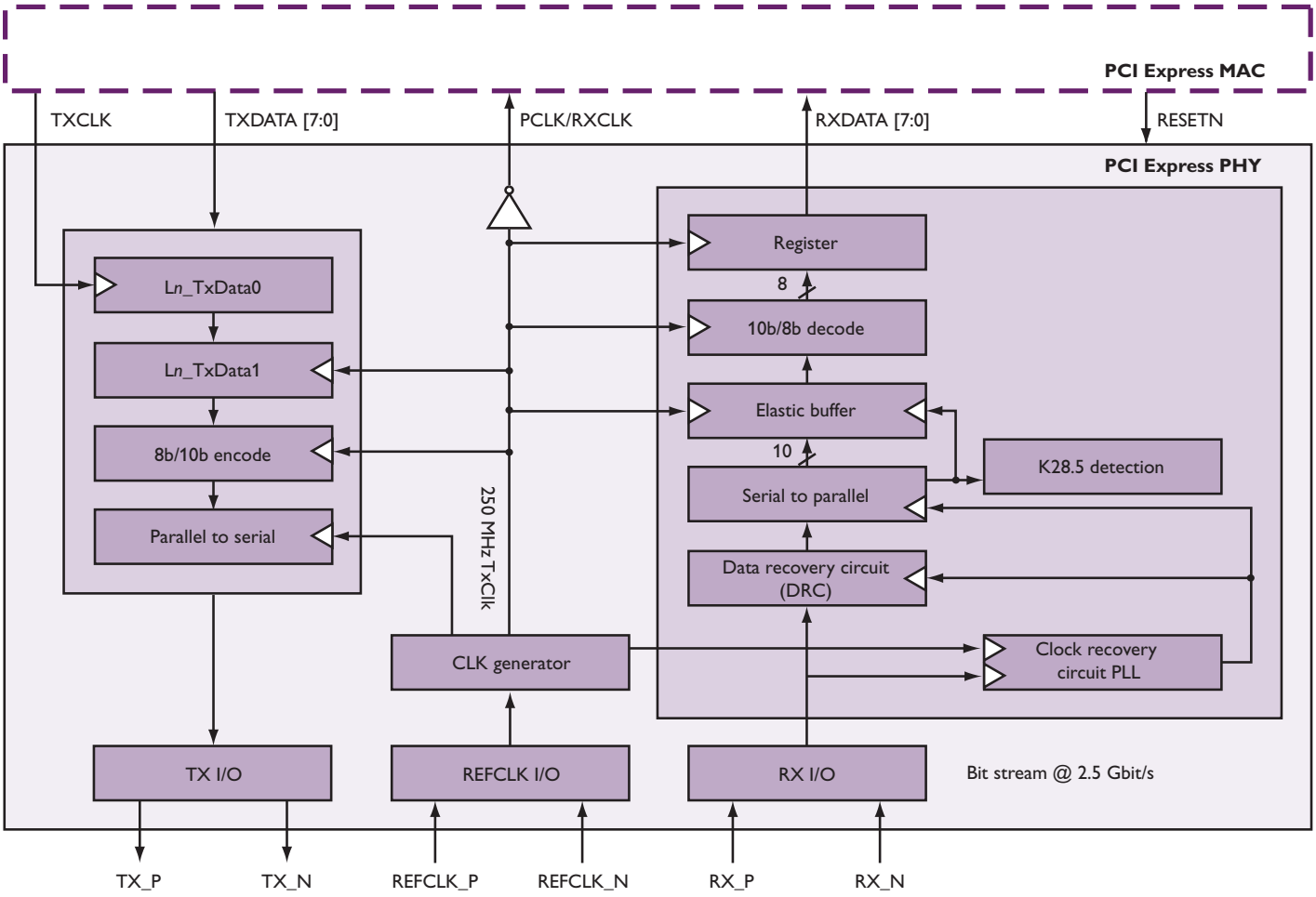
The PX1011A provides digital ASICs and low-cost FPGAs with mixed-signal PHY functionality



PX1011A's small package fits into applications of various sizes

Data is serialized and converted into small-amplitude differential signals. When multiple bits of the same polarity are transmitted, the second and subsequent bits are "de-emphasized" – effectively reducing the low-frequency components at the transmitter. This "transmitter pre-equalization" allows the received waveform to exhibit less inter-symbol interference at the receiver end, after its high-frequency components are attenuated in the transmission path. Transmitter de-emphasis is an effective way to expand the receiver eye pattern.

The transmit clock is generated from an on-chip PLL using a 100-MHz clock reference. The PLL has a relatively high bandwidth to pass through an optional spread spectrum and reduces EMI.



PX1011A block diagram

Sophisticated power management

Mode	Function
L0	Full active link
L0s	Standby state, low latency to go back to L0 Automatic transition from L0 to L0s without software intervention
L1	Low-power standby, directed by software
L2	Aggressive low power, relying on auxiliary power only (partial support)
L3	Power link off

Ordering Information

Type Number	Package	Dimensions
PX1011A-EL1/G	LFBGA81 (lead-free)	9 x 9 x 1.05 mm
PX1011A-EL1	LFBGA81 (leaded)	9 x 9 x 1.05 mm

For more information visit:
http://www.standardics.philips.com/products/pcie/phys/

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