PEX 8111AA
PCI Express-to-PCI Bridge

Data Book

Version 0.82

June 2005

Website www.plxtech.com
Technical Support www.plxtech.com/support/
Phone 408 774-9060
800 759-3735
FAX 408 774-2169

Revision History

Revision	Date	Description of Changes
0.01	March 14, 2004	Initial spec.
0.02	May 25, 2004	Add pinouts and preliminary electrical specs. Part name change to PEX 8111.
0.03	June 2, 2004	Remove Theory of Operation Chapters.
0.04	September 28, 2004	Update pinouts, registers.
0.05	October 26, 2004	Add 144 pin package.
0.06	November 15, 2004	Miscellaneous changes.
0.80	December 2, 2004	Blue Book Initial Release. Miscellaneous changes; change EERDDATA from pull-down to pull-up.
0.81	December 28, 2004	Update to Mechanical Drawing in Chapter 23. “Preliminary” removed from drawing, and critical dimensions now appear in table form. Miscellaneous changes.
0.82	June 3, 2005	Silicon Revision AA update. Clock speed changed from 33 to 66 MHz. Changed non-connected pin NC2 to 66 MHz Enable, M66EN. Added new “Testability and Debug” (JTAG) chapter. Added new General Information” appendix, which includes Product Ordering Information.

Copyright Information

Preface

The information contained in this document is subject to change without notice. This PLX Document to be updated periodically as new information is made available.

Scope

This document describes the PEX 8111 bridge operation and provides operational data for customer use.

Intended Audience

This data book provides the functional details of PLX Technology PEX 8111 for both hardware designers and software/firmware engineers. This data book assumes that the reader has access to and is familiar with the documents referenced below.

Supplemental Documentation

This data book assumes that the reader is familiar with the documents referenced below.

- PCI Special Interest Group (PCI-SIG)

  5440 SW Westgate Drive #217, Portland, OR 97221 USA

  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com
  - *PCI Local Bus Specification, Revision 2.3*
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  - *PCI Express Base Specification 1.0a*
  - *PCI Bus Power Management Interface Specification, Revision 1.1*
  - *PCI Express to PCI/PCI-X Bridge Specification 1.0*
- The Institute of Electrical and Electronics Engineers, Inc.

  445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA

  Tel: 800 678-4333 (domestic only) or 732 981-0060, Fax: 732 981-1721, http://www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  - *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*

Supplemental Documentation Abbreviations

Note: *In this data book, shortened titles are provided to the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
P-to-P Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Management r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PICMG 2.1 R2.0 PICMG 2.1	*R2.0 CompactPCI Hot Swap Specification*
PCI Express Bridge	*PCI Express to PCI/PCI-X Bridge Specification 1.0*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*

Data Assignment Conventions

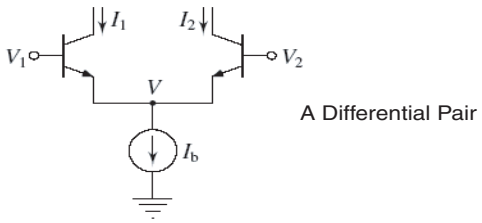
Data Width	PEX 8111 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32-bits)	DWORD/DWord/Dword
8 bytes (64-bits)	QWORD/QWord/Qword

General Definitions

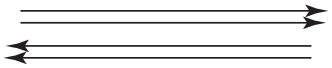
The ***root complex*** denotes the device that connects the CPU and memory subsystem to the PCI-E fabric. It may support 1 or more PCI-E ports.

A ***port*** is the interface between a PCI-E component and the ***link*** and consists of transmitters and receivers.

- An ***ingress*** port receives a packet.
- An ***egress*** port transmits a packet.
- A ***link*** is a physical connection between two devices that consists of xN ***lanes***.
- An x1 link consists of 1 transmit and 1 receive signal where each signal is a differential pair. This is one lane. There are four lines or signals in an x1 link.



A Differential Pair



A Differential Pair
in each direction
= one *Lane*

This is an *x1 Link*
There are four signals

A ***lane*** is a differential signal pair in each direction.

A ***switch*** appears to software as two or more logical PCI-to-PCI bridges.

Endpoints are devices, other than the root complex and switches, that are requesters or completers of PCI-E transactions.

- Endpoints may be PCI-E endpoints or ***legacy*** endpoints.
- ***Legacy*** endpoints may support I/O and locked transaction semantics.

  PCI-E endpoints do not.

A ***requester*** is a device that originates a transaction or puts a transaction sequence into the PCI-E fabric.

A ***completer*** is a device addressed by a requester.

A ***non-posted request packet*** sent by a requester has a completion packet returned by the associated completer.

A ***posted request packet*** sent by a requester has no completion packet returned by the completer.

PCI Express defines three layers:

- ***Transaction Layer*** **-** The primary function of the Transaction Layer is assembly and disassembly of TLPs. The major components of a TLP are: Header, Data Payload, and an optional Digest Field.
- ***Data Link Layer*** - The primary task of the link layer is to provide link management and data integrity, including error detection and correction. It defines the data control for PCI Express.
- ***Physical Layer*** **-** The primary value to end users is that this layer appears to the upper layers to be PCI. It connects the lower protocols to the upper layers.

There are three packet types:

- ***TLP***, Transaction Layer Packet
- ***DLLP***, Data Link Layer Packet
- ***PLP***, Physical Layer Packet

A ***Transparent*** **bridge** provides connectivity from the conventional PCI or PCI-X bus system to the PCI Express hierarchy or subsystem. The bridge not only converts the physical bus to PCI Express point-to-point signaling; but it also translates the PCI or PCI-X bus protocol to PCI Express protocol. The Transparent bridge allows the address domain on one side of the bridge to be mapped into the CPU system hierarchy on the primary side of the bridge.

PCI-PCI Express Specific Acronyms

Acronym	Definition
#	Indicates an Active-Low signal
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge the receipt of a data packet. A signal that acknowledges the receipt of a signal.
ADB	Allowable Disconnect Boundary
ADQ	Allowable Disconnect Quantity. In PCI Express, the ADQ is a buffer size. It is used to indicate memory requirements or reserves.
BAR	Base Address Register
Byte	8-bit quantity of data.
CA	Completion with Completer Abort status.
CIS	Card Information Structure. Describes resource requirements and other characteristics of a PC card. The operating system uses this information to configure the device in Plug and Play operations.
Clock cycle	One period of the PCI bus clock.
CRS	Configuration Retry Status.
CSR	Configuration Status Register; Control and status register; Command and status register
DAC	Dual address cycle. A PCI transaction where a 64-bit address is transferred across a 32-bit data path in two clock cycles.
Destination Bus	The target of a transaction that crosses a bridge is said to reside on the destination bus.
DLLP	Data Link Layer Packet (originate at the Data Link Layer); can have Flow Control (FCx DLLPs) acknowledge packets (ACK and NAK DLLPs); and power management (PMx DLLPs).
DMA	Direct Memory Access. Method of transferring data between a device and main memory without intervention by the CPU.
Downstream	Transactions that are forwarded from the primary bus to the secondary bus of a bridge are said to be flowing downstream.
DWORD	32-bit quantity of data.
FCP	Flow Control Packet Devices on each link exchange FCPs, which carry *header* and *data payload* credit information for one of three packet types: posted requests, non-posted requests and completions.
Forward Bridge Mode	The primary bus is closest to the PCI Express Root Complex.
host	A host computer provides services to computers that connect to it on a network. It is considered to be in charge over the rest of the devices connected on the bus.
HwInit	Hardware initialized register or register bit: The register bits are initialized by either PEX 8111 hardware initialization mechanism or PEX 8111 EEPROM register initialization feature. The register bits are read-only after initialization and can only be reset with "Power Good Reset"
I	CMOS Input
I/O	CMOS Bi-Directional Input Output
LVDSRn	Differential low-voltage, high-speed, LVDS negative Receiver Inputs
LVDSRp	Differential low-voltage, high-speed, LVDS positive Receiver Inputs
LVDSTn	Differential low-voltage, high-speed, LVDS negative Transmitter Outputs
LVDSTp	Differential low-voltage, high-speed, LVDS positive Transmitter Outputs
MAM	Master Abort Mode
MSI	Message Signaled Interrupt
MWI	Memory Write and Invalidate
NAK	Negative Acknowledge
Non-Posted Transaction	A Memory Read, I/O Read or Write, or Configuration Read or Write that returns a completion to the master.
NS	No Snoop
O	CMOS Output
OD	Open Drain
Originating Bus	The master of a transaction that crosses a bridge is said to reside on the originating bus.
PCI	Peripheral Component Interconnect. A PCI bus is a high-performance bus that is 32-bit or 64-bit. It is designed to be used with devices that contain high-bandwidth requirements—for example the display subsystem. It is an I/O bus that can be configured dynamically.
PCI	PCI/PCI-X Compliant
PCI-E	PCI Express

PCI-PCI Express Specific Acronyms

Acronym	Definition
PCI Master (Initiator)	Drives the address phase and transaction boundary (FRAME#). Initiates a transaction and drives data handshaking (IRDY#) with the target.
PCI Target	Claims the transaction by asserting DEVSEL# and handshakes the transaction (TRDY#) with the initiator.
PCI Transaction	A read, write, read burst, or write burst operation on the PCI bus. It includes an address phase followed by one or more data phases.
PCI Transfer	During a transfer, data is moved from the source to the destination on the PCI bus. The assertion of TRDY# and IRDY# indicates a data transfer.
Posted Transaction	A memory write that does not return a completion to the master.
Primary Bus	The bus closest to the PCI Express Root Complex (Forward Bridge mode) or the PCI host CPU (Reverse Bridge mode).
PU	Signal is internally pulled up
QoS	Quality of Service
RCB	Read Boundary Completion
Reverse Bridge Mode	The primary bus is closest to the PCI host CPU.
R/W	Read-write register or register bit: The register bits are read-write and may be either set or cleared by software to the desired state.
R/W1C	Read-only status – write 1b to clear status register or register bit. The register bits indicate status when read. A status bit set by the system to 1b to indicate status may be cleared by writing a 1b to that bit.
R/W1CS	Read-only status – write 1b to clear status register or register bit: The register bits indicate status when read. A status bit set by the system to 1b to indicate status may be cleared by writing a 1b to that bit. Writing 0b does not have any effect. Bits are not initialized or modified by reset. Devices that consume AUX power preserve register values when AUX power consumption is enabled (either by way of AUX power or PME Enable).
R/WS	Read-Write register or bit: The register bits are read-write and may be either set or cleared by software to the desired state. Bits are not initialized or modified by reset. Devices that consume AUX power preserve register values when AUX power consumption is enabled (either by way of AUX power or PME Enable).
RC	Root Complex
RO	Relaxed Ordering
RO	Read only register or register bit: The register bits are read-only and cannot be altered by software. The register bits may be initialized by either PEX 8111 hardware initialization mechanism or PEX 8111 EEPROM register initialization feature
RX	Received Packet
SC	Successful Completion.
Secondary Bus	The bus farthest from the PCI Express Root Complex (Forward Bridge mode) or the PCI host CPU (Reverse Bridge mode).
STRAP	Strapping pads must be connected to H or L on the board
STS	PCIX Sustained Three-State Output, Driven High for One CLK before Float
TC	Traffic Class
TLP	Translation Layer Packet.
TP	Totem Pole
TS	Three-State Bi-Directional
TX	Transmitted Packet
Upstream	Transactions that are forwarded from the secondary bus to the primary bus of a bridge are said to be flowing upstream.
UR	Unsupported Request.
VC	Virtual Channel
Word	16-bit quantity of data.

Contents

Chapter 1 Introduction

1.1 Features

- PCI Express Specification Revision 1.0a Compliant
- PCI Specification Revision 3.0 Compliant
- Forward and reverse transparent bridging between PCI Express and the PCI bus
- PCI Express 1 Lane Port (1 virtual channel)
- PCI Express 2.5 GBps per direction
- PCI Express full split completion protocol
- PCI 32-bit 66 MHz Bus
- Internal PCI Arbiter supporting up to 4 external PCI Masters
- PCI Bus Power Management Interface 1.1 Compliant
- SPI EEPROM Port
- Internal 8 KByte shared RAM available to PCI Express and PCI buses
- Four GPIO pins
- Low power CMOS in 144 Pin PBGA or161 Pin FBGA Package
- 1.5V core operating voltage, 3.3V I/O, 5V Tolerant PCI

1.2 Overview

The PEX 8111 PCI Express to PCI Bridge allows for the use of ubiquitous PCI silicon with the high performance PCI Express Network. As PCI Express systems proliferate, there remain many applications that do not need the extensive bandwidth or performance features of PCI Express. With the PEX 8111, many existing chips and entire subsystems can be used with PCI Express motherboards without modification.

PCI Express Endpoint Interface

- Full 2.5 Gbps per direction
- Single lane and Single virtual channel operation
- Compatible with multi lane and multi virtual channel PCI Express chips
- Packetized serial traffic with PCI Express split completion protocol
- Data link layer CRC generator and checker.
- Automatic retry of bad packets
- Integrated low voltage differential drivers
- 8b/10b signal encoding
- In-band interrupts and messages
- Support of message signaled interrupts

PCI Bus Interface

- PCI Revision 3.0-compliant 32-bit, 66 MHz PCI interface
- PCI master controller allows PCI Express access to PCI target devices
- PCI target controller allows full transparent access to PCI Express resources
- PCI target controller allows memory-mapped access to shared RAM and configuration registers
- PCI arbiter supports up to four external PCI bus masters
- Support of power management registers and PME# pin
- Support of message signaled interrupts

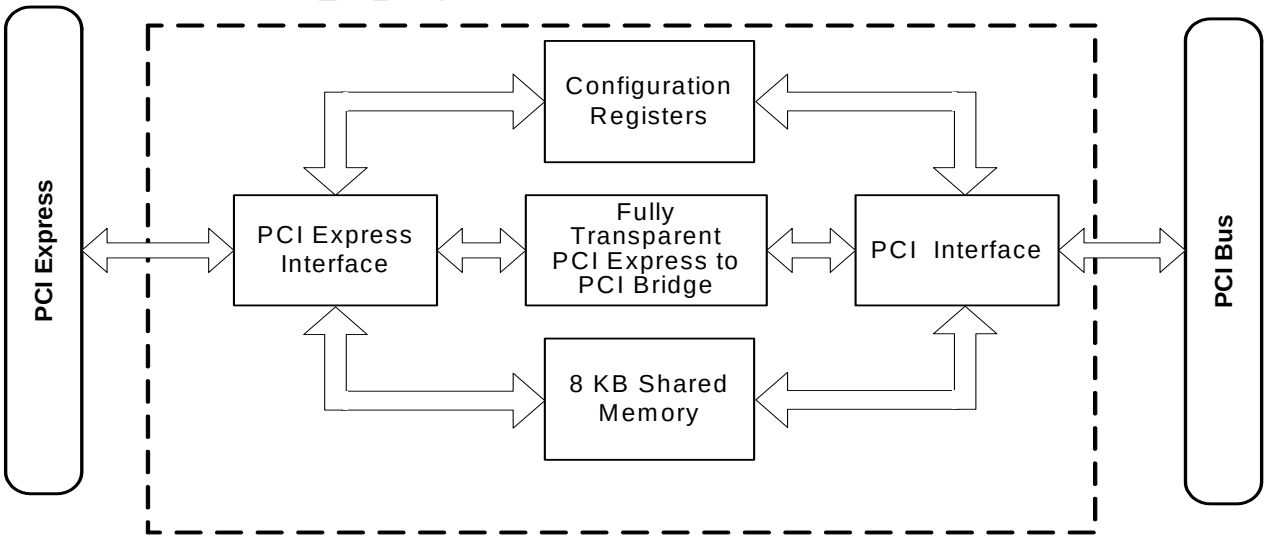
Configuration Registers

- All internal registers are accessible from the PCI Express or PCI buses
- All internal registers can be set up through an external EEPROM
- Internal registers allow write and read to an external EEPROM
- Internal registers allow control of GPIO pins

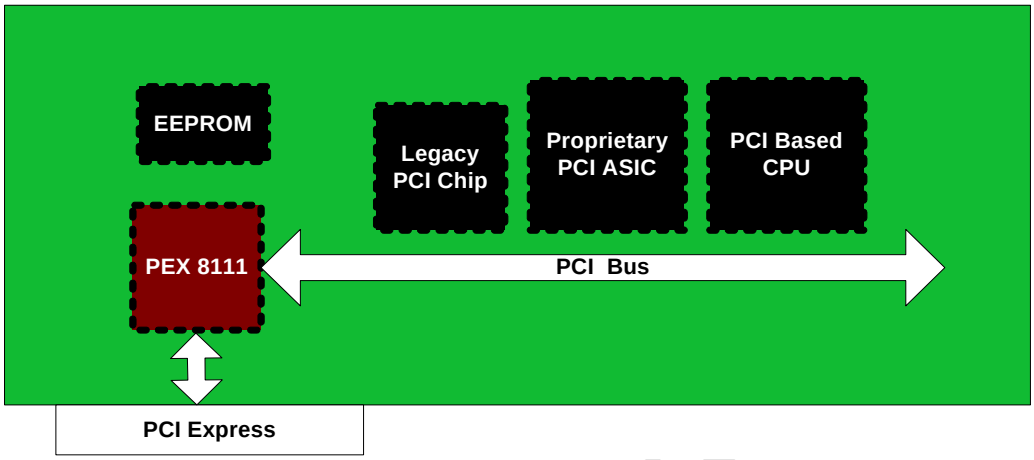
Data Transfer Pathways

- PCI transparent bridge access to PCI Express
- PCI memory-mapped single access to internal configuration registers
- PCI memory-mapped single/burst access to internal shared RAM
- PCI configuration access to PCI configuration registers (Reverse Bridge mode only)
- PCI Express transparent bridge access to PCI bus targets
- PCI Express memory-mapped single access to internal configuration registers
- PCI Express memory-mapped single/burst access to internal shared RAM
- PCI Express configuration access to PCI configuration registers (Forward Bridge mode only)

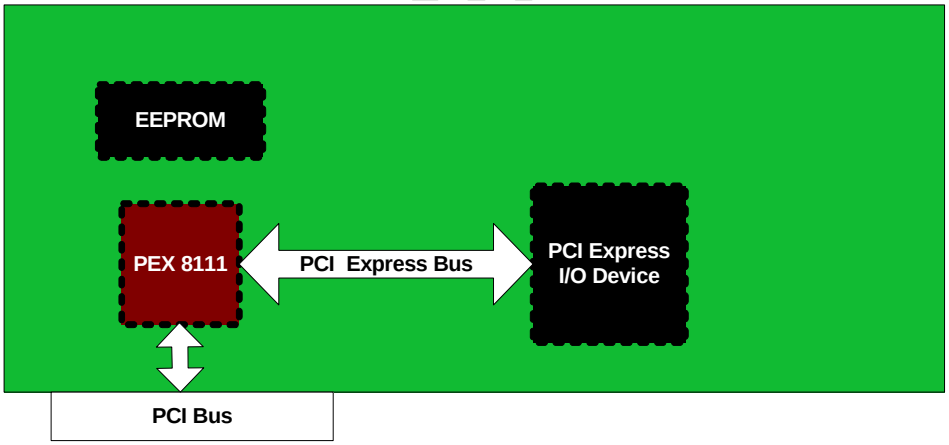
1.3 PEX 8111 Block Diagram



1.3.1 PEX 8111 Typical Forward Bridge Block Diagram



1.3.2 PEX 8111 Typical Reverse Bridge Block Diagram



Chapter 2 Pin Descriptions

2.1 Pin Description Abbreviations

Table 2-1. Pin Description Abbreviations (PBGA and FBGA Packages)

Abbreviation	Description
I	Input
O	Output
I/O	Bi-Directional
PCI	PCI-Compatible buffer, 26mA drive
DIFF	PCI Express Differential buffer
S	Schmitt Trigger
TS	Tri-State
STS	Sustained Tri-State, driven inactive one clock cycle before float
TP	Totem-Pole
OD	Open-Drain
PD	50K Pull-Down
PU	50K Pull-Up
#	Active low

2.2 Pin Description (144 Pin PBGA Package)

Table 2-2. Power and Ground (46 pins) (144 Pin PBGA Package)

Signal	Type	Pins	Description
AVDD	Power	E7	**Analog Supply Voltage.** Connect to the +1.5V supply.
AVSS	Ground	C7	**Analog Ground.** Connect to ground.
GND	Ground	A12, B4, C3, C11, D9, E6, F12, G5, H4, H7, J4, J8, K2, K10	**Ground.** Connect to ground
VDD_P	Power	D5	**PLL Supply Voltage.** Connect to the +1.5V filtered PLL supply.
VDD_R	Power	A7	**Receiver Supply Voltage.** Connect to the +1.5V supply.
VDD_T	Power	A5	**Transmitter Supply Voltage.** Connect to the +1.5V supply.
VDD1.5	Power	C10, D4, F6, F8, G6, G7, J9, K3	**Core Supply Voltage.** Connect to the +1.5V supply.
VDD3.3	Power	B3, B11, L2, M10	**I/O Supply Voltage.** Connect to the +3.3V supply.
VDD5	Power	F5, G8, H6	**PCI I/O Clamp Voltage.** Connect to the +5.0V supply for PCI buffers. In a 3.3V PCI environment, these pins can be connected to the 3.3V supply.
VDDQ	Power	E5, F9, G4, H5, H8, J7	**I/O Supply Voltage.** Connect to the +3.3V supply for PCI buffers.
VSS_C	Ground	D7	**Common Ground.** Connect to ground.
VSS_P0	Ground	D6	**PLL Ground.** Connect to ground.
VSS_P1	Ground	C6	**PLL Ground.** Connect to ground.
VSS_R	Ground	B8	**Receiver Ground.** Connect to ground.
VSS_RE	Ground	F7	**Receiver Ground.** Connect to ground.
VSS_T	Ground	C5	**Transmitter Ground.** Connect to ground.

Table 2-3. PCI Express Pins (9 pins) (144 Pin PBGA Package)

Signal Name	Type	Pins	Description
PERn0	I DIFF	B7	**Receive Minus.** PCI Express Differential Receive Signal
PERp0	I DIFF	A8	**Receive Plus.** PCI Express Differential Receive Signal
PERST#	I/O 6mA 3.3V	B12	**PCI Express Reset.** In Forward Bridge mode, this bit is an input. It resets the entire chip when asserted. In Reverse Bridge mode, this bit is an output. It is asserted when a PCI reset is detected.
PETn0	O DIFF	A4	**Transmit Minus.** PCI Express Differential Transmit Signal
PETp0	O DIFF	B5	**Transmit Plus.** PCI Express Differential Transmit Signal
REFCLK-	I DIFF	B6	**PCI Express Clock Input Minus.** PCI Express differential, 100 MHz spread spectrum reference clock. This signal is connected to the PCI Express bus REFCLK- pin in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
REFCLK+	I DIFF	A6	**PCI Express Clock Input Plus.** PCI Express differential, 100 MHz spread spectrum reference clock. This signal is connected to the PCI Express bus REFCLK+ pin in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
WAKEIN#	I 3.3V	C12	**Wake In Signal.** In Reverse Bridge mode, this signal is an input, and indicates that the PCI Express Device has requested a wakeup while the link is in the L2 state.
WAKEOUT#	OD 6mA 3.3V	A9	**Wake Out Signal.** In Forward Bridge mode, this signal is an output, and is asserted when the PME# pin is asserted and the link is in the L2 state.

Table 2-4. PCI Pins (63 pins) (144 Pin PBGA Package)

Signal	Type	Pins	Description
AD[31:0]	I/O TS PCI	J10, J12, J11, K12, L9, M9, K8, L8, K7, L7, M7, J6, K6, M6, L6, J5, H2, H1, G3, G2, G1, F4, F3, F2, E4, E3, E2, E1, D2, D1, C1, D3	**Address/Data Bus.** The PCI address and data are multiplexed onto the same bus. During the address phase, AD[31:0] contain the physical address of the transfer. During the data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M8, K5, H3, F1	**Command/Byte Enable Bus.** The bus command and byte enables are multiplexed onto the same bus. During the address phase, CBE[3:0]# contain the bus command. During the data phase, CBE[3:0]# contain the byte enables. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]). **CBE[3:0]#** — **Command** 0000 — Interrupt Acknowledge 0001 — Special Cycle 0010 — I/O Read 0011 — I/O Write 0100 — ***Reserved*** 0101 — ***Reserved*** 0110 — Memory Read 0111 — Memory Write 1000 — ***Reserved*** 1001 — ***Reserved*** 1010 — Configuration Read 1011 — Configuration Write 1100 — Memory Read Multiple 1101 — Dual Address Cycle 1110 — Memory Read Line 1111 — Memory Write and Invalidate
DEVSEL#	I/O STS PCI	K4	**Device Select.** This signal indicates that the target (bus slave) has decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	I/O STS PCI	M5	**Frame.** This signal is driven by the initiator, and indicates the beginning and duration of an access. When FRAME# is first asserted, the address phase is indicated. When FRAME# is negated, the transaction is in the last data phase.
GNT[3:0]#	I/O TS PCI	E11, F11, G9, G10	**Bus Grant.** These signals indicate that the central arbiter has granted the bus to an agent. If the internal PCI arbiter is enabled, these pins are outputs used to grant the bus to external devices. If the internal PCI arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8111.
IDSEL	I PCI	K9	**Initialization Device Select.** This signal is used as a chip select during Configuration Read and Write cycles. Each PCI slot or device typically has its IDSEL connected to a signal address line, allowing the PCI host to select individual sets of configuration registers. This pin is only used in Reverse Bridge mode. In Forward Bridge mode, it can either be grounded or pulled up to 3.3V.

Table 2-4. PCI Pins (63 pins) (144 Pin PBGA Package) *(Cont.)*

Signal	Type	Pins	Description
INTA#, INTB#, INTC#, INTD#	I/O OD PCI	E12, E9, D11, E10	**Interrupt.** These signals are asserted to request an interrupt. Once asserted, it must remain asserted until the device driver clears it. INTx# is level sensitive and is asynchronous to the CLK. In Forward Bridge mode, INTx# is an input from PCI devices. All INTx# signals are mapped into Assert_INTx and Deassert_INTx messages on the PCI Express side. In Reverse Bridge mode, INTx# is an output to the PCI Central Resource Function. All Assert_INTx and Deassert_INTx PCI Express messages are translated to INTx# transitions on the PCI side.
IRDY#	I/O STS PCI	L5	**Initiator Ready.** This signal indicates that the initiator (bus master) is ready to transfer data. A data phase is completed when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	M3	**Lock an Atomic Operation.** Indicates an atomic operation to a bridge that may require multiple transactions to complete. It is an output in Forward Bridge mode and an input in Reverse Bridge mode.
M66EN	I PCI	D10	**66 MHz Enable.** Indicates whether the PCI bus is operating at 33 or 66 MHz. When low, and the PCLKO divider is 3, then the PCLKO pin oscillates at 33 MHz with a 50 percent duty cycle. When high, and the PCLKO divider is 3, then the PCLKO pin oscillates at 66 MHz with a 33 percent duty cycle. This pin can be read using the **PCICTL** register, bit 7. In 33-MHz systems, this pin should be grounded.
PAR	I/O TS PCI	J1	**Parity.** Even parity is generated across AD[31:0], and C/BE[3:0]#. This means that the number of '1's on AD[31:0], C/BE[3:0]#, and PAR is an even number. PAR is valid one clock after the address phase. For data phases, PAR is valid one clock after IRDY# is asserted on write cycles, and one clock after TRDY# is asserted on read cycles. PAR has the same timing as AD[31:0], except delayed by one clock cycle. The bus initiator drives PAR for address and write data phases, and the target drives PAR for read data phases.
PCIRST#	I/O OD PCI	F10	**PCI Reset.** In Forward Bridge mode, this pin is driven when either a PCI Express reset is detected, or when the Secondary Bus Reset bit in the Bridge Control register is set. In Reverse Bridge mode, this is an input pin that resets the entire chip. Reset is asserted and negated asynchronously to CLK, and is used to bring a PCI device to an initial state. All PCI signals are asynchronously tri-stated during reset.
PCLKI	I PCI	D12	**PCI Clock Input.** All PCI signals, except RST# and interrupts, are sampled on the rising edge of this clock. The frequency can vary from 0 to 66 MHz. This clock needs to be oscillating during the EEPROM initialization sequence.
PERR#	I/O STS PCI	J3	**Parity Error.** This signal indicates that a data parity error has occurred. It is driven active by the receiving agent two clocks following the data that had bad parity.
PMEIN#	I S PCI	H12	**Power Management Event In**. This pin as an input used to monitor requests to change the system's power state. This pin is only valid in Forward Bridge mode.
PMEOUT#	OD 24mA 3.3V	L12	**Power Management Event Out.** This pin is an open-drain output used to request a change in the power state. This pin is only valid in Reverse Bridge mode. This pin is **not** 5V tolerant. If it is used in a system with a 5V pull-up resistor on the PME# signal, then an external voltage translation circuit is required.

Table 2-4. PCI Pins (63 pins) (144 Pin PBGA Package) *(Cont.)*

Signal	Type	Pins	Description
REQ[3:0]#	I/O TS PCI	H11, G12, H9, G11	**Bus Request.** These signals indicate that an agent desires use of the bus. If the internal PCI arbiter is enabled, these pins are inputs used to service external bus requests. If the internal PCI arbiter is disabled, REQ0# is an output used to request control of the bus.
SERR#	I/O OD PCI	J2	**System Error.** This signal indicates that an address parity error, data parity error on the Special Cycle command, or other catastrophic error has occurred. It is driven active for one PCI clock period, and is synchronous to the CLK. This signal is only driven in Reverse Bridge mode.
STOP#	I/O STS PCI	L4	**Stop.** This signal indicates that the target (bus slave) is requesting that the master stop the current transaction. Once STOP# is asserted, it must remain asserted until FRAME# is negated, whereupon STOP# must be negated. Also, DEVSEL# and TRDY# cannot be changed until the current data phase completes. STOP# must be negated in the clock following the completion of the last data phase, and must be tri-stated in the next clock. Data is transferred when IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI	M4	**Target Ready.** This signal indicates that the target (bus slave) is ready to transfer data. A data phase is completed when both IRDY# and TRDY# are asserted.

Table 2-5. Clocks, Reset, Miscellaneous (14 pins) (144 Pin PBGA Package)

Signal	Type	Pins	Description
EECLK	O 3mA TP 3.3V	B2	**EEPROM Clock.** This pin provides the clock to the EEPROM. The frequency of this pin is determined by the **EECLKFREQ** register, and can vary from 2 MHz to 25 MHz.
EECS#	O 3mA TP 3.3V	C4	**EEPROM Chip Select.** Active low chip select.
EERDDATA	I 3.3V	A1	**EEPROM Read Data.** This pin is used to read data from the device. A 47K pull-up resistor is required on this pin.
EEWRDATA	O 3mA TP 3.3V	A2	**EEPROM Write Data.** This pin is used to write data to the device.
EXTARB	I 3.3V	K11	**External Arbiter Enable.** When low, the internal PCI arbiter services requests from an external PCI device. When high, the PEX 8111 requests the PCI bus from an external arbiter.
FORWARD	I 3.3V	L11	**Bridge Select.** When low, the chip acts as a PCI to PCI Express Bridge (reverse bridge). When this bit is high, the chip acts as a PCI Express to PCI Bridge (forward bridge).
GPIO[3:0]	I/O 12mA 3.3V	A11, B10, A10, C9	**General Purpose I/O.** Each of these bits can be programmed as either an input or output general-purpose pin. Interrupts can be generated on each of the pins that are programmed as inputs.
NC1, NC3	—	C2, E8	**No Connect.** These pins must be left open.
PCLKO	O 26mA TP PCI	H10	**PCI Clock Output.** This pin is a buffered clock output from the internal 100 MHz reference clock, with the frequency depending on the ***PCLKO Clock Frequency*** field of the **DEVINIT** register.
PWR_OK	O 6mA 3.3V	B9	**Power OK.** When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the **POWER** register, this pin is asserted. It is only valid in Forward Bridge mode.

Table 2-6. Test Pins (12 pins) (144 Pin PBGA Package)

Signal	Type	Pins	Description
BUNRI	I	D8	**Test Mode Select.** Connect to ground for normal operation.
TEST	I	A3	**Test Mode Select.** Connect to ground for normal operation.
SMC	I	K1	**Scan Path Mode Control.** Connect to ground for normal operation.
TMC	I	C8	**Test Mode Control.** Connect to ground for normal operation.
TMC1	I	B1	**IDDQ Test Control Input.** Connect to ground for normal operation.
TMC2	I	M1	**I/O Buffer Control.** Connect to ground for normal operation.
BTON	I	M11	**Test Enable.** Connect to ground for normal operation.
TDI	I PU	L3	**Test Data Input.** This pin is the serial data input to all JTAG instruction and data registers. The state of the TAP (Test Access Port) controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. This pin should be left open if JTAG is not used.
TDO	O 12mA TS 3.3V	L1	**Test Data Output.** This pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times. This pin should be left open if JTAG is not used.
TCK	I	M2	**Test Clock.** This pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers provided in the PEX 8111. This pin should be left open if JTAG is not used.
TMS	I PU	M12	**Test Mode Select.** This pin is the mode input signal to the TAP Controller. The TAP controller is a 16-state FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. This pin should be left open if JTAG is not used.
TRST#	I PU	L10	**Test Reset.** This pin resets the JTAG TAP controller when driven to ground. This pin should be left open if JTAG is not used.

2.2.1 Pin Tables (144 Pin PBGA Package)

Table 2-7. Grid Order (144 Pin PBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
A1	EERDDATA	D1	AD2	G1	AD11	K1	SMC
A2	EEWRDATA	D2	AD3	G2	AD12	K2	GND
A3	TEST	D3	AD0	G3	AD13	K3	VDD1.5
A4	PETn0	D4	VDD1.5	G4	VDDQ	K4	DEVSEL#
A5	VDD_T	D5	VDD_P	G5	GND	K5	CBE2#
A6	REFCLK+	D6	VSS_P0	G6	VDD1.5	K6	AD19
A7	VDD_R	D7	VSS_C	G7		K7	AD23
A8	PERp0	D8	BUNRI	G8	VDD5	K8	AD25
A9	WAKEOUT#	D9	GND	G9	GNT1#	K9	IDSEL
A10	GPIO1	D10	M66EN	G10	GNT0#	K10	GND
A11	GPIO3	D11	INTC#	G11	REQ0#	K11	EXTARB
A12	GND	D12	PCLKI	G12	REQ2#	K12	AD28
B1	TMC1	E1	AD4	H1	AD14	L1	TDO
B2	EECLK	E2	AD5	H2	AD15	L2	VDD3.3
B3	VDD3.3	E3	AD6	H3	CBE1#	L3	TDI
B4	GND	E4	AD7	H4	GND	L4	STOP#
B5	PETp0	E5	VDDQ	H5	VDDQ	L5	IRDY#
B6	REFCLK-	E6	GND	H6	VDD5	L6	AD17
B7	PERn0	E7	AVDD	H7	GND	L7	AD22
B8	VSS_R	E8	NC3	H8	VDDQ	L8	AD24
B9	PWR_OK	E9	INTB#	H9	REQ1#	L9	AD27
B10	GPIO2	E10	INTD#	H10	PCLKO	L10	TRST#
B11	VDD3.3	E11	GNT3#	H11	REQ3#	L11	FORWARD
B12	PERST#	E12	INTA#	H12	PMEIN#	L12	PMEOUT#
C1	AD1	F1	CBE0#	J1	PAR	M1	TMC2
C2	NC1	F2	AD8	J2	SERR#	M2	TCK
C3	GND	F3	AD9	J3	PERR#	M3	LOCK#
C4	EECS#	F4	AD10	J4	GND	M4	TRDY#
C5	VSS_T	F5	VDD5	J5	AD16	M5	FRAME#
C6	VSS_P1	F6	VDD1.5	J6	AD20	M6	AD18
C7	AVSS	F7	VSS_RE	J7	VDDQ	M7	AD21
C8	TMC	F8	VDD1.5	J8	GND	M8	CBE3#
C9	GPIO0	F9	VDDQ	J9	VDD1.5	M9	AD26
C10	VDD1.5	F10	PCIRST#	J10	AD31	M10	VDD3.3
C11	GND	F11	GNT2#	J11	AD29	M11	BTON
C12	WAKEIN#	F12	GND	J12	AD30	M12	TMS

Table 2-8. Signal Order (144 Pin PBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
D3	AD0	F1	CBE0#	E9	INTB#	M1	TMC2
C1	AD1	H3	CBE1#	D11	INTC#	M12	TMS
D1	AD2	K5	CBE2#	E10	INTD#	M4	TRDY#
D2	AD3	M8	CBE3#	L5	IRDY#	L10	TRST#
E1	AD4	K4	DEVSEL#	M3	LOCK#	D5	VDD_P
E2	AD5	B2	EECLK	C2	NC1	A7	VDD_R
E3	AD6	C4	EECS#	D10	M66EN	A5	VDD_T
E4	AD7	A1	EERDDATA	E8	NC3	C10	VDD1.5
F2	AD8	A2	EEWRDATA	J1	PAR	D4	
F3	AD9	K11	EXTARB	F10	PCIRST#	F6	
F4	AD10	L11	FORWARD	D12	PCLKI	F8	
G1	AD11	M5	FRAME#	H10	PCLKO	G6	
G2	AD12	A12	GND	B7	PERn0	G7	
G3	AD13	B4		A8	PERp0	J9	
H1	AD14	C3		J3	PERR#	K3	
H2	AD15	C11		B12	PERST#	B3	VDD3.3
J5	AD16	D9		A4	PETn0	B11	
L6	AD17	E6		B5	PETp0	L2	
M6	AD18	F12		H12	PMEIN#	M10	
K6	AD19	G5		L12	PMEOUT#	F5	VDD5
J6	AD20	H4		B9	PWR_OK	G8	
M7	AD21	H7		B6	REFCLK-	H6	
L7	AD22	J4		A6	REFCLK+	E5	VDDQ
K7	AD23	J8		G11	REQ0#	F9	
L8	AD24	K2		H9	REQ1#	G4	
K8	AD25	K10		G12	REQ2#	H5	
M9	AD26	G10	GNT0#	H11	REQ3#	H8	
L9	AD27	G9	GNT1#	J2	SERR#	J7	
K12	AD28	F11	GNT2#	K1	SMC	D7	VSS_C
J11	AD29	E11	GNT3#	L4	STOP#	D6	VSS_P0
J12	AD30	C9	GPIO0	M2	TCK	C6	VSS_P1
J10	AD31	A10	GPIO1	L3	TDI	B8	VSS_R
E7	AVDD	B10	GPIO2	L1	TDO	F7	VSS_RE
C7	AVSS	A11	GPIO3	A3	TEST	C5	VSS_T
M11	BTON	K9	IDSEL	C8	TMC	C12	WAKEIN#
D8	BUNRI	E12	INTA#	B1	TMC1	A9	WAKEOUT#

2.2.2 Physical Pin Assignment (144 Pin PBGA) — Bottom View

M	L	K	J	H	G	F	E	D	C	B	A	
TMS	PMEOUT#	AD28	AD30	PMEIN#	REQ2#	GND	INTA#	PCLKI	WAKEIN#	PERST#	GND	12
BTON	FORWARD	EXTARB	AD29	REQ3#	REQ0#	GNT2#	GNT3#	INTC#	GND	VDD3.3	GPIO3	11
VDD3.3	TRST#	GND	AD31	PCLKO	GNT0#	PCIRST#	INTD#	M66EN	VDD1.5	GPIO2	GPIO1	10
AD26	AD27	IDSEL	VDD1.5	REQ1#	GNT1#	VDDQ	INTB#	GND	GPIO0	PWR_OK	WAKEOUT#	9
CBE3#	AD24	AD25	GND	VDDQ	VDD5	VDD1.5	NC3	BUNRI	TMC	VSS_R	PERp0	8
AD21	AD22	AD23	VDDQ	GND	VDD1.5	VSS_RE	AVDD	VSS_C	AVSS	PERn0	VDD_R	7
AD18	AD17	AD19	AD20	VDD5	VDD1.5	VDD1.5	GND	VSS_P0	VSS_P1	REFCLK-	REFCLK+	6
FRAME#	IRDY#	CBE2#	AD16	VDDQ	GND	VDD5	VDDQ	VDD_P	VSS_T	PETp0	VDD_T	5
TRDY#	STOP#	DEVSEL#	GND	GND	VDDQ	AD10	AD7	VDD1.5	EECS#	GND	PETn0	4
LOCK#	TDI	VDD1.5	PERR#	CBE1#	AD13	AD9	AD6	AD0	GND	VDD3.3	TEST	3
TCK	VDD3.3	GND	SERR#	AD15	AD12	AD8	AD5	AD3	NC1	EECLK	EEWRDATA	2
TMC2	TDO	SMC	PAR	AD14	AD11	CBE0#	AD4	AD2	AD1	TMC1	EERDDATA	1

2.3 Pin Description (161 Pin FBGA Package)

Table 2-9. Power and Ground (46 pins) (161 Pin FBGA Package)

Signal	Type	Pins	Description
AVDD	Power	C8	**Analog Supply Voltage.** Connect to the +1.5V supply.
AVSS	Ground	C6	**Analog Ground.** Connect to ground.
GND	Ground	A4, C13, D5, D12, E4, E11, F11, J2, K4, K11, L4, M6, N9, P12	**Ground.** Connect to ground.
VDD_P	Power	B6	**PLL Supply Voltage.** Connect to the +1.5V filtered PLL supply.
VDD_R	Power	C7	**Receiver Supply Voltage.** Connect to the +1.5V supply.
VDD_T	Power	D6	**Transmitter Supply Voltage.** Connect to the +1.5V supply.
VDD1.5	Power	B10, C1, C14, G2, G13, L3, L11, N7	**Core Supply Voltage.** Connect to the +1.5V supply.
VDD3.3	Power	B4, C11, L10, N3	**I/O Supply Voltage.** Connect to the +3.3V supply.
VDD5	Power	G3, H13, L7	**PCI I/O Clamp Voltage.** Connect to the +5.0V supply for PCI buffers. In a 3.3V PCI environment, these pins can be connected to the 3.3V supply.
VDDQ	Power	F4, G12, H4, J12, L8, N5	**I/O Supply Voltage.** Connect to the +3.3V supply for PCI buffers.
VSS_C	Ground	D9	**Common Ground.** Connect to ground.
VSS_P0	Ground	D7	**PLL Ground.** Connect to ground.
VSS_P1	Ground	D8	**PLL Ground.** Connect to ground.
VSS_R	Ground	A9	**Receiver Ground.** Connect to ground.
VSS_RE	Ground	B8	**Receiver Ground.** Connect to ground.
VSS_T	Ground	A5	**Transmitter Ground.** Connect to ground.

Table 2-10. PCI Express Pins (9 pins) (161 Pin FBGA Package)

Signal Name	Type	Pins	Description
PERn0	I DIFF	B9	**Receive Minus.** PCI Express Differential Receive Signal
PERp0	I DIFF	A8	**Receive Plus.** PCI Express Differential Receive Signal
PERST#	I/O 6mA 3.3V	C12	**PCI Express Reset.** In Forward Bridge mode, this bit is an input. It resets the entire chip when asserted. In Reverse Bridge mode, this bit is an output. It is asserted when a PCI reset is detected.
PETn0	O DIFF	B5	**Transmit Minus.** PCI Express Differential Transmit Signal
PETp0	O DIFF	A6	**Transmit Plus.** PCI Express Differential Transmit Signal
REFCLK-	I DIFF	A7	**PCI Express Clock Input minus.** PCI Express differential, 100 MHz spread spectrum reference clock. This signal is connected to the PCI Express bus REFCLK- pin in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
REFCLK+	I DIFF	B7	**PCI Express Clock Input plus.** PCI Express differential, 100 MHz spread spectrum reference clock. This signal is connected to the PCI Express bus REFCLK+ pin in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
WAKEIN#	I 3.3V	D14	**Wake In Signal.** In Reverse Bridge mode, this signal is an input, and indicates that the PCI Express Device has requested a wakeup while the link is in the L2 state.
WAKEOUT#	OD 6mA 3.3V	A11	**Wake Out Signal.** In Forward Bridge mode, this signal is an output, and is asserted when the PME# pin is asserted and the link is in the L2 state.

Table 2-11. PCI Pins (62 pins) (162 Pin FBGA Package)

Signal	Type	Pins	Description
AD[31:0]	I/O TS PCI	L13, J11, K12, L12, M10, P11, P10, P9, L9, N8, P8, M8, M7, L6, N6, P7, K2, J3, J1, H2, H3, H1, G4, F3, F2, F1, E2, E3, E1, D3, D1, D2	**Address/Data Bus.** The PCI address and data are multiplexed onto the same bus. During the address phase, AD[31:0] contain the physical address of the transfer. During the data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M9, P6, K1, G1	**Command/Byte Enable Bus.** The bus command and byte enables are multiplexed onto the same bus. During the address phase, CBE[3:0]# contain the bus command. During the data phase, CBE[3:0]# contain the byte enables. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]). **CBE[3:0]#** — **Command** 0000 — Interrupt Acknowledge 0001 — Special Cycle 0010 — I/O Read 0011 — I/O Write 0100 — ***Reserved*** 0101 — ***Reserved*** 0110 — Memory Read 0111 — Memory Write 1000 — ***Reserved*** 1001 — ***Reserved*** 1010 — Configuration Read 1011 — Configuration Write 1100 — Memory Read Multiple 1101 — Dual Address Cycle 1110 — Memory Read Line 1111 — Memory Write and Invalidate
DEVSEL#	I/O STS PCI	M4	**Device Select.** This signal indicates that the target (bus slave) has decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	I/O STS PCI	L5	**Frame.** This signal is driven by the initiator, and indicates the beginning and duration of an access. When FRAME# is first asserted, the address phase is indicated. When FRAME# is negated, the transaction is in the last data phase.
GNT[3:0]#	I/O TS PCI	F12, G11, J13, J14	**Bus Grant.** These signals indicate that the central arbiter has granted the bus to an agent. If the internal PCI arbiter is enabled, these pins are outputs used to grant the bus to external devices. If the internal PCI arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8111.
IDSEL	I PCI	N10	**Initialization Device Select.** This signal is used as a chip select during Configuration Read and Write cycles. Each PCI slot or device typically has its IDSEL connected to a signal address line, allowing the PCI host to select individual sets of configuration registers. This pin is only used in Reverse Bridge mode. In Forward Bridge mode, it can either be grounded or pulled up to 3.3V.

Table 2-11. PCI Pins (62 pins) (162 Pin FBGA Package) *(Cont.)*

Signal	Type	Pins	Description
INTA#, INTB#, INTC#, INTD#	I/O OD PCI	F14, F13, E14, E13	**Interrupt**. These signals are asserted to request an interrupt. Once asserted, it must remain asserted until the device driver clears it. INTx# is level sensitive and is asynchronous to the CLK. In Forward Bridge mode, INTx# is an input from PCI devices. All INTx# signals are mapped into Assert_INTx and Deassert_INTx messages on the PCI Express side. In Reverse Bridge mode, INTx# is an output to the PCI Central Resource Function. All Assert_INTx and Deassert_INTx PCI Express messages are translated to INTx# transitions on the PCI side.
IRDY#	I/O STS PCI	P5	**Initiator Ready.** This signal indicates that the initiator (bus master) is ready to transfer data. A data phase is completed when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	P4	**Lock an Atomic Operation.** Indicates an atomic operation to a bridge that may require multiple transactions to complete. It is an output in Forward Bridge mode and an input in Reverse Bridge mode.
M66EN	I PCI	D13	**66 MHz Enable.** Indicates whether the PCI bus is operating at 33 or 66 MHz. When low, and the PCLKO divider is 3, then the PCLKO pin oscillates at 33 MHz with a 50 percent duty cycle. When high, and the PCLKO divider is 3, then the PCLKO pin oscillates at 66 MHz with a 33 percent duty cycle. This pin can be read using the **PCICTL** register, bit 7. In 33-MHz systems, this pin should be grounded.
PAR	I/O TS PCI	J4	**Parity.** Even parity is generated across AD[31:0], and C/BE[3:0]#. This means that the number of ‘1’s on AD[31:0], C/BE[3:0]#, and PAR is an even number. PAR is valid one clock after the address phase. For data phases, PAR is valid one clock after IRDY# is asserted on write cycles, and one clock after TRDY# is asserted on read cycles. PAR has the same timing as AD[31:0], except delayed by one clock cycle. The bus initiator drives PAR for address and write data phases, and the target drives PAR for read data phases.
PCIRST#	I/O OD PCI	G14	**PCI Reset.** In Forward Bridge mode, this pin is driven when either a PCI Express reset is detected, or when the Secondary Bus Reset bit in the Bridge Control register is set. In Reverse Bridge mode, this is an input pin that resets the entire chip. Reset is asserted and negated asynchronously to CLK, and is used to bring a PCI device to an initial state. All PCI signals are asynchronously tri-stated during reset
PCLKI	I PCI	E12	**PCI Clock Input.** All PCI signals, except RST# and interrupts, are sampled on the rising edge of this clock. The frequency can vary from 0 to 66 MHz. This clock needs to be oscillating during the EEPROM initialization sequence.
PERR#	I/O STS PCI	L2	**Parity Error**. This signal indicates that a data parity error has occurred. It is driven active by the receiving agent two clocks following the data that had bad parity.
PMEIN#	I S PCI	L14	**Power Management Event In**. This pin as an input used to monitor requests to change the power state of the system.This pin is only valid in Forward Bridge mode.
PMEOUT#	OD 24mA 3.3V	M14	**Power Management Event Out.** This pin is an open-drain output used to request a change in the power state. This pin is only valid in Reverse Bridge mode. This pin is **not** 5V tolerant. If it is used in a system with a 5V pull-up resistor on the PME# signal, then an external voltage translation circuit is required.

Table 2-11. PCI Pins (62 pins) (162 Pin FBGA Package) *(Cont.)*

Signal	Type	Pins	Description
REQ[3:0]#	I/O TS PCI	H11, H12, K13, K14	**Bus Request.** These signals indicate that an agent desires use of the bus. If the internal PCI arbiter is enabled, these pins are inputs used to service external bus requests. If the internal PCI arbiter is disabled, REQ0# is an output used to request control of the bus.
SERR#	I/O OD PCI	L1	**System Error.** This signal indicates that an address parity error, data parity error on the Special Cycle command, or other catastrophic error has occurred. It is driven active for one PCI clock period, and is synchronous to the CLK. This signal is only driven in Reverse Bridge mode.
STOP#	I/O STS PCI	N4	**Stop.** This signal indicates that the target (bus slave) is requesting that the master stop the current transaction. Once STOP# is asserted, it must remain asserted until FRAME# is negated, whereupon STOP# must be negated. Also, DEVSEL# and TRDY# cannot be changed until the current data phase completes. STOP# must be negated in the clock following the completion of the last data phase, and must be tri-stated in the next clock. Data is transferred when IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI	M5	**Target Ready.** This signal indicates that the target (bus slave) is ready to transfer data. A data phase is completed when both IRDY# and TRDY# are asserted.

Table 2-12. Clocks, Reset, Misc. (31 pins) (161 Pin FBGA Package)

Signal	Type	Pins	Description
EECLK	O 3mA TP 3.3V	C2	**EEPROM Clock.** This pin provides the clock to the EEPROM. The frequency of this pin is determined by the **EECLKFREQ** register, and can vary from 2 MHz to 25 MHz.
EECS#	O 3mA TP 3.3V	C5	**EEPROM Chip Select.** Active low chip select.
EERDDATA	I 3.3V	B3	**EEPROM Read Data.** This pin is used to read data from the device. A 47K pull-up resistor is required on this pin.
EEWRDATA	O 3mA TP 3.3V	A3	**EEPROM Write Data.** This pin is used to write data to the device.
EXTARB	I 3.3V	M12	**External Arbiter Enable.** When low, the internal PCI arbiter services requests from an external PCI device. When high, the PEX 8111 requests the PCI bus from an external arbiter.
FORWARD	I 3.3V	M13	**Bridge Select.** When low, the chip acts as a PCI to PCI Express Bridge (reverse bridge). When this bit is high, the chip acts as a PCI Express to PCI Bridge (forward bridge).
GPIO[3:0]	I/O 12mA 3.3V	B12, D11, A12, C10	**General Purpose I/O.** Each of these bits can be programmed as either an input or output general-purpose pin. Interrupts can be generated on each of the pins that are programmed as inputs.
NA	—	A1, A2, A13, A14, B1, B2, B13, B14, E5, N1, N2, N13, N14, P1, P2, P13, P14	**Not Available.** These pins are never used, and should be left open.
NC1, NC3	—	C3, A10	**No Connect.** These pins must be left open.
PCLKO	O 26mA TP PCI	H14	**PCI Clock Output.** This pin is a buffered clock output from the internal 100 MHz reference clock, with the frequency depending on the ***PCLKO Clock Frequency*** field of the **DEVINIT** register.
PWR_OK	O 6mA 3.3V	B11	**Power OK.** When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the **POWER** register, this pin is asserted. It is only valid in Forward Bridge mode.

Table 2-13. Test Pins (12 pins) (161 Pin FBGA Package)

Signal	Type	Pins	Description
BTON	I	M11	**Test Enable.** Connect to ground for normal operation.
BUNRI	I	C9	**Test Mode Select.** Connect to ground for normal operation.
SMC	I	K3	**Scan Path Mode Control**. Connect to ground for normal operation.
TCK	I	M2	**Test Clock.** This pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers provided in the PEX 8111. This pin should be left open if JTAG is not used.
TDI	I PU	P3	**Test Data Input.** This pin is the serial data input to all JTAG instruction and data registers. The state of the TAP (Test Access Port) controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. This pin should be left open if JTAG is not used.
TDO	O 12mA TS 3.3V	M3	**Test Data Output.** This pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times. This pin should be left open if JTAG is not used.
TEST	I	C4	**Test Mode Select.** Connect to ground for normal operation.
TMC	I	D10	**Test Mode Control.** Connect to ground for normal operation.
TMC1	I	D4	**IDDQ Test Control Input**. Connect to ground for normal operation.
TMC2	I	M1	**I/O Buffer Control**. Connect to ground for normal operation.
TMS	I PU	N12	**Test Mode Select.** This pin is the mode input signal to the TAP Controller. The TAP controller is a 16-state FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. This pin should be left open if JTAG is not used.
TRST#	I PU	N11	**Test Reset.** This pin resets the JTAG TAP controller when driven to ground. This pin should be left open if JTAG is not used.

2.3.1 Pin Tables (161 Pin FBGA Package)

Table 2-14. Grid Order (161 Pin FBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
A1	NA	C14	VDD1.5	H2	AD12	M5	TRDY#
A2		D1	AD1	H3	AD11	M6	GND
A3	EEWRDATA	D2	AD0	H4	VDDQ	M7	AD19
A4	GND	D3	AD2	H11	REQ3#	M8	AD20
A5	VSS_T	D4	TMC1	H12	REQ2#	M9	CBE3#
A6	PETp0	D5	GND	H13	VDD5	M10	AD27
A7	REFCLK-	D6	VDD_T	H14	PCLKO	M11	BTON
A8	PERp0	D7	VSS_P0	J1	AD13	M12	EXTARB
A9	VSS_R	D8	VSS_P1	J2	GND	M13	FORWARD
A10	NC3	D9	VSS_C	J3	AD14	M14	PMEOUT#
A11	WAKEOUT#	D10	TMC	J4	PAR	N1	NA
A12	GPIO1	D11	GPIO2	J11	AD30	N2	
A13	NA	D12	GND	J12	VDDQ	N3	VDD3.3
A14		D13	M66EN	J13	GNT1#	N4	STOP#
B1		D14	WAKEIN#	J14	GNT0#	N5	VDDQ
B2		E1	AD3	K1	CBE1#	N6	AD17
B3	EERDDATA	E2	AD5	K2	AD15	N7	VDD1.5
B4	VDD3.3	E3	AD4	K3	SMC	N8	AD22
B5	PETn0	E4	GND	K4	GND	N9	GND
B6	VDD_P	E5	NA	K11		N10	IDSEL
B7	REFCLK+	E11	GND	K12	AD29	N11	TRST#
B8	VSS_RE	E12	PCLKI	K13	REQ1#	N12	TMS
B9	PERn0	E13	INTD#	K14	REQ0#	N13	NA
B10	VDD1.5	E14	INTC#	L1	SERR#	N14	
B11	PWR_OK	F1	AD6	L2	PERR#	P1	
B12	GPIO3	F2	AD7	L3	VDD1.5	P2	
B13	NA	F3	AD8	L4	GND	P3	TDI
B14		F4	VDDQ	L5	FRAME#	P4	LOCK#
C1	VDD1.5	F11	GND	L6	AD18	P5	IRDY#
C2	EECLK	F12	GNT3#	L7	VDD5	P6	CBE2#
C3	NC1	F13	INTB#	L8	VDDQ	P7	AD16
C4	TEST	F14	INTA#	L9	AD23	P8	AD21
C5	EECS#	G1	CBE0#	L10	VDD3.3	P9	AD24
C6	AVSS	G2	VDD1.5	L11	VDD1.5	P10	AD25
C7	VDD_R	G3	VDD5	L12	AD28	P11	AD26
C8	AVDD	G4	AD9	L13	AD31	P12	GND
C9	BUNRI	G11	GNT2#	L14	PMEIN#	P13	NA
C10	GPIO0	G12	VDDQ	M1	TMC2	P14	
C11	VDD3.3	G13	VDD1.5	M2	TCK		
C12	PERST#	G14	PCIRST#	M3	TDO		
C13	GND	H1	AD10	M4	DEVSEL#		

Table 2-15. Signal Order (161 Pin FBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
D2	AD0	C2	EECLK	B1		M3	TDO
D1	AD1	C5	EECS#	B2		C4	TEST
D3	AD2	B3	EERDDATA	B13		D10	TMC
E1	AD3	A3	EEWRDATA	B14		D4	TMC1
E3	AD4	M12	EXTARB	E5		M1	TMC2
E2	AD5	M13	FORWARD	N1		N12	TMS
F1	AD6	L5	FRAME#	N2	NA	M5	TRDY#
F2	AD7	A4		N13		N11	TRST#
F3	AD8	C13		N14		B6	VDD_P
G4	AD9	D5		P1		C7	VDD_R
H1	AD10	D12		P2		D6	VDD_T
H3	AD11	E4		P13		B10	
H2	AD12	E11		P14		C1	
J1	AD13	F11	GND	C3	NC1	C14	
J3	AD14	J2		D13	M66EN	G2	VDD1.5
K2	AD15	K4		A10	NC3	G13	
P7	AD16	K11		J4	PAR	L3	
N6	AD17	L4		G14	PCIRST#	L11	
L6	AD18	M6		E12	PCLKI	N7	
M7	AD19	N9		H14	PCLKO	B4	
M8	AD20	P12		B9	PERn0	C11	VDD3.3
P8	AD21	J14	GNT0#	A8	PERp0	L10	
N8	AD22	J13	GNT1#	L2	PERR#	N3	
L9	AD23	G11	GNT2#	C12	PERST#	G3	
P9	AD24	F12	GNT3#	B5	PETn0	H13	VDD5
P10	AD25	C10	GPIO0	A6	PETp0	L7	
P11	AD26	A12	GPIO1	L14	PMEIN#	F4	
M10	AD27	D11	GPIO2	M14	PMEOUT#	G12	
L12	AD28	B12	GPIO3	B11	PWR_OK	H4	VDDQ
K12	AD29	N10	IDSEL	A7	REFCLK-	J12	
J11	AD30	F14	INTA#	B7	REFCLK+	L8	
L13	AD31	F13	INTB#	K14	REQ0#	N5	
C8	AVDD	E14	INTC#	K13	REQ1#	D9	VSS_C
C6	AVSS	E13	INTD#	H12	REQ2#	D7	VSS_P0
M11	BTON	P5	IRDY#	H11	REQ3#	D8	VSS_P1
C9	BUNRI	P4	LOCK#	L1	SERR#	A9	VSS_R
G1	CBE0#	A1		K3	SMC	B8	VSS_RE
K1	CBE1#	A2	NA	N4	STOP#	A5	VSS_T
P6	CBE2#	A13		M2	TCK	D14	WAKEIN#
M9	CBE3#	A14		P3	TDI	A11	WAKEOUT#
M4	DEVSEL#						

2.3.2 Physical Pin Assignment (161 Pin FBGA Package) — Bottom View

P	N	M	L	K	J	H	G	F	E	D	C	B	A	
NC	NC	PMEOUT#	PMEIN#	REQ0#	GNT0#	PCLKO	PCIRST#	INTA#	INTC#	WAKEIN#	VDD1.5	NC	NC	14
NC	NC	FORWARD	AD31	REQ1#	GNT1#	VDD5	VDD1.5	INTB#	INTD#	M66EN	GND	NC	NC	13
GND	TMS	EXTARB	AD28	AD29	VDDQ	REQ2#	VDDQ	GNT3#	PCLKI	GND	PERST#	GPIO3	GPIO1	12
AD26	TRST#	BTON	VDD1.5	GND	AD30	REQ3#	GNT2#	GND	GND	GPIO2	VDD3.3	PWR_OK	WAKEOUT#	11
AD25	IDSEL	AD27	VDD3.3							TMC	GPIO0	VDD1.5	NC3	10
AD24	GND	CBE3#	AD23							VSS_C	BUNRI	PERn0	VSS_R	9
AD21	AD22	AD20	VDDQ			Bottom View				VSS_P1	AVDD	VSS_RE	PERp0	8
AD16	VDD1.5	AD19	VDD5			(PEX 8111)				VSS_P0	VDD_R	REFCLK+	REFCLK-	7
CBE2#	AD17	GND	AD18							VDD_T	AVSS	VDD_P	PETp0	6
IRDY#	VDDQ	TRDY#	FRAME#						NC	GND	EECS#	PETn0	VSS_T	5
LOCK#	STOP#	DEVSEL#	GND	GND	PAR	VDDQ	AD9	VDDQ	GND	TMC1	TEST	VDD3.3	GND	4
TDI	VDD3.3	TDO	VDD1.5	SMC	AD14	AD11	VDD5	AD8	AD4	AD2	NC1	EERDDATA	EEWRDATA	3
NC	NC	TCK	PERR#	AD15	GND	AD12	VDD1.5	AD7	AD5	AD0	EECLK	NC	NC	2
NC	NC	TMC2	SERR#	CBE1#	AD13	AD10	CBE0#	AD6	AD3	AD1	VDD1.5	NC	NC	1

Chapter 3 Reset Summary

3.1 Forward Bridge Mode

Table 3-1 shows which device resources are reset when each of the forward bridge reset sources are asserted.

Table 3-1. Forward Bridge Reset

Device Resources / Reset Sources	PCI Express Interface Logic	PCI Interface Logic	PCI RST# Pin	Configuration Registers
PCI Express PERST# pin	X	X	X	X
PCI Express Link Down	X	X	X	X
PCI Express Hot Reset	X	X	X	X
Secondary Bus Reset bit		X	X	
D3 to D0 Power Management Reset	X	X	X	X

3.2 Reverse Bridge Mode

Table 3-2 shows which device resources are reset when each of the reverse bridge reset sources are asserted.

Table 3-2. Reverse Bridge Reset

Device Resources / Reset Sources	PCI Express Interface Logic	PCI Interface Logic	PCI PERST# Pin	PCI Express Hot Reset	Configuration Registers
PCI RST# pin	X	X	X	X	X
Secondary Bus Reset bit	X			X	
D3 to D0 Power Management Reset	X	X		X	X

3.3 Initialization Summary

Various initialization sequences of the PEX 8111 are described below:

- No EEPROM, blank EEPROM, or invalid EEPROM
  - If the EERDDATA pin is always high, then an invalid EEPROM is detected. In this case, the default PCI product ID (8111h) is selected. A 47K pull-up resistor ensures that EERDDATA is high if no EEPROM is installed.
  - Enable the PCI Express and PCI interfaces using default register values.
- Valid EEPROM with configuration register data.
  - Enable the PCI Express and PCI interfaces using register values loaded from the EEPROM. The interface enable bits in the **DEVINIT** register should be the last ones set by the EEPROM.

Chapter 4 EEPROM Controller

4.1 Overview

The PEX 8111 provides an interface to SPI (Serial Peripheral Interface) compatible serial EEPROMs. This interface consists of a chip select, clock, write data, and read data pins, and operates at up to 25 MHz. Some 128 byte EEPROMs compatible with this interface are the Atmel AT25010A, Catalyst CAT25C01, or ST Microelectronics M95010W. The PEX 8111 supports up to a 16 MB EEPROM, utilizing 1, 2, or 3 byte addressing. The appropriate addressing mode is determined automatically by the PEX 8111.

4.2 EEPROM Data Format

The data in the EEPROM is stored in the following format.

Table 4-1. EEPROM Data

Location	Value	Description
0	5A	Validation Signature
1	See Table 4-2	EEPROM Format Byte
2	REG BYTE COUNT (LSB)	Configuration register byte count (LSB)
3	REG BYTE COUNT (MSB)	Configuration register byte count (MSB)
4	REGADDR (LSB)	1st Configuration Register Address (LSB)
5	REGADDR (MSB)	1st Configuration Register Address (MSB)
6	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
10	REGADDR (LSB)	2nd Configuration Register Address (LSB)
11	REGADDR (MSB)	2nd Configuration Register Address (MSB)
12	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
13	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
14	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
15	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
……		
REG BYTE COUNT + 4	MEM BYTE COUNT (LSB)	Shared memory byte count (LSB)
REG BYTE COUNT + 5	MEM BYTE COUNT (MSB)	Shared memory byte count (MSB)
REG BYTE COUNT + 6	SHARED MEM (byte 0)	1st byte Shared memory
REG BYTE COUNT + 7	SHARED MEM (byte 1)	2nd byte of shared memory
……		
FFFF	SHARED MEM (byte n)	Last byte of shared memory

The EEPROM Format Byte is organized as follows.

Table 4-2. EEPROM Format Byte

Bits	Description
0	**Configuration Register Load.** When set, configuration registers are loaded from the EEPROM. The address of the first configuration register is located at bytes 3 and 4 in the EEPROM. If this bit is clear but REG BYTE COUNT is non-zero, the configuration data is read from the EEPROM and discarded.
1	**Shared Memory Load.** When set, the shared memory is loaded from the EEPROM starting at location REG BYTE COUNT + 6. The number of bytes to load is determined by the value in EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5.
7:2	***Reserved***

4.3 Initialization

After the device reset is de-asserted, the EEPROM internal status register is read to determine whether an EEPROM is installed. A pull-up resistor on the EERDDATA pin produces a value of 0xFF if there is no EEPROM installed. If an EEPROM is detected, the first byte is read. If a value of 'h5A is read, it is assumed that the EEPROM is programmed for the PEX 8111. If the first byte is not 'h5A, then the EEPROM is blank, or programmed with invalid data. In this case, the PCI Express and PCI interfaces are enabled for a default enumeration.

If the EEPROM has valid data, then the second byte (EEPROM Format Byte) is read to determine which sections of the EEPROM should be loaded into the PEX 8111 configuration registers and memory.

Bytes 2 and 3 determine how many EEPROM locations contain configuration register addresses and data. Each configuration register entry consists of two bytes of register address (bit 12 low selects the PCI configuration registers, and bit 12 high selects the memory-mapped configuration registers) and four bytes of register write data. If bit 1 of the EEPROM Format Byte is set, locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5 are read to determine how many bytes to transfer from the EEPROM into the shared memory.

The REG BYTE COUNT must be a multiple of 6 and MEM BYTE COUNT must be a multiple of 4.

The EECLK pin frequency is determined by the *EE Clock Frequency* field of the **EECLKFREQ** register. The default clock frequency is 2 MHz. At this clock rate, it takes about 24 µs per DWORD during configuration register or shared memory initialization. For faster loading of large EEPROMs that support a faster clock, the first configuration register load from the EEPROM could be to the **EECLKFREQ** register.

Note: *If operating in Reverse Bridge mode, be sure to have the EEPROM set the PCI Enable bit in the **DEVINIT** register. If operating in Forward Bridge mode, be sure to have the EEPROM set the PCI Express Enable bit in the **DEVINIT** register.*

4.4 EEPROM Random Read/Write Access

Either a PCI Express or PCI bus master can use the **EECTL** register to access the EEPROM. This register contains 8-bit read and write data fields, read and write start signals, and related status bits.

The following "C" routines demonstrate the firmware protocol required to access the EEPROM through the **EECTL** register. An interrupt can be generated whenever the EEPROM BUSY bit of the **EECTL** register goes from true to false.

4.4.1 EEPROM Opcodes

```
READ_STATUS_EE_OPCODE = 5
WREN_EE_OPCODE = 6
WRITE_EE_OPCODE = 2
READ_EE_OPCODE = 3
```

4.4.2 EEPROM Low-Level Access Routines

```
int EE_WaitIdle()
{
    int eeCtl, ii;
    for (ii = 0; ii < 100; ii++)
    {
        PEX 8111Read(EECTL, eeCtl);      /* read current value in EECTL */
        if ((eeCtl & (1 << EEPROM_BUSY)) == 0)    /* loop until idle */
            return(eeCtl);
    }
    PANIC("EEPROM Busy timeout!\n");
}
void EE_Off()
{
    EE_WaitIdle();          /* make sure EEPROM is idle */
    PEX 8111Write(EECTL, 0);/* turn off everything (especially EEPROM_CS_ENABLE)*/
}
int EE_ReadByte()
{
    int eeCtl = EE_WaitIdle();              /* make sure EEPROM is idle */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_READ_START);
    PEX 8111Write(EECTL, eeCtl);/* start reading */
    eeCtl = EE_WaitIdle();                   /* wait until read is done */
    return((eeCtl >> EEPROM_READ_DATA) & 0xff); /* extract read data from EECTL */
}
void EE_WriteByte(int val)
{
    int eeCtl = EE_WaitIdle();          /* make sure EEPROM is idle */
    eeCtl &= ~(0xff << EEPROM_WRITE_DATA);  /* clear current WRITE value */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_WRITE_START) |
             ((val & 0xff) << EEPROM_WRITE_DATA);
    PEX 8111Write(EECTL, eeCtl);
}
```

4.4.3 EEPROM Read Status Routine

```
...
EE_WriteByte(READ_STATUS_EE_OPCODE); /* read status opcode */
status = EE_ReadByte();              /* get EEPROM status */
EE_Off();                            /* turn off EEPROM */
...
```

4.4.4 EEPROM Write Data Routine

```
...
EE_WriteByte(WREN_EE_OPCODE);          /* must first write-enable */
EE_Off();                              /* turn off EEPROM */
EE_WriteByte(WRITE_EE_OPCODE);         /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM    /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);               /* send next byte of address */
EE_WriteByte(addr);                    /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    EE_WriteByte(buffer[ii]);          /* send data to be written */
}
EE_Off();                              /* turn off EEPROM */
...
```

4.4.5 EEPROM Read Data Routine

```
...
EE_WriteByte(READ_EE_OPCODE);         /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM   /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);               /* send next byte of address */
EE_WriteByte(addr);                    /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    buffer[ii] = EE_ReadByte(buffer[ii]);          /* store read data in buffer */
}
EE_Off();                              /* turn off EEPROM */
```

Chapter 5 Address Spaces

5.1 Introduction

The PEX 8111 supports the following address spaces:

- PCI-compatible configuration (00h to FFh; 256 bytes)
- PCI Express Extended configuration (100h to FFFh)
- I/O (32-bit)
- Memory-mapped I/O (32-bit non-prefetchable)
- Prefetchable memory (64-bit)

The first two spaces are used for accessing configuration registers, and is described in chapter on Configuration Transactions.

The PCI Express Extended configuration space (100h – FFFh) is only supported in Forward Bridge mode.

Table 5-1 lists which bus is primary or secondary for the two bridge modes of the PEX 8111.

Table 5-1. Primary and Secondary Bus Definitions for Forward or Reverse Mode

Bridge Mode	Primary Bus	Secondary Bus
Forward Bridge	PCI Express	PCI
Reverse Bridge	PCI	PCI Express

The other three address spaces determine which transactions are forwarded from the primary bus to the secondary bus and from the secondary bus to the primary bus. The memory and I/O ranges are defined by a set of base and limit registers in the configuration header. Transactions falling within the ranges defined by the base and limit registers are forwarded from the primary to secondary bus. Transactions falling outside these ranges are forwarded from the secondary bus to the primary bus.

The PEX 8111 does not perform any address translation (flat address space) as transactions cross the bridge.

5.2 I/O Space

The I/O addressing space determines whether to forward I/O Read or I/O Write transactions across the bridge. PCI Express uses the 32-bit Short Address Format (DWORD-aligned) for I/O transactions.

5.2.1 Enable Bits

The response of the bridge to I/O transactions is controlled by the following configuration register bits:

- *I/O Space Enable* bit in the **PCI Command** register
- *Bus Master Enable* bit in the **PCI Command** register
- *ISA Enable* bit in the **Bridge Control** register
- *VGA Enable* bit in the **Bridge Control** register
- *VGA 16-bit Decode* bit in the **Bridge Control** register

The *I/O Enable* bit must be set for any I/O transaction to be forwarded downstream. If this bit is not set, all I/O transactions on the secondary bus are forwarded to the primary bus. If this bit is not set in Forward Bridge mode, all primary interface I/O requests are completed with Unsupported Request status. If this bit is not set in Reverse Bridge mode, all I/O transactions are ignored (no DEVSEL# assertion) on the primary (PCI) bus.

The *Bus Master Enable* bit must be set for any I/O transaction to be forwarded upstream.

- If this bit is not set in Forward Bridge mode, all I/O transactions on the secondary (PCI) bus are ignored.
- If this bit is not set in Reverse Bridge mode, all I/O requests on the secondary (PCI Express) bus are completed with Unsupported Request status.

The *ISA Enable* and *VGA Enable* bits are discussed in the ISA and VGA mode sections.

5.2.2 I/O Base and Limit Registers

The following I/O Base and Limit configuration registers are used to determine whether to forward I/O transactions across the bridge.

- **I/O Base** (upper 4 bits of 8-bit register correspond to address bits 15:12)
- **I/O Base Upper** (16-bit register corresponds to address bits 31:16)
- **I/O Limit** (upper 4 bits of 8-bit register correspond to address bits 15:12)
- **I/O Limit Upper** (16-bit register correspond to address bits 31:16)

The I/O base consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits 15:12 of the I/O base address. The lower four bits of the 8-bit register determine the I/O address capability of this device. The 16 bits of the **I/O Base Upper** register define bits 31:16 of the I/O base address.

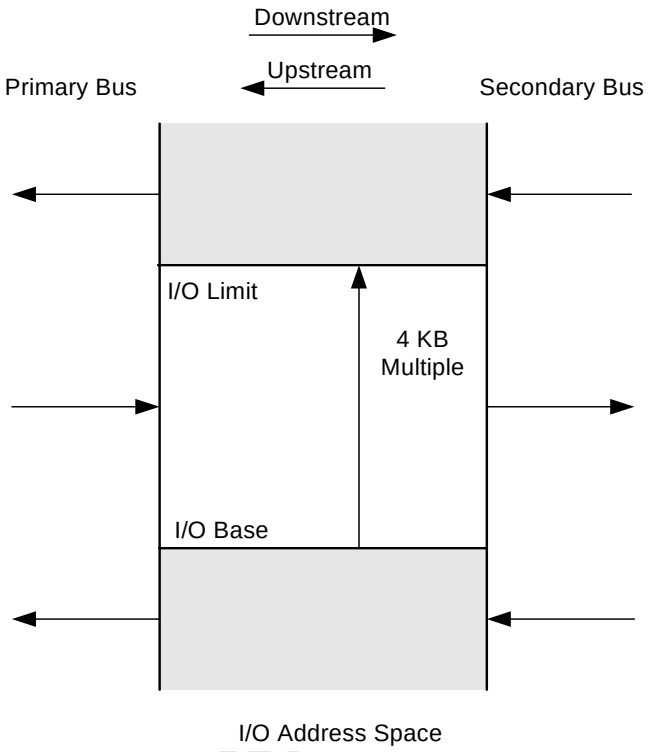
The I/O limit consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits 15:12 of the I/O limit. The lower four bits of the 8-bit register determine the I/O address capability of this device, and reflect the value of the same field in the **I/O Base** register. The 16 bits of the **I/O Limit Upper** register define bits 31:16 of the I/O limit.

Since address bits 11:0 are not included in the address space decoding, the I/O address range has a granularity of 4 KB, and is always aligned to a 4 KB boundary. The maximum I/O range is 4 GB.

I/O transactions on the primary bus that fall within the range defined by the base and limit are forwarded downstream to the secondary bus, and I/O transactions on the secondary bus that are within the range are ignored. I/O transactions on the primary bus that do not fall within the range defined by the base and limit are ignored, and I/O transactions on the secondary bus that do not fall within the range are forwarded upstream to the primary bus.

Figure 5-1 illustrates I/O forwarding.

Figure 5-1. I/O Forwarding



For 16-bit I/O addressing, if the **I/O Base** has a value greater than the **I/O Limit**, then the I/O range is disabled. For 32-bit I/O addressing, if the I/O base specified by the **I/O Base** and **I/O Base Upper** registers has a value greater than the I/O limit specified by the **I/O Limit** and **I/O Limit Upper** registers, then the I/O range is disabled. In these cases, all I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

5.2.3 ISA Mode

The ***ISA Enable*** bit in the **Bridge Control** register supports I/O forwarding in a system that has an ISA bus. The *ISA Enable* bit only affects I/O addresses that are within the range defined by the I/O base and limits registers, and are in the first 64 KB of the I/O addressing space.

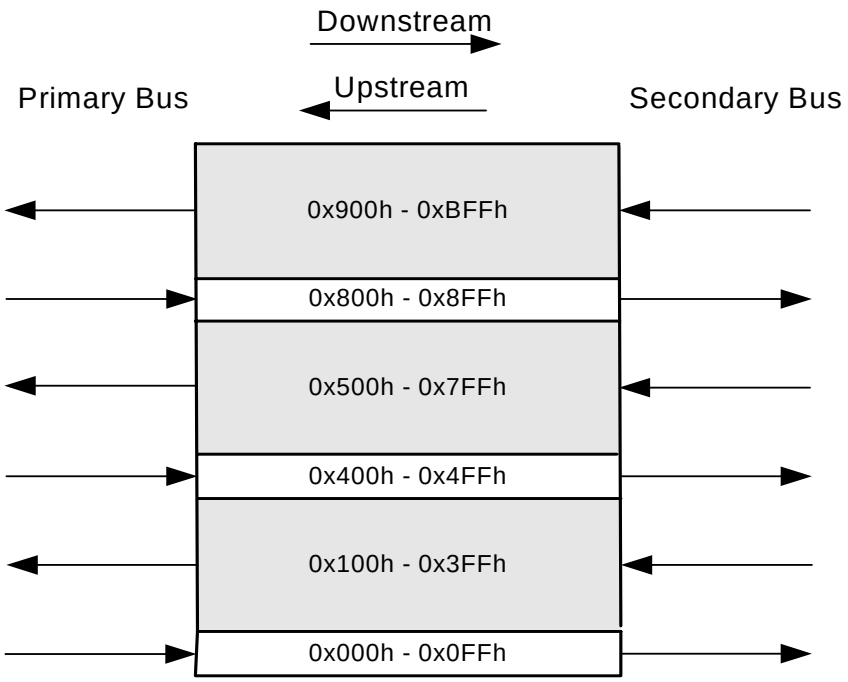
If the *ISA Enable* bit is set, the bridge does not forward downstream any I/O transactions on the primary bus that are in the top 768 bytes of each 1 KB block within the first 64 KB of address space. Only transactions in the bottom 256 bytes of each 1 KB block are forwarded downstream. If the *ISA Enable* bit is clear, then all addresses within the range defined by the I/O base and limit registers are forwarded downstream. I/O transactions with addresses above 64 KB are forwarded according to the range defined by the I/O base and limit registers.

If the *ISA Enable* bit is set, the bridge forwards upstream any I/O transactions on the secondary bus that are in the top 768 bytes of each 1 KB block within the first 64 KB of address space, even if the address is within the I/O base and limit. All other transactions on the secondary bus are forwarded upstream if they fall outside the range defined by the I/O base and limit registers. If the *ISA Enable* bit is clear, then all secondary bus I/O addresses outside the range defined by the I/O base and limit registers are forwarded upstream.

As with all upstream I/O transactions, the *Master Enable* bit in the **PCI Command** register must be set to enable upstream forwarding.

Figure 5-2 illustrates I/O forwarding with the *ISA Enable* bit set.

Figure 5-2. I/O Forwarding with the *ISA Enable* Bit Set



ISA I/O Address Space Example

5.2.4 VGA Mode

The *VGA Enable* bit in the **Bridge Control** register enables VGA register accesses to be forwarded downstream from the primary to secondary bus, independent of the I/O base and limit registers. The *VGA 16-bit Decode* bit selects between 10-bit and 16-bit VGA I/O address decoding, and is applicable when the *VGA Enable* bit is set.

The following VGA I/O addresses are controlled by the *VGA Enable* and *VGA 16-bit Decode* bits:

- Address bits 9:0 = 3B0h through 3BBh, and 3C0h through 3DFh (10-bit addressing)
- Address bits 15:0 = 3B0h through 3BBh, and 3C0h through 3DFh (16-bit addressing)

These ranges only apply to the first 64K of I/O address space.

5.2.4.1 VGA Palette Snooping

Separate VGA palette snooping is not supported by PCI Express to PCI bridges, but the PEX 8111 supports palette snooping in Reverse Bridge mode. In Forward Bridge mode, the VGA Enable bit determines whether the VGA palette accesses are forwarded from PCI Express to PCI. The VGA Snoop Enable bit is forced to 0 in Forward Bridge mode.

The following I/O addresses are used by VGA graphic devices to control the palette:

- Address bits 9:0 = 3C6h, 3C8h, and 3C9h

The PEX 8111 supports the following three modes of palette snooping:

- Ignore VGA palette accesses if there are no graphics agents downstream that need to snoop or respond to VGA palette access cycles (reads or writes).
- Positively decode and forward VGA palette writes if there are graphics agents downstream of the PEX 8111 that need to snoop palette writes (reads are ignored).
- Positively decode and forward VGA palette reads and writes if there are graphics agents downstream that need to snoop or respond to VGA palette access cycles (reads or writes).

The *VGA Enable* bit in the **Bridge Control** register and the *VGA Snoop Enable* bit in the **PCI Command** register select the bridge response to palette accesses as listed in Table 5-2.

Table 5-2. Bridge Response to Palette Access

VGA Enable	VGA Snoop Enable	Response to Palette Accesses
0	0	Ignore all palette accesses
0	1	Positively decode palette writes (ignore reads)
1	x	Positively decode palette reads and writes

5.3 Memory-Mapped I/O Space

The memory-mapped I/O addressing space determines whether to forward non-prefetchable memory read or write transactions across the bridge. Devices that have side-effects during reads, such as FIFOs, should be mapped into this space. For PCI to PCI Express reads, prefetching occurs in this space only if the Memory Read Line or Memory Read Multiple commands are issued on the PCI bus. For PCI Express to PCI reads, the number of bytes to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this address space are limited to a 32-bit range.

5.3.1 Enable Bits

The response of the bridge to memory-mapped I/O transactions is controlled by the following configuration register bits:

- *Memory Space Enable* bit in the **PCI Command** register
- *Bus Master Enable* bit in the **PCI Command** register
- *VGA Enable* bit in the **Bridge Control** register

The *Memory Space Enable* bit must be set for any memory transaction to be forwarded downstream. If this bit is not set, all memory transactions on the secondary bus are forwarded to the primary bus.

- If this bit is not set in Forward Bridge mode, all non-posted memory requests are completed with an Unsupported Request status. Posted write data is discarded.
- If this bit is not set in Reverse Bridge mode, all memory transactions are ignored on the primary (PCI) bus.

The *Bus Master Enable* bit must be set for any memory transaction to be forwarded upstream.

- If this bit is not set in Forward Bridge mode, all memory transactions on the secondary (PCI) bus are ignored.
- If this bit is not set in Reverse Bridge mode, all non-posted memory requests on the secondary (PCI Express) bus are completed with an Unsupported Request status. Posted write data is discarded.

The *VGA Enable* bit is discussed in the section on VGA Mode (6.3.3).

5.3.2 Memory-Mapped I/O Base and Limit Registers

The following Memory Base and Limit configuration registers are used to determine whether to forward memory-mapped I/O transactions across the bridge.

- **Memory Base** (bits 15:4 of 16-bit register correspond to address bits 31:20)
- **Memory Limit** (bits 15:4 of 16-bit register correspond to address bits 31:20)

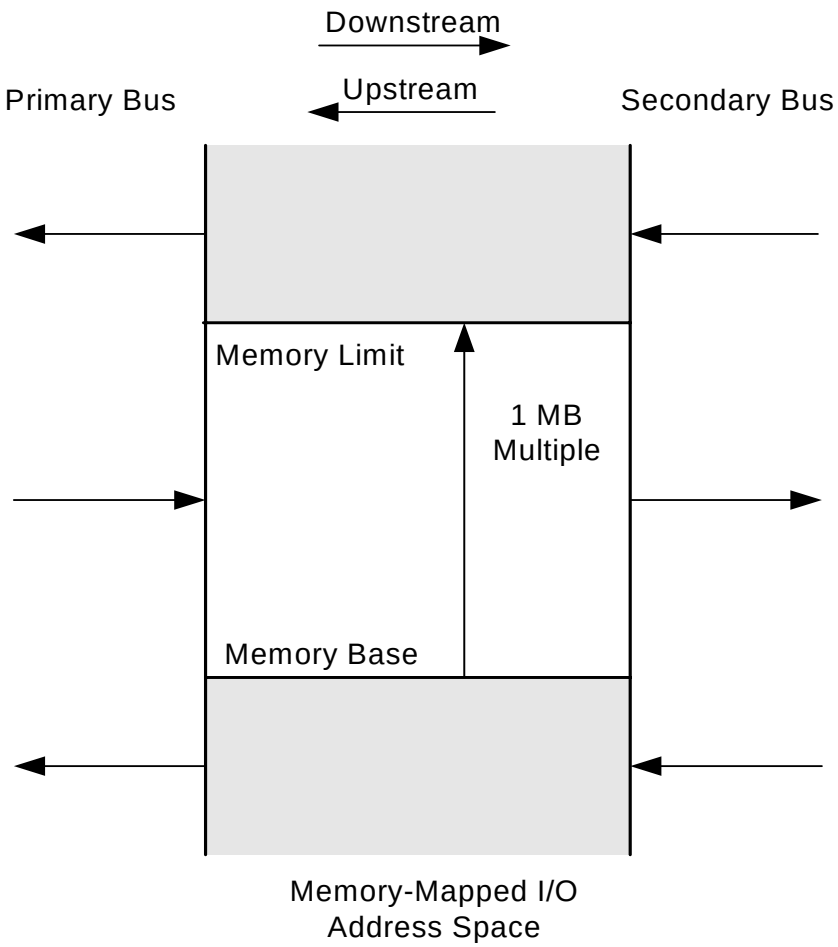
Bits 15:4 of the **Memory Base** register define bits 31:20 of the memory-mapped I/O base address. Bits 15:4 of the **Memory Limit** register define bits 31:20 of the memory-mapped I/O limit. Bits 3:0 of each register are hardwired to 0.

Since address bits 19:0 are not included in the address space decoding, the memory-mapped I/O address range has a granularity of 1 MB, and is always aligned to a 1 MB boundary. The maximum memory-mapped I/O range is 4 GB.

Memory transactions that fall within the range defined by the base and limit are forwarded downstream from the primary to secondary bus, and memory transactions on the secondary bus that are within the range are ignored. Memory transactions that do not fall within the range defined by the base and limit are ignored on the primary bus and are forwarded upstream from the secondary bus (provided they are not in the address range defined by the set of prefetchable memory address registers or are not forwarded downstream by the VGA mechanism).

Figure 5-3 illustrates memory-mapped I/O forwarding.

Figure 5-3. Memory-Mapped I/O Forwarding



If the Memory Base is programmed to have a value greater than the Memory Limit, then the Memory-mapped I/O range is disabled. In this case, all memory transaction forwarding is determined by the prefetchable base and limit registers and the VGA enable bit.

5.3.3 VGA Mode

The *VGA Enable* bit in the **Bridge Control** register enables VGA frame buffer accesses to be forwarded downstream from the primary to secondary bus, independent of the memory-mapped I/O base and limit registers.

The following VGA memory addresses are controlled by the *VGA Enable* bit:

- 0A0000h – 0BFFFFh

5.4 Prefetchable Space

The prefetchable addressing space determines whether to forward prefetchable memory read or write transactions across the bridge. Devices that do not have side-effects during reads should be mapped into this space.

- For PCI to PCI Express reads, prefetching occurs in this space for all memory read commands (MemRd, MemRdLine, MemRdMult).issued on the PCI bus.
- For MemRd commands, the *Blind Prefetch Enable* bit in the **DEVSPECCTL** register must be set for prefetching to occur.
- For PCI Express to PCI reads, the number of bytes to read is determined by the Memory Read Request, so prefetching does not actually occur.

5.4.1 Enable Bits

The prefetchable space responds to the enable bits as described in the earlier section on Enable Bits.

5.4.2 Prefetchable Base and Limit Registers

The following Prefetchable Memory Base and Limit configuration registers are used to determine whether to forward prefetchable memory transactions across the bridge.

- **Prefetchable Memory Base** (bits 15:4 of 16-bit register correspond to address bits 31:20)
- **Prefetchable Memory Base Upper** (32-bit register corresponds to address bits 63:32)
- **Prefetchable Memory Limit** (bits 15:4 of 16-bit register correspond to address bits 31:20)
- **Prefetchable Memory Limit Upper** (32-bit register corresponds to address bits 63:32)

Bits 15:4 of the **Prefetchable Memory Base** register define bits 31:20 of the prefetchable memory base address. Bits 15:4 of the **Prefetchable Memory Limit** register define bits 31:20 of the prefetchable memory limit. Bits 3:0 of each register are hardwired to 0. For 64-bit addressing, the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are also used to define the space.

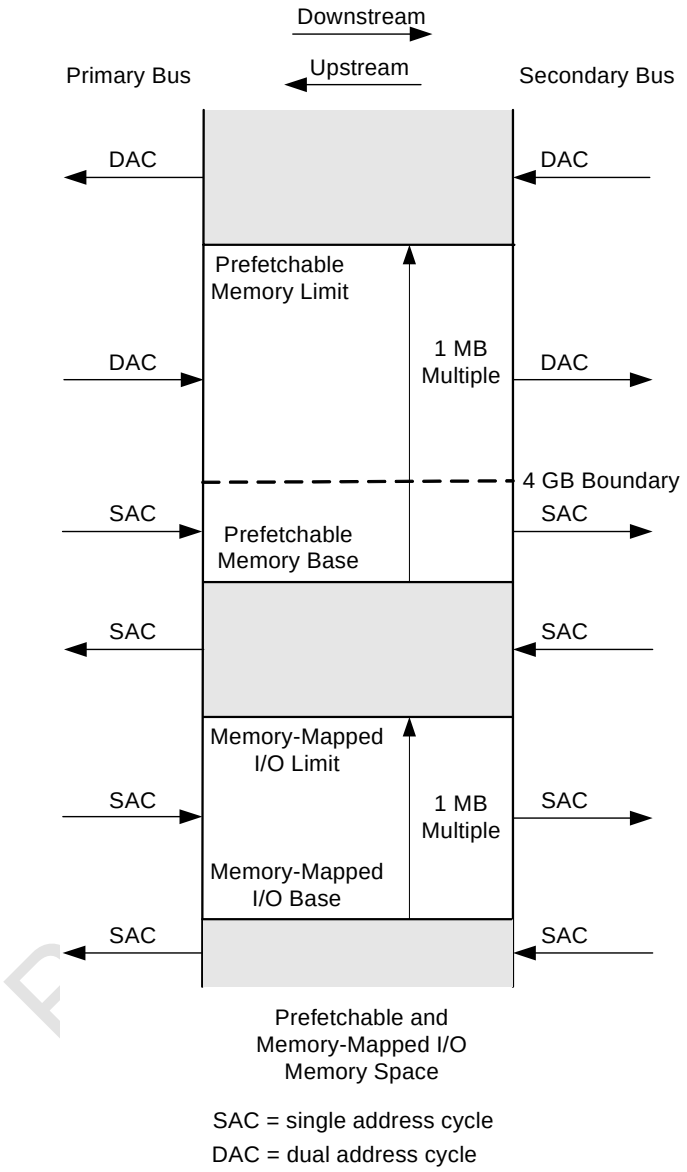
Since address bits 19:0 are not included in the address space decoding, the prefetchable memory address range has a granularity of 1 MB, and is always aligned to a 1 MB boundary. The maximum prefetchable memory range is 4 GB with 32-bit addressing, and 2^{64} with 64-bit addressing.

Memory transactions that fall within the range defined by the base and limit are forwarded downstream from the primary to secondary bus, and memory transactions on the secondary bus that are within the range are ignored.

Memory transactions that do not fall within the range defined by the base and limit are ignored on the primary bus and are forwarded upstream from the secondary bus (provided they are not in the address range defined by the set of memory-mapped I/O address registers or are not forwarded downstream by the VGA mechanism).

Figure 5-4 illustrates both memory-mapped I/O and prefetchable memory forwarding.

Figure 5-4. Memory-Mapped I/O and Prefetchable Memory Forwarding



If the **Prefetchable Memory Base** is programmed to have a value greater than the **Prefetchable Memory Limit**, then the prefetchable memory range is disabled. In this case, all memory transaction forwarding is determined by the memory-mapped I/O base and limit registers and the *VGA Enable* bit.

All four prefetchable base and limit registers must be considered when disabling the prefetchable range.

5.4.3 64-Bit Addressing

Unlike memory-mapped I/O memory that must be below the 4 GB boundary, prefetchable memory may be located below, above, or span the 4 GB boundary. Memory locations above the 4 GB boundary must be accessed using 64-bit addressing. PCI Express memory transactions that use the Short Address (32-bit) format may target the non-prefetchable memory space, or a prefetchable memory window that is below the 4 GB boundary. PCI Express memory transactions that use the Long Address (64-bit) format may target locations anywhere in the 64-bit memory space.

PCI memory transactions that use single address cycles may only target locations below the 4 GB boundary. PCI memory transactions that use dual address cycles may target locations anywhere in the 64-bit memory space. The first address phase of a dual-address transaction contains the lower 32-bits of the address, and the second address phase contains the upper 32 bits of the address. If the upper 32 bits of the address are 0, a single-address transaction is always performed.

5.4.3.1 Forward Bridge Mode

If both the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are set to 0, then addresses above 4 GB are not supported.

In Forward Bridge mode, if a PCI Express memory transaction is detected with an address above 4 GB, the transaction is completed with Unsupported Request status. All dual-address transactions on the PCI bus are forwarded upstream to the PCI Express bus.

If the prefetchable memory is located entirely above the 4 GB boundary, both the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are both set to non-zero values.

If a PCI Express memory transaction is detected with an address below 4 GB, the transaction is completed with Unsupported Request status, and all single-address transactions on the PCI bus are forwarded upstream to the PCI Express bus (unless they fall within the memory-mapped I/O or VGA memory range). A PCI Express memory transaction above 4 GB that falls within the range defined by the **Prefetchable Base**, **Prefetchable Memory Base Upper**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper** registers is forwarded downstream and becomes a dual address cycle on the PCI bus.

If a dual address cycle is detected on the PCI bus that is outside the range defined by these registers, it is forwarded upstream to the PCI Express bus.

If a PCI Express memory transaction above 4 GB does not fall into the range defined by these registers, it is completed with Unsupported Request status.

If a PCI dual address cycle falls into the range determined by these registers, it is ignored.

If the prefetchable memory spans the 4 GB boundary, the **Prefetchable Memory Base Upper** is set to 0, and the **Prefetchable Memory Limit Upper** registers is set to a non-zero value.

If a PCI Express memory transaction is detected with an address below 4 GB, and is greater than or equal to the prefetchable memory base address, then the transaction is forwarded downstream. A single-address transaction on the PCI bus is forwarded upstream to the PCI Express bus if the address is less than the prefetchable memory base address.

If a PCI Express memory transaction above 4 GB is less than or equal to the prefetchable memory limit register, it is forwarded downstream to the PCI bus as a dual-address cycle.

If a dual-address cycle on the PCI bus is less than or equal to the **Prefetchable Memory Limit** register, it is ignored.

If a PCI Express memory transaction above 4 GB is greater than the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status.

If a dual-address cycle on the PCI bus is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Express bus.

5.4.3.2 Reverse Bridge Mode

If both the Prefetchable **Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are set to 0, then addresses above 4 GB are not supported.

In Reverse Bridge mode, if a dual address transaction on the PCI is detected, the transaction is ignored.

If a PCI Express memory transaction is detected with an address above 4 GB, it is forwarded upstream to the PCI bus as a dual-address cycle.

If the prefetchable memory is located entirely above the 4 GB boundary, both the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are set to non-zero values. The PEX 8111 ignores all single address memory transactions on the PCI bus, and forwards all PCI Express memory transactions with addresses below 4 GB upstream to the PCI bus (unless they fall within the memory-mapped I/O or VGA memory range).

A dual address transaction on the PCI bus that falls within the range defined by the **Prefetchable Base**, **Prefetchable Memory Base Upper**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper** registers is forwarded downstream to the PCI Express bus.

If a PCI Express memory transaction is above the 4 GB boundary and falls outside the range defined by these registers, it is forwarded upstream to the PCI bus as a dual-address cycle.

If a dual address transaction on the PCI bus does not fall into the range defined by these registers, it is ignored.

If a PCI Express memory transaction above 4 GB falls into the range defined by these registers, it is completed with Unsupported Request status.

If the prefetchable memory spans the 4 GB boundary, the **Prefetchable Memory Base Upper** is set to 0, and the **Prefetchable Memory Limit Upper** registers is set to a non-zero value.

If a PCI single address cycle is greater than or equal to the prefetchable memory base address, then the transaction is forwarded downstream to the PCI Express bus.

If a PCI Express memory transaction is detected with an address below 4 GB, and is less than the prefetchable memory base address, then the transaction is forwarded upstream to the PCI bus. If a dual-address PCI transaction is less than or equal to the **prefetchable memory limit** register, it is forwarded downstream to the PCI Express bus.

If a PCI Express memory transaction above 4 GB is less than or equal to **the prefetchable memory limit** register, it is completed with Unsupported Request status.

If a dual-address PCI transaction is greater than the **prefetchable memory limit** register, it is ignored.

If a PCI Express memory transaction above 4 GB is greater than the **prefetchable memory limit** register, it is forwarded upstream to the PCI bus as a dual-address cycle.

5.4.4 VGA Mode

The *VGA Enable* bit in the **Bridge Control** register enables VGA frame buffer accesses to be forwarded downstream from the primary to secondary bus, independent of the prefetchable memory base and limit registers.

The following VGA memory address are controlled by the *VGA Enable* bit:

- 0A0000h – 0BFFFFh

Chapter 6 Configuration Transactions

6.1 Introduction

Configuration requests are only initiated by the Root Complex in a PCI Express-based system or by the Central Resource Function in a PCI-based system. Every device in a PCI Express or PCI system has a configuration space that is accessed using configuration transactions.

- A Type 0 configuration transaction is used to access the internal PEX 8111 configuration registers.
- A Type 1 configuration transaction is used to access a device that resides downstream of the PEX 8111.

The configuration address is formatted as follows.

Table 6-1. PCI Express

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	Rsvd	Extended Register Address	Register Address	Rsvd

Table 6-2. PCI Type 0 (at Initiator)

31 16	15 11	10 8	7 2	1 0
Single bit decoding of device number	Rsvd	Function Number	Register Number	0 0

Table 6-3. PCI Type 0 (at Target)

31 11	10 8	7 2	1 0
Rsvd	Function Number	Register Number	0 0

Table 6-4. PCI Type 1

31 24	23 16	15 11	10 8	7 2	1 0
Rsvd	Bus Number	Device Number	Function Number	Register Number	0 1

6.2 Type 0 Configuration Transactions

The PEX 8111 only responds to Type 0 configuration transactions on its primary bus that address the PEX 8111 configuration space. A Type 0 configuration transaction is used to configure the PEX 8111, and is not forwarded downstream to the secondary bus. The PEX 8111 ignores Type 0 configuration transactions on its secondary bus. Type 0 configuration transactions always result in the transfer of one DWORD.

If Configuration Write data is poisoned, the data is discarded and a Non-Fatal Error message is generated, if enabled.

6.3 Type 1 Configuration Transactions

Type 1 configuration transactions are used for device configuration in a hierarchical bus system. Bridges and switches are the only types of devices that respond to a Type 1 configuration transaction. Type 1 configuration transactions are used when the transaction is intended for a device residing on a bus other than the one where the Type 1 request is issued.

The Bus Number field in a configuration transaction request specifies a unique bus in the hierarchy on which the target of the transaction resides. The bridge compares the specified bus number with two PEX 8111 configuration registers to determine whether to forward a Type 1 configuration transaction across the bridge. The two configuration registers are the **Secondary Bus Number** and the **Subordinate Bus Number.**

If a Type 1 configuration transaction is received on the primary interface, the following tests are applied, in sequence, to the Bus Number field to determine how the transaction must be handled:

- If the Bus Number field is equal to the **Secondary Bus Number** register value, and the conditions for converting the transaction into a Special Cycle transaction are met, the PEX 8111 forwards the configuration request to the secondary bus as a Special Cycle transaction. If the conditions are not met, the PEX 8111 forwards the configuration request to the secondary bus as a Type 0 configuration transaction.
- If the Bus Number field is not equal to the **Secondary Bus Number** register value but is in the range of the **Secondary Bus Number** and **Subordinate Bus Number** (inclusive) registers, the Type 1 configuration request is specifying a bus that is located behind the bridge. In this case, the PEX 8111 forwards the configuration request to the secondary bus as a Type 1 configuration transaction.
- If the Bus Number field does not satisfy the above criteria, the Type 1 configuration request is specifying a bus that is not located behind the bridge. In this case, the configuration request is invalid.
  - If the primary interface is PCI Express, a completion with Unsupported Request status is returned.
  - If the primary interface is PCI, the configuration request is ignored, resulting in a Master Abort.

6.4 Type 1 to Type 0 Conversion

The PEX 8111 performs a Type 1 to Type 0 conversion when the Type 1 transaction is generated on the primary bus and is intended for a device attached directly to the secondary bus. The PEX 8111 must convert the Type 1 configuration transaction to Type 0 so that the device can respond to it.

Type 1 to Type 0 conversions are only performed in the downstream direction. The PEX 8111 only generates Type 0 configuration transactions on the secondary interface, never on the primary interface.

6.4.1 Forward Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Express bus to a Type 0 transaction on the PCI bus if the following are true:

- The Type 1 Bus Number field of the configuration request is equal to the **Secondary Bus Number** register value.
- The conditions for conversion to a Special Cycle transaction are not met.

The PEX 8111 then performs the following on the secondary interface:

- Set address bits AD[1:0] to 0.
- Derive address bits AD[7:2] directly from the Register Address field of the configuration request.
- Derive address bits AD[10:8] directly from the Function Number field of the configuration request.
- Set address bits AD[15:11] to 0.
- Decode the Device Number field and assert a single address bit in the range AD[31:16] during the address phase.
- Verify that the Extended Register Address field in the configuration request is zero. If the value is non-zero, the PEX 8111 does not forward the transaction, and treats it as an Unsupported Request on the PCI Express bus, and a received Master Abort on the PCI bus.

Type 1 to Type 0 transactions are performed as non-posted transactions.

6.4.2 Reverse Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI bus to a Type 0 transaction on the PCI Express bus if the following are true during the PCI address phase:

- Address bits AD[1:0] are 01b.
- The Type 1 configuration request Bus Number field (AD[23:16]) is equal to the **Secondary Bus Number** register value.
- The bus command on CBE[3:0]# is a Configuration Read or Write.
- The Type 1 configuration request Device Number field (AD[15:11]) is zero. If it is non-zero, the transaction is ignored, resulting in a Master Abort.

The PEX 8111 then creates a PCI Express configuration request according to the following:

- Set the request Type field to Configuration Type 0.
- Set the Register Address field [7:2] directly from the Register Address field of the configuration request
- Set the Extended Register Address field [11:8] to 0.
- Set the Function Number field [18:16] directly from the Function Number field of the configuration request.
- Set the Device Number field [23:19] directly from the Device Number field (forced to zero) of the configuration request.
- Set the Bus Number field [31:24] directly from the Bus Number field of the configuration request.

Type 1 to Type 0 transactions are performed as non-posted (delayed) transactions.

6.5 Type 1 to Type 1 Forwarding

Type 1 to Type 1 transaction forwarding provides a hierarchical configuration mechanism when two or more levels of bridges are used. When the PEX 8111 detects a Type 1 configuration transaction intended for a PCI bus downstream from the secondary bus, it forwards the transaction unchanged to the secondary bus.

In this case, the target of the transaction does not reside on the secondary interface of the PEX 8111, but is located on a bus segment further downstream. Ultimately, this transaction is converted to a Type 0 or Special Cycle transaction by a downstream bridge.

6.5.1 Forward Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Express bus to a Type 1 transaction on the PCI bus if the following are true:

- A Type 1 configuration transaction is detected on the PCI Express.
- The value specified by the Bus Number field is within the range of bus numbers between the **Secondary Bus Number** (exclusive) and the **Subordinate Bus Number** (inclusive).

The PEX 8111 then performs the following on the secondary interface:

- Generate address bits AD[1:0] as 01b.
- Generate PCI Register Number, Function Number, Device Number, and Bus Number directly from the Register Address, Function Number, Device Number, and Bus Number fields, respectively, of the PCI Express Configuration Request.
- Generate address bits AD[31:24] as 0.
- Verify that the Extended Register Address field in the configuration request is zero. If the value is non-zero, the PEX 8111 does not forward the transaction, and returns a completion with Unsupported Request status on the PCI Express bus, and a received Master Abort on the PCI bus.

Type 1 to Type 1 forwarding transactions are performed as non-posted transactions.

6.5.2 Reverse Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI bus to a Type 1 transaction on the PCI Express bus if the following are true during the PCI address phase:

- Address bits AD[1:0] are 01b.
- The value specified by the Bus Number field is within the range of bus numbers between the **Secondary Bus Number** (exclusive) and the **Subordinate Bus Number** (inclusive).
- The bus command on CBE[3:0]# is a Configuration Read or Write.

The PEX 8111 then creates a PCI Express configuration request according to the following:

- Set the request Type field to Configuration Type 1.
- Set the Register Address field [7:2] directly from the Register Address field of the configuration request.
- Set the Extended Register Address field [11:8] to 0.
- Set the Function Number field [18:16] directly from the Function Number field of the configuration request.
- Set the Device Number field [23:19] directly from the Device Number field of the configuration request.
- Set the Bus Number field [31:24] directly from the Bus Number field of the configuration request.

Type 1 to Type 1 forwarding transactions are performed as non-posted (delayed) transactions.

6.6 Type 1 to Special Cycle Forwarding

The Type 1 configuration mechanism is used to generate Special Cycle transactions in hierarchical systems. Special Cycle transactions are ignored by the PEX 8111 acting as a target, and are not forwarded across the bridge.

In Forward Bridge mode, Special Cycle transactions can only be generated in the downstream direction (PCI Express to PCI).

In Reverse Bridge mode, Special Cycle transactions are also generated in the downstream direction (PCI to PCI Express).

A Type 1 Configuration Write Request on the PCI Express bus is converted to a Special Cycle on the PCI bus when all of the following conditions are met:

- The Type 1 configuration request Bus Number field is equal to the **Secondary Bus Number** register value.
- The Device Number field is all ones.
- The Function Number field is all ones.
- The Register Address field is all zeroes
- The Extended Register Address field is all zeros.

When the PEX 8111 initiates the transaction on the PCI bus, the bus command is converted from a Configuration Write to a Special Cycle. The address and data fields are forwarded unchanged from the PCI Express to the PCI. Target devices that recognize the Special Cycle ignore the address, and the message is passed in the data word. The transaction is performed as a non-posted transaction, but the PCI target response (always Master Abort in this case) is not returned back to the PCI Express. Once the Master Abort has been detected on the PCI bus, the successful completion TLP is returned to the PCI Express.

6.7 PCI Express Enhanced Configuration Mechanisms

The PCI Express Enhanced Configuration Mechanism adds four extra bits to the Register Address field to expand the space to 4096 bytes. The PEX 8111 only forwards configuration transactions if the Extended Register Address bits are all zero. This prevents address aliasing on the PCI bus which does not support Extended Register Addressing.

If a configuration transaction targets the PCI bus and has a non-zero value in the Extended Register Address, the PEX 8111 treats the transaction as if it received a Master Abort on the PCI bus. The PEX 8111 then does the following:

- Sets the appropriate status bits for the destination bus as if the transaction had actually executed and received a Master Abort.
- Generates a PCI Express completion with Unsupported Request status.

6.7.1 Memory-Mapped Indirect

In Reverse Bridge mode, the PEX 8111 provides the capability for a PCI host to access all of the downstream PCI Express configuration registers using PCI memory transactions. The 4 KByte region of the memory range defined by the **PCIBASE0** register is used for this mechanism. Memory reads and writes to **PCIBASE0** offsets 'h2000 to 'h2FFF result in a PCI Express configuration transaction. The address of the transaction is determined by the **ECFGADDR** register.

The format of this address register is as follows.

Table 6-5. Address Register Format

31	30 29	27 20	19 15	14 12	11 0
Enhanced Enable	Rsvd	Bus Number	Device Number	Function Number	Rsvd

Once the **ECFGADDR** has been programmed to point to a particular device, the entire 4 KByte configuration space of a PCI Express endpoint can be accessed directly using memory read and write transactions. Only single DWORDs are transferred during Enhanced Configuration transactions.

6.8 Configuration Retry Mechanism

6.8.1 Forward Bridge Mode

Bridges are required to return a completion for all configuration requests that traverse the bridge from PCI Express to PCI prior to expiration of the Completion Timeout timer in the Root Complex. This requires that bridges take ownership of all configuration requests forwarded across the bridge.

If the configuration request to PCI completes successfully prior to the bridge timer expiration, the bridge returns a completion with Successful Status to PCI Express.

If the configuration request to PCI encounters an error condition prior to the bridge timer expiration, the bridge returns an appropriate error completion to PCI Express.

If the configuration request to PCI does not complete either successfully or with an error, prior to timer expiration, then the bridge returns a completion with Configuration Retry Status (CRS) to PCI Express.

Even after the PEX 8111 has returned a completion with CRS to PCI Express, the PEX 8111 continues to keep the configuration transaction alive on the PCI bus. The PCI Specification states that once a PCI master detects a target retry, it must continue to retry the transaction until at least one DWORD is transferred. The PEX 8111 keeps retrying the transaction until it completes on the PCI bus or until the PCI Express to PCI Retry timer expires.

If another PCI Express to PCI configuration transaction is detected while the previous one is being retried, a completion with CRS is returned immediately.

When the configuration transaction completes on the PCI bus after the return of a completion with CRS on PCI Express, the PEX 8111 discards the completion information. Bridges that implement this option are also required to implement bit 15 of the **Device Control** register as the *Bridge Configuration Retry Enable* bit.

If this bit is cleared, the bridge does not return a completion with CRS on behalf of configuration requests forwarded across the bridge. The lack of a completion should result in eventual Completion Timeout at the Root Complex.

Bridges, by default, do not return CRS for Configuration Requests to a PCI device behind the bridge. This may result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

6.8.2 Reverse Bridge Mode

In Reverse Bridge mode, the PEX 8111 may detect a completion with CRS status from a downstream PCI Express device. The *CRS Retry Control* field of the **DEVSPECCTL** register determines the response of the PEX 8111 in Reverse Bridge Mode when a PCI to PCI Express configuration transaction is terminated with a Configuration Request Retry Status.

Table 6-6. CRS Retry Control

CRS Retry Control	Response
00	Retry once after 1 second. If another CRS is received, Target Abort on the PCI bus.
01	Retry 8 times, once per second. If another CRS is received, Target Abort on the PCI bus.
10	Retry once per second until successful completion.
11	***Reserved***

Chapter 7 Error Handling (Forward Bridge)

7.1 Introduction

For all errors detected by the bridge, the bridge sets the appropriate error status bit (both legacy PCI error bit(s) and PCI Express error status bit(s)), and optionally generates an error message on PCI Express. Each error condition has a default error severity level, and has a corresponding error message generated on PCI Express.

Error message generation on the PCI Express bus is controlled by three control bits:

- The *SERR Enable* bit in the **PCI Command** register.
- The *Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register.
- The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register.
- The *Correctable Error Reporting Enable* bit in the **PCI Express Device Control** register.

ERR_FATAL PCI Express messages are enabled for transmission if either the *SERR Enable* bit or the *Fatal Error Reporting Enable* bit is set. ERR_NONFATAL Messages are enabled for transmission if either the *SERR Enable* bit or the *Non-Fatal Error Reporting Enable* bit is set. ERR_COR Messages are enabled for transmission if the *Correctable Error Reporting Enable* bit is set. The *Fatal Error Detected*, *Non-Fatal Error Detected*, and *Correctable Error Detected* status bits in the **DEVSTAT** register are set for the corresponding errors on the PCI Express, regardless of the error reporting enable bits.

7.2 PCI Express Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI Express interface, and the destination side is the PCI bus. If a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction must be considered as corrupt. Invert the parity for every data when completing the transaction on the PCI bus.

Table 7-1 provides the translation a bridge has to perform when it forwards a non-posted PCI Express request (read or write) to the PCI bus, and the request is completed immediately on the PCI bus either normally or with an error condition.

Table 7-1. Translation Performed when Bridge Forwards a Non-Posted PCI Express Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with parity error (reads)	Successful (poisoned TLP)
Completion with parity error (non-posted writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

7.2.1 Received Poisoned TLP

When a write request or read completion is received by the PCI Express interface, and the data is poisoned, the following occur:

- The *Detected Parity Error* bit in the **PCI Status** register is set.
- The *Master Data Parity Error* bit in the **PCI Status** register is set if the poisoned TLP is a read completion and the *Parity Error Response Enable* bit in the **PCI Command** register is set.
- An ERR_NONFATAL Message is generated on PCI Express, if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.
- The parity bit associated with each DWORD of data is inverted.
- For a poisoned write request, the *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set, and the bridge sees PERR# asserted when the inverted parity is detected by the PCI target device.

7.2.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI bus, and an uncorrectable PCI error is detected.

7.2.2.1 Immediate Reads

When the PEX 8111 forwards a read request (I/O, Memory, or Configuration) from the PCI Express and detects an uncorrectable data error on the secondary bus while receiving an immediate response from the completer, the following occur:

- The *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit is set in the **Bridge Control** register.
- The *Secondary Detected Parity Error* bit in the **Secondary Status** register is set.
- PERR# is asserted on the secondary interface if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.

After detecting an uncorrectable data error on the destination bus for an immediate read transaction, the PEX 8111 continues to fetch data until the byte count is satisfied or the target ends the transaction. When the bridge creates the PCI Express completion, it forwards it with Successful Completion and poisons the TLP.

7.2.2.2 Non-Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI secondary interface while forwarding a non-poisoned non-posted write transaction from PCI Express, the following occur:

- The *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.
- A PCI Express completion with Unsupported Request status is generated.
- An ERR_NONFATAL Message is generated on PCI Express, if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.

7.2.2.3 Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI secondary interface while forwarding a non-poisoned posted write transaction from PCI Express, the following occur:

- The *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.
- An ERR_NONFATAL Message is generated on PCI Express, if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.
- After the error is detected, the remainder of the data is forwarded.

7.2.3 PCI Address Errors

When the PEX 8111 forwards transactions from PCI Express to PCI, PCI address errors are reported by the assertion of the SERR# pin. When the PEX 8111 detects SERR# asserted, the following occur:

- The *Secondary Received System Error* bit in the **Secondary Status** register is set.
- An ERR_FATAL message is generated on PCI Express, if the following conditions are met:
  - The *Secondary SERR Enable* bit in the **Bridge Control** register is set.
  - The *SERR Enable* bit in the **PCI Command** register or the *Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *Secondary SERR Enable* and *SERR Enable* bits are set.

7.2.4 PCI Master Abort on Posted Transaction

When a posted write transaction forwarded from PCI Express to PCI results in a Master Abort on the PCI bus, the following occur:

- The entire transaction is discarded.
- The *Secondary Received Master Abort* bit in the **Secondary Status** register is set.
- An ERR_NONFATAL Message is generated on PCI Express if the following conditions are met:
  - The *Master Abort Mode* bit in the **Bridge Control** register is set.
  - The *SERR Enable* bit in the **PCI Command** register or the *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *Master Abort Mode* and *SERR Enable* bits are set.

7.2.5 PCI Master Abort on Non-Posted Transaction

When a non-posted transaction forwarded from PCI Express to PCI results in a Master Abort on the PCI bus, the following occur:

- A completion with Unsupported Request status is returned on the PCI Express.
- The *Secondary Received Master Abort* bit in the **Secondary Status** register is set.

7.2.6 PCI Target Abort on Posted Transaction

When a transaction forwarded from PCI Express to PCI results in a Target Abort on the PCI bus, the following occur:

- The entire transaction is discarded.
- The *Secondary Received Target Abort* bit in the **Secondary Status** register is set.
- An ERR_NONFATAL Message is generated on PCI Express if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.

7.2.7 PCI Target Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express to PCI results in a Target Abort on the PCI bus, the following occur:

- A completion with Completer Abort status is returned on the PCI Express.
- The *Secondary Received Target Abort* bit in the **Secondary Status** register is set.
- The *Signaled Target Abort* bit in the **PCI Status** register is set.
- An ERR_NONFATAL Message is generated on PCI Express if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.

7.2.8 PCI Retry Abort on Posted Transaction

When a transaction forwarded from PCI Express to PCI results in the maximum number of PCI retries (selectable in **PCICTL** register), the following occur:

- The remaining data is discarded.
- The *PCI Express to PCI Retry Interrupt* bit in the **IRQSTAT** register is set.

7.2.9 PCI Retry Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express to PCI results in the maximum number of PCI retries (selectable in **PCICTL** register), the following occur:

- A completion with the status of Completer Abort is returned on the PCI Express.
- The *PCI Express to PCI Retry Interrupt* bit in the **IRQSTAT** register is set.
- The *Signaled Target Abort* bit in the **PCI Status** register is set.

7.3 PCI Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI bus, and the destination side is the PCI Express. The PEX 8111 supports TLP poisoning as a transmitter to permit proper forwarding of parity errors that occur on the PCI interface. Posted write data received on the PCI interface with bad parity are forwarded to PCI Express as Poisoned TLPs.

Table 7-2 provides the error forwarding requirements for Uncorrectable data errors detected by the PEX 8111 when a transaction targets the PCI Express interface.

Table 7-2. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with parity error	Write request with poisoned TLP
Read Completion with parity error in data phase	Read completion with poisoned TLP
Configuration or I/O Completion with parity error in data phase	Read/Write completion with Completer Abort Status

Table 7-3 describes the bridge behavior on a PCI delayed transaction that is forwarded by a bridge to PCI Express as a Memory Read request or an I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 7-3. Bridge Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Target Abort	Normal completion
Completer Abort	Target Abort	

7.3.1 Received PCI Errors

7.3.1.1 Uncorrectable Data Error on Non-Posted Write

When a non-posted write is addressed such that it crosses the bridge, and the PEX 8111 detects an uncorrectable data error on the PCI interface, the following occur:

- The *Secondary Detected Parity Error* status bit in the **Secondary Status** register is set.
- If the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set, the transaction is discarded and is not forwarded to PCI Express. The PERR# pin is asserted on the PCI bus.
- If the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is not set, the data is forwarded to PCI Express as a poisoned TLP. Also, set the *Master Data Parity Error* bit in the **PCI Status** register if the *Parity Error Response Enable* bit in the **PCI Command** register is set. The PERR# pin is not asserted on the PCI bus.

7.3.1.2 Uncorrectable Data Error on Posted Write

When the PEX 8111 detects an uncorrectable data error on the PCI secondary interface for a posted write transaction that crosses the bridge, the following occur:

- The PCI PERR# signal is asserted if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.
- The *Secondary Detected Parity Error* status bit in the **Secondary Status** register is set.
- The posted write transaction is forwarded to PCI Express as a poisoned TLP.
- The *Master Data Parity Error* bit in the **PCI Status** register is set if the *Parity Error Response Enable* bit in the **PCI Command** register is set.

7.3.1.3 Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8111 forwards a non-poisoned read completion from PCI Express to PCI, and it detects PERR# asserted by the PCI master, the remainder of the completion is forwarded.

When the PEX 8111 forwards a poisoned read completion from PCI Express to PCI, the PEX 8111 proceeds with the above mentioned actions when it detects the PERR# pin asserted by the PCI master, but no error message is generated on PCI Express.

7.3.1.4 Uncorrectable Address Error

When an uncorrectable address error is detected by the PEX 8111, and parity error detection is enabled via the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register, the following occur:

- The transaction is terminated with a Target Abort.
- The *Secondary Detected Parity Error* bit in the **Secondary Status** register is set, independent of the setting of the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register.
- The *Secondary Signaled Target Abort* bit in the **Secondary Status** register is set.
- An ERR_FATAL message is generated on PCI Express if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.

7.3.2 Unsupported Request (UR) Completion Status

The PEX 8111 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the PCI interface. The response is controlled by the *Master Abort Mode* bit in the **Bridge Control** register. In either case, the *Received Master Abort* bit in the **PCI Status** register is set.

7.3.2.1 Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and an Unsupported Request is not considered to be an error.

When a read transaction initiated on the PCI results in the return of a completion with Unsupported Request status, the PEX 8111 returns FFFFFFFFh to the originating master and terminates the read transaction on the originating interface normally (by asserting TRDY#).

When a non-posted write transaction results in a completion with Unsupported Request status, the PEX 8111 completes the write transaction on the originating bus normally (by asserting TRDY#) and discards the write data.

7.3.2.2 Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8111 signals a Target Abort to the originating master of an upstream read or non-posted write transaction when the corresponding request on the PCI Express interface results in a completion with UR Status. In addition, the *Secondary Signaled Target Abort* bit in the **Secondary Status** register is set.

7.3.3 Completer Abort (CA) Completion Status

If the PEX 8111 receives a completion with Completer Abort status on the PCI Express primary interface in response to any forwarded non-posted PCI transaction, the *Received Target Abort* bit is set in the **PCI Status** register. A CA response results in a Delayed Transaction Target Abort on the PCI bus. The PEX 8111 provides data to the requesting PCI agent up to the point where data was successfully returned from the PCI Express interface and then signals Target Abort. The *Secondary Signaled Target Abort* status bit in the **Secondary Status** register is set when signaling Target Abort to a PCI agent.

7.4 Timeout Errors

7.4.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout Mechanism allows requesters to abort a non-posted request if a completion does not arrive within a reasonable time. Bridges, when acting as initiators on PCI Express on behalf of internally-generated requests or when forwarding requests from a secondary interface, behave as endpoints for requests that they take ownership of.

If a completion timeout is detected and the link is up, the PEX 8111 responds as if a completion with Unsupported Request status has been received. The following action is taken:

- An ERR_NONFATAL Message is generated on PCI Express if the following conditions are met:
  - The *SERR Enable* bit in the **PCI Command** register is set OR
  - The *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.

If the link is down, the *P2PE_RETRY_COUNT* field in the **PCICTL** register determines how many PCI retries occur before a Master Abort is returned to the PCI bus.

7.4.2 PCI Delayed Transaction Timeout Errors

The PEX 8111 has Delayed Transaction Timers for each queued delayed transaction. If a delayed transaction timeout is detected, the following occur:

- An ERR_NONFATAL Message is generated on PCI Express if the following conditions are met:
  - The *Discard Timer SERR# Enable* bit in the **Bridge Control** register is set.
  - The *SERR Enable* bit in the **PCI Command** register or the *Non-Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *SERR Enable* bit is set.
- The *Discard Timer Status* in the **Bridge Control** register is set.

7.5 Other Errors

PCI devices can assert SERR# when detecting errors that compromise system integrity. When the PEX 8111 detects SERR# asserted on the secondary PCI bus, the following occur:

- The *Secondary Received System Error* bit in the **Secondary Status** register is set.
- An ERR_FATAL message is generated on PCI Express, if the following conditions are met:
  - The *Secondary SERR Enable* bit in the **Bridge Control** register is set.
  - The *SERR Enable* bit in the **PCI Command** register or the *Fatal Error Reporting Enable* bit in the **PCI Express Device Control** register is set.
- The *Signaled System Error* in the **PCI Status** register is set if the *Secondary SERR Enable* and *SERR Enable* bits are set.

Chapter 8 Error Handling (Reverse Bridge)

8.1 Introduction

For all errors detected by the bridge, the bridge sets the appropriate error status bit (both legacy PCI error bit(s) and PCI Express error status bit(s)). No PCI Express error messages are generated in Reverse Bridge mode.

8.2 PCI Express Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI Express (secondary) interface, and the destination side is the PCI (primary) interface.

If a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction is considered corrupt. The PEX 8111 inverts the parity for every data when completing the transaction on the PCI bus.

Table 8-1 provides the translation the PEX 8111 performs when it forwards a non-posted PCI Express request (read or write) to the PCI bus, and the request is completed immediately on the PCI bus either normally or with an error condition.

Table 8-1. PEX 8111 Translation - Non-Posted PCI Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with parity error (reads)	Successful (poisoned TLP)
Completion with parity error (non-posted writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

8.2.1 Received Poisoned TLP

When a write request or read completion is received by the PCI Express interface, and the data is poisoned, the following occur:

- The *Secondary Detected Parity Error* bit is set in the **Secondary Status** register.
- The *Secondary Master Data Parity Error* bit is set in the **Secondary Status** register if the poisoned TLP is a read completion and the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.
- The parity bit associated with each DWORD of data is inverted.
- For a poisoned write request, the *Master Data Parity Error* bit in the **PCI Status** register is set if the *Parity Error Response Enable* bit in the **PCI Command** register is set, and the bridge sees PERR# asserted when the inverted parity is detected by the PCI target device.

8.2.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI bus, and an uncorrectable PCI error is detected.

8.2.2.1 Immediate Reads

When the PEX 8111 forwards a read request (I/O or Memory) from the PCI Express secondary interface and detects an uncorrectable data error on the PCI primary bus while receiving an immediate response from the completer, the following occur:

- The *Master Data Parity Error* bit in the **PCI Status** register is set if the *Parity Error Response Enable* bit is set in the **PCI Command** register.
- The *Detected Parity Error* bit in the **PCI Status** register is set.
- PERR# is asserted on the PCI interface if the *Parity Error Response Enable* bit in the **PCI Command** register is set.

After detecting an uncorrectable data error on the destination bus for an immediate read transaction, the PEX 8111 continues to fetch data until the byte count is satisfied or the target ends the transaction.

When the bridge creates the PCI Express completion, it forwards it with Successful Completion status and poisons the TLP.

8.2.2.2 Non-Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI primary interface while forwarding a non-poisoned non-posted write transaction from PCI Express, the following occur:

- The *Master Data Parity Error* bit in the **PCI Status** register is set if the *Parity Error Response Enable* bit is set in the **PCI Command** register.
- A PCI Express completion with Unsupported Request status is returned.

8.2.2.3 Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI primary interface while forwarding a non-poisoned posted write transaction from PCI Express, the following occur:

- The *Master Data Parity Error* bit in the **PCI Status** register is set if the *Parity Error Response Enable* bit is set in the **PCI Command** register.
- After the error is detected, the remainder of the data is forwarded.

8.2.3 PCI Address Errors

When the PEX 8111 forwards transactions from PCI Express to PCI, PCI Address errors are reported by the assertion of the SERR# pin by the PCI target. The PEX 8111 ignores the assertion of SERR#, and lets the PCI Central Resource service the error.

8.2.4 PCI Master Abort on Posted Transaction

When a transaction forwarded from PCI Express to PCI results in a Master Abort on the PCI bus, the following occur:

- The entire transaction is discarded.
- The *Received Master Abort* bit in the **PCI Status** register is set.

8.2.5 PCI Master Abort on Non-Posted Transaction

When a non-posted transaction forwarded from PCI Express to PCI results in a Master Abort on the PCI bus, the following occur:

- A PCI Express completion with Unsupported Request status is returned.
- Set the *Received Master Abort* bit in the **PCI Status** register.

8.2.6 PCI Target Abort on Posted Transaction

When a posted transaction forwarded from PCI Express to PCI results in a Target Abort on the PCI bus, the following occur:

- The entire transaction is discarded.
- The *Received Target Abort* bit in the **PCI Status** register is set.

8.2.7 PCI Target Abort on Non-Posted Transaction

When a non-posted transaction forwarded from PCI Express to PCI results in a Target Abort on the PCI bus, the following occur:

- A PCI Express completion with Completer Abort status is returned.
- The *Received Target Abort* bit in the **PCI Status** register is set.

8.2.8 PCI Retry Abort on Posted Transaction

When a posted transaction forwarded from PCI Express to PCI results in a Retry Abort on the PCI bus, the following occur:

- The entire transaction is discarded.
- The *PCI Express to PCI Retry Interrupt* bit in the **IRQSTAT** register is set.

8.2.9 PCI Retry Abort on Non-Posted Transaction

When a non-posted transaction forwarded from PCI Express to PCI results in a Retry Abort on the PCI bus, the following occur:

- A PCI Express completion with Completer Abort status is returned.
- The *PCI Express to PCI Retry Interrupt* bit in the **IRQSTAT** register is set.
- The *Secondary Signaled Target Abort* bit in the **Secondary Status** register is set.

8.3 PCI Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI bus, and the destination side is the PCI Express. The PEX 8111 supports TLP poisoning as a transmitter to permit proper forwarding of parity errors that occur on the PCI interface. Posted write data received on the PCI interface with bad parity are forwarded to PCI Express as Poisoned TLPs.

Table 8-2 provides the error forwarding requirements for Uncorrectable data errors detected by the PEX 8111 when a transaction targets the PCI Express interface.

Table 8-2. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with parity error	Write request with poisoned TLP
Read Completion with parity error in data phase	Read completion with poisoned TLP
Configuration or I/O Completion with parity error in data phase	Read/Write completion with Completer Abort Status.

Table 8-3 describes the bridge behavior on a PCI delayed transaction that is forwarded to PCI Express as a Memory Read request or an I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 8-3. Bridge Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Target Abort	Normal completion
Completer Abort	Target Abort	

8.3.1 Received PCI Errors

8.3.1.1 Uncorrectable Data Error on Non-Posted Write

When a non-posted write is addressed such that it crosses the bridge, and the PEX 8111 detects an uncorrectable data error on the PCI interface, the following occur:

- The *Detected Parity Error* status bit in the **PCI Status** register is set.
- If the *Parity Error Response Enable* bit in the **PCI Command** register is set, the transaction is discarded and is not forwarded to PCI Express. The PCI PERR# signal is asserted.
- If the *Parity Error Response Enable* bit in the **PCI Command** register is not set, the data is forwarded to PCI Express as a poisoned TLP. The *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set. The PCI PERR# signal is not asserted.

8.3.1.2 Uncorrectable Data Error on Posted Write

When the PEX 8111 detects an uncorrectable data error on the PCI interface for a posted write transaction that crosses the bridge, the following occur:

- The PCI PERR# signal is asserted if the *Parity Error Response Enable* bit in the **PCI Command** register is set.
- The *Detected Parity Error* status bit in the **PCI Status** register is set.
- The posted write transaction is forwarded to PCI Express as a poisoned TLP.
- The *Secondary Master Data Parity Error* bit in the **Secondary Status** register is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set.

8.3.1.3 Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8111 forwards a non-poisoned or poisoned read completion from PCI Express to PCI, and PERR# is asserted by the PCI master, the following occur:

- The remainder of the completion is forwarded.
- The PCI Central Resource Function services the PERR# assertion.

8.3.1.4 Uncorrectable Address Error

When an uncorrectable address error is detected by the PEX 8111 and parity error detection is enabled via the *Parity Error Response Enable* bit in the **PCI Command** register, the following occur:

- The transaction is terminated with a Target Abort.
- The *Signaled Target Abort* bit in the **PCI Status** register is set.
- The *Detected Parity Error* bit in the **PCI Status** register is set, independent of the setting of the *Parity Error Response Enable* bit in the **PCI Command** register.
- SERR# is asserted if enabled via the *SERR Enable* bit in the **PCI Command** register.
- The *Signaled System Error* bit in the **PCI Status** register is set if SERR# is asserted.

8.3.2 Unsupported Request (UR) Completion Status

The PEX 8111 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the PCI interface. The response is controlled by the *Master Abort Mode* bit in the **Bridge Control** register. In either case, the *Secondary Received Master Abort* bit in the **Secondary Status** register is set.

8.3.2.1 Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and an Unsupported Request is not considered to be an error. When a read transaction initiated on the PCI results in the return of a completion with UR status, the PEX 8111 returns FFFFFFFFh to the originating master and terminates the read transaction on the originating interface normally (by asserting TRDY#). When a non-posted write transaction results in a completion with UR status, the PEX 8111 completes the write transaction on the originating bus normally (by asserting TRDY#) and discards the write data.

8.3.2.2 Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8111 signals a Target Abort to the originating master of a downstream read or non-posted write transaction when the corresponding request on the PCI Express interface results in a completion with UR status. Additionally, the *Signaled Target Abort* bit in the **PCI Status** register is set.

8.3.3 Completer Abort (CA) Completion Status

If the PEX 8111 receives a completion with Completer Abort status on the PCI Express interface in response to any forwarded non-posted PCI transaction, the *Secondary Received Target Abort* bit in the **Secondary Status** register is set. A completion with CA status results in a Delayed Transaction Target Abort on the PCI bus. The PEX 8111 provides data to the requesting PCI agent up to the point where data was successfully returned from the PCI Express interface and then signals Target Abort. The *Signaled Target Abort* status bit in the **PCI Status** register is set when signaling Target Abort to a PCI agent.

8.4 Timeout Errors

8.4.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout Mechanism allows requesters to abort a non-posted request if a completion does not arrive within a reasonable time. Bridges, when acting as initiators on PCI Express on behalf of internally-generated requests and requests forwarded from a secondary interface, behave as endpoints for requests that they take ownership of. If a completion timeout is detected and the link is up, the PEX 8111 responds as if an unsupported request completion has been received.

If the link is down, the *P2PE_RETRY_COUNT* field in the **PCICTL** register determines how many PCI retries occur before a Master Abort is returned to the PCI bus.

8.4.2 PCI Delayed Transaction Timeout Errors

The PEX 8111 has Delayed Transaction Timers for each queued delayed transaction. If a delayed transaction timeout is detected, the following occur:

- The *Discard Timer Status* bit in the **Bridge Control** Register is set.
- The delayed request is removed from the Non-Posted Transaction Queue.
- SERR# is asserted if the *SERR Enable* bit in the **PCI Command** register is set.

8.5 Other Errors

PCI devices can assert SERR# when detecting errors that compromise system integrity. The PEX 8111 never monitors the SERR# pin in Reverse Bridge mode, but instead lets the PCI Central Resource Function service the SERR# interrupt.

8.6 PCI Express Error Messages

When the PEX 8111 detects an ERR_FATAL, ERR_NONFATAL, or ERR_COR error, or receives an ERR_FATAL, ERR_NONFATAL, or ERR_COR message, the PCI SERR# signal is asserted if the corresponding reporting enable bit in the **ROOTCTL** register is set. When an ERR_FATAL or ERR_NONFATAL message is received, the *Secondary Received System Error* bit in the **Secondary Status** register is set, independent of the reporting enable bits in the **ROOTCTL** register.

If an Unsupported Request is received by the PEX 8111, an interrupt status bit is set in the **IRQSTAT** register. This status bit can be enabled to generate an INTx# or MSI interrupt.

Chapter 9 Exclusive (Locked) Access (Forward Bridge)

9.1 Exclusive Accesses

The exclusive access mechanism allows non-exclusive accesses to proceed in the face of exclusive accesses. This allows a master to hold a hardware lock across several accesses without interfering with non-exclusive data transfers. Masters and targets not involved in the exclusive accesses are allowed to proceed with non-exclusive accesses while another master retains a bus lock.

Exclusive access support in the PEX 8111 is enabled by the *Lock Enable* bit in the **PCICTL** register. If this bit is clear, PCI Express Memory Read Locked requests are terminated with a completion with UR status.

9.2 Lock Sequence across PEX 8111

Locked transaction sequences are generated by the Host CPU as one or more reads followed by a number of writes to the same locations. In Forward Bridge mode, the PEX 8111 only supports locked transaction in the downstream direction (PCI Express to PCI). Upstream locked transactions are not allowed. The initiation of a locked transaction sequence through the PEX 8111 is as follows:

- A locked transaction begins with a MRdLk Request.
- Any successive reads for the locked transaction also use MRdLk Requests.
- The completions for any successful MRdLk Request use the CplDLk Completion type, or the CplLk Completion type for unsuccessful Requests.
- When the Locked Completion for the first Locked Read Request is returned, the PEX 8111 does not accept new requests from the PCI bus.
- All writes for the locked sequence use MWr Requests.
- The PEX 8111 remains locked until it is unlocked by the PCI Express. The unlock is then propagated to the PCI bus by terminating the locked sequence.
- The PCI Express Unlock Message is used to indicate the end of a locked sequence. Upon receiving an Unlock Message, the PEX 8111 unlocks itself. If the PEX 8111 is not locked, it ignores the unlock message.

When the locked read request is queued in the PE2P Non-Posted Transaction Queue, subsequent non-posted non-locked requests from the PCI Express are completed with Unsupported Request status. Any requests that were queued before the locked read request are allowed to complete.

9.3 PCI Master Rules for supporting LOCK#

The PEX 8111 must obey the following rules when performing locked sequences on the PCI bus:

- A master can access only a single resource during a lock operation.
- The first transaction of a lock operation must be a Memory Read transaction.
- LOCK# must be asserted during the clock cycle following the address phase and kept asserted to maintain control.
- LOCK# must be released if the initial transaction of the lock request is terminated with Retry (Lock was not established).
- LOCK# must be released whenever an access is terminated by Target Abort or Master Abort.
- LOCK# must be de-asserted between consecutive lock operations for a minimum of one clock cycle while the bus is in the Idle state.

9.4 Acquiring Exclusive Access across PEX 8111

When a PCI Express Locked Memory Read request appears at the output of the non-posted request queue, the locked request is performed on the PCI bus. The PEX 8111 monitors the state of the PCI LOCK# pin when attempting to establish lock. If it is asserted, the PEX 8111 does not request the PCI bus to start the transaction.

Once LOCK# is de-asserted and the PCI bus is idle, REQ# is asserted. While waiting for GNT#, the PEX 8111 continues to monitor LOCK#. If LOCK# is ever busy, the PEX 8111 de-asserts REQ# because another agent has gained control of LOCK#.

When the PEX 8111 is granted the bus and LOCK# is not asserted, ownership of LOCK# has been obtained. The PEX 8111 is free to perform an exclusive operation when the current transaction completes. LOCK# is de-asserted during the first address phase, and then is asserted one clock cycle later. A locked transaction is not established on the bus until completion of the first data phase of the first transaction (IRDY# and TRDY# asserted).

If the target terminates the first transaction with Retry, the PEX 8111 terminates the transaction and releases LOCK#. Once the first data phase completes, the PEX 8111 keeps LOCK# asserted until either the lock operation completes or a Master Abort or Target Abort causes an early termination.

9.5 Non-Posted Transactions and Lock

The PEX 8111 must consider itself locked when a locked memory read request is detected on the output of the non-posted request queue, even though no data has transferred. This condition is referred to as a target-lock. While in target-lock, the PEX 8111 does not process any new requests on the PCI Express.

The bridge locks the PCI bus when lock sequence on the PCI bus has completed. A target-lock becomes a full-lock when the locked request is completed on the PCI Express. At this point, the PCI Express master has established the lock.

9.6 Continuing Exclusive Access

When the PEX 8111 performs another transaction to a locked target, LOCK# is de-asserted during the address phase. The locked target accepts and responds to the request. LOCK# is asserted one clock cycle after the address phase to keep the target in the locked state and allow the PEX 8111 to retain ownership of LOCK# beyond the end of the current transaction.

9.7 Completing Exclusive Access

When the PEX 8111 receives an Unlock Message from the PCI Express, it de-asserts LOCK# on the PCI bus.

9.8 Invalid PCI Express Requests while Locked

When the PEX 8111 is locked, it only accepts PCI Express MRdLk or MWr transactions that are being forwarded to the PCI bus. Any other type of transaction is terminated with a completion with Unsupported Request status, including non-posted accesses to internal configuration registers and shared memory.

9.9 Locked Transaction Originating on PCI Bus

Locked transactions originating on the secondary bus are not allowed to propagate to the primary bus. If a locked transaction is performed on the PCI bus and is intended for the PEX 8111, the PEX 8111 ignores the transaction.

9.10 PCI Bus Errors while Locked

9.10.1 PCI Master Abort during Non-Posted Transaction

If a PCI Master Abort occurs during a PCI Express to PCI locked read transaction, the PEX 8111 de-asserts LOCK#, thus releasing the PCI bus from the locked state. Also, the PCI Express bus is released from the locked state, even though no Unlock Message has been received. A CplLk with Unsupported Request status is returned to the PCI Express bus.

Refer to Section 7.2.5 "PCI Master Abort on Non-Posted Transaction," for additional details describing the action taken if a Master Abort is detected during a non-posted transaction.

9.10.2 PCI Master Abort during Posted Transaction

If a PCI Master Abort occurs during a PCI Express to PCI locked write transaction, the PEX 8111 de-asserts LOCK#, thus releasing the PCI bus from the locked state. Also, the PCI Express bus is released from the locked state, even though no Unlock Message has been received. The write data is discarded.

See section PCI Master Abort during Posted Transaction for additional details describing the action taken if a Master Abort is detected during a posted transaction.

9.10.3 PCI Target Abort during Non-Posted Transaction

If a PCI Target Abort occurs during a PCI Express to PCI locked read transaction, the PEX 8111 de-asserts LOCK#, thus releasing the PCI bus from the locked state. Also, the PCI Express bus is released from the locked state, even though no Unlock Message has been received. A CplLk with Completer Abort status is returned to the PCI Express bus.

See section PCI Target Abort during Non- Posted Transaction for additional details describing the action taken if a Target Abort is detected during a non-posted transaction.

9.10.4 PCI Target Abort during Posted Transaction

If a PCI Target Abort occurs during a PCI Express to PCI locked write transaction, the PEX 8111 de-asserts LOCK#, thus releasing the PCI bus from the locked state. Also, the PCI Express bus is released from the locked state, even though no Unlock Message has been received. The write data is discarded.

See section PCI Master Abort on Posted Transaction for additional details describing the action taken if a Target Abort is detected during a posted transaction.

Chapter 10 Exclusive (Locked) Access (Reverse Bridge)

10.1 Exclusive Accesses

A reverse bridge is allowed to pass locked transactions from the primary interface (PCI) to the secondary interface (PCI Express). If a locked request (LOCK# asserted) is initiated on the PCI bus, then a Memory Read Locked Request is issued to the PCI Express bus. All subsequent locked read transactions targeting the PEX 8111 use the Memory Read Locked Request on the PCI Express bus. All subsequent locked write transactions use the Memory Write Request on the PCI Express bus. The PEX 8111 must send the Unlock message when PCI Lock sequence is complete.

Exclusive access support in the PEX 8111 is enabled by the *Lock Enable* bit in the **PCICTL** register. If this bit is clear, the PCI LOCK# pin is ignored, and locked transactions are treated as unlocked transactions.

10.2 PCI Target Rules for Supporting LOCK#

- The PEX 8111, acting as a target of an access, locks itself when LOCK# is de-asserted during the address phase and is asserted during the following clock cycle.
- Lock is established when LOCK# is de-asserted during the address phase, asserted during the following clock cycle, and data is transferred during the current transaction.
- Once lock is established, the PEX 8111 remains locked until both FRAME# and LOCK# are sampled de-asserted, regardless of how the transaction is terminated.
- The PEX 8111 is not allowed to accept any new requests (from either PCI or PCI Express) while it is in a locked condition except from the owner of LOCK#.

10.3 Acquiring Exclusive Access across PEX 8111

A PCI master attempts to forward a locked memory read transaction to the PCI Express bus. The transaction is terminated by the PEX 8111 with a Retry, and the locked request is written to the P2PE Non-Posted Transaction Queue. When this locked request reaches the top of the queue, the locked request is performed on the PCI Express bus as a MRdLk Request. When the PCI Express responds with a locked completion, the locked request is updated with completion status. When the PCI master retries the locked memory read request, the PEX 8111 responds with TRDY#, thus completing the lock sequence.

When the PEX 8111 is locked, it only accepts PCI locked transactions that are being forwarded to the PCI Express bus. Other bus transactions are terminated with a Retry, including accesses to internal configuration registers and shared memory. All PCI Express requests are terminated with a completion with Unsupported Request status.

10.4 Completing Exclusive Access

When the PEX 8111 detects LOCK# and FRAME# de-asserted, it sends an Unlock message to the PCI Express.

10.5 PCI Express Locked Read Request

If a locked read request is performed on the PCI Express bus, the PEX 8111 responds with a completion with Unsupported Request status.

10.6 Limitations

In a system with multiple PCI masters that perform exclusive transactions to the PCI Express bus, the *Lock Enable* bit in the **PCICTL** register must be set.

Chapter 11 Power Management (Forward Bridge)

11.1 Link State Power Management

PCI Express defines Link power management states, replacing the bus power management states that were defined by the PCI Power Management (PCI-PM) specification. Link states are not visible to PCI-PM legacy compatible software, and are either derived from the power management D-states or by Active State power management protocols.

11.1.1 Link Power States

The following link power states are supported by the PEX 8111.

- L0 – Active state. All PCI Express operations are enabled.
- L0s – A low resume latency, energy saving "standby" state
- L1 – Higher latency, lower power "standby" state. L1 support is required for PCI-PM compatible power management. L1 is optional for Active State Link power management.

  All platform provided main power supplies and component reference clocks must remain active at all times in L1. The internal PLLs of the component may be shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered whenever all functions of a downstream component on a given PCI Express Link are either programmed to a D-state other than D0, or if the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request.

  Exit from L1 is initiated by an upstream initiated transaction targeting the downstream component, or by the desire of the downstream component to initiate a transaction heading upstream. Transition from L1 to L0 is typically a few microseconds. TLP and DLLP communication over a Link that is in the L1 state is prohibited.
- L2/L3 Ready – Staging point for removal of main power. L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to PCI-PM D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for either L2 or L3, but not actually in either of those states until main power has been removed. Depending upon the implementation choices of the platform with respect to providing a Vaux supply, after main power has been removed, the Link either settles into L2 (i.e., Vaux is provided), or it settles into a zero power "off" state (see L3).

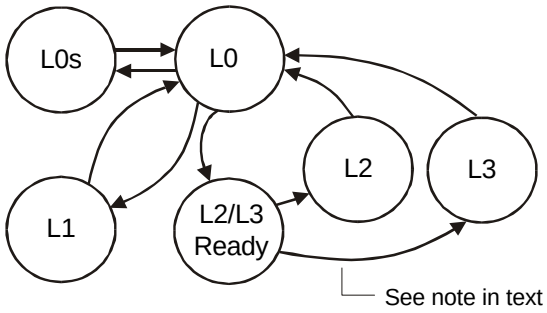
  The PEX 8111 does not support L2, so it settles into the L3 state. The L2/L3 Ready state entry transition process must begin as soon as possible following the PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its transmit Port. TLP and DLLP communication over a Link that is in L2/L3 Ready is prohibited.

  Exit from L2/L3 Ready back to L0 may only be initiated by an upstream initiated transaction targeting the downstream component in the same manner that an upstream initiated transaction would trigger the transition from L1 back to L0.

  The case where an upstream initiated exit from L2/L3 Ready would occur corresponds to the scenario where, sometime following the transition of the Link to L2/L3 Ready but before main power is removed, and the platform power manager decides not to enter the system sleep state. A Link transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol leading up to the platform entering into in a system sleep state wherein main power has been shut off (e.g., ACPI S3 or S4 sleep state).
- L2 – Auxiliary powered link deep energy saving state. Not supported by PEX 8111.
- L3 – Link off state. Power off state.

11.1.2 Link State Transitions

The following figure highlights the L-state transitions that may occur during the course of Link operation.



The arc noted in the above figure indicates the case where the platform does not provide Vaux, as in the case of the PEX 8111. In this case, the L2/L3 Ready state transition protocol results in a state of readiness for loss of main power, and once removed the Link settles into the L3 state. Link PM Transitions from any L-state to any other L-state pass through the L0 state during the transition process with the exception of the L2/L3 Ready to L2 or L3 transitions. In this case, the Link transitions from L2/L3 Ready directly to either L2 or L3 when main power to the component is removed. (This follows along with a D-state transition from D3 for the corresponding component.)

The following sequence, leading up to entering a system sleep state, illustrates the multi-step Link state transition process:

1. System Software directs all functions of a downstream component to $D3_{hot}$.
2. The downstream component then initiates the transition of the Link to L1 as required.
3. System Software then causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
4. This message causes the subject Link to transition back to L0 to send it, and to enable the downstream component to respond with PME_TO_Ack.
5. After the PME_TO_Ack is sent, the downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

- L0 —> L1 —> L0 —> L2/L3 Ready
- The L2/L3 Ready entry sequence is initiated at the completion of the PME_Turn_Off/ PME_TO_Ack protocol handshake.

It is also possible to remove power without first placing all devices into $D3_{hot}$:

1. System Software causes the Root Complex to broadcast the PME_Turn_Off Message in preparation for removing the main power source.
2. The Downstream components respond with PME_TO_Ack.
3. After the PME_TO_Ack is sent, the Downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

1. L0 —> L2/L3 Ready

11.2 Power Management States

The PEX 8111 provides the configuration registers and support hardware required by the PCI Power Management Specification. The **PCICAPPTR** register points to the base address of the power management registers (40h in the PEX 8111).

The PEX 8111 also supports the PCI Express Active State Link power management protocol as described in the previous section.

11.2.1 Power States

The following power states are supported by the PEX 8111, and are selected by the *Power State* field in the **PWRMNGCSR** register:

- $D0_{uninitialized}$ – Power-on default state. This state is entered when power is initially applied. The *Memory Space Enable, I/O Space Enable,* and *Bus Master Enable* bits in the **PCICMD** register are all clear.
- $D0_{active}$ – Fully operational. At lease one of the following **PCICMD** bits must be set: *Memory Space Enable, I/O Space Enable, Bus Master Enable*.
- D1 – Light sleep. Only PCI Express configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. All PCI Express requests generated by the PEX 8111 are disabled except for PME Messages.
- D2 – Heavy sleep. Same restrictions as D1.
- $D3_{hot}$ – Function context not maintained. Only PCI Express configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. All PCI Express requests generated by the PEX 8111 are disabled except for PME Messages. From this state, the next power state can be either $D3_{cold}$ or $D0_{uninitialized}$. When transitioning from $D3_{hot}$ to D0, the entire chip is reset.
- $D3_{cold}$ – Device is powered-off. A power-on sequence transitions a function from the $D3_{cold}$ state to the $D0_{uninitialized}$ state. At this point software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its $D0_{active}$ state.

When transitioning from D0 to any other state, the PCI Express link transitions to link state L1.

System software must allow a minimum recovery time following a $D3_{hot}$ to D0 transition of at least 10 ms, prior to accessing the function. This recovery time may, for example, be used by the $D3_{hot}$ to D0 transitioning component to bootstrap any of its component interfaces (e.g., from serial ROM) prior to being accessible. Attempts to target the function during the recovery time (including configuration request packets) results in undefined behavior.

11.3 Power Management Signaling

PCI devices assert the PME# pin to signal a power management event. The PEX 8111 converts the PME# signal to PCI Express PME Messages. There are no internal events that cause a PME message to be sent upstream.

Power Management Messages are used to support Power Management Events signaled by devices downstream of the PEX 8111. System software needs to identify the source of a PCI Power Management Event that is reported by a PM_PME message. When the PME comes from an agent on a PCI bus, then the PM_PME Message Requester ID reports the Bus Number from which the PME was collected, and the Device Number and Function Number reported must both be zero.

When the PME message is sent to the host, the *PME Status* bit in the **PWRMNGCSR** register is set and a 100 ms timer is started. If the status bit is not cleared within 100 ms, another PME message is sent.

When the upstream device is powering down the downstream devices, it first places all devices into the $D3_{hot}$ state. It then sends a PCI Express PME_Turn_Off message. Once the PEX 8111 has received this message, it does not send any more PME messages upstream. The PEX 8111 then sends a PME_TO_Ack message to the upstream device and puts its link into the L2/L3 Ready state. It is now ready to be powered-down. If the upstream device changes the power state of the PEX 8111 back to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8111, and is not communicated to the PCI devices. The PEX 8111 does not issue a PM_PME message on behalf of a downstream PCI device while its upstream Link is in the L2/L3 non-communicating state.

To avoid loss of PME# assertions in the conversion of the level-sensitive PME# signal to the edge triggered PCI Express PM_PME message, the PCI PME# signal is polled every 256 ms by the PEX 8111 and a PCI Express PM_PME message is generated if PME# is asserted.

11.3.1 Wakeup

If the link is in the L2 state, a device on the secondary PCI bus can signal the root complex to wake up the link.

The PEX 8111 asserts the WAKEOUT# pin or sends a PCI Express beacon for the following:

- PCI PME# pin is asserted while link is in L2 state
- PCI Express beacon is received while link is in L2 state.
- PCI Express PM_PME Message is received.

A beacon is transmitted if the following are true:

- PCI PME# pin is asserted while link is in L2 state
- *Beacon Generate Enable* bit in the **DEVSPECCTL** register is set.
- *PME Enable* bit in the **PWRMNGCSR** register is set.

11.4 Set Slot Power

When a PCI Express link first comes up, or the *Slot Power Limit Value* or *Slot Power Limit Scale* fields in the Root Complex **SLOTCAP** register are changed, the Root Complex sends a Set Slot Power Message.

When the PEX 8111 receives this message, it updates its *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields in the **DEVCAP** register.

When the available power indicated by the *Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields in the **DEVCAP** register is greater than or equal to the power requirement indicated in the **POWER** register, the PWR_OK pin is asserted

Chapter 12 Power Management (Reverse Bridge)

12.1 Power Management States

The PEX 8111 provides the configuration registers and support hardware required by the PCI Power Management Specification. The **PCICAPPTR** register points to the base address of the power management registers (40h in the PEX 8111).

12.1.1 Power States

The following power states are supported by the PEX 8111, and are selected by the *Power State* field in the **PWRMNGCSR** register:

- $D0_{uninitialized}$ – Power-on default state. This state is entered when power is initially applied. The *Memory Space Enable, I/O Space Enable,* and *Bus Master Enable* bits in the **PCICMD** register are all clear.
- $D0_{active}$ – fully operational. At lease one of the following **PCICMD** bits must be set: *Memory Space Enable, I/O Space Enable, Bus Master Enable.*
- D1 – Light sleep. Only PCI configuration transactions are accepted. No master cycles are allowed, and the INTx# interrupts are disabled. The PMEOUT# pin can be asserted by the PEX 8111. The PCI clock continues to run in this state.
- D2 – Heavy sleep. Same as D1, except that the PCI host can stop the PCI clock.
- $D3_{hot}$ – Function context not maintained. Only PCI configuration transactions are accepted. From this state, the next power state can be either $D3_{cold}$ or $D0_{uninitialized}$. When transitioning from $D3_{hot}$ to D0, the entire chip is reset.
- $D3_{cold}$ – Device is powered-off. A power-on sequence transitions a function from the $D3_{cold}$ state to the $D0_{uninitialized}$ state. At this point software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its $D0_{active}$ state.

An interrupt, indicated by the *Power State Change Interrupt* bit in the **IRQSTAT** register, can be generated when the power state is changed.

12.2 Power Down Sequence

During a link power-down, the following sequence occurs:

- PCI host puts downstream PCI Express device in power state D3.
- Downstream device initiates a transition to link state L1.
- PCI host puts PEX 8111 in power state D3.
- PEX 8111 initiates a transition to L0 on the link.
- PEX 8111 generates a PCI Express PME_Turn_Off message to the PCI Express downstream device.
- Downstream device responds with a PME_TO_Ack message.
- Downstream device sends a DLLP to request transition to L2/L3 Ready state (L2.Idle Link state).
- PEX 8111 acknowledges the request, completing the transition to the L2.Idle Link State.
- PME# pin is asserted to the PCI host.
- PCI host can now remove power from the PEX 8111.

12.3 PME# Signal

PME messages from the PCI Express interface are translated to the PME# signal on the PCI bus. The *PME Status* bit in the **PWRMNGCSR** register is set when a PCI Express PME Message is received, the WAKEIN# pin is asserted, a beacon is detected, or the link transitions to the L2/L3 Ready state. The PME# pin is asserted whenever the *PME Status* bit is set and PME is enabled.

12.4 Set Slot Power

When a PCI Express link first comes up, or the *Slot Power Limit Value* or *Slot Power Limit Scale* fields in the PEX 8111 **SLOTCAP** register are changed, the PEX 8111 sends a Set Slot Power Message to the downstream PCI Express device.

When the downstream device receives this message, it updates its *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields in the **DEVCAP** register.

Chapter 13 Interrupts (Forward Bridge)

13.1 PCI Interrupts

In Forward Bridge mode, the PCI INTx# signals are inputs to the PEX 8111. The interrupt is routed to the PCI Express bus using virtual wire interrupt messages. The PCI Express supports the INTx virtual wire interrupt feature for legacy systems that still support the PCI INTx# interrupt signals. PCI INTx# interrupts are "virtualized" in PCI Express using Assert_INTx and Deassert_INTx messages, where x is A, B, C, or D for the respective PCI INTx# interrupt signals defined in PCI Specification 3.0. This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INTx and Deassert_INTx messages transmitted on the PCI Express link capture the asserting/de-asserting edge of the respective PCI INTx# signal.

The Requester ID used in the PCI Express Assert_INTx and Deassert_INTx messages transmitted by the PEX 8111 (irrespective of whether the source is internal or external to the bridge) equals the bridge primary interface Bus Number and Device Number. The Function Number sub-field is set to zero.

13.2 Internally Generated Interrupts

The following internal events can be programmed to generate an interrupt:

- EEPROM transaction done
- GPIO bit change
- Mailbox register written

When one of these interrupts occurs, the interrupt can be produced using one of two methods:

13.2.1 Virtual Wire Interrupts

If MSI is disabled, virtual wire interrupts can be used to support internal interrupt events. Internal interrupt sources are masked by the *Interrupt Disable* bit in the **PCI Command** register and are routed to one of the virtual interrupts using the **PCI Interrupt Pin** register. PCI Express Assert_INTx and Deassert_INTx messages are not masked by the *Bus Master Enable* bit located in the **PCI Command** register. The internal interrupt is processed the same as the corresponding PCI interrupt signal.

13.2.2 Message Signaled Interrupts

The PCI Express bus supports interrupts using Message Signaled Interrupts (MSI). With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8111 uses the 64-bit Message Address version of the MSI capability structure and clears the No Snoop and Relaxed Ordering bits in the Requester Attributes. There are address and data configuration registers associated with the MSI feature (**MSIADDR, MSIUPPERADDR, MSIDATA)**. When an internal interrupt event occurs, the value in the MSI Data configuration register is written to the PCI Express address specified by the MSI Address configuration registers.

The MSI feature is enabled by the *MSI Enable* bit in the **MSICTL** register. If MSI is enabled, the virtual wire interrupt feature is disabled. MSI interrupts are generated independently of the *Interrupt Disable* bit in the **PCI Command** register. MSI interrupts are gated by the *Bus Master Enable* bit in the **PCI Command** register.

Chapter 14 Interrupts (Reverse Bridge)

14.1 PCI Interrupts

In Reverse Bridge mode, the PCI INTx# signals are outputs from the PEX 8111. Each INTx# signal is asserted or de-asserted when the corresponding PCI Express Assert_INTx or Deassert_INTx message is received. The INTx# signals are asserted independently of the *Interrupt Disable* bit in the **PCI Command** register. The INTx# signals are only asserted when the PEX 8111 is in power state D0.

14.2 Internally Generated Interrupts

The following internal events can be programmed to generate an interrupt:

- EEPROM transaction done
- GPIO bit change
- Mailbox register written

When one of these interrupts occurs, the interrupt can be produced using one of two methods:

14.2.1 INTx# Signals

When an internal interrupt event occurs, it can cause one of the PCI INTx# signals to be asserted. Internal interrupt sources are masked by the *Interrupt Disable* bit in the **PCI Command** register and are routed to one of the INTx# signals using the **PCI Interrupt Pin** register. The INTx# signals are only asserted when Message Signaled Interrupts are disabled.

14.2.2 Message Signaled Interrupts

The PCI bus supports interrupts using Message Signaled Interrupts (MSI). With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8111 uses the 64-bit Message Address version of the MSI capability structure. There are address and data configuration registers associated with the MSI feature (**MSIADDR, MSIUPPERADDR, MSIDATA)**. When an internal interrupt event occurs, the value in the MSI Data configuration register is written to the PCI Express address specified by the MSI Address configuration registers.

The MSI feature is enabled by the *MSI Enable* bit in the **MSICTL** register. If MSI is enabled, the INTx# interrupt signals for internally generated interrupts are disabled. MSI interrupts are generated independently of the *Interrupt Disable* bit in the **PCI Command** register. MSI interrupts are gated by the *Bus Master Enable* bit in the **PCI Command** register.

Chapter 15 PCI Express Messages (Forward Bridge)

15.1 Introduction

PCI Express defines a set of messages that are used as a method for in-band communication of events (e.g., interrupts), generally replacing the need for sideband signals. These messages may also be used for general purpose messaging. PCI Express to PCI bridge support requirements for these messages are described in the sections below.

PCI Express messages are routed either explicitly or implicitly depending on specific bit field encodings in the message request header. An explicitly routed message is routed based either on a specific address or on an ID field contained within the message header. The destination of an implicitly routed message is inferred from the message Type field.

15.2 INTx# Interrupt Signaling

INTx# Interrupt Signaling messages are used for in-band communication of the state of the PCI line based interrupts INTA#, INTB#, INTC#, and INTD# for devices downstream of the bridge. Refer to Chapter 13, "Interrupts (Forward Bridge)," for details.

15.3 Power Management Messages

Power Management Messages are used to support Power Management Events signaled by sources integrated into the bridge and for devices downstream of the bridge. Refer to Chapter 11, "Power Management (Forward Bridge)," for details.

15.4 Error Signaling Messages

Error Signaling Messages are transmitted by the bridge on its PCI Express primary interface to signal an error for a particular transaction, for the link interface, for errors internal to the bridge, or for PCI related errors detected on the secondary interface. The message types include ERR_COR, ERR_NONFATAL, and ERR_FATAL and the relevant mask bits are located in the PCI Express Capability Structure. Refer to Chapter 7, "Error Handling (Forward Bridge)," for details.

15.5 Locked Transactions Support

The PCI Express Unlock Message is used to support Locked Transaction sequences in the downstream direction. Refer to Chapter 9, "Exclusive (Locked) Access (Forward Bridge)," for details.

15.6 Slot Power Limit Support

The Set_Slot_Power_Limit Message is transmitted to endpoints, including bridges, by the Root Complex or a Switch. The PEX 8111 supports and complies with these messages. These messages are particularly relevant to bridges implemented on add-in cards. Refer to Chapter 11, "Power Management (Forward Bridge)," and Chapter 12, "Power Management (Reverse Bridge)," for details.

15.7 Hot Plug Signaling Messages

The PEX 8111 does not support Hot Plug Signaling, and ignores the associated messages.

Chapter 16 PCI Express Messages (Reverse Bridge)

16.1 INTx# Interrupt Message Support

The PEX 8111 controls the state of the corresponding PCI interrupt pins based on the Assert_INTx and Deassert_INTx messages received.

16.2 Power Management Message Support

The PEX 8111 generates a PME_Turn_Off message when placed into power state D3. The PEX 8111 then waits for the PME_TO_Ack message from the downstream device before proceeding with the power-down sequence.

16.2.1 PME Handling Requirements

The PEX 8111 translates PME messages from the PCI Express interface to the PME# signal on the PCI bus. The PEX 8111 converts the edge triggered PME events on the PCI Express interface to the level triggered PME# signal on PCI. The PEX 8111 signals PME# on the PCI bus for the following:

- PCI Express WAKEIN# signal is asserted while link is in L2 state.
- PCI Express beacon is received while link is in L2 state.
- PCI Express PM_PME Message is received.

For compatibility with existing software, the PEX 8111 does not signal PME# unless the PME signaling is enabled by the *PME Enable* bit in the **PWRMSGCSR** register. The PEX 8111 sets its *PME Status* bit when PME# is signaled and clears PME# when the *PME Status* bit or the *PME Enable* bit is cleared. All PME messages received while the *PME Enable* bit is cleared are ignored and the *PME Status* bit is not set during this time.

16.3 Error Signaling Message Support

The PEX 8111 converts all ERR_COR, ERR_FATAL and ERR_NONFATAL Messages to SERR# on the PCI interface.

16.4 Locked Transaction Support

The PEX 8111 is allowed to pass locked transactions from the primary interface to the secondary interface. The PEX 8111 uses the Memory Read Locked request to initiate a locked sequence when a locked request is sent on the PCI bus. All subsequent locked read transactions targeting the bridge use the Memory Read Locked request on PCI Express. All subsequent locked write transactions use the Memory Write request on PCI Express. The PEX 8111 sends the Unlock Message when PCI Lock sequence is complete.

Chapter 17 Initialization (Forward Bridge)

17.1 Introduction

The actions that the PEX 8111 takes upon receipt of various reset events and interface initialization requirements are described in the following sections.

17.2 Reset Behavior

There are three types of reset that the PEX 8111 receives over the PCI Express primary interface:

- Physical layer resets that are platform specific and referred to as "Fundamental Resets" (cold/warm reset)
- PCI Express Physical Layer mechanism (Hot Reset)
- PCI Express Data Link transitioning to the Down state of primary interface.

These three primary interface reset sources are each described in sections that follow. All primary interface reset events initiate a Secondary Bus Reset which resets the PCI bus. In addition to primary interface reset sources, the PEX 8111 supports a PCI bus reset by way of the **Bridge Control** Register.

When attempting a Configuration access to devices on the PCI bus behind the PEX 8111, the timing parameter Trhfa (2^{25} PCI Clocks) must be respected after reset.

17.2.1 Fundamental Reset (Cold/Warm Reset)

The PEX 8111 uses the PCI Express PERST# signal as a fundamental reset input. When the assertion of PERST# follows the power-on event, it is referred to as a cold reset. The PCI Express system may also generate this signal without removing power; this is referred to as a warm reset. The PEX 8111 treats cold and warm resets without distinction. The PEX 8111 state machines are asynchronously reset, and the configuration registers are initialized to their default values when this signal is asserted. The PEX 8111 also tri-states its PCI outputs unless it is configured as the PCI bus parking agent.

The PEX 8111 propagates the warm/cold reset from its primary interface to PCI reset on the secondary interface. The PCI RST# signal is asserted while PERST# is asserted. During a cold reset, the PCI RST# is asserted for at least 100 ms after the power levels are valid. During any other types of PCI resets, PCI RST# is asserted for at least 1 ms.

17.2.2 Primary Reset Due to Physical Layer Mechanism (Hot Reset)

PCI Express supports the Link Training Control Reset (a training sequence with the reset bit asserted), or hot reset, for propagating reset requests downstream. When the PEX 8111 receives a hot reset on its PCI Express primary interface, it propagates that reset to the PCI RST# signal. In addition, the PEX 8111 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state specified default or initial conditions. Software is responsible for ensuring that the Link Reset assertion and de-assertion messages are timed such that the bridge adheres to proper reset assertion and de-assertion durations on the PCI RST# signal.

17.2.3 Primary Reset Due to Data Link Down

When the PCI Express primary interface of the PEX 8111 is in normal operation and, for whatever reason, the Link goes down, the Transaction and Data Link Layers enter the DL_Down state. The PEX 8111 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state specified default or initial conditions. In addition, the entry of the primary interface of the PEX 8111 into DL_Down status initiates a reset of the PCI bus using the PCI RST# signal.

17.2.4 Secondary Bus Reset by way of Bridge Control Register

A reset of the PCI secondary interface may be initiated by software through assertion of the *Secondary Bus Reset* bit in the **Bridge Control** Register. This targeted reset may be used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration. A write to *the Secondary Bus Reset* bit forces the assertion of the secondary interface PCI reset (RST#) signal without affecting the primary interface or any configuration space registers. Additionally, the logic associated with the secondary interface is re-initialized and any transaction buffers associated with the secondary interface are cleared.

RST# is asserted as long as the *Secondary Bus Reset* bit is asserted, so software must take care to observe proper PCI reset timing requirements. Software is responsible for ensuring that the PEX 8111 does not receive transactions that require forwarding to the secondary interface while *Secondary Bus Reset* is asserted.

17.2.5 Bus Parking during Reset

The PEX 8111 drives the secondary PCI bus AD[31:0], C/BE[3:0]#, and PAR signals to a logic low level (zero) when the secondary interface RST# is asserted.

Chapter 18 Initialization (Reverse Bridge)

18.1 Reset Behavior

A PCI Express hot reset (PCI Express Link Training Sequence) is generated for the following cases:

- *Secondary Bus Reset* bit is set in the **Bridge Control** register.
- Power management state transitions from D3 to D0.

Assertion of the PCI RST# pin causes the PCI Express sideband reset signal (PERST#) to be asserted.

18.2 Secondary Bus Reset by way of Bridge Control Register

A reset of the PCI Express secondary interface may be initiated by software through assertion of the *Secondary Bus Reset* bit in the **Bridge Control** register. This targeted reset may be used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration.

A write to the *Secondary Bus Reset* bit causes a PCI Express Link Reset Training Sequence to be transmitted without affecting the primary interface or any configuration space registers. Additionally, the logic associated with the secondary interface is re-initialized and any transaction buffers associated with the secondary interface are cleared.

Chapter 19 PCI Arbiter

19.1 Overview

A PCI system using the PEX 8111 can either utilize an external bus arbiter, or use the PEX 8111 internal arbiter. This internal arbiter can accept bus requests from up to four external PCI devices. The PCI Express to PCI bridge controller logic can also request control of the PCI bus.

19.2 Internal Arbiter Mode

When the EXTARB pin is de-asserted, the PEX 8111 accepts and arbitrates PCI requests from up to four external devices. The PEX 8111 supports single and multi-level arbiter modes, selected by the *PCI Multi-Level Arbiter* bit in the **PCICTL** register.

19.2.1 Single-Level Mode

The four external requests and the PCI Express to PCI Bridge Controller request are all placed into a single-level arbiter. After a device is granted the bus, it becomes the lowest level requester. All devices have the same priority. For example, if all internal and external agents are requesting the bus, then the order of the agents granted the bus would be:

- PEX 8111 PCI Initiator
- External Requester 0
- External Requester 1
- External Requester 2
- External Requester 3
- Bridge

and so forth.

19.2.2 Multi-Level Mode

The four external requests are placed into a two-level round robin arbiter with the PCI Express to PCI Bridge Controller. Level 0 alternates between the PCI Express to PCI Bridge controller and level 1, guaranteeing that the PCI Express to PCI Bridge is granted up to 50% of the accesses. Level 1 consists of the four external PCI requesters.

For example, if all internal and external agents are requesting the bus, then the order of the agents that are granted the bus would be:

- PEX 8111 PCI Initiator
- External Requester 0
- PEX 8111 PCI Initiator
- External Requester 1
- PEX 8111 PCI Initiator
- External Requester 2
- PEX 8111 PCI Initiator
- External Requester 3

and so forth.

19.3 External Arbiter Mode

When the EXTARB pin is asserted, the PEX 8111 PCI request inputs to the internal arbiter are disabled. The PEX 8111 generates a PCI request (REQ0#) to an external arbiter when it needs to use the PCI bus. The PCI grant input (GNT0#) to the PEX 8111 allows it to become the PCI bus master.

19.4 Arbitration Parking

The PCI bus is not allowed to float for more than 8 clock cycles. When there are no requests for the bus, the arbiter selects a device to drive the bus to a known state by driving its GNT# pin active. When the EXTARB pin is de-asserted (internal arbiter mode), the PEX 8111 selects a PCI master to be parked on the bus during idle periods. The *PCI Arbiter Park Select* field of the **PCICTL** register determines which master is parked on the bus. When parked (GNT# driven during idle bus), the device drives AD[31:0], C/BE[3:0]#, and PAR to a known state.

In Forward Bridge mode, the PEX 8111 parks on the PCI bus during reset, independent of the EXTARB signal.

Chapter 20 Shared Memory

20.1 Overview

The PEX 8111 has a 2Kx32 bit (8 KByte) memory block that can be accessed from the EEPROM, PCI Express bus, or PCI bus.

20.2 EEPROM Accesses

When the *Shared Memory Load* bit in the EEPROM format byte is set, the shared memory is loaded from the EEPROM starting at location REG BYTE COUNT + 6. The number of bytes to load is determined by the value in EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5. The EEPROM data is always loaded into the shared memory starting at address 0. Data is transferred from the EEPROM to the shared memory in units of DWORDs. Refer to Chapter 4, "EEPROM Controller," for details.

20.3 PCI Express Accesses

The shared memory is accessed using the 64 KByte address space defined by the **Base Address Register 0** register. The shared memory is located at address offset 'h8000 in this space. PCI Express posted writes are used to write data to the shared memory. Either single or burst writes are accepted, and PCI Express first and last byte enables are supported. If shared memory write data is poisoned, the data is discarded and an ERR_NONFATAL Message is generated if enabled. PCI Express non-posted reads are used to read data from the shared memory. Either single or burst reads are accepted. If the 8K boundary of the shared memory is reached during a burst write or read, the address wraps around to the beginning of the memory.

20.4 PCI Accesses

The shared memory is accessed using the 64 KByte address space defined by the **Base Address Register 0** register. The shared memory is located at address offset 'h8000 in this space. PCI single or burst writes are used to write data to the shared memory. PCI byte enables are supported for each DWORD transferred. PCI single or burst reads are used to read data from the shared memory. If the 8K boundary of the shared memory is reached during a burst write or read, a PCI Disconnect is generated.

Chapter 21 Configuration Registers

21.1 Register Description

The PCI-Compatible Configuration Registers are accessed by the PCI Express host (Forward Bridge mode) or by the PCI host (Reverse Bridge mode) using the PCI configuration address space. All configuration registers can be accessed from the PCI Express or PCI bus using the 64 KByte memory space defined by PCI Base Address 0. Any register that can be written by the EEPROM controller can also be written using memory writes through PCI Base Address 0.

In Reverse Bridge mode, a PCI master cannot access any of the PCI Express Extended Capability Registers using PCI Configuration transactions.

When the configuration registers are accessed using memory transactions to Base Address Register 0, the following address mapping is used.

Table 21-1. Base Address Register 0 Address Mapping

A15	A13	A12	Register Space
0	0	0	PCI-Compatible Configuration Registers
0	0	1	Memory-Mapped Configuration Registers
0	1	x	Memory-Mapped PCI Express Endpoint Registers (Reverse Bridge mode only)
1	x	x	8 KB Internal shared memory

The EEPROM controller can write to any of the configuration registers. An upper address bit is used to select one of the two register spaces.

Table 21-2. Selecting Register Space

A12	Register Space
0	PCI-Compatible Configuration Registers
1	Memory-Mapped Configuration registers

Each register is 32 bits wide, and can be accessed a byte, word, or DWORD at a time. These registers utilize little endian byte ordering which is consistent with the PCI Local Bus Specification. The least significant byte in a DWORD is accessed at address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8111 is powered-up or reset, the registers are set to their default values. Writes to unused registers are ignored, and reads from unused registers return a value of 0.

21.2 Configuration Access Types

CFG – These are accesses initiated by PCI Configuration transactions on the primary bus.

MM – These are accesses initiated by PCI Memory transactions on either the primary or secondary bus using the address range defined by PCI Base Address 0.

EE – These are accesses initiated by the EEPROM controller during initialization.

21.3 Register Attributes

The following register attributes are used to indicate the type of access provided by each register bit.

Table 21-3. Access Provided by Each Register Bit

Register Attribute	Description
HwInit	**Hardware Initialized**. Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. Bits are read-only after initialization and can only be reset with "Fundamental Reset."
RO	**Read-only register**. Register bits are read-only and cannot be altered by software. Register bits may be initialized by hardware mechanisms such as pin strapping or serial EEPROM.
RW	**Read-Write register.** Register bits are read-write and may be either set or cleared by software to the desired state.
RW1C	**Read-only status, Write-1-to-clear status register.** Register bits indicate status when read; a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1C bits has no effect.
WO	**Write-only**. This attribute is used to indicate that a register can be written by the EEPROM controller.
RsvdP	**Reserved and Preserved**. Reserved for future RW implementations. Registers are read-only and must return 0 when read. Software must preserved value read for writes to bits.
RsvdZ	**Reserved and Zero.** Reserved for future RW1C implementations. Registers are read-only and must return 0 when read. Software must use 0 for writes to bits.

21.4 Register Summary

Table 21-4. Register Summary

Register Group	PCI Space	Address Range
PCI-Compatible Configuration Registers	PCI Express Configuration (Forward Bridge mode); PCI Configuration (Reverse Bridge mode)	000-0FFh
	Memory-Mapped, BAR0	000-0FFh
PCI Express Extended Capability Configuration Registers	PCI Express Configuration (Forward Bridge mode)	100-1FFh
	Memory-Mapped, BAR0	100-1FFh
Main Control Registers	Memory-Mapped, BAR0	1000-10FFh
PCI Express Configuration Registers using Enhanced Configuration Access	Memory-Mapped, BAR0	2000-2FFFh
8 KBytes General Purpose Memory	Memory-Mapped, BAR0	8000-9FFFh

21.5 Register Mapping

21.5.1 PCI-Compatible Configuration Registers (Type 1)

Table 21-5. PCI-Compatible Configuration Registers (Type 1)

PCI Configuration Register Address	31 24	23 16	15 8	7 0
00h	Device ID		Vendor ID	
04h	Status		Command	
08h	Class Code			Revision ID
0Ch	BIST	Header Type	Primary Latency Timer	Cache Line Size
10h	PCI Base Address 0 for Memory-Mapped Configuration Registers			
14h	PCI Base Address 1 (Not used)			
18h	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Base Upper 32 Bits			
2Ch	Prefetchable Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	***Reserved***			Capabilities Pointer
38h	PCI Base Address for Expansion ROM (Not Supported)			
3Ch	Bridge Control		Interrupt Pin	Interrupt Line

21.5.2 PCI-Compatible Extended Capability Registers for PCI Express Bus

Table 21-6. PCI-Compatible Extended Capability Registers for PCI Express Bus

PCI Configuration Register Address	31 24	23 16	15 8	7 0
40h	Power Management Capabilities		Next Item Pointer	Capability ID
44h	Data	Bridge Extensions	Power Management CSR	
48h	Device Specific Control			
4C-4Fh	***Reserved***			
50h	Message Control		Next Item Pointer	Capability ID
54h	Message Address			
58h	Message Upper Address			
5Ch	***Reserved***		Message Data	
60h	PCI Express Capabilities		Next Item Pointer	Capability ID
64h	Device Capabilities			
68h	Device Status		Device Control	
6Ch	Link Capabilities			
70h	Link Status		Link Control	
74h	Slot Capabilities			
78h	Slot Status		Slot Control	
7Ch	***Reserved***		Root Control	
80h	Root Status			

21.5.3 PCI Express Extended Capability Registers

Table 21-7. Power Budgeting Capability and Device Serial Number Registers

PCI Express Configuration Register Address	31 24	23 16	15 8	7 0
100h	Next Capability Offset	Capability Version	PCI Express Extended Capability ID	
104h	***Reserved***			Data Select Register
108h	Data Register			
10Ch	***Reserved***			Power Budget Capability Register
110h	Next Capability Offset	Capability Version	PCI Express Extended Capability ID	
114h	Serial Number Register (Lower DW)			
118h	Serial Number Register (Upper DW)			

21.5.4 Main Control Registers

Table 21-8. Main Control Registers

Register	Address	Description	Page
DEVINIT	1000h	Device Initialization	142
EECTL	1004h	EEPROM Control	143
EECLKFREQ	1008h	EEPROM Clock Frequency	143
PCICTL	100Ch	PCI Control	144
PCIEIRQENB	1010h	PCI Express Interrupt Enable	145
PCIIRQENB	1014h	PCI Interrupt Enable	145
IRQSTAT	1018h	Interrupt Status	146
POWER	101Ch	Power Required	146
GPIOCTL	1020h	General-Purpose I/O Control	147
GPIOSTAT	1024h	General-Purpose I/O Status	148
MAILBOX0	1030h	Mailbox 0	148
MAILBOX1	1034h	Mailbox 1	148
MAILBOX2	1038h	Mailbox 2	148
MAILBOX3	103Ch	Mailbox 3	148
CHIPREV	1040h	Chip Silicon Revision	149
DIAG	1044h	Diagnostics	149
TLPCFG0	1048h	TLP Controller Configuration 0	150
TLPCFG1	104Ch	TLP Controller Configuration 1	150
TLPCFG2	1050h	TLP Controller Configuration 2	150
TLPTAG	1054h	TLP Controller Tag	151
TLPTIMELIMIT0	1058h	TLP Controller Time Limit 0	151
TLPTIMELIMIT1	105Ch	TLP Controller Time Limit 1	151
CRSTIMER	1060h	CRS Retry Timer	152
ECFGADDR	1064h	Enhanced Configuration Address	152

21.6 PCI-Compatible Configuration Registers (Type 1)

Table 21-9. (Address 00h; PCIVENDID) PCI Vendor ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID**. This field identifies the manufacturer of the device.	RO	RW	WO	10B5h

Table 21-10. (Address 02h; PCIDEVID) PCI Device ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Device ID**. This field identifies the particular device, as specified by the Vendor.	RO	RW	WO	8111h

Table 21-11. (Address 04h; PCICMD) PCI Command (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Space Enable.** This bit enables the device to respond to I/O space accesses on the primary interface (PCI Express). These accesses must be directed to a target on the PCI bus, because the PEX 8111 does not have any internal I/O mapped resources.	RW	RW	WO	0
1	**Memory Space Enable.** This bit enables the device to respond to Memory space accesses on the primary interface (PCI Express). These accesses may be directed to either a target on the PCI bus, or to internal memory-mapped registers. When this bit is clear, respond to all Memory Requests on the primary interface with an Unsupported Request completion.	RW	RW	WO	0
2	**Bus Master Enable.** This bit enables the PEX 8111 to issue memory and I/O read/write requests on the primary interface (PCI Express). Requests other than memory or I/O requests are not controlled by this bit. If this bit is clear, the bridge must disable response as a target to all memory or I/O transactions on the secondary interface (PCI bus) (they cannot be forwarded to the primary interface).	RW	RW	WO	0
3	**Special Cycle Enable.** Does not apply to PCI Express, so this bit is forced to 0.	RO	RO	—	0
4	**Memory Write and Invalidate.** When set, this bit enables the PEX 8111 PCI bus master logic to use the Memory Write-and-Invalidate command. When clear, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop.** This bit does not apply to PCI Express, so it is forced to 0.	RO	RO	—	0
6	**Parity Error Response Enable.** This bit controls the response to data parity errors forwarded from the primary interface (e.g., a poisoned TLP). If clear, the bridge must ignore (but may record status such as setting the *Detected Parity Error* bit) any data parity errors that it detects and continue normal operation. If set, the bridge must take its normal action when a data parity error is detected.	RW	RW	WO	0
7	**Address Stepping Enable.** The PEX 8111 performs address stepping for PCI Configuration cycles, so this bit is read/write with an initial value of 1.	RW	RW	WO	1
8	**SERR Enable.** This bit enables reporting of non-fatal and fatal errors to the Root Complex. ***Note:*** *Errors are reported if enabled either through this bit or through the PCI-Express specific bits in the* ***Device Control Register****.*	RW	RW	WO	0
9	**Fast Back-to-Back Enable.** This bit does not apply to PCI Express, so it is forced to 0.	RO	RO	—	0
10	**Interrupt Disable.** When set, the PEX 8111 is prevented from generating INTx# interrupt messages on behalf of functions integrated into the bridge. This bit has no effect on INTx# messages generated on behalf of INTx# inputs associated with the PCI secondary interface. Any INTx# emulation interrupts already asserted must be de-asserted when this bit is set.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	—	0

Table 21-12. (Address 04h; PCICMD) PCI Command (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Space Enable.** This bit enables the PEX 8111 to respond to I/O space accesses on the primary interface (PCI). These accesses would be directed to a target on the PCI Express bus, because the PEX 8111 does not have any internal I/O mapped devices. When this bit is clear, PCI I/O accesses to the PEX 8111 result in a Master Abort.	RW	RW	WO	0
1	**Memory Space Enable.** This bit enables the PEX 8111 to respond to Memory space accesses on the primary interface (PCI). These accesses may be directed to either a target on the PCI Express bus, or to internal memory-mapped registers. When this bit is clear, PCI memory accesses to the PEX 8111 result in a Master Abort.	RW	RW	WO	0
2	**Bus Master Enable.** When set, this bit enables the PEX 8111 to perform memory or I/O transactions on the PCI bus. Configuration transactions can be forwarded from the PCI Express bus and performed on the PCI bus independent of this bit. When clear, the bridge must disable response as a target to all memory or I/O transactions on the secondary interface (PCI Express bus) (they cannot be forwarded to the primary interface). In this case, all Memory and I/O requests are terminated with an Unsupported Request completion.	RW	RW	WO	0
3	**Special Cycle Enable.** A bridge does not respond to Special Cycle transactions, so this bit is forced to 0.	RO	RO	—	0
4	**Memory Write and Invalidate.** When set, this bit enables the PEX 8111 PCI bus master logic to use the Memory Write-and-Invalidate command. When clear, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop.** If set, I/O Writes in the first 64 KB of the I/O address space with address bits 9:0 equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA aliases – AD[15:10] are not decoded and may be any value) must be positively decoded on the PCI interface and forwarded to the secondary interface (PCI Express).	RW	RW	WO	0
6	**Parity Error Response Enable.** This bit enables PCI parity checking.	RW	RW	WO	0
7	***Reserved***	RsvdP	RsvdP	—	0
8	**SERR Enable.** When asserted, this bit enables the SERR# pin to be asserted.	RW	RW	WO	0
9	**Fast Back to Back Enable.** The PEX 8111 PCI master interface does not perform fast back-to-back transactions, so this bit is forced to 0.	RO	RO	—	0
10	**Interrupt Disable.** When set, the PEX 8111 is prevented from asserting INTx# signals on behalf of functions integrated into the bridge. This bit has no effect on INTx# signals asserted on behalf of INTx# messages associated with the PCI Express secondary interface.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	—	0

Table 21-13. (Address 06h; PCISTAT) PCI Status (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	—	0
3	**Interrupt Status.** When set, indicates that an INTx# interrupt message is pending on behalf of functions integrated into the bridge. This bit does not reflect the status of INTx# inputs associated with the secondary interface.	RO	RO	—	0
4	**Capabilities List.** This bit indicates if the **New Capabilities Pointer** at address 34h is valid. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit is hardwired to 1.	RO	RO	—	1
5	**66MHz Capable.** This optional read-only bit indicates whether the PEX 8111 is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the PEX 8111 is 66 MHz capable.	RO	RO	—	0
6	***Reserved***	RsvdZ	RsvdZ	—	0
7	**Fast Back-To-Back Transactions Capable.** Does not apply to PCI Express, so this bit is forced to 0.	RO	RO	—	0
8	**Master Data Parity Error.** This bit is used to report the detection of a data parity error by the bridge. This bit is set if the *Parity Error Response Enable* bit in the **PCI Command** register is set and either of the following two conditions occur: • The bridge receives a completion marked poisoned on the primary interface • The bridge poisons a write request or read completion on the primary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
10:9	**Devsel Timing.** Does not apply to PCI Express, so this field is forced to 0.	RO	RO	—	0
11	**Signaled Target Abort.** This bit is set when the bridge completes a request as a target of a transaction on its primary interface using Completer Abort completion status. Writing a 1 clears this bit.	RW1C	RW1C	—	0
12	**Received Target Abort.** This bit is set when the bridge receives a completion with Completer Abort completion status on its primary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
13	**Received Master Abort.** This bit is set when the bridge receives a completion with Unsupported Request completion status on its primary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
14	**Signaled System Error.** This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL Message to the Root Complex, and the *SERR Enable bit* in the **PCI Command** register is set. Writing a 1 clears this bit.	RW1C	RW1C	—	0
15	**Detected Parity Error.** This bit is set by the bridge whenever it receives a poisoned TLP on the primary interface, regardless of the state of the *Parity Error Response Enable* bit in the **PCI Command** register. Writing a 1 clears this bit.	RW1C	RW1C	—	0

Table 21-14. (Address 06h; PCISTAT) PCI Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	—	0
3	**Interrupt Status.** This bit reflects the state of the PEX 8111 internal PCI interrupt status. One of the INTx# signals is asserted when this bit is high, the *Interrupt Disable* bit in the **PCI Command** register is low, and the Power State is D0.	RO	RO	—	0
4	**Capabilities List.** This bit indicates if the **New Capabilities Pointer** at address 34h is valid. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit is hardwired to 1.	RO	RO	—	1
5	**66MHz Capable.** The PEX 8111 does not support 66 MHz, so this bit is forced to 0.	RO	RO	—	0
6	***Reserved***	RsvdZ	RsvdZ	—	0
7	**Fast Back-To-Back Transactions Capable.** The PEX 8111 does not accept fast back-to-back transactions, so this bit is forced to 0.	RO	RO	—	0
8	**Master Data Parity Error.** This bit indicates that a data parity error has occurred when this device was the PCI bus master. The *Parity Error Response Enable* bit in the **PCI Command** register must be set for this bit to be set. Writing a 1 clears this bit.	RW1C	RW1C	—	0
10:9	**Devsel Timing.** This field determines how quickly this device responds to a transaction with DEVSEL#. A value of 1 indicates a medium response.	RO	RO	—	1
11	**Signaled Target Abort.** This bit is set whenever the device is acting as a PCI bus target, and terminates its transaction with a Target-Abort. A Target-Abort occurs when a target detects a fatal error and is unable to complete the transaction. This never occurs in the PEX 8111, so a zero is always returned.	RsvdZ	RsvdZ	—	0
12	**Received Target Abort.** This bit is set whenever the device is acting as a PCI bus master, and has its transaction terminated with a Target-Abort. A Target-Abort occurs when a target detects a fatal error and is unable to complete the transaction. It de-asserts DEVSEL# and asserts STOP# to signal the Target Abort. Writing a 1 clears this bit.	RW1C	RW1C	—	0
13	**Received Master Abort.** This bit is set whenever the device is acting as a PCI bus master, and has its transaction terminated with a Master-Abort. A Master-Abort occurs when no target responds with a DEVSEL. Writing a 1 clears this bit.	RW1C	RW1C	—	0
14	**Signaled System Error.** This bit is set whenever the device asserts the SERR# pin. Writing a 1 clears this bit.	RW1C	RW1C	—	0
15	**Detected Parity Error.** This bit is set whenever the device detects a parity error on incoming addresses or data from the PCI bus, regardless of the state of the *Parity Error Response Enable* bit in the **PCI Command** register. Writing a 1 clears this bit.	RW1C	RW1C	—	0

Table 21-15. (Address 08h; PCIDEVREV) PCI Device Revision ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Device Revision ID.** This field identifies the silicon revision of the device. Bits 3:0 represent the minor revision number and bits 7:4 represent the major revision number.	RO	RO	—	'h10

Table 21-16. (Address 09h; PCICLASS) PCI Class Code

Bits	Description	CFG	MM	EE	Default
7:0	**Interface**	RO	RW	WO	0
15:8	**Sub Class**	RO	RW	WO	4
23:16	**Base Class**	RO	RW	WO	6

Table 21-17. (Address 0Ch; PCICACHESIZE) PCI Cache Line Size

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size.** This register specifies the system cache line size in units of DWORDs. The value in this register is used by PCI master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple or Memory Write Invalidate commands for accessing memory. This device only supports cache line sizes of 8, 16, or 32 DWORDs. Writes of values other than these are ignored.	RW	RW	WO	0

Table 21-18. (Address 0Dh; PCILATENCY) PCI Bus Latency Timer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Bus Latency Timer.** This register is also referred to as primary latency timer for Type 1 Configuration Space Header devices. The primary/master latency timer does not apply to PCI Express (Forward Bridge mode). In Reverse Bridge mode, this field specifies, in units of PCI clocks, the value of the Latency Timer during bus master bursts. When the Latency Timer expires, the device must terminate its tenure on the bus.	RO (F) RW (R)	RO (F) RW (R)	— (F) WO (R)	0

Table 21-19. (Address 0Eh; PCIHEADER) PCI Header Type

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Header Type.** This field specifies the format of the second part of the predefined configuration header starting at address 10h. For PCI Bridges, this bit is forced to 1.	RO	RO	—	1

Table 21-20. (Address 0Fh; PCIBIST) PCI Built-In Self Test

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self Test.** The built-in self-test function is not supported, and always returns a value of 0.	RO	RO	—	0

Table 21-21. (Address 10h; PCIBASE0) PCI Base Address 0

Bits	Description	CFG	MM	EE	Default
0	**Space Type.** When low, this space is accessed as memory. When high, this space is accessed as I/O. ***Note: Hardcoded to 0.***	RO	RO	—	0
2:1	**Address Type.** This field indicates the type of addressing for this space. 00 = Locate anywhere in 32-bit address space (default) 01 = Locate below 1 Meg 10 = Locate anywhere in 64-bit address space 11 = ***Reserved*** ***Note: Hardcoded to 0.***	RO	RO	—	0
3	**Prefetch Enable.** When set, indicates that pre-fetching has no side effects on reads.	RO	RW	WO	1
15:4	**Base Address.** This part of the base address is ignored for a 64 KByte space. ***Note: Hardcoded to 0.***	RO	RO	—	0
31:16	**Base Address.** Specifies the upper 16 bits of the 32-bit starting base address of the 64 KByte addressing space for the PEX 8111 Configuration registers and shared memory.	RW	RW	WO	0

Table 21-22. (Address 14h; PCIBASE1) PCI Base Address 1

Bits	Description	CFG	MM	EE	Default
31:0	**Base Address 1.** This base address register is unused.	Rsvd P	Rsvd P	—	0

Table 21-23. (Address 18h; PRIMBUSNUM) Primary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number.** This field is used to record the bus number of the PCI bus segment to which the primary interface of the bridge is connected.	RW	RW	WO	0

Table 21-24. (Address 19h; SECBUSNUM) Secondary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number.** This field is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected.	RW	RW	WO	0

Table 21-25. (Address 1Ah; SUBBUSNUM) Subordinate Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number.** This field is used to record the bus number of the highest numbered PCI bus segment which is behind (or subordinate to) the bridge.	RW	RW	WO	0

Table 21-26. (Address 1Bh; SECLATTIMER) Secondary Latency Timer

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Latency Timer.** This field specifies, in units of PCI clocks, the value of the Latency Timer during secondary PCI bus master bursts. When the Latency Timer expires, the device must terminate its tenure on the bus. This field is only valid in Forward Bridge mode.	RW	RW	WO	0

Table 21-27. (Address 1Ch; IOBASE) I/O Base

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability.** This field indicates the type of addressing for this space. 00 = 16-bit I/O addressing 01 = 32-bit I/O addressing Others = ***Reserved***	RO	RW	WO	0
7:4	**I/O Base.** This field defines the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. The upper 4 bits of this register correspond to address bits AD[15:12]. For purposes of address decoding, the bridge assumes that the lower 12 address bits, AD[11:0], of the I/O base address are zero. Thus, the bottom of the defined I/O address range is aligned to a 4 KByte boundary, and the top is one less than a 4 KByte boundary.	RW	RW	WO	0

Table 21-28. (Address 1Dh; IOLIMIT) I/O Limit

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability.** This field indicates the type of addressing for this space. 00 = 16-bit I/O addressing 01 = 32-bit I/O addressing Others = ***Reserved*** The value returned in this field is derived from the *I/O Base Address Capability* field of the **IOBASE** register.	RO	RO	—	0
7:4	**I/O Limit.** This field determines the range of the I/O space that is forwarded from the primary interface to the secondary interface. The upper 4 bits of this register correspond to address bits AD[15:12]. For purposes of address decoding, the bridge assumes that the lower 12 address bits, AD[11:0], of the I/O limit address are FFFh. If there are no I/O addresses on the secondary side of the bridge, the *I/O Limit* field can be programmed to a smaller value than the *I/O Base* field. In this case, the bridge does not forward any I/O transactions from the primary bus to the secondary, and does forward all I/O transactions from the secondary bus to the primary bus.	RW	RW	WO	0

Table 21-29. (Address 1Eh; SECSTAT) Secondary Status (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	—	0
5	**Secondary 66MHz Capable.** This bit indicates whether or not the secondary interface of the bridge is capable of operating at 66 MHz. The PEX 8111 only supports 66 MHz, so this bit is hardwired to 0.	RO	RO	—	0
6	***Reserved***	RsvdZ	RsvdZ	—	0
7	**Secondary Fast Back-To-Back Transactions Capable.** This bit indicates whether or not the secondary interface of the bridge is capable of decoding fast back-to-back transactions when the transactions are from the same master but to different targets. (A bridge is required to support fast back-to-back transactions from the same master.) The PEX 8111 does not support fast back-to-back decoding.	RO	RO	—	0
8	**Secondary Master Data Parity Error.** This bit is used to report the detection of a data parity error by the bridge when it is the master of the transaction on the secondary interface. This bit is set if the following three conditions are true: • The bridge is the bus master of the transaction on the secondary interface. • The bridge asserted PERR# (read transaction) or detected PERR# asserted (write transaction). • The *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set. Writing a 1 clears this bit.	RW1C	RW1C	—	0
10:9	**Secondary Devsel Timing.** This field encodes the timing of the secondary interface DEVSEL#. The encoding must indicate the slowest response time that the bridge uses to assert DEVSEL# on its secondary interface when it is responding as a target to any transaction except a Configuration Read or Configuration Write. This field is hardwired to a value of 1, indicating medium DEVSEL# timing.	RO	RO	—	1
11	**Secondary Signaled Target Abort.** This bit reports the signaling of a Target-Abort termination by the bridge when it responds as the target of a transaction on its secondary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
12	**Secondary Received Target Abort.** This bit reports the detection of a Target-Abort termination by the bridge when it is the master of a transaction on its secondary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
13	**Secondary Received Master Abort.** This bit reports the detection of a Master-Abort termination by the bridge when it is the master of a transaction on its secondary interface. This bit is also set for a PCI Express to PCI configuration transaction with an extended address not equal to 0. Writing a 1 clears this bit.	RW1C	RW1C	—	0
14	**Secondary Received System Error.** This bit reports the detection of an SERR# assertion on the secondary interface of the bridge. Writing a 1 clears this bit.	RW1C	RW1C	—	0
15	**Secondary Detected Parity Error.** This bit reports the detection of an address or data parity error by the bridge on its secondary interface. This bit is set when any of the following three conditions are true: • Bridge detects an address parity error as a potential target • Bridge detects a data parity error when the target of a write transaction • Bridge detects a data parity error when the master of a read transaction This bit is set irrespective of the state of the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register. Writing a 1 clears this bit.	RW1C	RW1C	—	0

Table 21-30. (Address 1Eh; SECSTAT) Secondary Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	—	0
5	**Secondary 66MHz Capable.** This bit indicates whether or not the secondary interface of the bridge is capable of operating at 66 MHz. This bit is not valid for the PCI Express and is forced to 0.	RO	RO	—	0
6	***Reserved***	RsvdZ	RsvdZ	—	0
7	**Secondary Fast Back-To-Back Transactions Capable.** This bit indicates whether or not the secondary interface of the bridge is capable of decoding fast back-to-back transactions when the transactions are from the same master but to different targets. This bit is not valid for the PCI Express and is forced to 0.	RO	RO	—	0
8	**Secondary Master Data Parity Error.** This bit is used to report the detection of a data parity error by the bridge. This bit is set if the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register is set and either of the following two conditions occur: • The bridge receives a completion marked poisoned on the secondary interface • The bridge poisons a write request or read completion on the secondary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
10:9	**Secondary Devsel Timing.** This field encodes the timing of the secondary interface DEVSEL#. This field is not valid for the PCI Express and is forced to 0.	RO	RO	—	0
11	**Secondary Signaled Target Abort.** This bit is set when the bridge completes a request as a target of a transaction on its secondary interface using Completer Abort completion status. Writing a 1 clears this bit.	RW1C	RW1C	—	0
12	**Secondary Received Target Abort.** This bit is set when the bridge receives a completion with Completer Abort completion status on its secondary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
13	**Secondary Received Master Abort.** This bit is set when the bridge receives a completion with Unsupported Request completion status on its secondary interface. Writing a 1 clears this bit.	RW1C	RW1C	—	0
14	**Secondary Received System Error.** This bit is set when the PEX 8111 receives an ERR_FATAL or ERR_NONFATAL message from the downstream PCI Express device. Writing a 1 clears this bit.	RW1C	RW1C	—	0
15	**Secondary Detected Parity Error.** This bit is set by the bridge whenever it receives a poisoned TLP on the secondary interface, regardless of the state of the *Secondary Parity Error Response Enable* bit in the **Bridge Control** register. Writing a 1 clears this bit.	RW1C	RW1C	—	0

Table 21-31. (Address 20h; MEMBASE) Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved***	RsvdP	RsvdP	—	0
15:4	**Memory Base.** This field defines the starting address at which Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to address bits AD[31:20]. For purposes of address decoding, the bridge assumes that the lower 20 address bits, AD[19:0], of the memory base address are zero. The bottom of the defined memory address range is aligned to a 1 Mbyte boundary, and the top is one less than a 1 MByte boundary.	RW	RW	WO	—

Table 21-32. (Address 22h; MEMLIMIT) Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved***	RsvdP	RsvdP	—	0
15:4	**Memory Limit.** This field determines the range of the Memory space that is forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to address bits AD[31:20]. For purposes of address decoding, the bridge assumes that the lower 20 address bits, AD[19:0], of the memory limit address are FFFFFh. If there are no memory-mapped I/O addresses on the secondary side of the bridge, the *Memory Limit* field must be programmed to a smaller value than the *Memory Base* field. If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus.	RW	RW	WO	—

Table 21-33. (Address 24h; PREBASE) Prefetchable Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability.** This field indicates the type of addressing for this space. 00 = 32-bit I/O addressing 01 = 64-bit I/O addressing Others = ***Reserved***	RO	RW	WO	0
15:4	**Prefetchable Memory Base.** This field defines the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to address bits AD[31:20]. For purposes of address decoding, the bridge assumes that the lower 20 address bits, AD[19:0], of the prefetchable memory base address are zero. The bottom of the defined prefetchable memory address range is aligned to a 1 Mbyte boundary, and the top is one less than a 1 Mbyte boundary.	RW	RW	WO	—

Table 21-34. (Address 26h; PRELIMIT) Prefetchable Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability.** This field indicates the type of addressing for this space. 00 = 32-bit addressing 01 = 64-bit addressing Others = ***Reserved*** The value returned in this field is derived from the *Prefetchable Base Address Capability* field of the **PREBASE** register.	RO	RO	—	0
15:4	**Prefetchable Memory Limit.** This field determines the range of the Prefetchable Memory space that is forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to address bits AD[31:20]. For purposes of address decoding, the bridge assumes that the lower 20 address bits, AD[19:0], of the prefetchable memory limit address are FFFFFh. If there is no prefetchable memory on the secondary side of the bridge, the *Prefetchable Memory Limit* field must be programmed to a smaller value than the *Prefetchable Memory Base* field. If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus.	RW	RW	WO	—

Table 21-35. Address 28h; PREBASEUPPER) Prefetchable Memory Base Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits.** If the *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is read-only and returns a 0. If the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register provides the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	0

Table 21-36. (Address 2Ch; PRELIMITUPPER) Prefetchable Memory Limit Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits.** If the *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is read-only and returns a 0. If the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the range of the Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	0

Table 21-37. (Address 30h; IOBASEUPPER) I/O Base Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits.** If the *I/O Base Address Capability* field indicates 16-bit addressing, this register is read-only and returns a 0. If the *I/O Base Address Capability* field indicates 32-bit addressing, this register provides the upper 16 bits of the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	—

Table 21-38. (Address 32h; IOLIMITUPPER) I/O Limit Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits.** If the *I/O Base Address Capability* field indicates 16-bit addressing, this register is read-only and returns a 0. If the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the range of the I/O transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	—

Table 21-39. (Address 34h; PCICAPPTR) PCI Capabilities Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Capabilities Pointer.** This field provides the configuration address of the first New Capabilities register.	RO	RW	WO	'h40
31:8	***Reserved***	RsvdP	RsvdP	—	0

Table 21-40. (Address 3Ch; PCIINTLINE) PCI Interrupt Line

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Line.** This field indicates which input of the system interrupt controller the interrupt pin of the device is connected to. Device drivers and operating systems use this field.	RW	RW	WO	0

Table 21-41. (Address 3Dh; PCIINTPIN) PCI Interrupt Pin

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Pin.** For Forward Bridge mode, this register identifies the legacy interrupt message(s) the device uses. Valid values are 1, 2, 3, and 4 that map to legacy interrupt messages for INTA#, INTB#, INTC#, and INTD#. A value of 0 indicates that the device uses no legacy interrupt message(s). For Reverse Bridge mode, this register selects which interrupt pin the device uses.	RO	RW	WO	1

Table 21-42. (Address 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable.** This bit controls the response of the bridge to address and data parity errors on the secondary interface (PCI). If this bit is set, the bridge must take its normal action when a parity error is detected. If this bit is cleared, the bridge must ignore any parity errors that it detects and continue normal operation. A bridge must generate parity even if the parity error reporting is disabled. Also, the bridge must always forward posted write data with poisoning, from PCI to PCI Express on a PCI data parity error, regardless of the setting of this bit.	RW	RW	WO	0
1	**Secondary SERR Enable.** This bit controls the forwarding of secondary interface (PCI) SERR# assertions to the primary interface (PCI Express). The bridge transmits an ERR_FATAL message on the primary interface when all of the following are true: • SERR# is asserted on the secondary interface. • This bit is set. • The *SERR Enable* bit is set in the **PCI Command** register or the *Fatal or Non-Fatal Error Reporting Enable* bits are set in the **PCI Express Device Control** register.	RW	RW	WO	0
2	**ISA Enable.** This bit modifies the response by the bridge to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and are in the first 64 KBytes of the PCI I/O address space. If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KByte block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1 KByte block.	RW	RW	WO	0
3	**VGA Enable.** This bit modifies the response by the bridge to VGA-compatible addresses. If this bit is set, the bridge positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A0000h to 000B FFFFh. • I/O address in the first 64 KB of the I/O address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] may possess any value and is not used in the decoding) If the *VGA Enable* bit is set, forwarding of VGA addresses is independent of the value of the *ISA Enable* bit (located in the **Bridge Control** register), the I/O address range and memory address ranges defined by the **I/O Base and Limit** registers, the **Memory Base and Limit** registers, and the **Prefetchable Memory Base and Limit** registers of the bridge. The forwarding of VGA addresses is qualified by the *I/O Enable* and *Memory Enable* bits in the **PCI Command** register. 0 – Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 – Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the *I/O Enable* and *Memory Enable* bits are set) independent of the I/O and memory address ranges and independent of the *ISA Enable* bit.	RW	RW	WO	0

Table 21-42. (Address 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-bit Decode.** This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1KB. This bit only has meaning if bit 3 (*VGA Enable)* of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. This bit enables system configuration software to select between 10 and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary whenever the *VGA Enable* bit is set to 1. 0 – execute 10-bit address decodes on VGA I/O accesses. 1 – execute 16-bit address decodes on VGA I/O accesses.	RW	RW	WO	0
5	**Master Abort Mode.** This bit controls the behavior of a bridge when it receives a Master-Abort termination on the PCI bus or an Unsupported Request on PCI Express. 0 – Do not report Master-Aborts. If PCI Express UR is received: • Return FFFFFFFFh to PCI bus for reads • Complete non-posted write normally on PCI bus (assert TRDY#) and • Discard the write data • Discard posted PCI to PCI Express write data If PCI transaction terminates with Master Abort: • Complete non-posted transaction with Unsupported Request • Discard posted write data from PCI Express to PCI 1 – Report Master-Aborts If PCI Express UR is received: • Complete reads and non-posted writes with PCI Target Abort • Discard posted PCI to PCI Express write data If PCI transaction terminates with Master Abort: • Complete non-posted transaction with Unsupported Request • Discard posted write data from PCI Express to PCI • Send ERR_NONFATAL Message for posted writes.	RW	RW	WO	0
6	**Secondary Bus Reset.** When set, forces the assertion of RST# on the secondary bus. The bridge secondary bus interface and any buffers between the two interfaces (primary and secondary) must be initialized back to their default state whenever this bit is set. The primary bus interface and all configuration space registers must not be affected by the setting of this bit. Because RST# is asserted for as long as this bit is set, software must observe proper PCI reset timing requirements.	RW	RW	WO	0
7	**Fast Back to Back Enable.** This bit controls the ability of the bridge to generate fast back-to-back transactions to different devices on the secondary interface. The PEX 8111 does not support this feature.	RO	RO	—	0

Table 21-42. (Address 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer.** In Forward Bridge mode, this bit does not apply and is forced to 0.	RO	RO	—	0
9	**Secondary Discard Timer.** Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a Delayed Transaction request. The counter starts once the completion (PCI Express Completion associated with the Delayed Transaction Request) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the secondary bus). If the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets the *Discard Timer Status* bit. 0 – The Secondary Discard Timer counts 2^{15} PCI clock periods. 1 – The Secondary Discard Timer counts 2^{10} PCI clock periods.	RW	RW	WO	0
10	**Discard Timer Status.** This bit is set to a 1 when the Secondary Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge. Writing a 1 clears this bit.	RW1C	RW1C	WO	0
11	**Discard Timer SERR Enable.** When set to 1, this bit enables the bridge to generate an ERR_NONFATAL Message on the primary interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. 0 – Do not generate ERR_NONFATAL Message on the primary interface as a result of the expiration of the Secondary Discard Timer. 1 – Generate ERR_NONFATAL Message on the primary interface if the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge.	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	—	0

Table 21-43. (Address 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable.** This bit controls the response of the bridge to data parity errors forwarded from the primary interface (e.g., a poisoned TLP). If clear, the bridge must ignore any data parity errors that it detects and continue normal operation. If set, the bridge must take its normal action when a data parity error is detected.	RW	RW	WO	0
1	**Secondary SERR Enable.** This bit has no affect in Reverse Bridge mode. Secondary bus error reporting using SERR# is controlled by the **ROOTCTL** register.	RW	RW	WO	0
2	**ISA Enable.** This bit modifies the response by the bridge to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and are in the first 64 KBytes of the PCI I/O address space. If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KByte block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1 KByte block.	RW	RW	WO	0
3	**VGA Enable.** This bit modifies the response by the bridge to VGA-compatible addresses. If this bit is set, the bridge positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A0000h to 000B FFFFh. • I/O address in the first 64 KB of the I/O address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] may possess any value and is not used in the decoding) If the *VGA Enable* bit is set, forwarding of VGA addresses is independent of the value of the *ISA Enable* bit (located in the **Bridge Control** register), the I/O address range and memory address ranges defined by the **I/O Base and Limit** registers, the **Memory Base and Limit** registers, and the **Prefetchable Memory Base and Limit** registers of the bridge. The forwarding of VGA addresses is qualified by the *I/O Enable* and *Memory Enable* bits in the **PCI Command** register. 0 – Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 – Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the *I/O Enable* and *Memory Enable* bits are set) independent of the I/O and memory address ranges and independent of the *ISA Enable* bit.	RW	RW	WO	0

Table 21-43. (Address 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-bit Decode.** This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1KB. This bit only has meaning if bit 3 (*VGA Enable)* of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. This bit enables system configuration software to select between 10 and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary whenever the *VGA Enable* bit is set to 1. 0 – execute 10-bit address decodes on VGA I/O accesses. 1 – execute 16-bit address decodes on VGA I/O accesses.	RW	RW	WO	0
5	**Master Abort Mode.** This bit controls the behavior of a bridge when it receives a Master-Abort termination on the PCI bus or an Unsupported Request on PCI Express. 0 – Do not report Master-Aborts. If PCI Express UR is received: • Return FFFFFFFFh to PCI bus for reads • Complete non-posted write normally on PCI bus (assert TRDY#) and discard the write data • Discard posted PCI to PCI Express write data If PCI transaction terminates with Master Abort: • Complete non-posted transaction with Unsupported Request • Discard posted write data from PCI Express to PCI 1 – Report Master-Aborts If PCI Express UR is received: • Complete reads and non-posted writes with PCI Target Abort • Discard posted PCI to PCI Express write data If PCI transaction terminates with Master Abort: • Complete non-posted transaction with Unsupported Request • Discard posted write data from PCI Express to PCI • Send ERR_NONFATAL Message for posted writes.	RW	RW	WO	0
6	**Secondary Bus Reset.** When set, causes a Hot Reset to be communicated on the secondary bus. The bridge's secondary bus interface and any buffers between the two interfaces (primary and secondary) must be initialized back to their default state whenever this bit is set. The primary bus interface and all configuration space registers are not affected by the setting of this bit.	RW	RW	WO	0
7	**Fast Back to Back Enable.** This bit controls the ability of the bridge to generate fast back-to-back transactions to different devices on the secondary interface. The PEX 8111 does not support this feature.	RO	RO	—	0

Table 21-43. (Address 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer.** Selects the number of PCI clocks that the bridge waits for a master on the primary interface to repeat a Delayed Transaction request. The counter starts once the completion (PCI Express Completion associated with the Delayed Transaction Request) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the secondary bus). If the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets the *Discard Timer Status* bit. 0 – The Secondary Discard Timer counts 2^{15} PCI clock periods. 1 – The Secondary Discard Timer counts 2^{10} PCI clock periods.	RW	RW	WO	0
9	**Secondary Discard Timer.** In Reverse Bridge mode, this bit does not apply and is forced to 0.	RO	RO	—	0
10	**Discard Timer Status.** This bit is set to a 1 when the Primary Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge.	RW1C	RW1C	—	0
11	**Discard Timer SERR Enable.** When set to 1, this bit enables the bridge to assert SERR# on the primary interface when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. 0 – Do not assert SERR# on the primary interface as a result of the expiration of the Primary Discard Timer. 1 – Generate SERR# on the primary interface if the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge.	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	—	0

21.7 PCI-Compatible Extended Capability Registers

Table 21-44. (Address 40h; PWRMNGID) Power Management Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID.** This register specifies the Power Management Capability ID.	RO	RO	—	1

Table 21-45. (Address 41h; PWRMNGNEXT) Power Management Next Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Pointer.** This register points to the first location of the next item in the capabilities linked list.	RO	RW	WO	50h

Table 21-46. (Address 42h; PWRMNGCAP) Power Management Capabilities (Forward)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version.** This field specifies the revision of the *PCI Power Management Interface Specification* to which this device complies	RO	RW	WO	2
3	**PME Clock.** For Forward Bridge mode, does not apply to PCI Express, so this bit should always have a value of 0.	RO	RO	—	0
4	***Reserved***	RsvdP	RsvdP	—	0
5	**Device Specific Initialization.** This bit indicates that the device requires special initialization following a transition to the $D0_{uninitialized}$ state before the generic class device driver can use it.	RO	RW	WO	0
8:6	**AUX Current.** This field reports the 3.3Vaux auxiliary current requirements for the PCI function. If PME# generation from $D3_{cold}$ is not supported by the function, this field must return a value of 0.	RO	RW	WO	0
9	**D1 Support.** This bit specifies that the device supports the D1 state.	RO	RW	WO	1
10	**D2 Support.** This bit specifies that the device supports the D2 state.	RO	RW	WO	0
15:11	**PME Support.** This field indicates the power states in which the device may send a PME message Value Description XXXX1 Can be asserted from D0 XXX1X Can be asserted from D1 XX1XX Can be asserted from D2 X1XXX Can be asserted from $D3_{hot}$ 1XXXX Can be asserted from $D3_{cold}$	RO	RW	WO	0Bh

Table 21-47. (Address 42h; PWRMNGCAP) Power Management Capabilities (Reverse)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version.** This field specifies the revision of the *PCI Power Management Interface Specification* to which this device complies	RO	RW	WO	2
3	**PME Clock.** When low, this bit indicates that no PCI clock is required to generate PME#. When high, this bit indicates that a PCI clock is required to generate PME#.	RO	RW	WO	0
4	***Reserved***	RsvdP	RsvdP	—	0
5	**Device Specific Initialization.** This bit indicates that the device requires special initialization following a transition to the $D0_{uninitialized}$ state before the generic class device driver can use it.	RO	RW	WO	0
8:6	**AUX Current.** This field reports the 3.3Vaux auxiliary current requirements for the PCI function. If PME# generation from $D3_{cold}$ is not supported by the function, this field must return a value of 0.	RO	RW	WO	0
9	**D1 Support.** This bit specifies that the device supports the D1 state.	RO	RW	WO	1
10	**D2 Support.** This bit specifies that the device supports the D2 state.	RO	RW	WO	0
15:11	**PME Support.** This field indicates the power states in which the device may assert the PME# pin. Value Description XXXX1 Can be asserted from D0 XXX1X Can be asserted from D1 XX1XX Can be asserted from D2 X1XXX Can be asserted from $D3_{hot}$ 1XXXX Can be asserted from $D3_{cold}$	RO	RW	WO	0Bh

Table 21-48. (Address 44h; PWRMNGCSR) Power Management Control/Status (Forward)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State.** This field is used to determine or change the current power state. Value State 00 **D0** 01 **D1** 10 **D2** 11 **$D3_{hot}$** A transition from state **D3** to state **D0** causes a soft reset to occur. In states **D1** and **D2**, if the corresponding *D1 Support* and *D2Support* bits are set, PCI memory and I/O accesses are disabled, as well as the PCI interrupt, and only configuration cycles are allowed. In state **$D3_{hot}$**, these functions are also disabled.	RW	RW	WO	0
7:2	***Reserved***	RsvdP	RsvdP	—	0
8	**PME Enable.** This bit enables a PME Message to be transmitted upstream.	RW	RW	WO	0
12:9	**Data Select.** This field is not supported, and always returns a value of 0	RO	RO	—	0
14:13	**Data Scale.** This field is not supported, and always returns a value of 0.	RO	RO	—	0
15	**PME Status.** This bit indicates that a PME Message has been transmitted upstream. Writing a 1 clears the bit.	RW1C	RW1C	—	0

Table 21-49. (Address 44h; PWRMNGCSR) Power Management Control/Status (Reverse)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State.** This field is used to determine or change the current power state. Value State 00 **D0** 01 **D1** 10 **D2** 11 **$D3_{hot}$** A transition from state **D3** to state **D0** causes a soft reset to occur. In states **D1** and **D2**, if the corresponding *D1 Support* and *D2 Support* bits are set, PCI memory and I/O accesses are disabled, as well as the PCI interrupt, and only configuration cycles are allowed. In state **$D3_{hot}$**, these functions are also disabled.	RW	RW	WO	0
7:2	***Reserved***	RsvdP	RsvdP	—	0
8	**PME Enable.** This bit enables the PME# pin to be asserted.	RW	RW	WO	0
12:9	**Data Select.** This field is not supported, and always returns a value of 0	RO	RO	—	0
14:13	**Data Scale.** This field is not supported, and always returns a value of 0.	RO	RO	—	0
15	**PME Status.** This bit indicates that the PME# pin is being driven if *PME Enable* bit is set high. Writing a 1 from the PCI bus clears the bit.	RW1C	RW1C	—	0

Table 21-50. (Address 46h; PWRMNGBRIDGE) Power Management Bridge Support (Forward)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	—	0
6	**B2/B3 Support.** Does not apply to PCI Express, so this bit is forced to 0.	RO	RO	—	0
7	**Bus Power/Clock Control Enable.** Does not apply to PCI Express, so this bit is forced to 0.	RO	RO	—	0

Table 21-51. Address 46h; PWRMNGBRIDGE) Power Management Bridge Support (Reverse)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	—	0
6	**B2/B3 Support.** When set, indicates that, when the bridge function is programmed to **$D3_{hot}$**, its secondary bus PCI clock is stopped (B2). When clear, indicates that, when the bridge function is programmed to **$D3_{hot}$**, its secondary bus has its power removed (B3). This bit is only meaningful if bit 7 is set.	RO	RW	WO	0
7	**Bus Power/Clock Control Enable.** When set, indicates that the bus power/clock control mechanism as defined in section 4.7.1 of the PCI Bridge spec is enabled.	RO	RW	WO	0

Table 21-52. (Address 47h; PWRMNGDATA) Power Management Data

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Data.** This function is not supported, and always returns a value of 0.	RO	RO	—	0

Table 21-53. (Address 48h; DEVSPECCTL) Device Specific Control

Bits	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable.** When this bit is clear, a Memory Read command on the PCI bus that targets the PCI Express prefetchable memory space causes only 1 word to be read from PCI Express bus. When this bit is set, a Memory Read command on the PCI bus that targets the PCI Express prefetchable memory space causes a cache line to be read from PCI Express bus.	RW	RW	WO	0
1	**PCI Base Address 0 Enable.** When set, this bit enables the PCI Base Address 0 space for memory-mapped access to the configuration registers and shared memory.	RW	RW	WO	1
2	***Reserved***	RsvdP	RsvdP	—	0
3	**PMU Power Off.** When set, the link has transitioned to the L2/L3 Ready state, and is ready to be powered-down.	RO	RO	—	0
7:4	**PMU Link State.** This field indicates the state of the link. Value State 0001 **L0** 0010 **L0s** 0100 **L1** 1000 **L2**	RO	RO	—	—
9:8	**CRS Retry Control.** This field determines the response of the PEX 8111 in Reverse Bridge Mode when a PCI to PCI Express configuration transaction is terminated with a Configuration Request Retry Status. **Value** **Response** 00 Retry once after 1 second. If another CRS is received, Target Abort on the PCI bus. 01 Retry 8 times, once per second. If another CRS is received, Target Abort on the PCI bus. 10 Retry once per second until successful completion. 11 ***Reserved***	RW	RW	WO	0
10	**WAKE Out Enable.** When set, the WAKEOUT# pin is asserted when the PME# pin is asserted and the link is in the L2 state. This bit is only valid in Forward Bridge mode.	RW	RW	WO	0
11	**Beacon Generate Enable.** When set, a beacon is generated when the PME# pin is asserted and the link is in the L2 state. This bit is only valid in Forward Bridge mode.	RW	RW	WO	0
12	**Beacon Detect Enable.** When set, a beacon detected while the link is in the L2 state causes the PME Status bit to be set. This bit is only valid in Reverse Bridge mode.	RW	RW	WO	0
15:13	***Reserved***	RsvdP	RsvdP	—	0
20:16	**Link State Machine.** For internal use only.	RO	RO	—	—
31:21	***Reserved***	RsvdP	RsvdP	—	0

Table 21-54. (Address 50h; MSIID) Message Signaled Interrupts Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID.** This register specifies the Message Signaled Interrupts Capability ID.	RO	RO	—	5

Table 21-55. (Address 51h; MSINEXT) Message Signaled Interrupts Next Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Next Pointer.** This register points to the first location of the next item in the capabilities linked list.	RO	RW	WO	60h

Table 21-56. (Address 52h; MSICTL) Message Signaled Interrupts Control

Bits	Description	CFG	MM	EE	Default
0	**MSI Enable.** When set, this bit enables the PEX 8111 to use MSI to request service. When set, virtual interrupt support for internal interrupt sources are disabled for Forward Bridge mode. When set, INTx# outputs are disabled in Reverse Bridge mode.	RW	RW	WO	0
3:1	**Multiple Message Capable.** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (if a function requires three messages, it requests four. The encoding is defined as: Value — Number of Messages Requested 000 — 1 001 — 2 010 — 4 011 — 8 100 — 16 101 — 32 110 — ***Reserved*** 111 — ***Reserved***	RO	RO	—	0
6:4	**Multiple Message Enable.** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. The encoding is defined as: Value — Number of Messages Requested 000 — 1 001 — 2 010 — 4 011 — 8 100 — 16 101 — 32 110 — ***Reserved*** 111 — ***Reserved***	RW	RW	WO	0
7	**MSI 64-Bit Address Capable.** When set, the PEX 8111 is capable of generating a 64-bit message address.	RO	RW	WO	1 (Fwd) 0 (Rev)
8	**Per Vector Masking Capable.** This feature is not supported by the PEX 8111, so this bit is forced to 0.	RO	RO	—	0
15:9	***Reserved***	RsvdP	RsvdP	—	0

Table 21-57. (Address 54h; MSIADDR) Message Signaled Interrupts Address

Bits	Description	CFG	MM	EE	Default
1:0	***Reserved***	RsvdP	RsvdP	—	0
31:2	**MSI Address.** If the *Message Enable* bit (bit 0 of the **Message Control** register) is set, the contents of this register specify the DWORD aligned address for the MSI memory write transaction. Address bits 1 and 0 are driven to zero during the address phase.	RW	RW	WO	0

Table 21-58. (Address 58h; MSIUPPERADDR) Message Signaled Interrupts Upper Address

Bits	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address.** This register is optional and is implemented only if the device supports a 64-bit message address (*64-bit Address Capable* bit in **Message Control** register set). If the *Message Enable* bit (bit 0 of the **Message Control** register) is set, the contents of this register specify the upper 32 bits of a 64-bit message address. If the contents of this register are zero, the PEX 8111 uses the 32-bit address specified by the **Message Address** register.	RW	RW	WO	0

Table 21-59. (Address 5Ch; MSIDATA) Message Signaled Interrupts Data

Bits	Description	CFG	MM	EE	Default
15:0	**MSI Data.** If the *Message Enable* bit is set, the message data is driven onto the lower word (AD[15:0]) of the memory write transaction data phase.	RW	RW	WO	0
31:16	***Reserved***	RsvdP	RsvdP	—	0

Table 21-60. (Address 60h; PCIEXID) PCI Express Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID.** This register specifies the PCI Express Capability ID.	RO	RW	—	10h

Table 21-61. (Address 61h; PCIEXNEXT) PCI Express Next Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Pointer.** This register points to the first location of the next item in the capabilities linked list.	RO	RW	WO	0

Table 21-62. (Address 62h; PCIEXCAP) PCI Express Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Capability Version.** This field indicates the PCI Express capability structure version number.	RO	RW	WO	1
7:4	**Device/Port Type.** This field indicates the type of PCI Express logical device. Device encodings are: Value Device/Port Type 0000 PCI Express Endpoint device 0001 Legacy PCI Express Endpoint Device 0100 Root Port of PCI Express Root Complex 0101 Upstream Port of PCI Express Switch 0110 Downstream Port of PCI Express Switch 0111 PCI Express-to-PCI/PCI-X Bridge 1000 PCI/PCI-X to PCI Express Bridge Others ***Reserved***	RO	RW	WO	7 (Forward Bridge) 8 (Reverse Bridge)
8	**Slot Implemented.** When set, this bit indicates that the PCI Express Link associated with this port is connected to a slot.	RO	RW	WO	0
13:9	**Interrupt Message Number.** If this function is allocated more than one MSI interrupt number, this field is required to contain the offset between the base **Message Data** and the MSI Message that is generated when any of the status bits in either the **Slot Status** register or the **Root Port Status** register of this capability structure are set. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the device changes.	RO	RO	—	0
15:14	***Reserved***	RsvdP	RsvdP	—	0

Table 21-63. (Address 64h; DEVCAP) Device Capabilities

Bits	Description	CFG	MM	EE	Default
2:0	**MAX Payload Size Supported.** This field indicates the maximum payload size that the device can support for TLPs. Defined encodings are: Value Max Payload Size 000 128 bytes 001 256 bytes 010 512 bytes 011 1024 bytes 100 2048 bytes 101 4096 bytes 110 ***Reserved*** 111 ***Reserved*** Since the PEX 8111 only supports a maximum payload size of 128 bytes, this field is hardwired to 0.	RO	RO	—	0
4:3	**Phantom Functions Supported.** This feature is not supported in the PEX 8111. This field is hardwired to 0.	RO	RO	—	0
5	**Extended Tag Field Supported.** This field indicates the maximum supported size of the Tag field. If clear, a 5-bit Tag field is supported. If set, an 8-bit Tag field is supported. ***Note:*** *8-bit Tag field support must be enabled by the corresponding control field in the* ***Device Control*** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency.** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the internal buffering of the Endpoint. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L0s entry can be used with no loss of performance. Defined encodings are: Value Latency 000 Less than 64 ns 001 64 ns to less than 128 ns 010 128 ns to less than 256 ns 011 256 ns to less than 512 ns 100 512 ns to 1 µs 101 1 µs to less than 2 µs 110 2 µs to 4 µs 111 More than 4 µs	RO	RW	WO	0
11:9	**Endpoint L1 Acceptable Latency.** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the internal buffering of the Endpoint. Power management software uses the report L1 Acceptable Latency number to compare against the L1 exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L1 entry can be used with no loss of performance. Defined encodings are: Value Latency 000 Less than 1 µs 001 1 µs to less than 2 µs 010 2 µs to less than 4 µs 011 4 µs to less than 8 µs 100 8 µs to less than 16 µs 101 16 µs to less than 32 µs 110 32 µs to 64 µs 111 More than 64 µs	RO	RW	WO	0

Table 21-63. (Address 64h; DEVCAP) Device Capabilities *(Cont.)*

Bits	Description	CFG	MM	EE	Default
12	**Attention Button Present.** The PEX 8111 does not support an attention button, so this bit is forced to 0.	RO	RO	—	0
13	**Attention Indicator Present.** The PEX 8111 does not support an attention indicator, so this bit is forced to 0.	RO	RO	—	0
14	**Power Indicator Present.** The PEX 8111 does not support a power indicator, so this bit is forced to 0.	RO	RO	—	0
17:15	***Reserved***	RsvdP	RsvdP	—	0
25:18	**Captured Slot Power Limit Value.** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. This value is set by the Set_Slot_Power_Limit message.	RO	RW	WO	0
27:26	**Captured Slot Power Limit Scale.** Specifies the scale used for the *Slot Power Limit Value*. Range of values: Value Scale 00 1.0x 01 0.1x 10 0.01x 11 0.001x This value is set by the Set_Slot_Power_Limit message.	RO	RW	WO	0
31:28	***Reserved***	RsvdP	RsvdP	—	0

Table 21-64. (Address 68h; DEVCTL) PCI Express Device Control

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable.** This bit controls reporting of correctable errors. If an ERR_COR is detected in Forward Bridge mode and this bit is set, an ERR_COR message is sent to the Root Complex.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable.** This bit controls reporting of non-fatal errors. If a non-fatal error is detected in Forward Bridge mode and this bit is set, an ERR_NONFATAL Message is sent to the Root Complex.	RW	RW	WO	0
2	**Fatal Error Reporting Enable.** This bit controls reporting of fatal errors. If a fatal error is detected in Forward Bridge mode and this bit is set, an ERR_FATAL Message is sent to the Root Complex.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable.** This bit controls reporting of Unsupported Requests. If an Unsupported Request response is received from the PCI Express in Forward Bridge mode and this bit is set, a non-ERR_FATAL Message is sent to the Root Complex.	RW	RW	WO	0
4	**Enable Relaxed Ordering.** If set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. The PEX 8111 does not support relaxed ordering, so this bit is forced to 0.	RO	RO	—	0
7:5	**MAX Payload Size.** This field sets the maximum TLP payload size for the device. As a receiver, the device must handle TLPs as large as the set value; as transmitter, the device must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the *MAX Payload Size Supported* field of the **Device Capabilities** register. Defined encodings are: Value Max Payload Size 000 128 bytes 001 256 bytes 010 512 bytes 011 1024 bytes 100 2048 bytes 101 4096 bytes 110,111 ***Reserved***	RW	RW	WO	0

Table 21-64. (Address 68h; DEVCTL) PCI Express Device Control *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable.** When clear, the device is restricted to a 5-bit Tag field. When set, this bit enables a device to use an 8-bit Tag field as a requester.	RW	RW	WO	0
9	**Phantom Function Enable.** This feature is not supported in the PEX 8111. This field is hardwired to 0.	RO	RO	—	0
10	**Auxiliary (AUX) Power PM Enable.** When set, this bit enables a device to draw AUX power independent of PME AUX power. Devices that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in the *AUX Current* field of the **Power Management Capabilities** register, independent of the *PME Enable* bit in the **Power Management Control/Status** register. The PEX 8111 does not support AUX power, so this bit is hardwired to 0.	RO	RO	—	0
11	**Enable No Snoop.** When set, the device is permitted to set the *No Snoop* bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Setting this bit to 1 should not cause a device to blindly set the *No Snoop* attribute on all transactions that it initiates. Even when this bit is set to 1, a device may only set the *No Snoop* attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The PEX 8111 never sets the No Snoop attribute, so this bit is forced to 0.	RO	RO	—	0
14:12	**MAX Read Request Size.** This field sets the maximum Read Request size for the Device as a Requester. The Device must not generate read requests with size exceeding the set value. Defined encodings are: Value — Max Payload Size 000 — 128 bytes 001 — 256 bytes 010 — 512 bytes 011 — 1024 bytes 100 — 2048 bytes 101 — 4096 bytes 110,111 — ***Reserved***	RW	RW	WO	‘b010
15	**Bridge Configuration Retry Enable.** When clear, the PEX 8111 does not generate completions with Completion Retry Status on behalf of PCI Express to PCI configuration transactions. When set, the PEX 8111 generates completions with Completion Retry Status on behalf of PCI Express to PCI configuration transactions. This occurs after a delay determined by the **CRSTIMER** register.	RW	RW	WO	0

Table 21-65. (Address 6Ah; DEVSTAT) PCI Express Device Status

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Detected.** This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the **Device Control** register.	RW1C	RW1C	—	0
1	**Non-Fatal Error Detected.** This bit indicates status of non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the **Device Control** register.	RW1C	RW1C	—	0
2	**Fatal Error Detected.** This bit indicates status of fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the **Device Control** register.	RW1C	RW1C	—	0
3	**Unsupported Request Detected.** This bit indicates that the device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the **Device Control** register.	RW1C	RW1C	—	0
4	**AUX Power Detected.** Devices that require AUX power report this bit as set if AUX power is detected by the device.	RO	RO	—	0
5	**Transactions Pending.** Since the PEX 8111 does not generate any non-posted transactions internally, this bit is forced to 0.	RO	RO	—	0
15:6	***Reserved***	RsvdZ	RsvdZ	—	0

Table 21-66. (Address 6Ch; LINKCAP) Link Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed.** This field indicates the maximum Link speed of the given PCI Express Link. Defined encodings are: Value Max Link Speed 0001 2.5 Gb/s Link Others ***Reserved***	RO	RO	—	1
9:4	**Maximum Link Width.** This field indicates the maximum width of the given PCI Express Link. Defined encodings are: Value Latency 000000 ***Reserved*** 000001 x1 000010 x2 000100 x4 001000 x8 001100 x12 010000 x16 100000 x32 Others ***Reserved***	RO	RO	—	1
11:10	**Active State Link PM Support.** This field indicates the level of active state power management supported on the given PCI Express Link. Defined encodings are: Value Latency 00 ***Reserved*** 01 L0s Entry Supported 10 ***Reserved*** 11 L0s and L1 Supported	RO	RW	WO	‘b11
14:12	**L0s Exit Latency.** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. Defined encodings are: Value Latency 000 Less than 64 ns 001 64 ns to less than 128 ns 010 128 ns to less than 256 ns 011 256 ns to less than 512 ns 100 512 ns to 1 µs 101 1 µs to less than 2 µs 110 2 µs to 4 µs 111 More than 4 µs	RO	RW	WO	‘b100
17:15	**L1 Exit Latency.** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L1 to L0. Defined encodings are: Value Latency 000 Less than 1 µs 001 1 µs to less than 2 µs 010 2 µs to less than 4 µs 011 4 µs to less than 8 µs 100 8 µs to less than 16 µs 101 16 µs to less than 32 µs 110 32 µs to 64 µs 111 More than 64 µs	RO	RW	WO	‘b100
23:18	***Reserved***	RsvdP	RsvdP	—	0
31:24	**Port Number.** This field indicates the PCI Express port number for the given PCI Express Link.	RO	RW	WO	0

Table 21-67. (Address 70h; LINKCTL) Link Control

Bits	Description	CFG	MM	EE	Default
1:0	**Active State Link PM Control.** This field controls the level of active state PM supported on the given PCI Express Link. Defined encodings are: Value PM Control 00 Disabled 01 L0s Entry Supported 10 ***Reserved*** 11 L0s and L1 Entry Supported ***Note:*** *"L0s Entry Enabled" indicates the Transmitter entering L0s.*	RW	RW	WO	0
2	***Reserved***	RsvdP	RsvdP	—	0
3	**Read Completion Boundary (RCB) Control.** When clear, the read completion boundary is 64 bytes. When set, the read completion boundary is 128 bytes.	RW (Fwd) RO (Rev)	RW	WO	1
4	**Link Disable.** This bit disables the Link when set to 1. This bit is only valid in Reverse Bridge mode in the PEX 8111. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RO (Fwd) RW (Rev)	RO (Fwd) RW (Rev)	— (Fwd) WO (Rev)	0
5	**Retrain Link.** This bit initiates Link retraining when set. It is only valid in Reverse Bridge mode in the PEX 8111. This bit always returns 0 when read.	RO (Fwd) RW (Rev)	RO (Fwd) RW (Rev)	— (Fwd) WO (Rev)	0
6	**Common Clock Configuration.** This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.	RW	RW	WO	0
7	**Extended Sync.** This bit when set forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication.	RW	RW	WO	0
15:8	***Reserved***	RsvdP	RsvdP	—	0

Table 21-68. (Address 72h; LINKSTAT) Link Status

Bits	Description	CFG	MM	EE	Default
3:0	**Link Speed.** This field indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are: Value Max Link Speed 0001 2.5 Gb/s Link Others ***Reserved***	RO	RO	—	1
9:4	**Negotiated Link Width.** This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: Value Width 000000 ***Reserved*** 000001 x1 000010 x2 000100 x4 001000 x8 001100 x12 010000 x16 100000 x32 Others ***Reserved***	RO	RO	—	1
10	**Link Training Error.** This read-only bit indicates that a Link training error occurred. This field is only applicable in Reverse Bridge mode. This bit is cleared by hardware upon successful training of the Link to the L0 Link state.	RO	RO	—	0
11	**Link Training.** This read-only bit indicates that Link training is in progress; hardware clears this bit once Link training is complete. This field is only applicable in Reverse Bridge mode.	RO	RO	—	0
12	**Slot Clock Configuration.** This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear.	HwInit	RW	WO	0
15:13	***Reserved***	RsvdZ	RsvdZ	—	0

Table 21-69. (Address 74h; SLOTCAP) Slot Capabilities

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Present.** The PEX 8111 does not support the Attention Button, so this bit is forced to 0.	RO	RO	—	0
1	**Power Controller Present.** The PEX 8111 does not support a Power Controller, so this bit is forced to 0.	RO	RO	—	0
2	**MRL Sensor Present.** The PEX 8111 does not support an MRL Sensor, so this bit is forced to 0.	RO	RO	—	0
3	**Attention Indicator Present.** The PEX 8111 does not support the Attention Indicator, so this bit is forced to 0.	RO	RO	—	0
4	**Power Indicator Present.** The PEX 8111 does not support the Power Indicator, so this bit is forced to 0.	RO	RO	—	0
5	**Hot-Plug Surprise.** The PEX 8111 does not support Hot-Plug Surprise, so this bit is forced to 0.	RO	RO	—	0
6	**Hot-Plug Capable.** The PEX 8111 does not support Hot-Plug, so this bit is forced to 0.	RO	RO	—	0
14:7	**Slot Power Limit Value.** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot. The Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. Writes to this register cause the PEX 8111 to send the Set Slot Power Limit Message downstream in Reverse Bridge mode. This field is only valid in Reverse Bridge mode.	RO	RW	WO	0
16:15	**Slot Power Limit Scale.** This field specifies the scale used for the Slot Power Limit Value. Writes to this register cause the PEX 8111 to send the Set Slot Power Limit Message downstream in Reverse Bridge mode. This field is only valid in Reverse Bridge mode. Defined encodings are: Value Scale 00 1.0x 01 0.1x 10 0.01x 11 0.001x	RO	RW	WO	‘b00
18:17	***Reserved***	RsvdP	RsvdP	—	0
31:19	**Physical Slot Number.** This field is not supported by the PEX 8111, and is forced to 0.	RO	RO	—	0

Table 21-70. (Address 78h; SLOTCTL) Slot Control

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable.** The PEX 8111 does not support the Attention Button, so this bit is ignored.	RW	RW	WO	0
1	**Power Fault Detected Enable.** The PEX 8111 does not support the Power Fault Detected feature, so this bit is ignored.	RW	RW	WO	0
2	**MRL Sensor Changed Enable.** The PEX 8111 does not support an MRL Sensor Changed feature, so this bit is ignored.	RW	RW	WO	0
3	**Presence Detect Changed Enable.** The PEX 8111 does not support the Presence Detect Changed feature, so this bit is ignored.	RW	RW	WO	0
4	**Command Completed Interrupt Enable.** The PEX 8111 does not support the Command Completed Interrupt, so this bit is ignored.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable.** The PEX 8111 does not support the Hot-Plug Interrupt, so this bit is ignored.	RW	RW	WO	0
10	**Power Controller Control.** The PEX 8111 does not support a Power Controller, so this bit is ignored.	RW	RW	WO	0
7:6	**Attention Indicator Control.** The PEX 8111 does not support the Attention Indicator, so this field is ignored.	RW	RW	WO	0
9:8	**Power Indicator Control.** The PEX 8111 does not support the Power Indicator, so this field is ignored.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	—	0

Table 21-71. (Address 7Ah; SLOTSTAT) Slot Status

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed.** The PEX 8111 does not support the Attention Button, so this bit is forced to 0.	RO	RO	—	0
1	**Power Fault Detected.** The PEX 8111 does not support the Power Fault feature, so this bit is forced to 0.	RO	RO	—	0
2	**MRL Sensor Changed.** The PEX 8111 does not support an MRL Sensor Changed feature, so this bit is forced to 0.	RO	RO	—	0
3	**Presence Detect Changed.** The PEX 8111 does not support the Presence Detect Changed feature, so this bit is forced to 0.	RO	RO	—	0
4	**Command Completed.** The PEX 8111 does not support the Command Completed Interrupt, so this bit is forced to 0.	RO	RO	—	0
5	**MRL Sensor State.** The PEX 8111 does not support the MRL Sensor feature, so this bit is forced to 0.	RO	RO	—	0
6	**Presence Detect State.** The PEX 8111 does not support the Presence Detect feature, so this field is forced to 1.	RO	RO	—	1
15:7	***Reserved***	RsvdP	RsvdP	—	0

Table 21-72. (Address 7Ch; ROOTCTL) Root Control (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**System Error on Correctable Error Enable.** When set, a system error (SERR#) is generated if an ERR_COR is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
1	**System Error on Non-Fatal Error Enable.** When set, a system error (SERR#) is generated if an ERR_NONFATAL is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
2	**System Error on Fatal Error Enable.** When set, a system error (SERR#) is generated if an ERR_FATAL is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
3	**PME Interrupt Enable.** When set, enables PME interrupt generation upon receipt of a PME message as reflected in the PME Status register bit. A PME interrupt is also generated if the PME Status register bit is set when this bit is set from a cleared state.	RW	RW	WO	0
31:4	***Reserved***	RsvdP	RsvdP	—	0

Table 21-73. (Address 80h; ROOTSTAT) Root Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
15:0	**PME Requester ID.** This field indicated the PCI Requester ID of the last PME requester.	RO	RO	—	—
16	**PME Status.** This bit indicates that PME was asserted by the Requester ID indicated in the *PME Requester ID* field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1.	RW1C	RW1C	—	0
17	**PME Pending.** This read-only bit indicates that another is pending when the PME Status bit is set. When the PME Status bit is cleared by software, the PME is delivered by hardware by setting the PME Status bit again and updating the Requester ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.	RO	RO	—	—
31:18	***Reserved***	RsvdP	RsvdP	—	0

21.8 PCI Express Extended Capability Registers

21.8.1 PCI Express Power Budgeting Registers

Table 21-74. (Address 100h; PWRCAPHDR) Power Budgeting Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID.** This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.	RO	RW	WO	4
19:16	**Capability Version.** This field is a PCI-SIG defined version number that indicates the version of the capability structure present.	RO	RW	WO	1
31:20	**Next Capability Offset.** This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.	RO	RW	WO	'h110

Table 21-75. (Address 104h; PWRDATASEL) Power Budgeting Data Select

Bits	Description	CFG	MM	EE	Default
7:0	**Data Select Register.** This register indexes the Power Budgeting Data reported through the Data register and selects the DWORD of Power Budgeting Data that should appear in the Data register. The PEX 8111 supports values from 0 to 31 for this field. For values greater than 31, a value of 0 is returned when the **PWRDATA** register is read.	RW	RW	WO	0
31:8	***Reserved***	RsvdP	RsvdP	—	0

This register returns the DWORD of Power Budgeting Data selected by the **Data Select** register. If the **Data Select** register contains a value greater than or equal to the number of operating conditions for which the device provides power information, this register should return all zeros. The PEX 8111 supports 32 operating conditions.

Table 21-76. (Address 108h; PWRDATA) Power Budgeting Data

Bits	Description	CFG	MM	EE	Default
7:0	**Base Power.** Specifies in watts the base power value in the given operating condition. This value must be multiplied by the data scale to produce the actual power consumption value.	RO	RW	WO	0
9:8	**Data Scale.** Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the contents of the *Base Power* register field with the value corresponding to the encoding return by this field. Defined encodings are: Value Scale Factor 00 1.0x 01 0.1x 10 0.01x 11 0.001x	RO	RW	WO	0
12:10	**PM Sub State.** Specifies the power management sub state of the operating condition being described. Defined encodings are: Value Sub State 000 Default Sub State Others Device Specific Sub State	RO	RW	WO	0
14:13	**PM State.** Specifies the power management state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in the *Type* field to specify the $D3_{cold}$ PM State. An encoding of 11b along with any other *Type* field value specifies the $D3_{hot}$ state. Defined encodings are: Value PM State 00 D0 01 D1 10 D2 11 D3	RO	RW	WO	0
17:15	**PM Type.** Specifies the type of the operating condition being described. Defined encodings are: Value PM Type 000 PME Aux 001 Auxiliary 010 Idle 011 Sustained 111 Maximum Other ***Reserved***	RO	RW	WO	0
20:18	**Power Rail.** Specifies the power rail of the operating condition being described. Defined encodings are: Value Power Rail 000 Power (12V) 001 Power (3.3V) 010 Power (1.8V) 111 Thermal Other ***Reserved***	RO	RW	WO	0
31:21	***Reserved***	RsvdP	RsvdP	—	0

Table 21-77. (Address 10Ch; PWRBUDCAP) Power Budget Capability

Bits	Description	CFG	MM	EE	Default
0	**System Allocated.** When set, this bit indicates that the power budget for the device is included within the system power budget. Reported Power Budgeting Data for this device should be ignored by software for power budgeting decision if this bit is set.	RO	RW	WO	0
31:1	***Reserved***	RsvdP	RsvdP	—	0

21.8.2 PCI Express Serial Number Registers

Table 21-78. (Address 110h; SERCAPHDR) Serial Number Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID.** This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.	RO	RO	—	3
19:16	**Capability Version.** This field is a PCI-SIG defined version number that indicates the version of the capability structure present.	RO	RO	—	1
31:20	**Next Capability Offset.** This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.	RO	RO	—	0

Table 21-79. (Address 114h; SERNUMLOW) Serial Number Low

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number.** This field contains the lower DWORD of the IEEE defined 64-bit extended unique identifier. This identifier includes a 24-bit company id value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer.	RO	RW	WO	0

Table 21-80. (Address 118h; SERNUMHI) Serial Number Hi

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number.** This field contains the upper DWORD of the IEEE defined 64-bit extended unique identifier. This identifier includes a 24-bit company id value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer.	RO	RW	WO	0

21.9 Main Control Registers

Table 21-81. (Address 1000h; DEVINIT) Device Initialization

Bits	Description	Access	Default
3:0	**PCLKO Clock Frequency.** This field controls the frequency of the PCLKO pin. When set to 0, the clock is stopped. Non-zero values represent divisors of the 100 MHz clock. The default value is 3, representing a frequency of 66 MHz. Value Frequency (MHz) 0000 0 0001 100 0010 50 0011 33.3/66 (If M66EN is high, then PCLKO frequency is 66 MHz) 0100 25 0101 20 0110 16.7 0111 14.3 1000 12.5 1001 11.1 1010 10 1011 9.1 1100 8.3 1101 7.7 1110 7.1 1111 6.7	RW	3
4	**PCI Express Enable.** When clear, all configuration accesses to the PEX 8111 result in a completion status of: Configuration Request Retry Status. When set, the PEX 8111 responds normally to PCI Express configuration accesses. If no valid EEPROM is detected, this bit is automatically set.	RW	0
5	**PCI Enable.** When clear, all PCI accesses to the PEX 8111 result in a Target Retry response. When set, the PEX 8111 responds normally to PCI accesses. If no valid EEPROM is detected, this bit is automatically set.	RW	0
31:6	***Reserved***	RsvdP	0

Table 21-82. (Address 1004h; EECTL) EEPROM Control

Bits	Description	Access	Default
7:0	**EEPROM Write Data.** This field determines the byte written to the EEPROM when the *EEPROM Byte Write Start* bit is set. This field can represent an opcode, address, or data being written to the EEPROM.	RW	0
15:8	**EEPROM Read Data.** This field determines the byte read from the EEPROM when the *EEPROM Byte Read Start* bit is set.	RO	—
16	**EEPROM Byte Write Start.** When set, the value in the *EEPROM Write Data* field is written to the EEPROM. This bit is automatically cleared when the write operation is complete.	RW	0
17	**EEPROM Byte Read Start.** When set, a byte is read from the EEPROM, and can be accessed using the *EEPROM Read Data* field. This bit is automatically cleared when the read operation is complete.	RW	0
18	**EEPROM Chip Select Enable.** When set, the EEPROM chip select is enabled.	RW	0
19	**EEPROM Busy.** When set, the EEPROM controller is busy performing a byte read or write operation. An interrupt can be generated whenever this bit goes false.	RO	0
20	**EEPROM Valid.** An EEPROM with 'h5A in the first byte has been detected.	RO	—
21	**EEPROM Present.** This bit is set if the EEPROM controller determines that an EEPROM is connected to the PEX 8111.	RO	—
22	**EEPROM Chip Select Active.** This bit is set if the chip select pin to the EEPROM is active. The chip select can be active across multiple byte operations.	RO	—
24:23	**EEPROM Address Width.** This field reports the addressing width of the installed EEPROM. If the addressing width cannot be determined, a zero is returned. Value — Address Width 00 — undetermined 01 — 1 byte 10 — 2 byte 11 — 3 byte	RO	—
30:25	***Reserved***	RsvdP	0
31	**EEPROM Reload.** Writing a 1 to this bit causes the EEPROM controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the EEPROM. Reading this bit returns a 0 while the initialization is in progress, and a 1 when it is complete.	RW	0

Table 21-83. (Address 1008h; EECLKFREQ) EEPROM Clock Frequency

Bits	Description	Access	Default
2:0	**EEPROM Clock Frequency.** This field controls the frequency of the EECLK pin. Value — Frequency 000 — 2 MHz 001 — 5 MHz 010 — 8.3 MHz 011 — 10 MHz 100 — 12.5 MHz 101 — 16.7 MHz 110 — 25 MHz 111 — ***Reserved***	RW	0
31:3	***Reserved***	RsvdP	0

Table 21-84. (Address 100Ch; PCICTL) PCI Control

Bits	Description	Access	Default
0	**PCI Multi-Level Arbiter.** When clear, all PCI requesters are placed into a single-level round-robin arbiter, each with equal access to the PCI bus. When set, a 2 level arbiter is selected.	RW	0
3:1	**PCI Arbiter Park Select.** This field determines which PCI master controller is granted the PCI bus when there are no pending requests. Value Park 000 Last Grantee 001 PCI Express Bus 010 ***Reserved*** 011 ***Reserved*** 100 External Requester 0 101 External Requester 1 110 External Requester 2 111 External Requester 3	RW	0
4	**Bridge Mode.** This bit reflects the status of the FORWARD pin. When low, the device operates as a Reverse Bridge (PCI to PCI Express). When high, the device operates as a Forward Bridge (PCI Express to PCI).	RO	—
5	**PCI External Arbiter.** This bit reflects the state of the EXTARB pin. When low, the PEX 8111 enables its internal arbiter. It then expects external requests on REQ[3:0]# and issues bus grants on GNT[3:0]#. When high, the PEX 8111 asserts REQ[0]# and expects GNT[0]# from an external arbiter.	RO	—
6	**Locked Transaction Enable.** When clear, PCI Express Memory Read Lock requests are completed with UR status, and the PCI LOCK# pin is not driven in Forward Bridge mode. In Reverse Bridge mode, the PCI LOCK# pin is ignored. When set, Locked Transactions are propagated through the bridge from the primary to secondary bus.	RW	0
7	**M66EN.** This bit reflects the state of the M66EN pin. When low, the PEX 8111 PCI bus is operating at 33 MHz. When high, the PEX 8111 PCI bus is operating at 66 MHz.	RO	0
15:8	**PCI to PCI Express Retry Count.** This field determines how many times to retry a PCI Type 1 Configuration transaction to PCI Express before aborting the transfer. Values range from 0 to 255. A value of 0 indicates that the transaction is retried forever. A value of 255 selects a retry count of 2^{24}. When the timer times out, a Master Abort is returned to the PCI bus. This field is only valid in Reverse Bridge mode when the PCI Express link is down.	RW	'hFF
23:16	**PCI Express to PCI Retry Count.** This field determines how many times to retry a PCI Express to PCI transaction before aborting the transfer. Values range from 0 to 255. A value of 0 indicates that the transaction is retried forever. A value of 255 selects a retry count of 2^{24}.	RW	0
24	**Memory Read Line Enable.** When clear, the PEX 8111 issues a Memory Read command for transactions that do not start on a cache boundary. When set, a Memory Read Line command is issued if a transaction is not aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst is stopped at the cache line boundary if the burst transfer size is less than one cache line of data or if a Memory Read Multiple command can be started.	RW	1
25	**Memory Read Multiple Enable.** When clear, the PEX 8111 issues a Memory Read command for transactions that start on a cache boundary. When set, a Memory Read Multiple command is issued if a transaction is aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst continues if the burst transfer size remains greater than or equal to one cache line of data.	RW	1
31:26	***Reserved***	RsvdP	0

Table 21-85. (Address 1010h; PCIEIRQENB) PCI Express Interrupt Request Enable

Bits	Description	Access	Default
0	**EEPROM Done Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when an EEPROM read or write transaction completes.	RW	0
1	**GPIO Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when an interrupt is active from one of the GPIO pins.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express to PCI Retry Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when the PCI Express to PCI retry count has been reached.	RW	0
4	**Mailbox 0 Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated when Mailbox 3 is written.	RW	0
30:8	***Reserved***	RsvdP	0
31	**PCI Express Internal Interrupt Enable.** When set, this bit enables a PCI Express interrupt to be generated as a result of an internal PEX 8111 interrupt source. The internal interrupt is serviced as either a Message Signaled Interrupt (MSI) or a virtual wire interrupt.	RW	1 (Fwd) 0 (Rev)

Table 21-86. (Address 1014h; PCIIRQENB) PCI Interrupt Request Enable

Bits	Description	Access	Default
0	**EEPROM Done Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when an EEPROM read or write transaction completes.	RW	0
1	**GPIO Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when an interrupt is active from one of the GPIO pins.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express to PCI Retry Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when the PCI Express to PCI retry count has been reached.	RW	0
4	**Mailbox 0 Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when Mailbox 3 is written.	RW	0
8	**Unsupported Request Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated when an Unsupported Request Completion response is received from the PCI Express.	RW	0
30:9	***Reserved***	RsvdP	0
31	**PCI Internal Interrupt Enable.** When set, this bit enables a PCI interrupt to be generated as a result of an internal PEX 8111 interrupt source.	RW	0 (Fwd) 1 (Rev)

Table 21-87. (Address 1018h; IRQSTAT) Interrupt Request Status

Bits	Description	Access	Default
0	**EEPROM Done Interrupt.** This bit is set when an EEPROM read or write transaction completes. Writing a 1 clears this status bit.	RW1C	0
1	**GPIO Interrupt.** This bit conveys the interrupt status for the four GPIO pins. When set, the GPIO Status register should be read to determine the cause of the interrupt. This bit is set independently of the interrupt enable bit.	RO	0
2	***Reserved***	RsvdP	0
3	**PCI Express to PCI Retry Interrupt.** This bit is set when the PCI Express to PCI retry count has been reached. Writing a 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt.** This bit is set when Mailbox 0 is written. Writing a 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt.** This bit is set when Mailbox 1 is written. Writing a 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt.** This bit is set when Mailbox 2 is written. Writing a 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt.** This bit is set when Mailbox 3 is written. Writing a 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt.** This bit is set when an Unsupported Request Completion is received from the PCI Express. Writing a 1 clears this bit	RW1C	0
31:9	***Reserved***	RsvdZ	0

Table 21-88. (Address 101Ch; POWER) Power Register

Bits	Description	Access	Default
7:0	**Power Compare 0.** This field specifies the power required for this device and any downstream PCI devices in Forward Bridge mode. It is compared with the *Captured Slot Power Limit Value* field in the **DEVCAP** register. If the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK pin is asserted. This field is used when the *Captured Slot Power Limit Scale* field is 00 (scale = 1.0x).	RW	0
15:8	**Power Compare 1.** This field specifies the power required for this device and any downstream PCI devices in Forward Bridge mode. It is compared with the *Captured Slot Power Limit Value* field in the **DEVCAP** register. If the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK pin is asserted. This field is used when the *Captured Slot Power Limit Scale* field is 01 (scale = 0.1x).	RW	0
23:16	**Power Compare 2.** This field specifies the power required for this device and any downstream PCI devices in Forward Bridge mode. It is compared with the *Captured Slot Power Limit Value* field in the **DEVCAP** register. If the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK pin is asserted. This field is used when the *Captured Slot Power Limit Scale* field is 10 (scale = 0.01x).	RW	0
31:24	**Power Compare 3.** This field specifies the power required for this device and any downstream PCI devices in Forward Bridge mode. It is compared with the *Captured Slot Power Limit Value* field in the **DEVCAP** register. If the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK pin is asserted. This field is used when the *Captured Slot Power Limit Scale* field is 11 (scale = 0.001x).	RW	0

Table 21-89. (Address 1020h; GPIOCTL) General Purpose I/O Control

Bits	Description	Access	Default
0	**GPIO0 Data.** When programmed as an output, values written to this bit appear on the GPIO0 pin. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 pin.	RW	0
1	**GPIO1 Data.** When programmed as an output, values written to this bit appear on the GPIO1 pin. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 pin.	RW	0
2	**GPIO2 Data.** When programmed as an output, values written to this bit appear on the GPIO2 pin. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 pin.	RW	0
3	**GPIO3 Data.** When programmed as an output, values written to this bit appear on the GPIO3 pin. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 pin.	RW	0
4	**GPIO0 Output Enable.** When clear, the GPIO0 pin is an input. When set, the GPIO0 pin is an output.	RW	1
5	**GPIO1 Output Enable.** When clear, the GPIO1 pin is an input. When set, the GPIO1 pin is an output.	RW	1
6	**GPIO2 Output Enable.** When clear, the GPIO2 pin is an input. When set, the GPIO2 pin is an output.	RW	0
7	**GPIO3 Output Enable.** When clear, the GPIO3 pin is an input. When set, the GPIO3 pin is an output.	RW	0
8	**GPIO0 Interrupt Enable.** When set, changes on the GPIO0 pin (when programmed as an input), are enabled to generate an interrupt.	RW	0
9	**GPIO1 Interrupt Enable.** When set, changes on the GPIO1 pin (when programmed as an input), are enabled to generate an interrupt.	RW	0
10	**GPIO2 Interrupt Enable.** When set, changes on the GPIO2 pin (when programmed as an input), are enabled to generate an interrupt.	RW	0
11	**GPIO3 Interrupt Enable.** When set, changes on the GPIO3 pin (when programmed as an input), are enabled to generate an interrupt.	RW	0
12	**LTSSM Output Enable.** When set, the lower four bits of the LTSSM state machine are output on the GPIO pins.	RW	0
31:13	***Reserved***	RsvdP	0

Table 21-90. (Address 1024h; GPIOSTAT) General Purpose I/O Status

Bits	Description	Access	Default
0	**GPIO0 Interrupt.** This bit is set when the state of the GPIO0 pin changes and the pin is programmed as an input. Writing a 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt.** This bit is set when the state of the GPIO1 pin changes and the pin is programmed as an input. Writing a 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt.** This bit is set when the state of the GPIO2 pin changes and the pin is programmed as an input. Writing a 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt.** This bit is set when the state of the GPIO3 pin changes and the pin is programmed as an input. Writing a 1 clears this bit.	RW1C	0
31:4	***Reserved***	RsvdZ	0

Table 21-91. (Address 1030h; MAILBOX 0) Mailbox 0

Bits	Description	Access	Default
31:0	**Mailbox Data.** This register can be written or read from the PCI Express or PCI. Interrupts can be generated to either of the buses when this register is written.	RW	'hFEED FACE

Table 21-92. (Address 1034h; MAILBOX 1) Mailbox 1

Bits	Description	Access	Default
31:0	**Mailbox Data.** This register can be written or read from the PCI Express or PCI. Interrupts can be generated to either of the buses when this register is written.	RW	0

Table 21-93. (Address 1038h; MAILBOX 2) Mailbox 2

Bits	Description	Access	Default
31:0	**Mailbox Data.** This register can be written or read from the PCI Express or PCI. Interrupts can be generated to either of the buses when this register is written.	RW	0

Table 21-94. (Address 103Ch; MAILBOX 3) Mailbox 3

Bits	Description	Access	Default
31:0	**Mailbox Data.** This register can be written or read from the PCI Express or PCI. Interrupts can be generated to either of the buses when this register is written.	RW	0

Table 21-95. (Address 1040h; CHIPREV) Chip Silicon Revision

Bits	Description	Access	Default
15:0	**Chip Revision.** This register returns the current silicon revision number of the PEX 8111.	RO	Current Revision
31:18	***Reserved***	RsvdP	0

Note: *CHIPREV is the silicon revision, encoded as a 4-digit BCD value. The value of CHIPREV for the first release of the chip is 0100h. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*

Table 21-96. Address 1044h; DIAG) Diagnostic Control

Bits	Description	Access	Default
0	**Fast Times.** When set, internal timers and counters operate at a fast speed for factory chip testing.	RW	0
1	**Force PCI Interrupt.** When set, this bit forces the PCI INTx# interrupt pin to be asserted. The particular INTx# pin that is asserted is determined by the **PCIINTPIN** register. This bit is only effective if the *Interrupt Disable* bit of the **PCICMD** register is low.	RW	0
2	**Force PCI SERR.** When set, this bit forces the PCI SERR# interrupt pin to be asserted if the *SERR# Enable* bit in the **PCI Command** register is set (Reverse Bridge mode). In Forward Bridge mode, the *Secondary SERR Enable* in the **Bridge Control** register must be set.	RW	0
3	**Force PCI Express Interrupt.** When set, this bit forces an interrupt to the PCI Express host using Message Signaled Interrupts or virtual INTx# interrupts.	RW	0
31:4	***Reserved***	RsvdP	0

Table 21-97. (Address 1048h; TLPCFG0) TLP Controller Configuration 0

Bits	Description	Access	Default
7:0	**CFG_NUM_FTS.** Forced NUM_FTS signal. NUM_FTS stands for number of Fast Training sequence (0 – 255). Read PCI Express Base Specification 1.0a, section 4.2.4.3, for detailed information.	RW	'h20
8	**CFG_ACK_FMODE.** PCI Express core ACK_DLLP sending interval mode. 0: Core hardware uses own interval value 1: Core hardware uses *CFG_ACK_COUNT* as interval value.	RW	0
9	**CFG_TO_FMODE.** PCI Express core Timeout detection mode for replay timer. 0: Core hardware uses own timer value. 1: Core hardware uses *CFG_TO_COUNT* as timer value	RW	0
10	**CFG_PORT_DISABLE.** When set, the SERDES in PCI Express core is disabled. This allows endpoint to disable the PCI Express connection when power up or before the configuration is completed.	RW	0
11	**CFG_RCV_DETECT.** This signal is asserted when the PCI Express core establishes the PCI Express connection.	RO	0
12	**CFG_LPB_MODE.** Link Loopback mode.	RW	0
13	**CFG_PORT_MODE.** When set, Link core is configured as downstream port (Root Complex). When clear, Link core is configured as upstream port (endpoint).	RW	F(0) R(1)
14	***Reserved***	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE.** When set, link is allowed generate ECRC. The PEX 8111 does not support ECRC, so this bit should be set to 0.	RW	0
16	**TLB_CPLD_NOSUCCESS_MALFORM_ENABLE.** When set, completion received when completion timeout expired is treated as a malformed TLB and is discarded. When clear, received completion is kept.	RW	1
17	**Scrambler Disable.** When clear, data scrambling is enabled. When set, data scrambling is disabled. This bit should only be set for testing and debugging.	RW	0
31:18	***Reserved***	RsvdP	'h20

Table 21-98. (Address 104Ch; TLPCFG1) TLP Controller Configuration 1

Bits	Description	Access	Default
20:0	**CFG_TO_COUNT.** PCI Express core replay timer timeout value if *CFG_TO_FMODE* is set to 1.	RW	'hD4
30:21	**CFG_ACK_COUNT.** PCI Express core ACK DLLP sending interval value if *CFG_ACK_MODE* is set to 1.	RW	0
31	***Reserved***	RsvdP	0

Table 21-99. (Address 1050h; TLPCFG2) TLP Controller Configuration 2

Bits	Description	Access	Default
15:0	**CFG_COMPLETER_ID0.** Bits [15:8]: Bus number Bits [7:3]: Device number Bits [2:0]: Function number When TLB0_TRANS is asserted with Type 0 Configuration Cycle, this signal latches CFG_TLB0_BUS_NUMBER[7:0] and CFG_TLB0_DEV_NUMBER[4:0] into corresponding bits.	RW	0
31:16	***Reserved***	RsvdP	0

Table 21-100. (Address 1054h; TLPTAG) TLP Controller Tag

Bits	Description	Access	Default
7:0	**TAG BME1.** Tag field for message request.	RW	0
15:8	**TAG ERM.** Tag field for Error Manager**.**	RW	0
23:16	**TAG PME.** Tag field for Power Manager**.**	RW	0
31:24	***Reserved***	RsvdP	0

Table 21-101. (Address 1058h; TLPTIMELIMIT0) TLP Controller Time Limit 0

Bits	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT.** Bus master engine completion timeout in units of PCI clocks. The default value produces a 10 ms timeout.	RW	'h6A4 (M66EN low) 'hA2C2A (M66EN high
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT.** This value determines the amount of time before power is removed after entering the L2 state. This value should be at least 100 ns. This field has units of PCI clocks.	RW	'h4 (M66EN low) 'h8 (M66EN high)
31:28	***Reserved***	RsvdP	0

Table 21-102. (Address 105Ch; TLPTIMELIMIT1) TLP Controller Time Limit 1

Bits	Description	Access	Default
10:0	**ASPM_L1_DLLP_INTERVAL_TIME_LIMIT.** This field determines the time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions. There should be at least 10 us spent in LTSSM L0 and L0s state before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP can be transmitted. Detailed information is on page 19 of the *PCI Express 1.0a Base Specification Errata*. This field has units of PCI clocks.	RW	'h14D (M66EN low) 'h29A (M66EN high)
31:11	***Reserved***	RsvdP	0

Table 21-103. (Address 1060h; CRSTIMER) CRS Time

Bits	Description	Access	Default
15:0	**CRS Timer.** This field determines how many microseconds to wait before returning a completion with CRS status in response to a PCI Express to PCI Configuration Transaction. If the timer times out and the completion with CRS status is returned, the transaction is discarded from the Non-Posted Transaction Queue. This field is only valid in Forward Bridge mode when the *Bridge Configuration Retry Enable* bit in the **DEVCTL** register is set.	RW	25
31:16	***Reserved***	RsvdP	0

Table 21-104. (Address 1064h; ECFGADDR) Enhanced Configuration Address

Bits	Description	Access	Default
11:0	***Reserved***	RsvdP	0
14:12	**Configuration Function Number.** This field provides the function number for an enhanced Configuration Transaction.	RW	0
19:15	**Configuration Device Number.** This field provides the device number for an enhanced Configuration Transaction.	RW	0
27:20	**Configuration Bus Number.** This field provides the bus number for an enhanced Configuration Transaction.	RW	0
30:28	***Reserved***	RsvdP	0
31	**Enhanced Configuration Enable.** When clear, accesses to Base Address Register 0 offset 'h2000 are not responded to by the PEX 8111. When set, accesses to Base Address Register 0 offset 'h2000 are forwarded to the PCI Express bus as a Configuration Request. This bit is only used in Reverse Bridge mode.	RW	0

Chapter 22 Testability and Debug

22.1 JTAG Interface

The PEX 8111 provides a JTAG Boundary Scan interface, which is utilized to debug board connectivity for each ball.

22.1.1 IEEE Standard 1149.1 Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG* (Joint Test Action Group) debug port, is an architectural standard described in the *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*. This standard describes a method for accessing internal chip facilities, using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG debug port implements the four required JTAG signals (TCK, TDI, TDO, TMS) and the optional TRST# signal.
- JTAG Clock Requirements – TCK signal frequency can range from DC to 10 MHz.
- JTAG Reset Requirements – Refer to Section 22.1.4, "JTAG Reset Input TRST#".

22.1.2 JTAG Instructions

The JTAG debug port provides the *IEEE standard 1149.1* EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE instructions, as listed in Table 22-1. PRIVATE instructions are for PLX use only. Invalid instructions behave as the BYPASS instruction. Table 22-1 lists the JTAG instructions, along with their input codes. The PEX 8111 returns the IDCODE values listed in Table 22-2

Table 22-1. EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE Instructions

Instruction	Input Code	Comments
EXTEST	00000b	*IEEE Standard 1149.1-1990*
IDCODE	00001b	
SAMPLE/PRELOAD	00011b	
BYPASS	11111b	
PRIVATE[a]	00011b	
	00100b	
	00101b	
	00110b	
	00111b	
	01000b	
	01001b	
	01010b	

*a. **Warning: Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.***

Table 22-2. PEX 8111 JTAG IDCODE Values

PEX 8111	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0000b	1000_0001_1101_0010	000_0001_0000	1
Hex	0h	81D2h	10h	1h
Decimal	0	33234	16	1

22.1.3 JTAG Boundary Scan Boundary

Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture. BSDL*, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, which allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. *BSDL* supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of *BSDL* include the logical port description, physical ball map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the chip balls. Each ball has a logical type of in, out, in out, buffer, or linkage that defines the logical direction of signal flow.

The physical ball map correlates the chip logical ports to the physical balls of a specific package. A *BSDL* description can have several physical ball maps; each map is given a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the chip in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the chip.

The boundary register description lists each cell or shift stage of the Boundary register. Each cell has a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

22.1.4 JTAG Reset Input TRST#

The TRST# input ball is the asynchronous JTAG logic reset. When TRST# is asserted, it causes the PEX 8111 TAP controller to initialize. In addition, when the TAP controller is initialized, it selects the PEX 8111 normal logic path (core-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, one of the following should be considered:
  - TRST# input signal should use a low-to-high transition once during the PEX 8111 boot-up, along with the RST# signal
  - Hold the PEX 8111 TMS ball high while transitioning the PEX 8111 TCK ball five times
- If JTAG functionality is not required, the TRST# signal must be directly connected to ground

Chapter 23 Electrical Specifications

23.1 Absolute Maximum Ratings

Note: *Conditions that exceed the Absolute Maximum limits may destroy the device.*

Table 23-1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages	With Respect to Ground	-0.5	1.8	V
VDD3.3, VDDQ	3.3V Supply Voltages	With Respect to Ground	-0.5	4.6	V
VDD5	5V Supply Voltage	With Respect to Ground	-0.5	6.6	V
V_I	DC input voltage	3.3 V buffer	-0.5	4.6	V
		5 V Tolerant buffer (PCI)	-0.5	6.6	V
I_{OUT}	DC Output Current, per pin	3mA Buffer	-10	10	mA
		6mA Buffer	-20	20	mA
		12mA Buffer	-40	40	mA
		24mA Buffer (PCI)	-70	70	mA
T_{STG}	Storage Temperature	No bias	-65	150	° C
T_{AMB}	Ambient temperature	Under bias	-40	85	° C
V_{ESD}	ESD Rating	R = 1.5K, C = 100pF		2	KV

23.2 Recommended Operating Conditions

Note: *Conditions that exceed the Operating limits may cause the device to function incorrectly.*

Table 23-2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages		1.4	1.6	V
VDD3.3, VDDQ	3.3V Supply Voltages		3.0	3.6	V
VDD5	5V Supply Voltage	Note 1	4.75	5.25	V
V_N	Negative trigger voltage	3.3 V buffer	0.8	1.7	V
		5 V tolerant buffer (PCI)	0.8	1.7	V
V_P	Positive trigger voltage	3.3 V buffer	1.3	2.4	V
		5 V tolerant buffer (PCI)	1.3	2.4	V
V_{IL}	Low Level Input Voltage	3.3 V buffer	0	0.7	V
		5 V tolerant buffer (PCI)	0	0.8	V
V_{IH}	High Level Input Voltage	3.3 V buffer	1.7	VDD3	V
		5 V tolerant buffer (PCI)	2.0	VDD5+0.5	V
I_{OL}	Low Level Output Current	3mA buffer (V_{OL} = 0.4)		3	mA
		6mA buffer (V_{OL} = 0.4)		6	mA
		12mA buffer (V_{OL} = 0.4)		12	mA
		24mA buffer (V_{OL} = 0.4) (PCI)		24	mA
I_{OH}	High Level Output Current	3mA buffer (V_{OH} = 2.4)		-3	mA
		6mA buffer (V_{OH} = 2.4)		-6	mA
		12mA buffer (V_{OH} = 2.4)		-12	mA
		24mA buffer (V_{OH} = 2.4) (PCI)		-24	mA
T_A	Operating Temperature		0	70	°C
t_R	Input rise times	Normal input	0	200	ns
t_F	Input fall time	Normal input	0	200	ns
t_R	Input rise times	Schmitt input	0	10	ms
t_F	Input fall time	Schmitt input	0	10	ms

Notes:

1, In a 3.3 V only system, the VDD5 pins can be connected to the 3.3 V supply (3.0 to 3.6 V).

2, Power up sequence
The power supply voltages should be applied in the following sequence: First: VDD5, Second: 3.3 V and 1.5 V supplies, in any order.
If the VDD5 pins are connected to the same 3.3 V supply used by the VDD3.3 and VDDQ pins, then power can be applied at the same time to the VDD5, VDD3.3, and VDDQ pins.

3, Power down sequence
The power supply voltages should be removed in the following sequence:
First: 3.3 V and 1.5 V supplies, in any order. Second: VDD5
If the VDD5 pins are connected to the same 3.3 V supply used by the VDD3.3 and VDDQ pins, then power can be removed at the same time from the VDD5, VDD3.3, and VDDQ pins.

23.3 DC Specifications

Operating Conditions: VDD1.5: 1.5V ±0.1V, VDD3.3: 3.3V ±0.3V, T_A = 0° C to 70° C

All typical values are at VDD1.5 = 1.5V, VDD3.3 = 3.3V and T_A = 25° C

Table 23-3. Core DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDD1.5}$	VDD1.5 Supply Current	VDD1.5 = 1.5V		180	207	mA
$I_{VDDSERDES}$	VDD_P, VDD_R, VDD_T, AVDD, Supply Currents	VDD_P, VDD_R, VDD_T, AVDD = 1.5V				
$I_{VDD3.3}$	VDD3.3 Supply Current	VDD3.3 = 3.3V		19	22	mA
I_{VDDQ}	VDDQ Supply Current	VDDQ= 3.3V				
I_{VDD5}	VDD5 Supply Current	VDD5= 5.0V		.003	.004	mA

23.3.1 PCI Bus DC Specification

Operating Conditions: VDD1.5: 1.5V ±0.1V, VDD3.3: 3.3V ±0.3V, T_A = 0° C to 70° C

All typical values are at VDD1.5 = 1.5V, VDD3.3 = 3.3V and T_A = 25° C

Table 23-4. PCI Bus DC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHd}	PCI 3.3V Input High Voltage		0.5*VDD3.3		VDD3.3	V
V_{ILd}	PCI 3.3V Input Low Voltage		0		0.7	V
V_{IH}	PCI 5.0V Input High Voltage		2.0		5.5	V
V_{IL}	PCI 5.0V Input Low Voltage		0		0.8	V
I_{IL}	Input Leakage	$0V < V_{IN} < VDD5$	-10		10	µA
I_{OZ}	Hi-Z State Data Line Leakage	$0V < V_{IN} < VDD5$			10	µA
V_{OH3}	PCI 3.3V Output High Voltage	I_{OUT} = -500 µA	0.9*VDD3.3			V
V_{OL3}	PCI 3.3V Output Low Voltage	I_{OUT} = 1500 µA			0.1*VDD3.3	V
V_{OH}	PCI 5.0V Output High Voltage	I_{OUT} = -12mA	2.4			V
V_{OL}	PCI 5.0V Output Low Voltage	I_{OUT} = 12mA			0.4	V
C_{IN}	Input Capacitance	Pin to GND			10	pF
C_{CLK}	CLK Pin Capacitance	Pin to GND	5		12	pF
C_{IDSEL}	IDSEL Pin Capacitance	Pin to GND			8	pF

23.4 AC Specifications

23.4.1 PCI Bus 33-MHz AC Specifications

Operating Conditions: VDD1.5: 1.5V ±0.1V, VDD3.3: 3.3V ±0.3V, T_A = 0° C to 70° C

All typical values are at VDD1.5 = 1.5V, VDD3.3 = 3.3V and T_A = 25° C

Table 23-5. PCI Bus 33-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		30	∞	ns	
T_{VAL}	CLK to signal valid delay – bused signals		2	11	ns	2, 3
T_{VAL}(ptp)	CLK to signal valid delay – point to point		2	12	ns	2, 3
T_{ON}	Float to Active Delay		2		ns	7
T_{OFF}	Active to Float Delay			28	ns	7
T_{SU}	Input Setup to CLK – bused signals		6		ns	3, 8
T_{SU}(ptp)	Input Setup to CLK – point to point		10,12		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset active time after power stable		1		ms	5
$T_{RST-CLK}$	Reset active time after CLK stable		100		µs	5
$T_{RST-OFF}$	Reset active to Output Float delay			40	ns	5, 6, 7
T_{RHFA}	RST# high to first configuration access		2^{25}		clocks	9
T_{RHFF}	RST# high to first FRAME# assertion		5		clocks	

Notes:

2, For parts compliant to the 5V signaling environment:

Minimum times are evaluated with 0pF equivalent load; maximum times are evaluated with 50pF equivalent load. Actual test capacitance may vary, but results must be correlated to these specifications.

Faster buffers may exhibit some ring back when attached to a 50pF lump load which should be of no consequence as long as the output buffers are in full compliance with slew rate and V/I curve specifications.

For parts compliant to the 3.3V signaling environment:

Minimum times are evaluated with the same load used for slew rate measurement; maximum times are evaluated with a parallel RC load of 25 ohms and 10pF.

3, REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bused signals. GNT# has a setup of 10; REQ# has a setup of 12. All other signals are bused.

5, CLK is stable when it meets the PCI CLK specifications. RST# is asserted and de-asserted asynchronously with respect to CLK.

6, All output drivers must be asynchronously floated when RST# is active.

7, For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8, Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

9, At 66 MHz, the device needs to be ready to accept a configuration access within 1 second after RST# is high.

23.4.2 PCI Bus 66-MHz AC Specifications

Operating Conditions: VDD1.5: 1.5V ±0.1V, VDD3.3: 3.3V ±0.3V, T_A = 0° C to 70° C

All typical values are at VDD1.5 = 1.5V, VDD3.3 = 3.3V and T_A = 25° C

Table 23-6. PCI Bus 66-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		15	∞	ns	
T_{VAL}	CLK to signal valid delay – bused signals		2	6	ns	3, 8
T_{VAL}(ptp)	CLK to signal valid delay – point to point		2	6	ns	3, 8
T_{ON}	Float to Active Delay		2		ns	8, 9
T_{OFF}	Active to Float Delay			14	ns	9
T_{SU}	Input Setup to CLK – bused signals		3		ns	3, 10
T_{SU}(ptp)	Input Setup to CLK – point to point		5		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset active time after power stable		1		ms	5
$T_{RST-CLK}$	Reset active time after CLK stable		100		µs	5
$T_{RST-OFF}$	Reset active to Output Float delay			40	ns	5, 6
T_{RHFA}	RST# high to first configuration access		2^{25}		clocks	9
T_{RHFF}	RST# high to first FRAME# assertion		5		clocks	

Notes:

3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.

5. If M66EN is asserted, CLK is stable when it meets the requirements in PCI Local Bus Specification Section 7.6.4.1. RST# is asserted and de-asserted asynchronously with respect to CLK. Refer to PCI r2.3, Section 4.3.2 for further information.

6. All output drivers must be floated when RST# is active.

8. When M66EN is asserted, the minimum specification for Tval(min), Tval(ptp)(min), and Ton may be reduced to 1 ns if a mechanism is provided to guarantee a minimum value of 2 ns when M66EN is de-asserted.

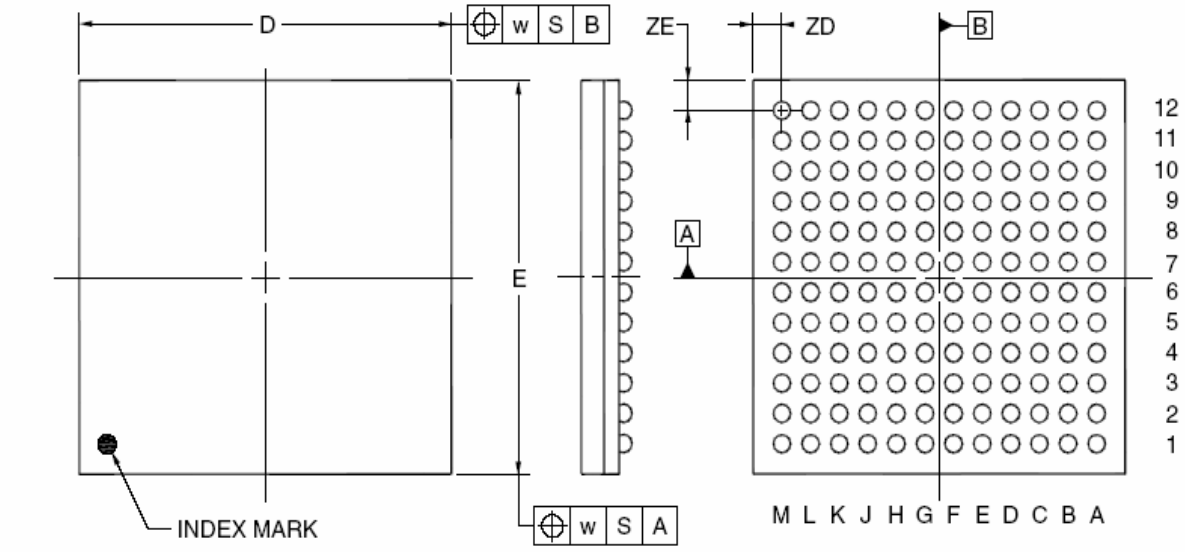
9. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

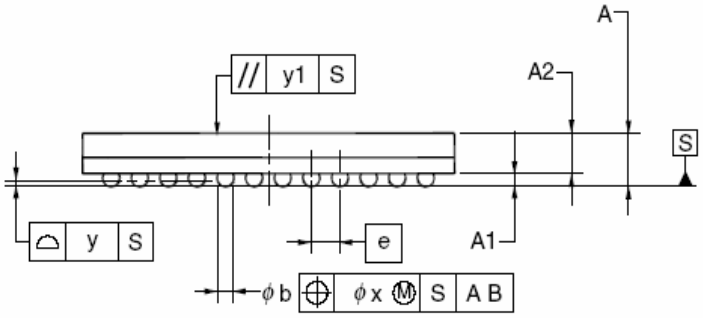
10. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time. Refer to PCI r2.3, Section 3.10, item 9 for further details.

Chapter 24 Mechanical

24.1 PBGA (144 Pin Package)

144-PIN PLASTIC BGA (13x13)





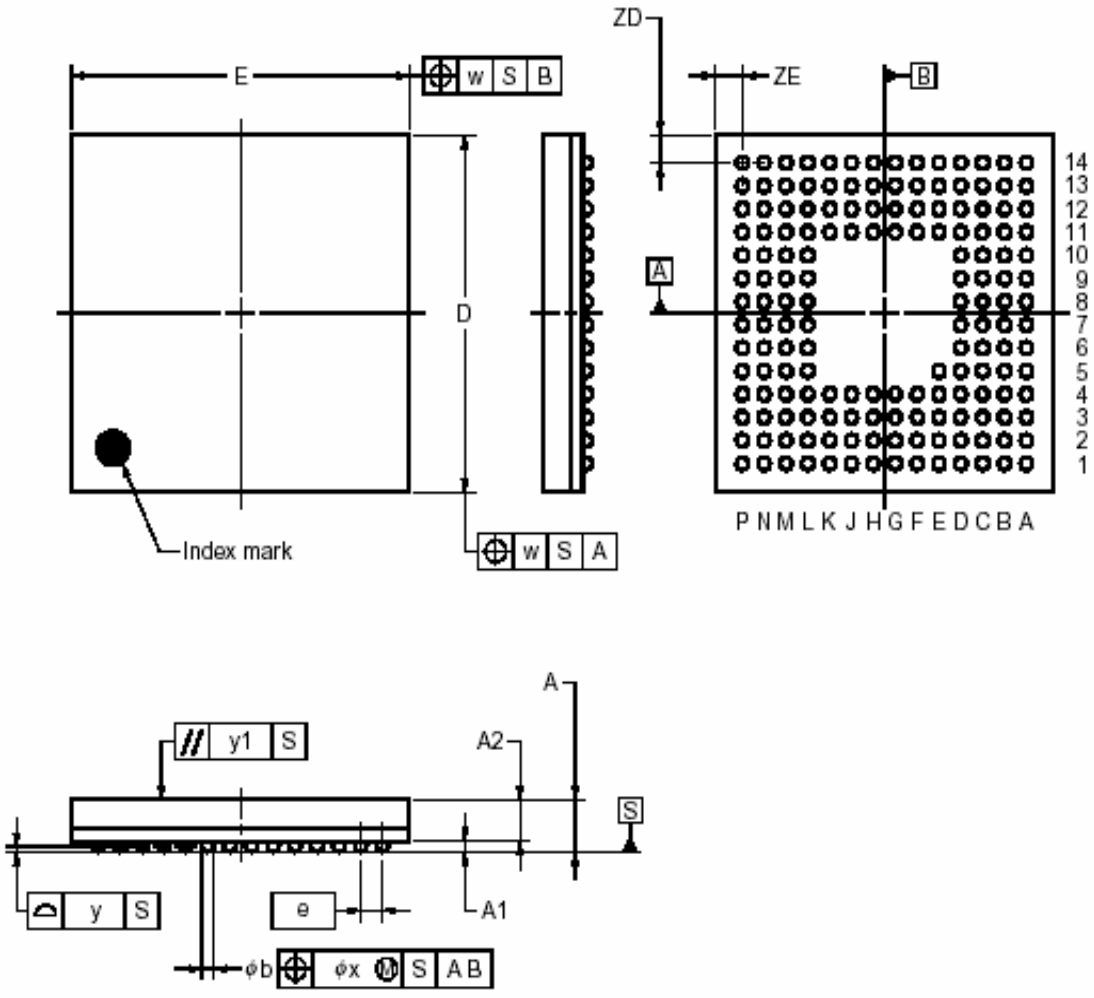
(UNIT:mm)

ITEM	DIMENSIONS
D	13.00±0.10
E	13.00±0.10
w	0.30
e	1.00
A	1.83±0.20
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P144F1-100-ENH

24.2 FBGA (161 Pin Package)

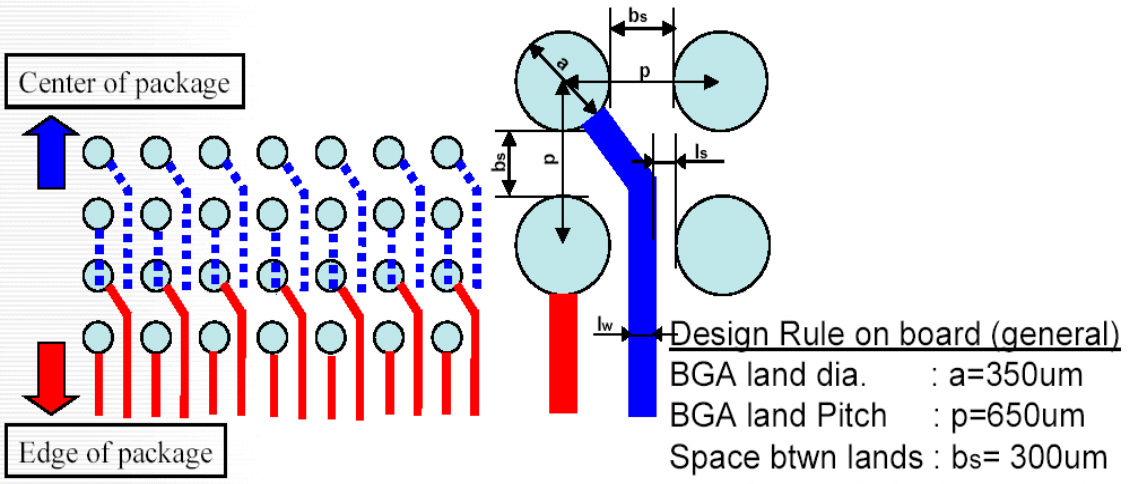
161-PIN PLASTIC FBGA (10x10)



ITEM	MILLIMETERS
D	10.00±0.10
E	10.00±0.10
w	0.20
A	1.43±0.10
A1	0.30±0.05
A2	1.13
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.775
ZE	0.775

P161F1-65-DA1

24.3 PCB Layout



Design Rule on board (general)
BGA land dia. : a=350um
BGA land Pitch : p=650um
Space btwn lands : bs= 300um
Line/Space : lw/ls=100um/100um

Red : traces on an upper signal layer for the PCB
Blue : traces on a lower signal layer for PCB

2 signal layers are required due to routing only one trace between BGA lands.

Appendix A General Information

A.1 Product Ordering Information

Table A-1. Product Ordering Information

Part Number	Description
PEX8111-AA66BC	PCI Express-to-PCI Bridge, Standard BGA Package (144-Ball, 13 x 13 mm)
PEX8111-AA66FBC	PCI Express-to-PCI Bridge, Fine-Pitch BGA Package (161-Ball, 10 x 10 mm)
PEX8111-AA66BC F	PCI Express-to-PCI Bridge, Standard BGA Package (144-Ball, 13 x 13 mm), Lead Free
PEX8111-AA66FBC F	PCI Express-to-PCI Bridge, Fine-Pitch BGA Package (161-Ball, 10 x 10 mm), Lead Free
PEX8111RDK-F	Forward Bridge Reference Design Kit
PEX8111RDK-R	Reverse Bridge Reference Design Kit

A.2 United States and International Representatives and Distributors

A list of PLX Technology, Inc., representatives and distributors can be found at http://www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at http://www.plxtech.com/support/, or call 408 774-9060 or 800 759-3735.