P82B96

Dual bidirectional bus buffer

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1. General description

The P82B96 is a bipolar IC that creates a non-latching, bidirectional, logic interface between the normal I^2C-bus and a range of other bus configurations. It can interface I^2C-bus logic signals to similar buses having different voltage and current levels.

For example, it can interface to the 350 μA SMBus, to 3.3 V logic devices, and to 15 V levels and/or low-impedance lines to improve noise immunity on longer bus lengths.

It achieves this interface without any restrictions on the normal I^2C-bus protocols or clock speed. The IC adds minimal loading to the I^2C-bus node, and loadings of the new bus or remote I^2C-bus nodes are not transmitted or transformed to the local node. Restrictions on the number of I^2C-bus devices in a system, or the physical separation between them, are virtually eliminated. Transmitting SDA and SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bidirectional signal line with I^2C-bus properties.

2. Features

- Bidirectional data transfer of I^2C-bus signals
- Isolates capacitance allowing 400 pF on Sx/Sy side and 4000 pF on Tx/Ty side
- Tx/Ty outputs have 60 mA sink capability for driving low-impedance or high capacitive buses
- 400 kHz operation over at least 20 meters of wire (see *AN10148*)
- Supply voltage range of 2 V to 15 V with I^2C-bus logic levels on Sx/Sy side independent of supply voltage
- Splits I^2C-bus signal into pairs of forward/reverse Tx/Rx, Ty/Ry signals for interface with opto-electrical isolators and similar devices that need unidirectional input and output signal paths.
- Low power supply current
- ESD protection exceeds 3500 V HBM per JESD22-A114, 250 V DIP package, 400 V SO package MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up free (bipolar process with no latching structures)
- Packages offered: DIP8, SO8 and TSSOP8

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3. Applications

- Interface between I^2C-buses operating at different logic levels (for example, 5 V and 3 V or 15 V)
- Interface between I^2C-bus and SMBus (350 μA) standard
- Simple conversion of I^2C-bus SDA or SCL signals to multi-drop differential bus hardware, for example, via compatible PCA82C250
- Interfaces with opto-couplers to provide opto-isolation between I^2C-bus nodes up to 400 kHz.

4. Ordering information

Table 1:   Ordering information

Type number	Package			
	Name	**Description**		**Version**
P82B96DP	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm		SOT505-1
P82B96PN	DIP8	plastic dual in-line package; 8 leads (300 mil)		SOT97-1
P82B96TD	SO8	plastic small outline package; 8 leads; body width 3.9 mm		SOT96-1
P82B96TD/S410	SO8	plastic small outline package; 8 leads; body width 3.9 mm		SOT96-1

4.1 Ordering options

Table 2:   Ordering options

Type number	Temperature range	Topside mark
P82B96DP	−40 °C to +85 °C	82B96
P82B96PN	−40 °C to +85 °C	P82B96PN
P82B96TD	−40 °C to +85 °C	P82B96T
P82B96TD/S410	−40 °C to +125 °C	P82B96T

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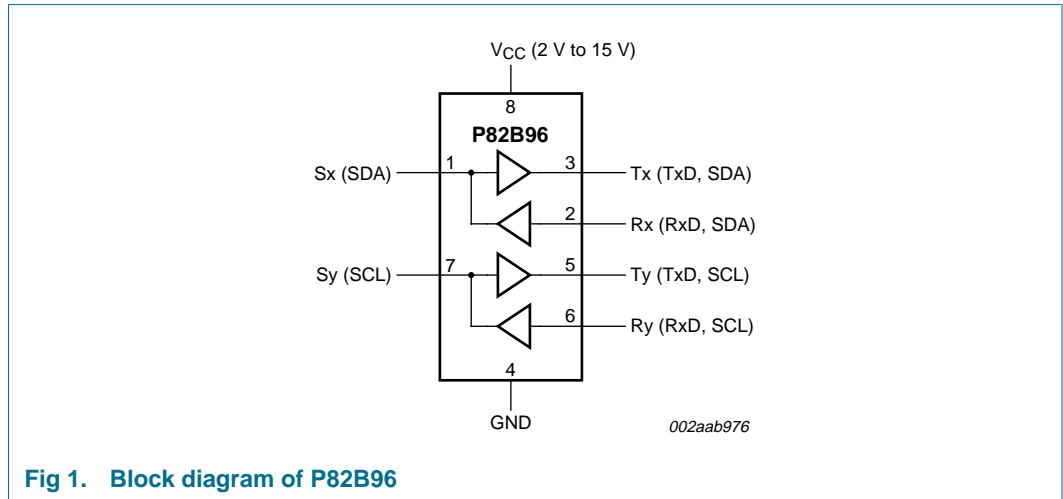
5. Block diagram

Fig 1.   Block diagram of P82B96

6. Pinning information
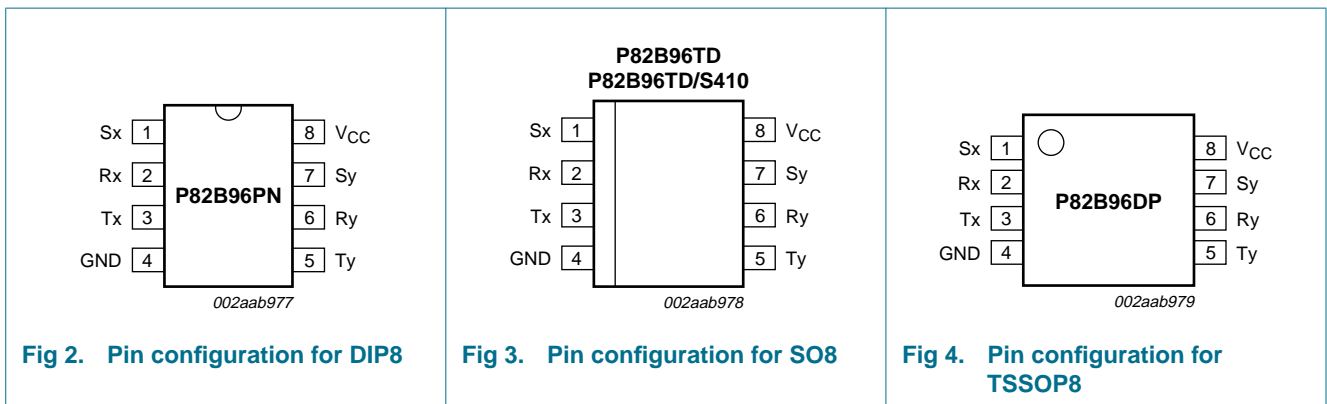
6.1 Pinning

Fig 2.   Pin configuration for DIP8

Fig 3.   Pin configuration for SO8

Fig 4.   Pin configuration for TSSOP8

6.2 Pin description

Table 3:   Pin description

Symbol	Pin	Description
Sx	1	I^{2}C-bus (SDA or SCL)
Rx	2	receive signal
Tx	3	transmit signal
GND	4	negative supply
Ty	5	transmit signal
Ry	6	receive signal
Sy	7	I^{2}C-bus (SDA or SCL)
V$_{CC}$	8	positive supply voltage

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7. Functional description

Refer to Figure 1 "Block diagram of P82B96".

The P82B96 has two identical buffers allowing buffering of both of the I^2C-bus (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I^2C-bus interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I^2C-bus interface. Thus these paths are:

- sense the voltage state of the I^2C-bus pin Sx (or Sy) and transmit this state to the pin Tx (Ty respectively), and
- sense the state of the pin Rx (Ry) and pull the I^2C-bus pin LOW whenever Rx (Ry) is LOW.

The rest of this discussion will address only the 'x' side of the buffer; the 'y' side is identical.

The I^2C-bus pin (Sx) is designed to interface with a normal I^2C-bus.

The logic threshold voltage levels on the I^2C-bus are independent of the IC supply V_{CC}. The maximum I^2C-bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 42 % of V_{CC}, and logic HIGH is above 58 % of V_{CC} (with a typical switching threshold of half V_{CC}).

Tx is an open-collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of V_{CC}, as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I^2C-bus device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I^2C-bus pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I^2C-bus (Sx) to be pulled to a logic LOW level in accordance with I^2C-bus requirements (maximum 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch LOW.

The minimum LOW level this chip can achieve on the I^2C-bus by a LOW at Rx is typically 0.8 V.

If the supply voltage V_{CC} fails, then neither the I^2C-bus nor the Tx output will be held LOW. Their open-collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on Sx and Rx also present no loading of external signals even when V_{CC} is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 7 pF for all bus voltages and supply voltages including V_{CC} = 0 V.

Remark: Two or more Sx or Sy I/Os must not be interconnected. The P82B96 design does not support this configuration. Bidirectional I^2C-bus signals do not allow any direction control pin so, instead, slightly different logic low voltage levels are used at Sx/Sy to avoid latching of this buffer. A 'regular I^2C-bus LOW' applied at the Rx/Ry of a P82B96 will be propagated to Sx/Sy as a 'buffered LOW' with a slightly higher voltage level. If this

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special 'buffered LOW' is applied to the Sx/Sy of another P82B96 that second P82B96 will not recognize it as a 'regular I²C-bus LOW' and will not propagate it to its Tx/Ty output. The Sx/Sy side of P82B96 may not be connected to similar buffers that rely on special logic thresholds for their operation, for example PCA9511, PCA9515, or PCA9518. The Sx/Sy side is only intended for, and compatible with, the normal I²C-bus logic voltage levels of I²C-bus master and slave chips, or even Tx/Rx signals of a second P82B96 if required. The Tx/Rx and Ty/Ry I/O pins use the standard I²C-bus logic voltage levels of all I²C-bus parts. There are **no** restrictions on the interconnection of the Tx/Rx and Ty/Ry I/O pins to other P82B96s, for example in a star or multipoint configuration with the Tx/Rx and Ty/Ry I/O pins on the common bus and the Sx/Sy side connected to the line card slave devices. For more details see *Application Note AN255*.

8. Limiting values

Table 4:   Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages with respect to pin GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	V_{CC} to GND	−0.3	+18	V
V_{Sx}	voltage on pin Sx	I²C-bus SDA or SCL	−0.3	+18	V
V_{Tx}	voltage on pin Tx	buffered output	−0.3	+18	V
V_{Rx}	voltage on pin Rx	receive input	−0.3	+18	V
I_n	current on any pin		-	250	mA
P_{tot}	total power dissipation		-	300	mW
T_j	junction temperature	operating range P82B96TD/S410	−40	+125	°C
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

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9. Characteristics

Table 5: Characteristics

T_{amb} = +25 °C; voltages are specified with respect to GND with V_{CC} = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = +25 °C			T_{amb} = −40 °C to +125 °C [1]		Unit
			Min	Typ	Max	Min	Max	
Power supply								
V_{CC}	supply voltage	operating	2.0	-	15	2.0	15	V
I_{CC}	supply current	buses HIGH	-	0.9	1.8	-	3	mA
		V_{CC} = 15 V; buses HIGH	-	1.1	2.5	-	4	mA
ΔI_{CC}	additional quiescent supply current	per Tx or Ty LOW	-	1.7	3.5	-	3.5	mA
Bus pull-up (load) voltages and currents								
V_{Sx}, V_{Sy}	maximum input/output voltage	open-collector; I²C-bus and V_{Rx}, V_{Ry} = HIGH	-	-	15	-	15	V
I_{Sx}, I_{Sy}	static output loading on I²C-bus	V_{Sx}, V_{Sy} = 1.0 V; V_{Rx}, V_{Ry} = LOW [2]	0.2	-	3	0.2	3	mA
I_{Sx}, I_{Sy}	dynamic output sink capability on I²C-bus	V_{Sx}, V_{Sy} = 2 V; V_{Rx}, V_{Ry} = LOW	7	18	-	7	-	mA
I_{Sx}, I_{Sy}	leakage current on I²C-bus	V_{Sx}, V_{Sy} = 5 V; V_{Rx}, V_{Ry} = LOW	-	-	1	-	10	µA
		V_{Sx}, V_{Sy} = 15 V; V_{Rx}, V_{Ry} = HIGH	-	1	-	-	10	µA
V_{Tx}, V_{Ty}	maximum output voltage level	open-collector	-	-	15	-	15	V
I_{Tx}, I_{Ty}	static output loading on buffered bus	V_{Tx}, V_{Ty} = 0.4 V; V_{Sx}, V_{Sy} = LOW on I²C-bus = 0.4 V	-	-	30	-	30	mA
I_{Tx}, I_{Ty}	dynamic output sink capability, buffered bus	V_{Tx}, V_{Ty} > 1 V; V_{Sx}, V_{Sy} = LOW on I²C-bus = 0.4 V	60	100	-	60	-	mA
I_{Tx}, I_{Ty}	leakage current on buffered bus	V_{Tx}, V_{Ty} = V_{CC} = 15 V; V_{Sx}, V_{Sy} = HIGH	-	1	-	-	10	µA
Input currents								
I_{Sx}, I_{Sy}	input current from I²C-bus	bus LOW; V_{Rx}, V_{Ry} = HIGH	-	−1	-	-	−10	µA
I_{Rx}, I_{Ry}	input current from buffered bus	bus LOW; V_{Rx}, V_{Ry} = 0.4 V	-	−1	-	-	−10	µA
I_{Rx}, I_{Ry}	leakage current on buffered bus input	V_{Rx}, V_{Ry} = V_{CC}	-	1	-	-	10	µA
Output logic LOW level								
V_{Sx}, V_{Sy}	output logic level LOW on normal I²C-bus	I_{Sx}, I_{Sy} = 3 mA [3]	0.8	0.88	1.0	(see Figure 6)		V
		I_{Sx}, I_{Sy} = 0.2 mA [3]	670	730	790	(see Figure 5)		mV
dV_{Sx}/dT, dV_{Sy}/dT	temperature coefficient of output LOW levels	I_{Sx}, I_{Sy} = 0.2 mA [3]	-	−1.8	-	-	-	mV/K

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Table 5: **Characteristics** *…continued*

T_{amb} = +25 °C; voltages are specified with respect to GND with V_{CC} = 5 V, unless otherwise specified.

| Symbol	Parameter	Conditions		T_{amb} = +25 °C			T_{amb} = −40 °C to +125 °C [1]		Unit
				Min	**Typ**	**Max**	**Min**	**Max**	
Input logic switching threshold voltages									
V_{Sx}, V_{Sy}	input logic voltage LOW	on normal I²C-bus	[4]	-	640	600	(see Figure 7)		mV
V_{Sx}, V_{Sy}	input logic level HIGH threshold	on normal I²C-bus	[4]	700	650	-	(see Figure 8)		mV
dV_{Sx}/dT, dV_{Sy}/dT	temperature coefficient of input thresholds			-	−2	-	-	-	mV/K
V_{Rx}, V_{Ry}	input logic HIGH level	fraction of applied V_{CC}		$0.58V_{CC}$	-	-	$0.58V_{CC}$	-	V
V_{Rx}, V_{Ry}	input threshold	fraction of applied V_{CC}		-	$0.5V_{CC}$	-	-	-	V
V_{Rx}, V_{Ry}	input logic LOW level	fraction of applied V_{CC}		-	-	$0.42V_{CC}$	-	$0.42V_{CC}$	V
Logic level threshold difference									
V_{Sx}, V_{Sy}	input/output logic level difference	V_{Sx} output LOW at 0.2 mA − V_{Sx} input HIGH maximum	[2]	50	85	-	50	-	mV
Thermal resistance									
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board	SOT96-1 (SO8); average lead temperature at board interface		-	127	-	-	-	K/W
Bus release on V_{CC} failure									
V_{Sx}, V_{Sy}, V_{Tx}, V_{Ty}	V_{CC} voltage at which all buses are guaranteed to be released			-	-	1	(see Figure 9)		V
dV/dT	temperature coefficient of guaranteed release voltage			-	−4	-	-	-	mV/K
Buffer response time [5]									
$T_{fall\ delay}$ V_{Sx} to V_{Tx}, V_{Sy} to V_{Ty}	buffer time delay on **falling** input between V_{Sx} = input switching threshold, and V_{Tx} output falling 50 %	R_{Tx} pull-up = 160 Ω; no capacitive load; V_{CC} = 5 V		-	70	-	-	-	ns
$T_{rise\ delay}$ V_{Sx} to V_{Tx}, V_{Sy} to V_{Ty}	buffer time delay on **rising** input between V_{Sx} = input switching threshold, and V_{Tx} output reaching 50 % V_{CC}	R_{Tx} pull-up = 160 Ω; no capacitive load; V_{CC} = 5 V		-	90	-	-	-	ns

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Table 5: **Characteristics** …continued

T_{amb} = +25 °C; voltages are specified with respect to GND with V_{CC} = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = +25 °C			T_{amb} = −40 °C to +125 °C [1]		Unit
			Min	**Typ**	**Max**	**Min**	**Max**	
$T_{fall\ delay}$ V_{Rx} to V_{Sx}, V_{Ry} to V_{Sy}	buffer time delay on **falling** input between V_{Rx} = input switching threshold, and V_{Sx} output falling 50 %	R_{Sx} pull-up = 1500 Ω; no capacitive load; V_{CC} = 5 V	-	250	-	-	-	ns
$T_{rise\ delay}$ V_{Rx} to V_{Sx}, V_{Ry} to V_{Sy}	buffer time delay on **rising** input between V_{Rx} = input switching threshold, and V_{Sx} output reaching 50 % V_{CC}	R_{Sx} pull-up = 1500 Ω; no capacitive load; V_{CC} = 5 V	-	270	-	-	-	ns
Input capacitance								
C_i	input capacitance	effective input capacitance of any signal pin measured by incremental bus rise times	-	-	7	-	7	pF

[1] Limit data for +125 °C applies to P82B96TD/S410 version. It is guaranteed by design/characterization, but not by 100 % test.

[2] The minimum value requirement for pull-up current, 200 µA, guarantees that the minimum value for V_{Sx} output LOW will always exceed the minimum V_{Sx} input HIGH level to eliminate any possibility of latching. The specified difference is guaranteed by design within any IC. While the tolerances on absolute levels allow a small probability the LOW from one Sx output is recognized by an Sx input of another P82B96, this has no consequences for normal applications. In any design the Sx pins of different ICs should never be linked because the resulting system would be very susceptible to induced noise and would not support all I2C-bus operating modes.

[3] The output logic LOW depends on the sink current. For scaling, see *Application Note AN255*.

[4] The input logic threshold is independent of the supply voltage.

[5] The fall time of V_{Tx} from 5 V to 2.5 V in the test is approximately 15 ns.
The fall time of V_{Sx} from 5 V to 2.5 V in the test is approximately 50 ns.
The rise time of V_{Tx} from 0 V to 2.5 V in the test is approximately 20 ns.
The rise time of V_{Sx} from 0.9 V to 2.5 V in the test is approximately 70 ns.
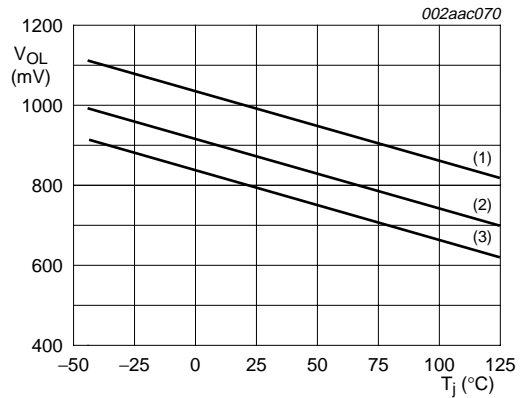
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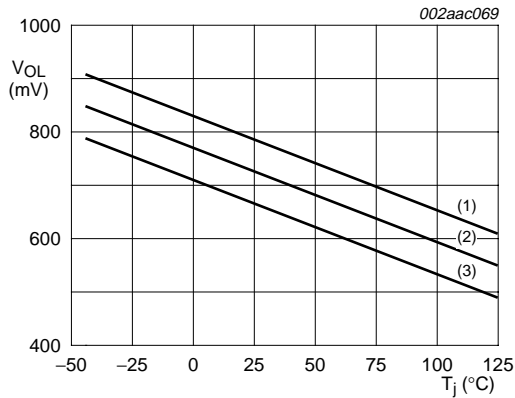
V_{OL} at Sx typical and limits over temperature

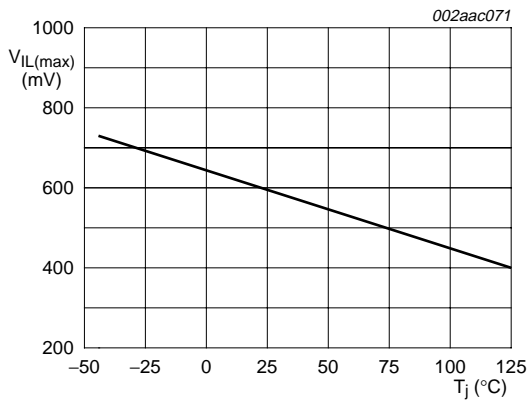(1) Maximum

(2) Typical

(3) Minimum

Fig 5. V_{OL} **as a function of junction temperature (I_{OL} = 0.2 mA)**

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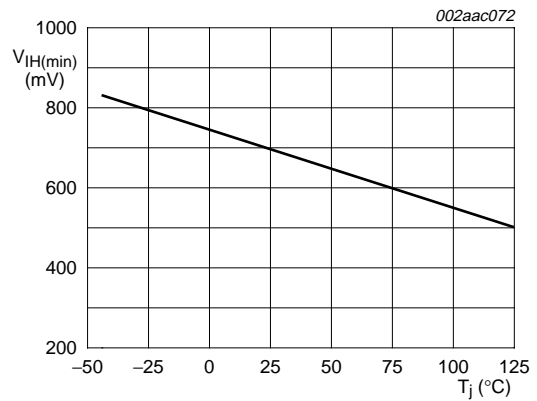V_{OL} at Sx typical and limits over temperature

(1) Maximum

(2) Typical

(3) Minimum

Fig 6. V_{OL} **as a function of junction temperature (I_{OL} = 3 mA)**

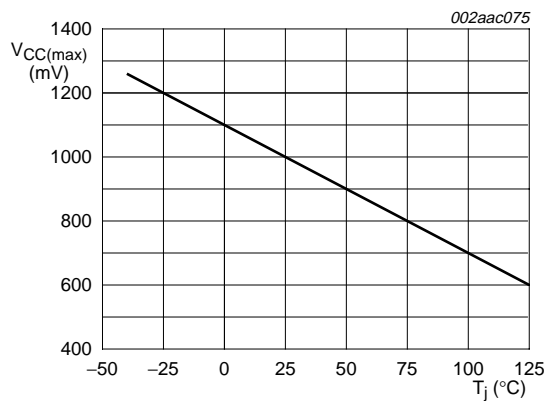*002aac071*

$V_{IL(max)}$ at Sx changes over temperature range

Fig 7. $V_{IL(max)}$ **as a function of junction temperature**

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$V_{IH(min)}$ at Sx changes over temperature range.

Fig 8. $V_{IH(min)}$ **as a function of junction temperature**

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Fig 9. $V_{CC(max)}$ **that guarantees bus release limit over temperature**

10. Application information

Refer to *AN460* and *AN255* for more application detail.

Fig 10. Interfacing an 'I2C' type of bus with different logic levels

Fig 11. Galvanic isolation of I2C-bus nodes via opto-couplers
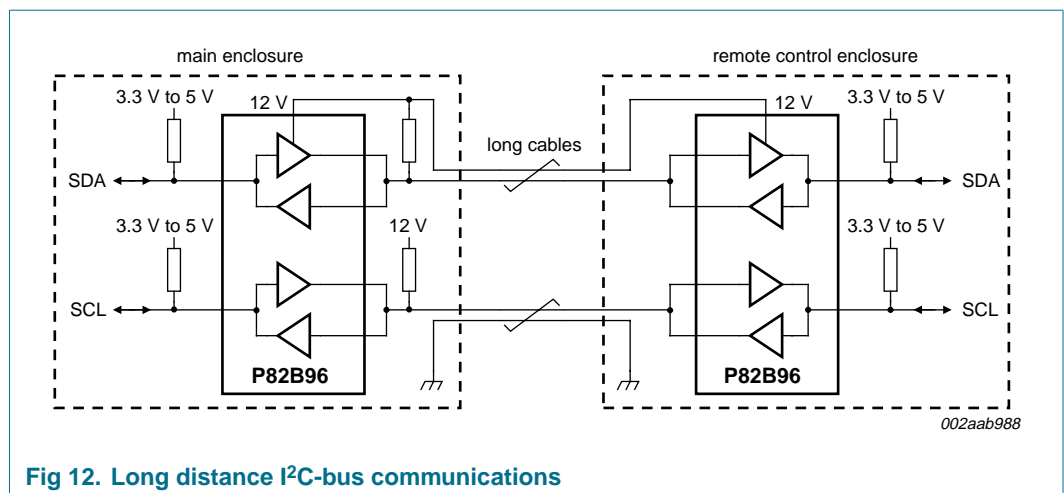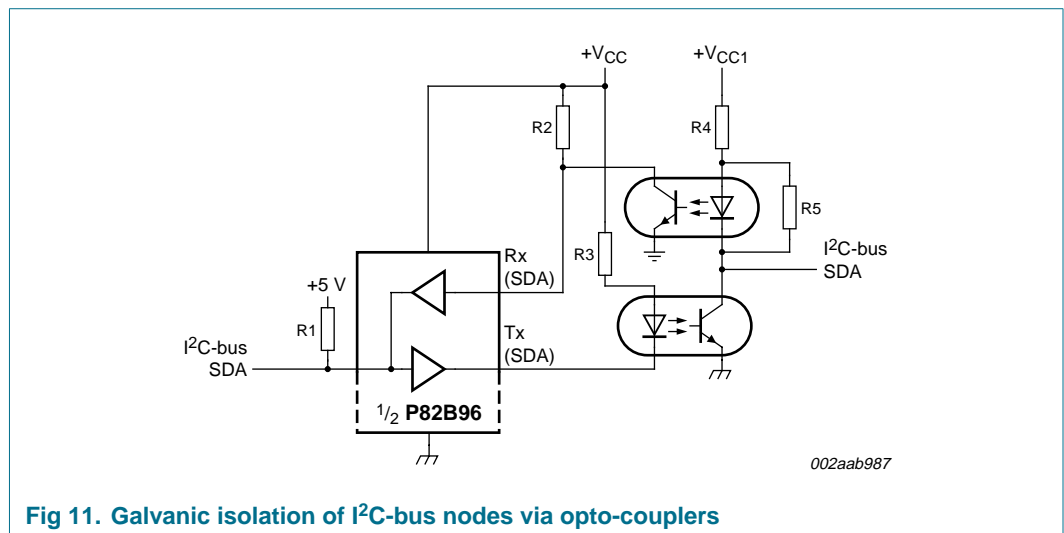

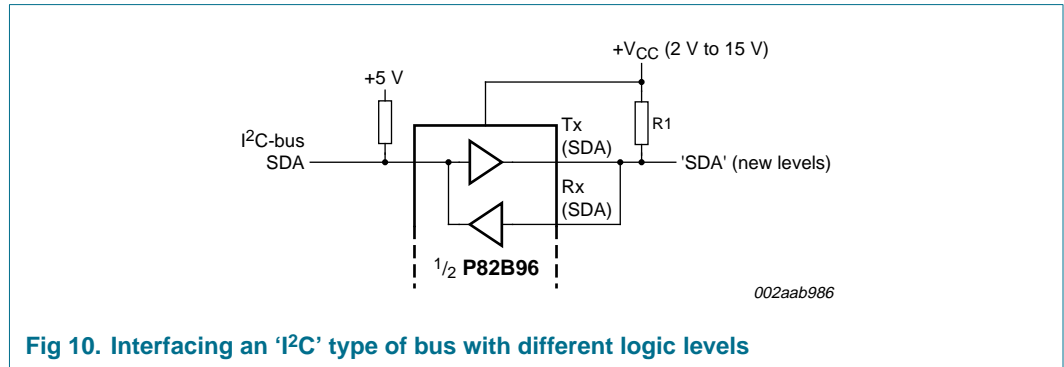**Fig 12. Long distance I2C-bus communications**

Figure 13 shows how a master I^{2}C-bus can be protected against short circuits or failures in applications that involve plug and socket connections and long cables that may become damaged. A simple circuit is added to monitor the SDA bus, and if its LOW time exceeds the design value, then the master bus is disconnected. P82B96 will free all its I/Os if its supply is removed, so one option is to connect its V_{CC} to the output of a logic gate from, say, the 74LVC family. The SDA and SCL lines could be timed and V_{CC} disabled via the gate if one or other lines exceeds a design value of 'LOW' period as in *Figure 28 of AN255*. If the supply voltage of logic gates restricts the choice of V_{CC} supply then the low-cost discrete circuit in Figure 13 can be used. If the SDA line is held LOW, the 100 nF capacitor will charge and the Ry input will be pulled towards V_{CC}. When it exceeds $0.5V_{CC}$ the Ry input will set the Sy input HIGH, which in practice means simply releasing it.

In this example the SCL line is made unidirectional by tying the Rx pin to V_{CC}. The state of the buffered SCL line cannot affect the master clock line which is allowed when clock-stretching is not required. It is simple to add an additional transistor or diode to control the Rx input in the same way as Ry when necessary. The +V cable drive can be any voltage up to 15 V and the bus may be run at a lower impedance by selecting pull-up resistors for a static sink current up to 30 mA. V_{CC1} and V_{CC2} may be chosen to suit the connected devices. Because DDC uses relatively low speeds (<100 kHz), the cable length is not restricted to 20 m by the I^{2}C-bus signalling, but it may be limited by the video signalling.
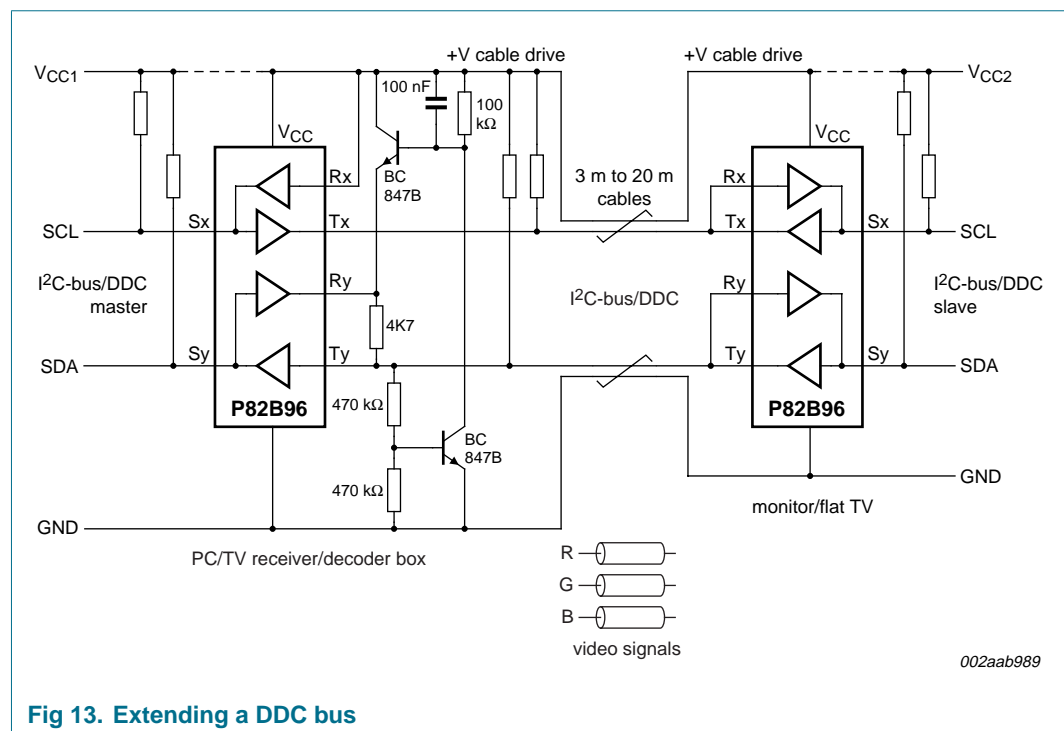

Fig 13. Extending a DDC bus

Figure 14 shows that P82B96 can achieve high clock rates over long cables. While calculating with lumped wiring capacitance yields reasonable approximations to actual timing, even 25 meters of cable is better treated using transmission line theory. Flat ribbon cables connected as shown, with the bus signals on the outer edge, will have a characteristic impedance in the range 100 Ω to 200 Ω. For simplicity they cannot be terminated in their characteristic impedance but a practical compromise is to use the minimum pull-up allowed for P82B96 and place half this termination at each end of the cable. When each pull-up is below 330 Ω, the rising edge waveforms have their first voltage 'step' level above the logic threshold at Rx and cable timing calculations can be based on the fast rise/fall times of resistive loading plus simple one-way propagation delays. When the pull-up is larger, but below 750 Ω, the threshold at Rx will be crossed after one signal reflection. So at the sending end it is crossed after 2 times the one-way propagation delay and at the receiving end after 3 times that propagation delay. For flat cables with partial plastic dielectric insulation (by using outer cores) the one-way propagation delays will be about 5 ns per meter. The 10 % to 90 % rise and fall times on the cable will be between 20 ns and 50 ns, so their delay contributions are small. There will be ringing on falling edges that can be damped, if required, by using Schottky diodes as shown.

When the Master SCL HIGH and LOW periods can be programmed separately, for example using control registers I2SCLH and I2SCLL of 89LPC932, the timings can allow for bus delays. The LOW period should be programmed to achieve the minimum 1300 ns plus the net delay in the slave's response data signal caused by bus and buffer delays. The longest data delay is the sum of the delay of the falling edge of SCL from master to slave and the delay of the rising edge of SDA from slave data to master. Because the buffer will 'stretch' the programmed SCL LOW period, the actual SCL frequency will be lower than calculated from the programmed clock periods. In the example for 25 meters the clock is stretched 400 ns, the falling edge of SCL is delayed 490 ns and the SDA rising edge is delayed 570 ns. The required additional LOW period is
(490 ns + 570 ns) = 1060 ns and the I^2C-bus specifications already include an allowance for a worst case bus rise time 0 % to 70 % of 425 ns. (The bus rise time can be 300 ns 30 % to 70 %, which means it can be 425 ns 0 % to 70 %. The 25 meter cable delay times as quoted already include all rise and fall times.) Therefore, the microcontroller only needs to be programmed with an additional (1060 ns – 400 ns – 425 ns) = 235 ns, making a total programmed LOW period 1535 ns. The programmed LOW will the be stretched by 400 ns to yield an actual bus LOW time of 1935 ns, which, allowing the minimum HIGH period of 600 ns, yields a cycle period of 2535 ns or 394 kHz.

Note that in both the 100 meter and 250 meter examples, the capacitive loading on the I^2C-buses at each end is within the maximum allowed Standard mode loading of 400 pF, but exceeds the Fast mode limit. This is an example of a 'hybrid' mode because it relies on the response delays of Fast mode parts but uses (allowable) Standard mode bus loadings with rise times that contribute significantly to the system delays. The cables cause large propagation delays, so these systems need to operate well below the 400 kHz limit, but illustrate how they can still exceed the 100 kHz limit provided all parts are capable of Fast mode operation. The fastest example illustrates how the 400 kHz limit can be exceeded, provided master and slave parts have delay specifications smaller than the maximum allowed. Many Philips slaves have delays shorter than 600 ns, but none have that guaranteed.
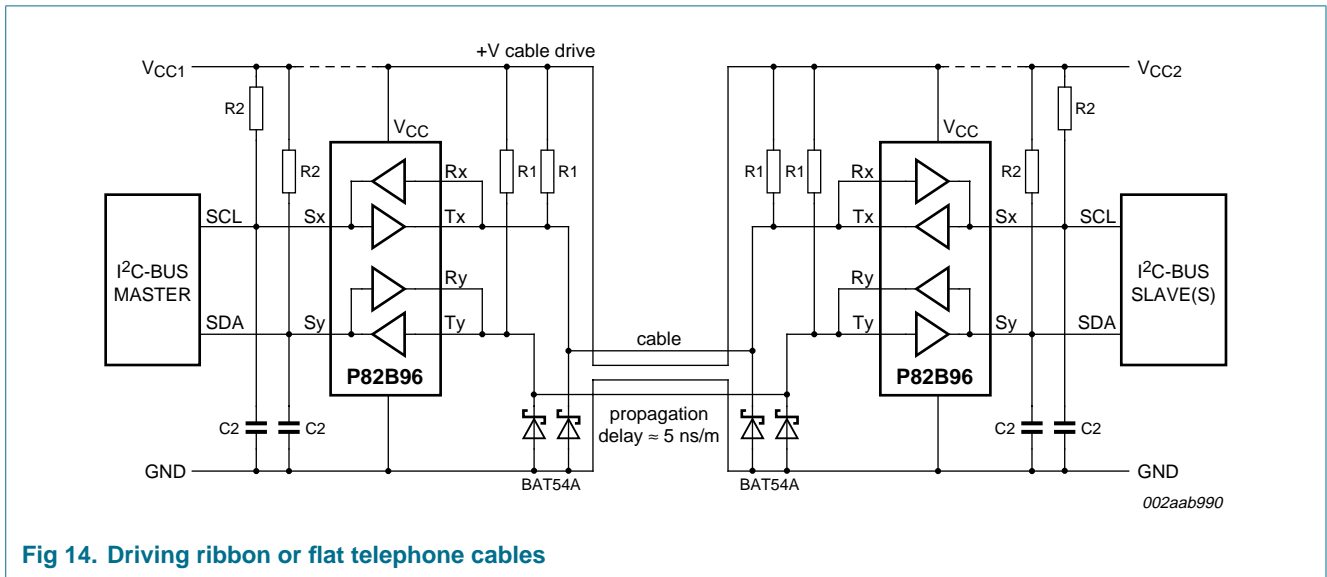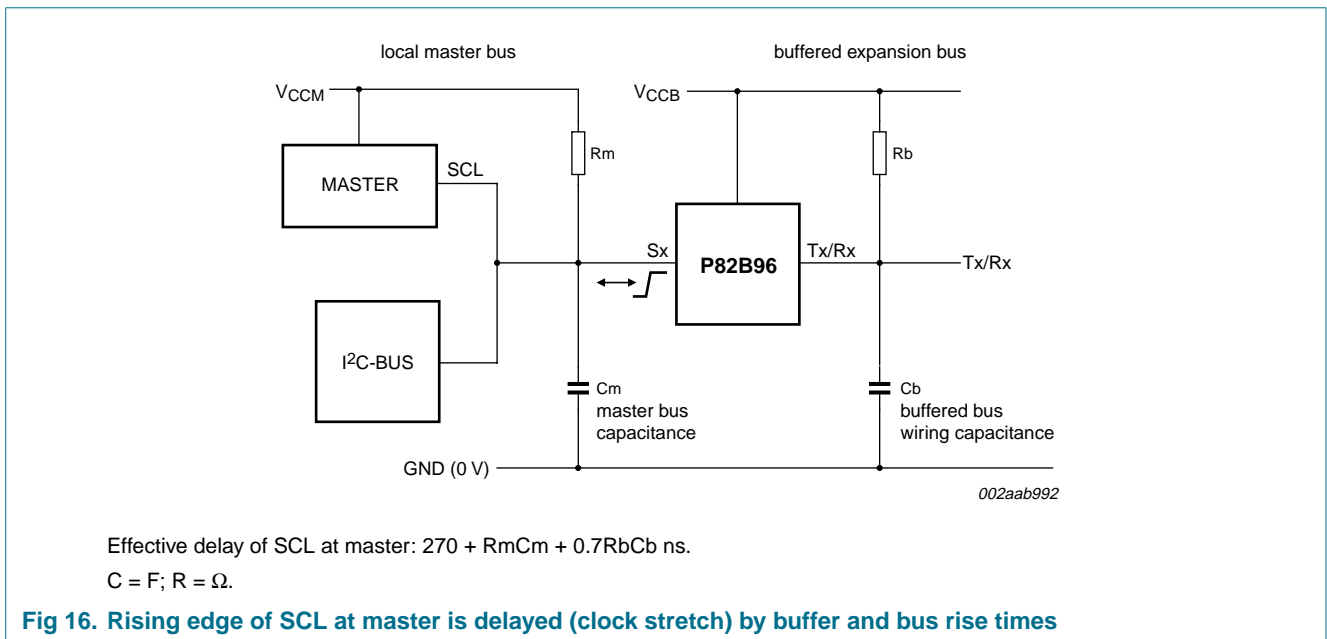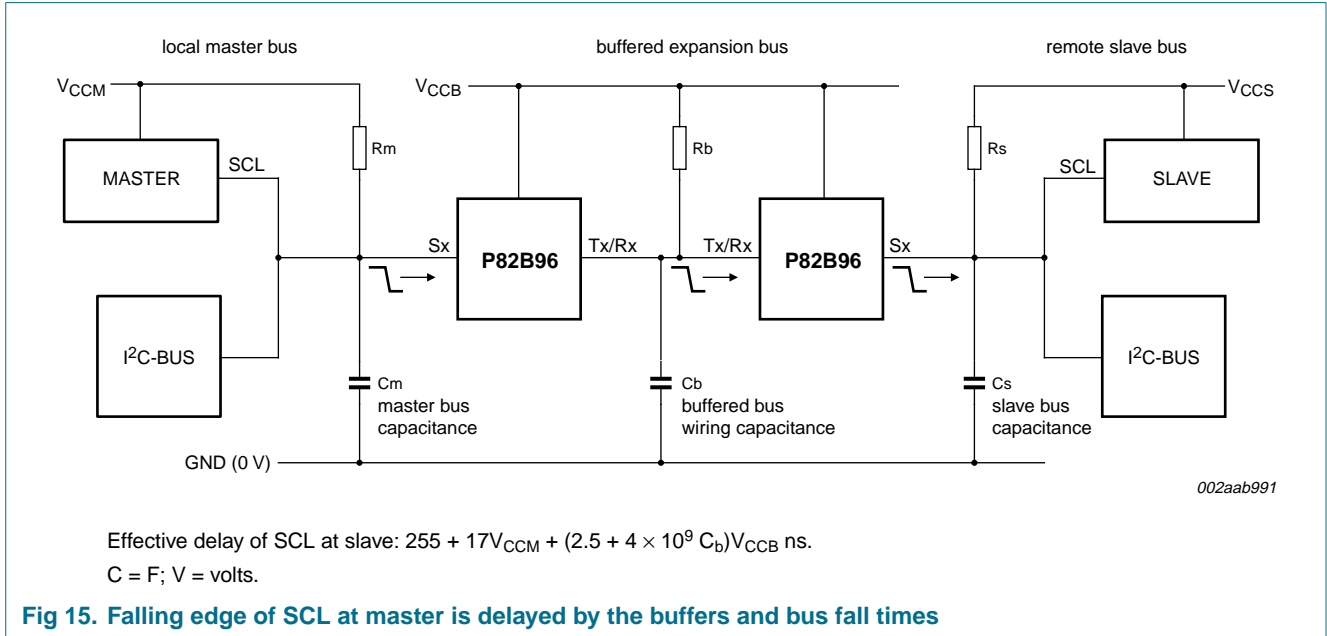
Fig 14. Driving ribbon or flat telephone cables

Table 6: **Examples of bus capability**
Refer to Figure 14.

+V_{CC1}	+V cable	+V_{CC2}	R1 (Ω)	R2 (Ω)	C2 (pF)	Cable length	Cable capacitance	Cable delay	Set master nominal SCL		Effective bus clock speed	Maximum slave response delay
									HIGH period	LOW period		
5 V	12 V	5 V	750	2.2 k	400	250 m	n/a (delay based)	1.25 µs	600 ns	4000 ns	120 kHz	Normal spec. 400 kHz parts
5 V	12 V	5 V	750	2.2 k	220	100 m	n/a (delay based)	500 ns	600 ns	2600 ns	185 kHz	Normal spec. 400 kHz parts
3.3 V	5 V	3.3 V	330	1 k	220	25 m	1 nF	125 ns	600 ns	1500 ns	390 kHz	Normal spec. 400 kHz parts
3.3 V	5 V	3.3 V	330	1 k	100	3 m	120 pF	15 ns	600 ns	1000 ns	500 kHz	600 ns

10.1 Calculating system delays and bus clock frequency for a Fast mode system

Effective delay of SCL at slave: $255 + 17V_{CCM} + (2.5 + 4 \times 10^9 \, C_b)V_{CCB}$ ns.

$C = F$; $V = $ volts.

Fig 15. Falling edge of SCL at master is delayed by the buffers and bus fall times

Effective delay of SCL at master: $270 + RmCm + 0.7RbCb$ ns.

$C = F$; $R = \Omega$.

Fig 16. Rising edge of SCL at master is delayed (clock stretch) by buffer and bus rise times

Effective delay of SDA at master = $270 + 0.2RsCs + 0.7(RbCb + RmCm)$ ns.

$C = F; R = \Omega$.

Fig 17. Rising edge of SDA at slave is delayed by the buffers and bus rise times
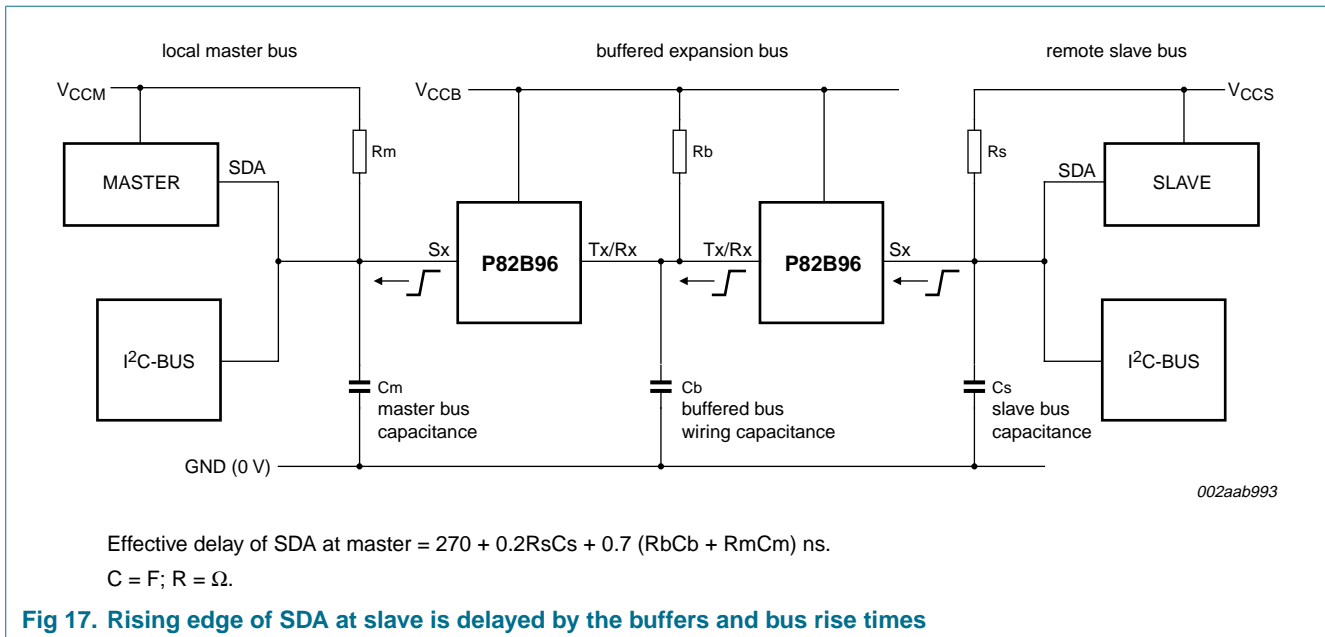
Figure 15, Figure 16, and Figure 17 show the P82B96 used to drive extended bus wiring, with relatively large capacitance, linking two Fast mode I^2C-bus nodes. It includes simplified expressions for making the relevant timing calculations for 3.3 V or 5 V operation. Because the buffers and the wiring introduce timing delays, it may be necessary to decrease the nominal SCL frequency below 400 kHz. In most cases the actual bus frequency will be lower than the nominal Master timing due to bit-wise stretching of the clock periods.

The delay factors involved in calculation of the allowed bus speed are:

A — The propagation delay of the master signal through the buffers and wiring to the slave. The important delay is that of the falling edge of SCL because this edge 'requests' the data or acknowledge from a slave. See Figure 15.

B — The effective stretching of the nominal LOW period of SCL at the master caused by the buffer and bus rise times. See Figure 16.

C — The propagation delay of the slave's response signal through the buffers and wiring back to the master. The important delay is that of a rising edge in the SDA signal. Rising edges are always slower and are therefore delayed by a longer time than falling edges. (The rising edges are limited by the passive pull-up while falling edges are actively driven). See Figure 17.

The timing requirement in any I^2C-bus system is that a slave's data response (which is provided in response to a falling edge of SCL) must be received at the master before the end of the corresponding LOW period of SCL as appears on the bus wiring at the master. Since all slaves will, as a minimum, satisfy the worst case timing requirements of a 400 kHz part, they must provide their response within the minimum allowed clock LOW period of 1300 ns. Therefore in systems that introduce additional delays it is only necessary to extend that minimum clock LOW period by any 'effective' delay of the slave's response. The effective delay of the slaves response equals the total delays in SCL falling

edge from the master reaching the slave (Figure 15) minus the effective delay (stretch) of the SCL rising edge (Figure 16) plus total delays in the slave's response data, carried on SDA, reaching the master (Figure 17).

The master microcontroller should be programmed to produce a nominal SCL LOW period = $(1300 + A - B + C)$ ns, and should be programmed to produce the nominal minimum SCL HIGH period of 600 ns. Then a check should be made to ensure the cycle time is not shorter than the minimum 2500 ns. If found necessary, just increase either clock period.

Due to clock stretching, the SCL cycle time will always be longer than $(600 + 1300 + A + C)$ ns.

Example:

The master bus has an RmCm product of 100 ns and $V_{CCM} = 5$ V.

The buffered bus has a capacitance of 1 nF and a pull-up resistor of 160 Ω to 5 V giving an RbCb product of 160 ns. The slave bus also has an RsCs product of 100 ns.

The microcontroller LOW period should be programmed to $\geq (1300 + 372.5 - 482 + 472)$ ns, that is ≥ 1662.5 ns.

Its HIGH period may be programmed to the minimum 600 ns.

The nominal microcontroller clock period will be $\geq (1662.5 + 600)$ ns = 2262.5 ns, equivalent to a frequency of 442 kHz.

The actual bus clock period, including the 482 ns clock stretch effect, will be below (nominal + stretch) = $(2262.5 + 482)$ ns or ≥ 2745 ns, equivalent to an allowable frequency of 364 kHz.
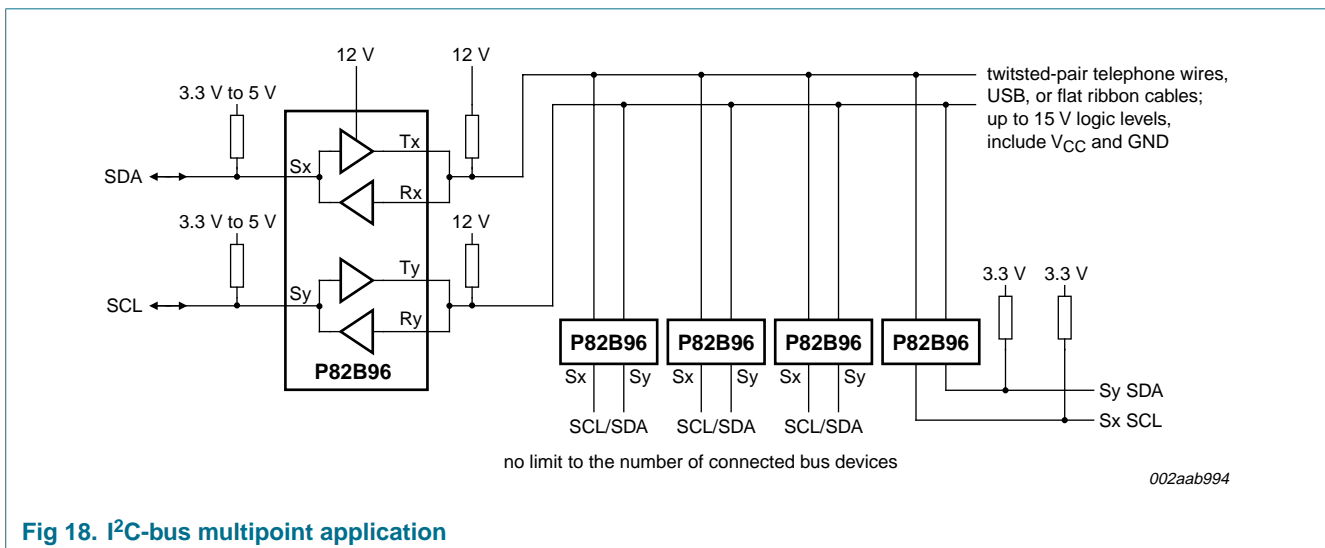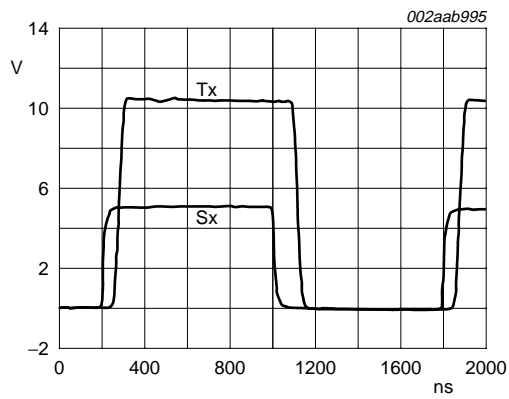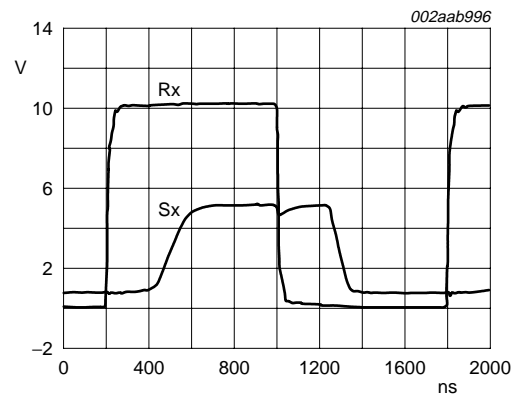

Fig 18. I²C-bus multipoint application

frequency = 624 kHz

Fig 19. Propagation Sx to Tx (Sx pull-up to 5 V; Tx pull-up to V_{CC} = 10 V)

ch1 frequency = 624 kHz

Fig 20. Propagation Rx to Sx (Sx pull-up to 5 V; Rx pull-up to V_{CC} = 10 V)

11. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil)
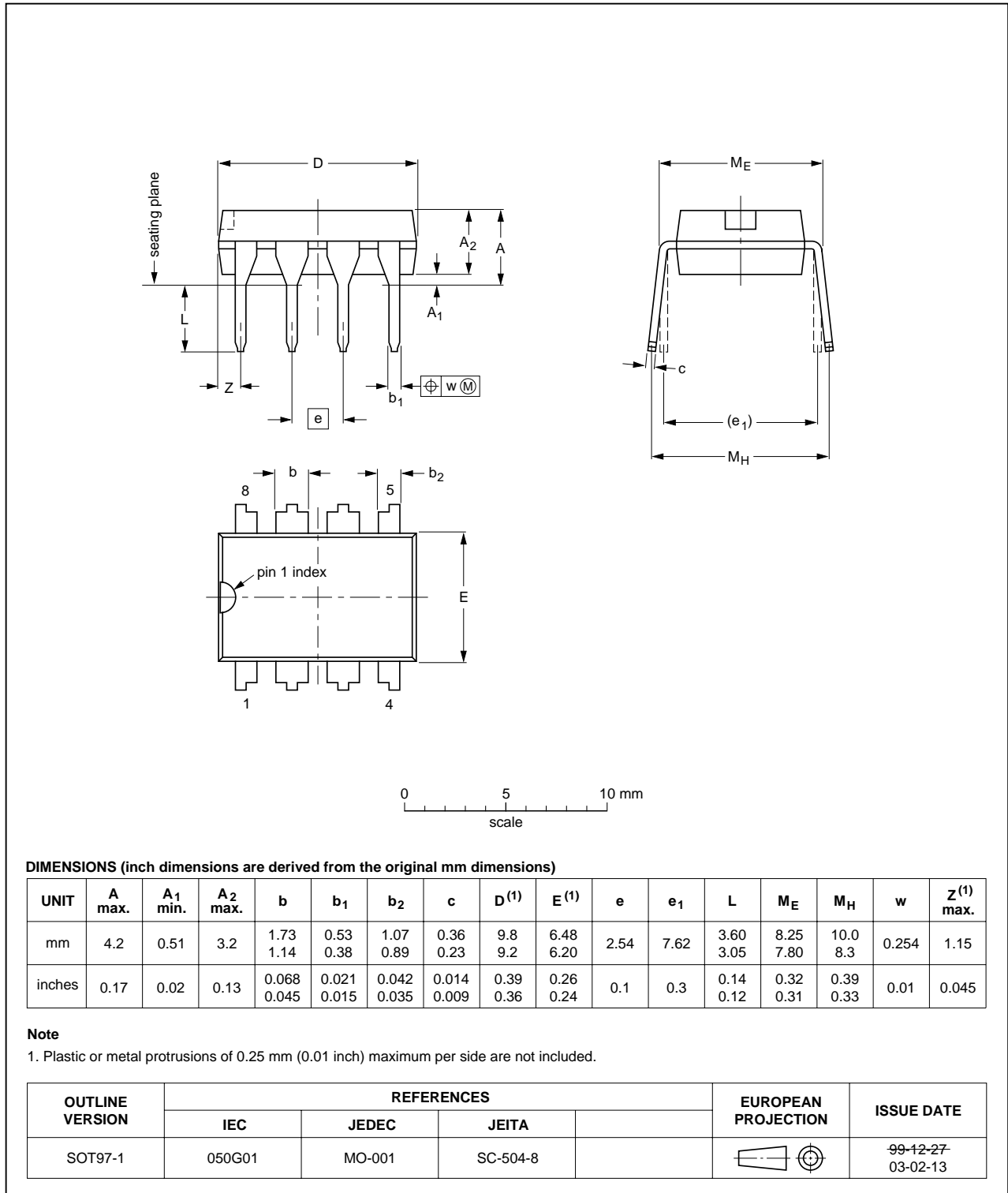
SOT97-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D[1]	E[1]	e	e₁	L	ME	MH	w	Z[1] max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 21. Package outline SOT97-1 (DIP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[1]	E[2]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

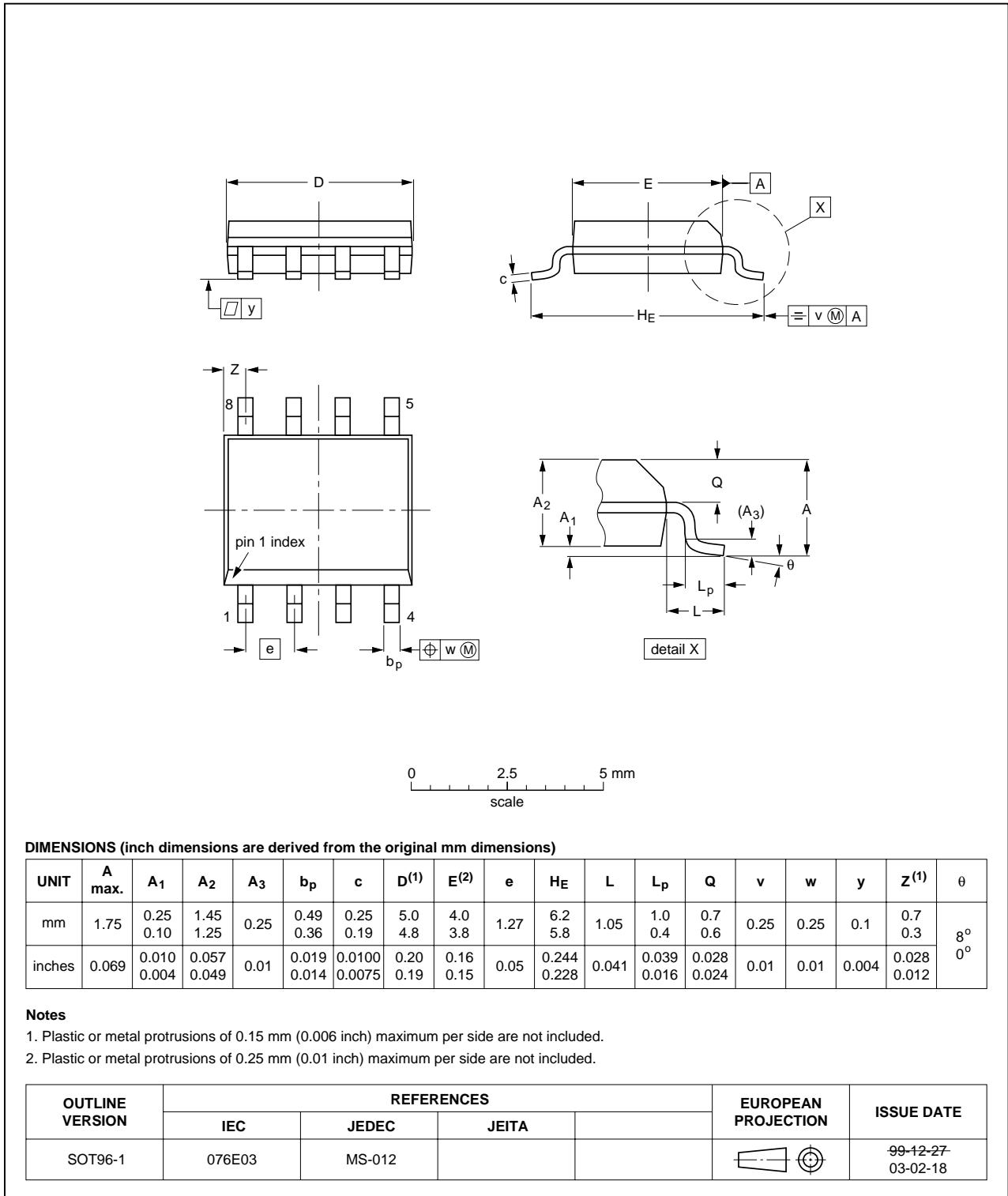| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				99-12-27 03-02-18

Fig 22. Package outline SOT96-1 (SO8)

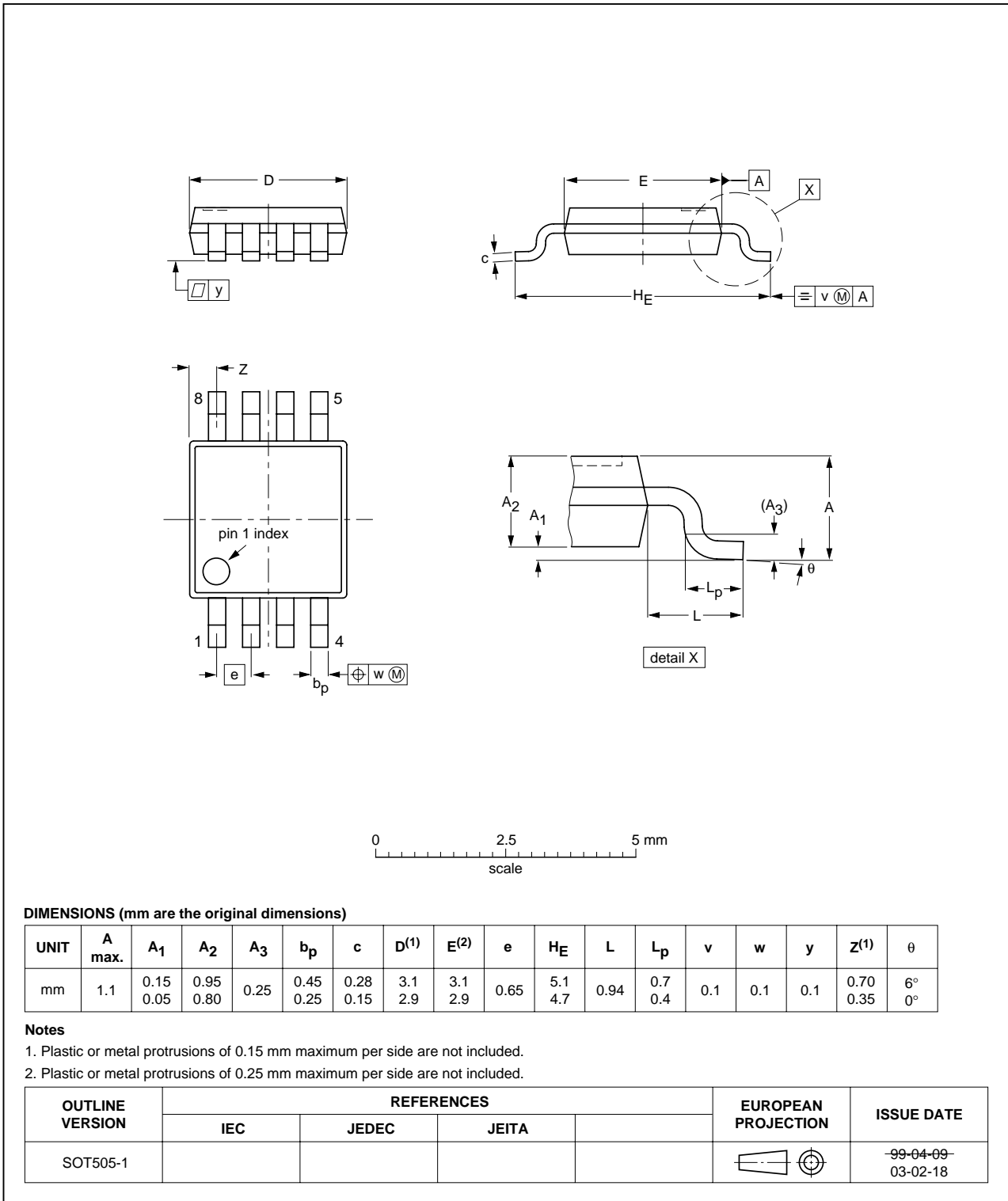**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm**   **SOT505-1**

detail X

0   2.5   5 mm

scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(2)}$	e	H$_E$	L	L$_p$	v	w	y	Z$^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						99-04-09 03-02-18

Fig 23. Package outline SOT505-1 (TSSOP8)

12. Soldering

12.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

12.2 Through-hole mount packages

12.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

12.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

12.3 Surface mount packages

12.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages

- for packages with a thickness $\geq$ 2.5 mm
- for packages with a thickness < 2.5 mm and a volume $\geq$ 350 mm^3 so called thick/large packages.

- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.4 Package related soldering information

Table 7:   Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package [1]	Soldering method		
		Wave	**Reflow** [2]	**Dipping**
Through-hole mount	CPGA, HCPGA	suitable	-	-
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable [3]	-	suitable
Through-hole-surface mount	PMFP [4]	not suitable	not suitable	-
Surface mount	BGA, HTSSON..T [5], LBGA, LFBGA, SQFP, SSOP..T [5], TFBGA, VFBGA, XSON	not suitable	suitable	-
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [6]	suitable	-
	PLCC [7], SO, SOJ	suitable	suitable	-
	LQFP, QFP, TQFP	not recommended [7] [8]	suitable	-
	SSOP, TSSOP, VSO, VSSOP	not recommended [9]	suitable	-
	CWQCCN..L [10], WQCCN..L [10]	not suitable	not suitable	-

[1]   For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2]   All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3]   For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4]   Hot bar soldering or manual soldering is suitable for PMFP packages.

[5]   These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C $\pm$ 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6]   These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7]   If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8]   Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9]   Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

13. Abbreviations

Table 8:   Abbreviations

Acronym	Description
CDM	Charged Device Model
DDC	Display Data Channel
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I^{2}C-bus	Inter IC bus
MM	Machine Model
SMBus	System Management Bus

14. Revision history

Table 9:   Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
P82B96_5	20060127	Product data sheet	-	-	P82B96_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 1 "Ordering information": added Type number P82B96TD/S410 • Table 4 "Limiting values": – added parameter T_j, junction temperature – changed symbol "V_{bus}" to "V_{Sx}" – corrected symbol "R_{tot}" to "P_{tot}" • Table 5 "Characteristics": – added sub-section "Resistance" – changed column heading "+85 °C" to "T_{amb} = +25 °C" – added column for T_{amb} = −40 °C to +125 °C values – sub-section "Input logic switching threshold voltages", for values with condition "fraction of applied V_{CC}": changed from numeric voltage value to "(value)V_{CC}" • Added new Figure 5, Figure 6, Figure 7, Figure 8 and Figure 9				
P82B96_4	20040329	Product data	-	9397 750 12932	P82B96_3
P82B96_3	20030402	Product data	853-2241 29602 of 2003 Feb 28	9397 750 11351	P82B96_2
P82B96_2	20030226	Product data	853-2241 29410 of 2003 Jan 22	9397 750 11093	P82B96_1
P82B96_1	20010306	Product data	853-2241 25758 of 2001 Mar 06	9397 750 08122	-

P82B96_5

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15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1]   Please consult the most recently issued data sheet before initiating or completing a design.

[2]   The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3]   For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents