CY62148EV30
MoBL®

4-Mbit (512K x 8) Static RAM

Features

- **Very high speed: 45 ns**
  - **— Wide voltage range: 2.20V – 3.60V**
- **Pin-compatible with CY62148DV30**
- **Ultra-low standby power**
  - **— Typical standby current: 1μA**
  - **— Maximum standby current: 7μA**
- **Ultra low active power**
  - **— Typical active current: 2 mA @ f = 1 MHz**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in Pb-free 36-ball VFBGA, 32-pin TSOP II and 32-pin SOIC packages**

Functional Description[1]

The CY62148EV30 is a high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ($\overline{CE}$ HIGH).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

The CY62148EV30 is available in 36-ball VFBGA, 32-pin TSOP II and 32-pin SOIC Packages.
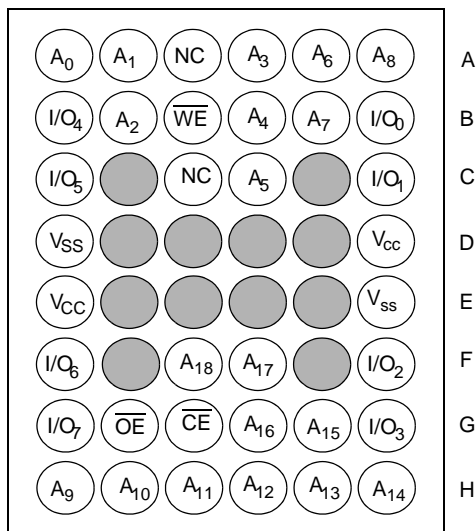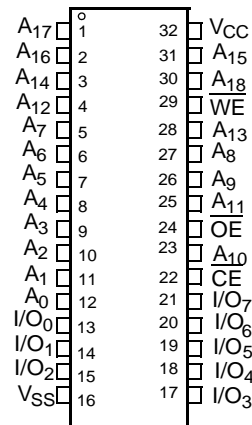
Logic Block Diagram
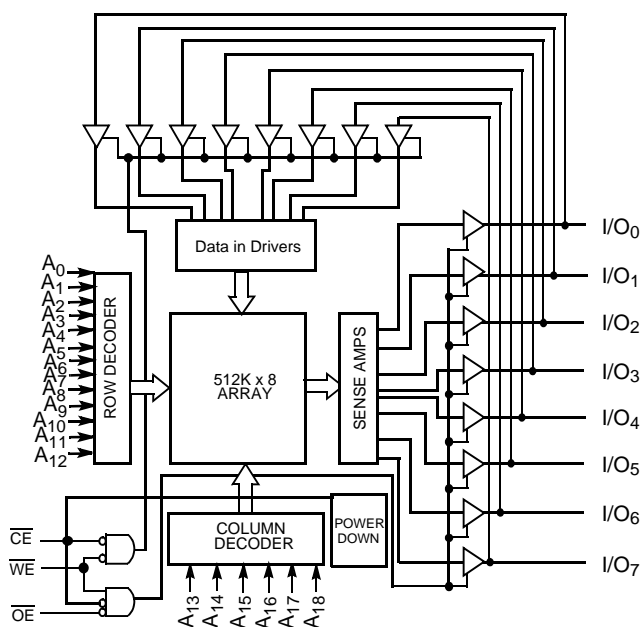
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

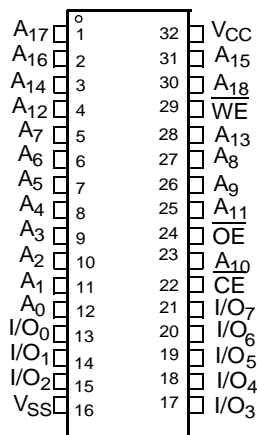## Pin Configuration[2]

36-ball VFBGA Pinout
Top View

	1	2	3	4	5	6	
A	A_0	A_1	NC	A_3	A_6	A_8	A
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0	B
C	I/O_5		NC	A_5		I/O_1	C
D	V_{SS}					V_{CC}	D
E	V_{CC}					V_{SS}	E
F	I/O_6		A_{18}	A_{17}		I/O_2	F
G	I/O_7	$\overline{OE}$	$\overline{CE}$	A_{16}	A_{15}	I/O_3	G
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	H

32-pin TSOP II Pinout
Top View

A_{17}	1	32	V_{CC}
A_{16}	2	31	A_{15}
A_{14}	3	30	A_{18}
A_{12}	4	29	$\overline{WE}$
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	$\overline{OE}$
A_2	10	23	A_{10}
A_1	11	22	$\overline{CE}$
A_0	12	21	I/O_7
I/O_0	13	20	I/O_6
I/O_1	14	19	I/O_5
I/O_2	15	18	I/O_4
V_{SS}	16	17	I/O_3

32-pin SOIC Pinout
Top View

A_{17}	1	32	V_{CC}
A_{16}	2	31	A_{15}
A_{14}	3	30	A_{18}
A_{12}	4	29	$\overline{WE}$
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	$\overline{OE}$
A_2	10	23	A_{10}
A_1	11	22	$\overline{CE}$
A_0	12	21	I/O_7
I/O_0	13	20	I/O_6
I/O_1	14	19	I/O_5
I/O_2	15	18	I/O_4
V_{SS}	16	17	I/O_3

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation				Standby I_{SB2} (uA)	
					Operating I_{CC} (mA)					
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[3]	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
CY62148EV30-45LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes:
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...55°C to +125°C

Supply Voltage to Ground
Potential .... –0.3V to $V_{CC(MAX)}$ + 0.3V

DC Voltage Applied to Outputs
in High-Z State[4,5]......................... –0.3V to $V_{CC(MAX)}$ + 0.3V

DC Input Voltage[4,5] .... –0.3V to $V_{CC(MAX)}$ + 0.3V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... > 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}[6]
CY62148EV30	Industrial	–40°C to +85°C	2.2V to 3.6V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		Min.	Typ.[3]	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V	2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V			0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70V			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3V	V
		V_{CC} = 2.7V to 3.6V		2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	V
		V_{CC} = 2.7V to 3.6V		–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels		15	20	mA
		f = 1 MHz			2	2.5	mA
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.2V, V_{IN}≥V_{CC}–0.2V, V_{IN}≤0.2V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC}=3.60V			1	7	μA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V			1	7	μA

The table header spans: CY62148EV30-45 over Min. / Typ.[3] / Max.

Notes:
4. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC}+0.75V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{cc}(min) and 200 μs wait time after V_{cc} stabilization.

Capacitance (for all packages)[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = V_{CC(typ.)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	SOIC Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[7]	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	75.13	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[7]		8.86	8.95	22	°C/W

AC Test Loads and Waveforms
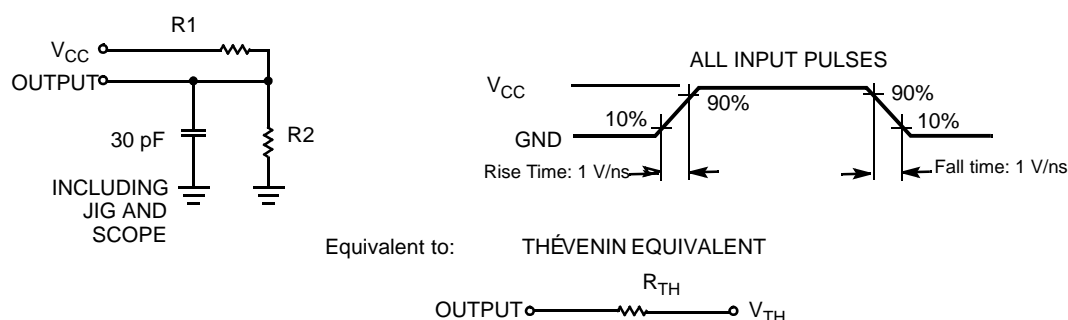
Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5V$, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.8	7	μA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0			ns
t_R[8]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform
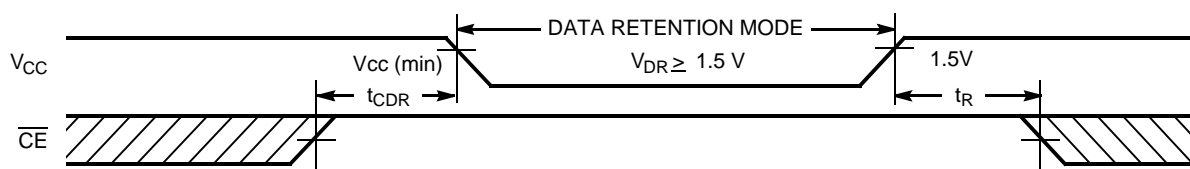
Notes:
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100\ \mu s$ or stable at $V_{CC(min.)} \geq 100\ \mu s$.

Switching Characteristics (Over the Operating Range)[9]

Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10,11]		18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[10, 11]		18	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-up		45	ns
Write Cycle[12]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		ns
t_{AW}	Address Set-up to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{SD}	Data Set-up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10, 11]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[10]	10		ns

Switching Waveforms

### Read Cycle No. 1 (Address Transition Controlled)[13, 14]
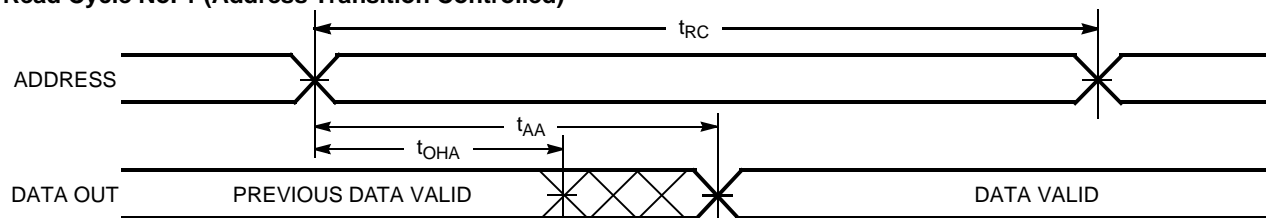
Notes:
9. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled) [14, 15]
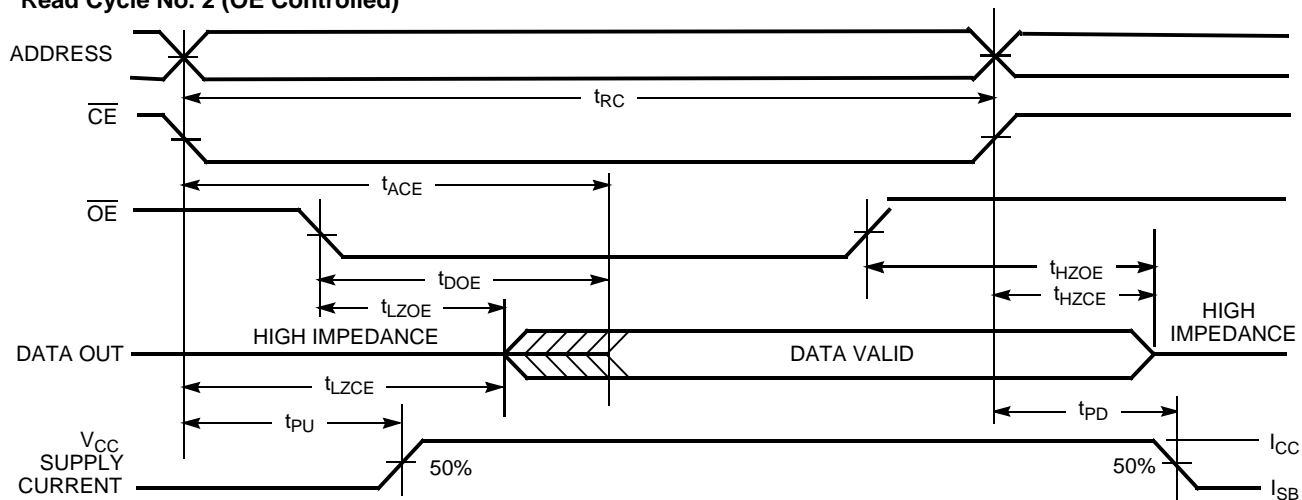
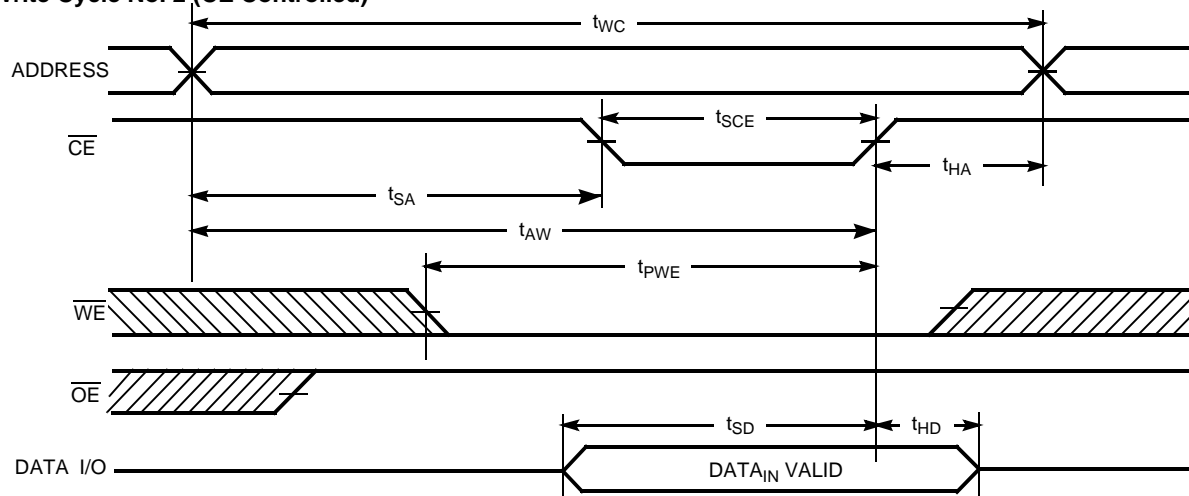### Write Cycle No. 1 ($\overline{WE}$ Controlled) [16, 18]
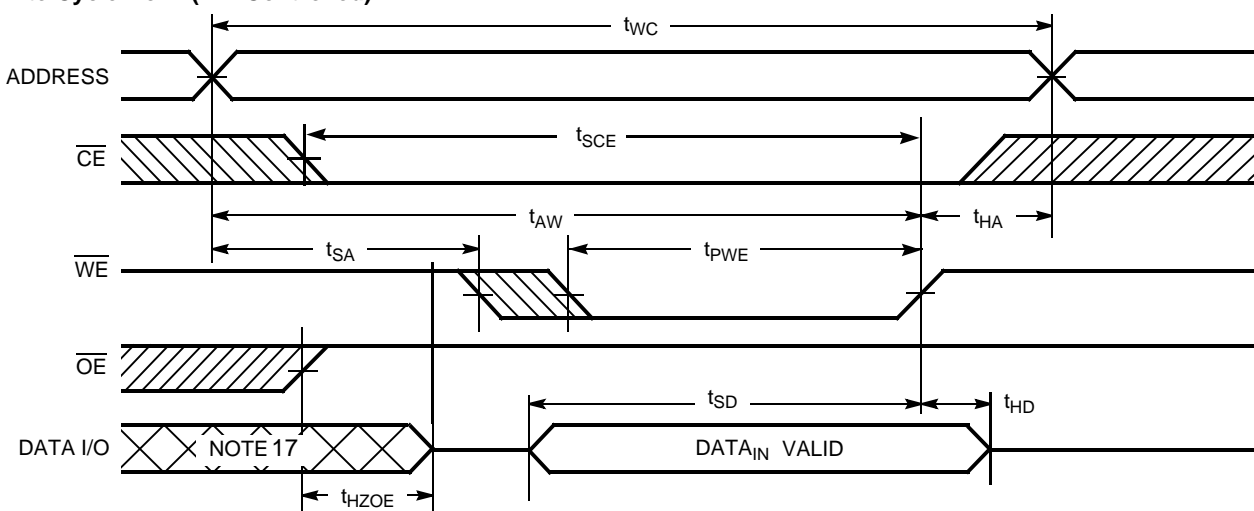
Notes:
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. During this period, the I/Os are in output state and input signals should not be applied.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled)[16, 18]

Write Cycle No. 3 (WE Controlled, OE LOW) [18]
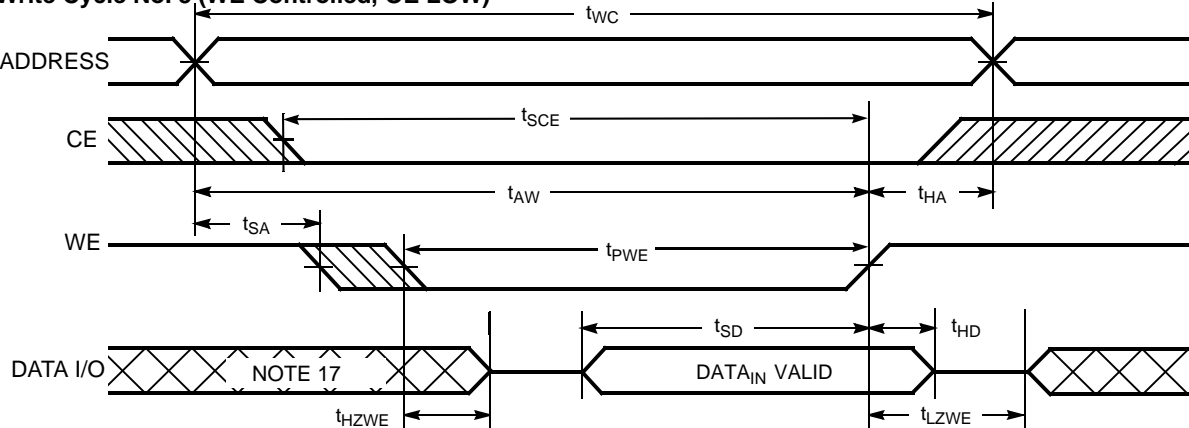
Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out (I/O$_0$-I/O$_7$)	Read	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (Icc)
L	L	X	Data in (I/O$_0$-I/O$_7$)	Write	Active (Icc)

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148EV30LL-45BVXI	51-85149	36-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62148EV30LL-45ZSXI	51-85095	32-pin Thin Small Outline Package II (Pb-free)	
	CY62148EV30LL-45SXI	51-85081	32-pin Small Outline Integrated Circuit (Pb-free)	

Please contact your local Cypress sales representative for availability of other parts
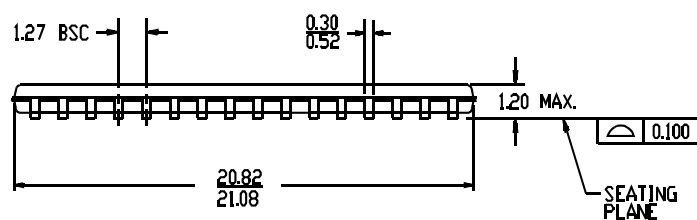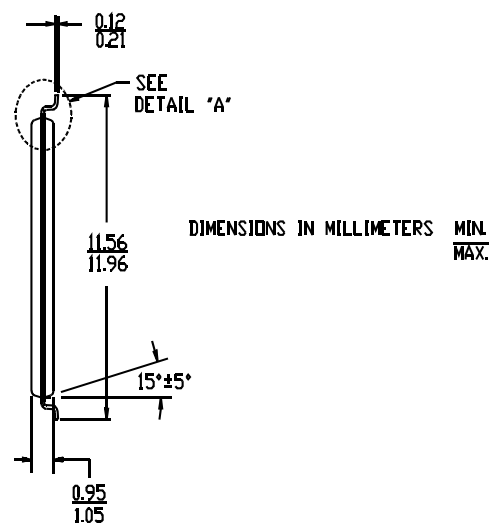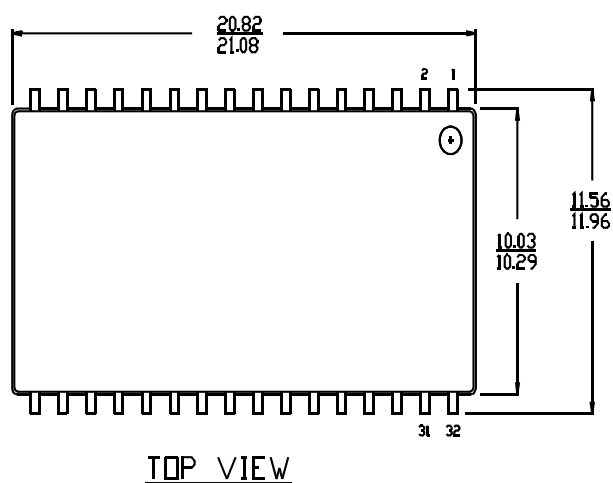
Package Diagrams

36-ball VFBGA (6 x 8 x 1 mm) (51- 85149)

51-85149-*C
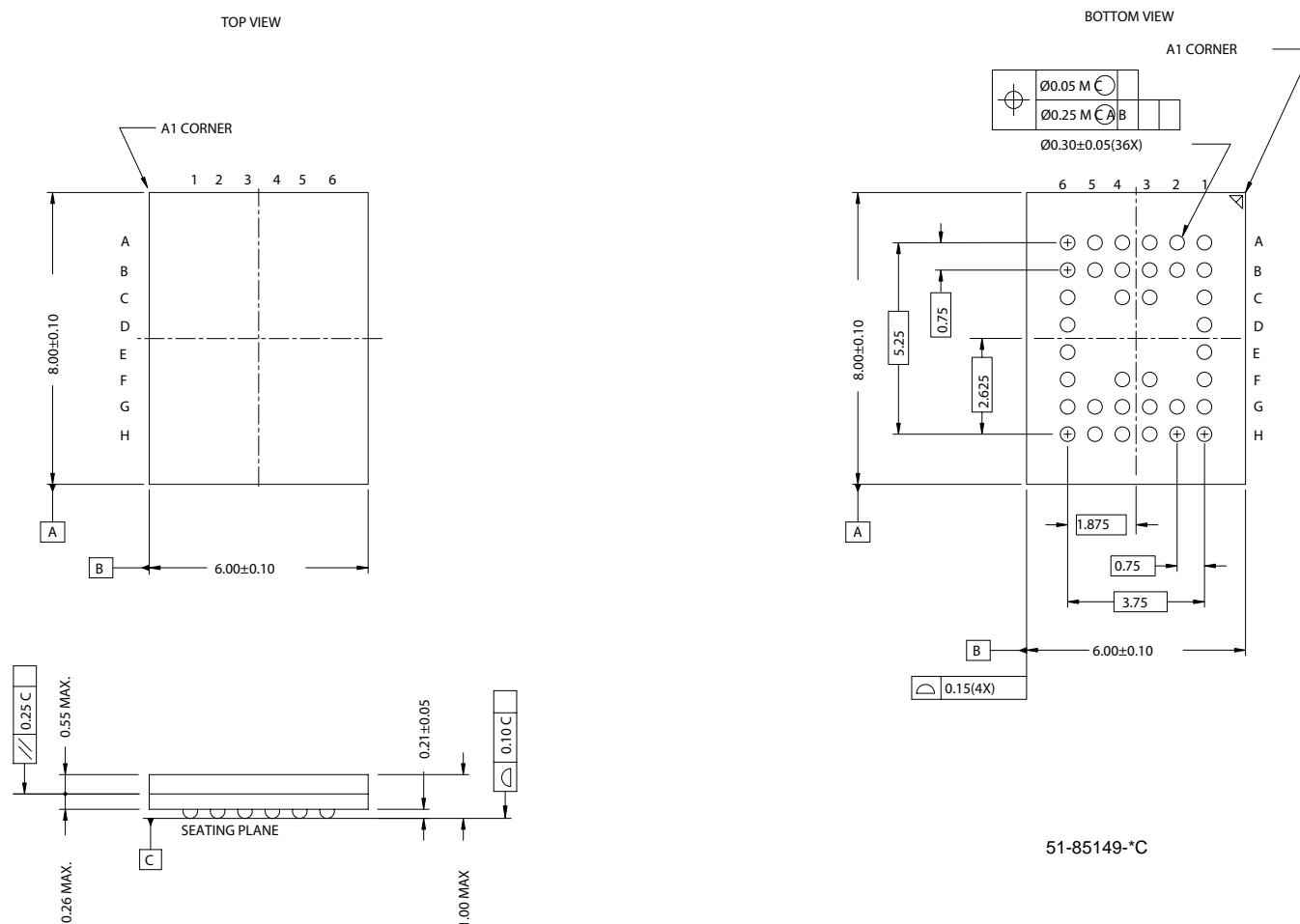
Package Diagrams (continued)

32-pin TSOP II (51- 85095)

TOP VIEW

DIMENSIONS IN MILLIMETERS $\frac{MIN.}{MAX.}$

DETAIL 'A'

51-85095-**
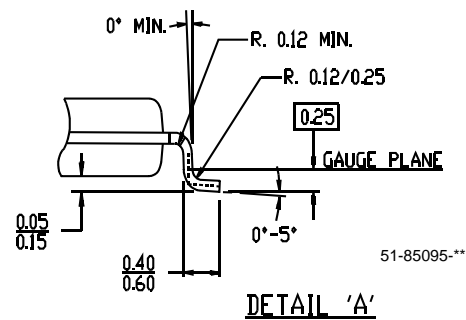
Package Diagrams (continued)

32-pin (450 MIL) Molded SOIC (51- 85081)

0.546[13.868]
0.566[14.376]

0.440[11.176]
0.450[11.430]

0.793[20.142]
0.817[20.751]

0.101[2.565]
0.111[2.819]

0.118[2.997]
MAX.

0.006[0.152]
0.012[0.304]

0.004[0.102]

0.050[1.270]
BSC.

0.014[0.355]
0.020[0.508]

0.004[0.102]
MIN.

0.047[1.193]
0.063[1.600]

0.023[0.584]
0.039[0.990]

SEATING PLANE

51-85081-*B
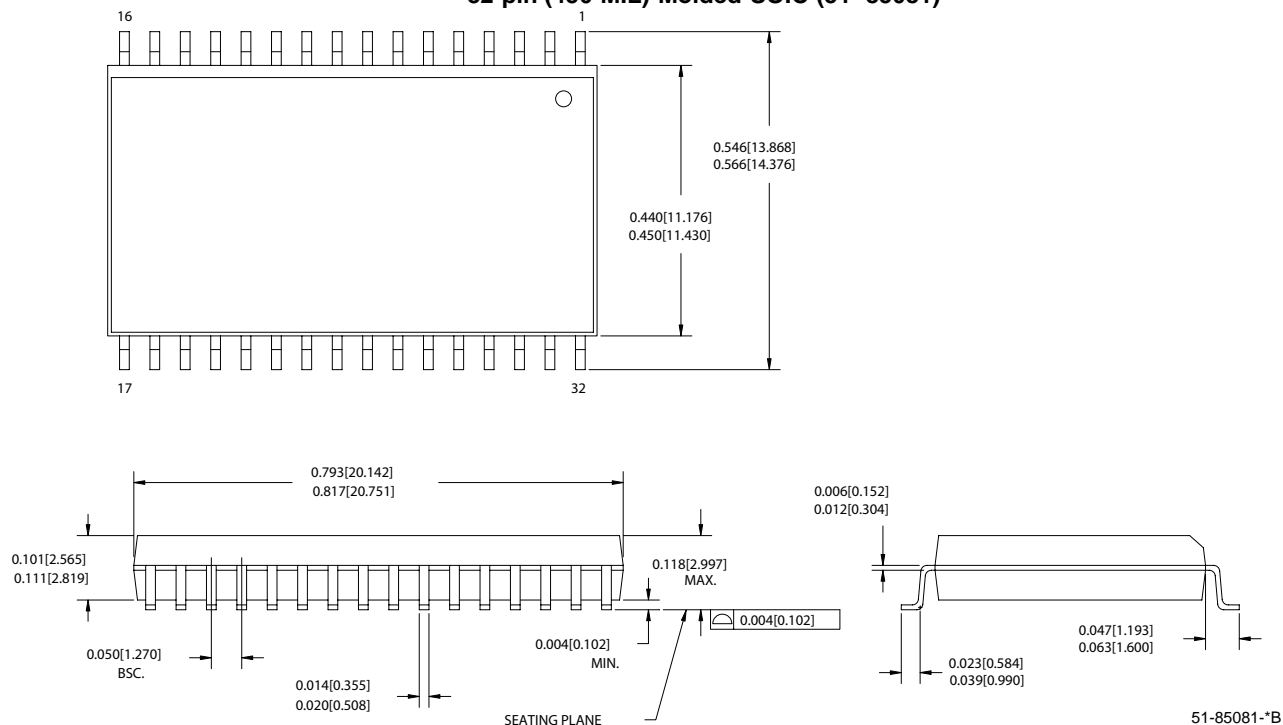
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Document History Page

Document Title:CY62148EV30 MoBL®4-Mbit (512K x 8) Static RAM				
Document Number: 38-05576				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	223225	See ECN	AJU	New data sheet
*A	247373	See ECN	SYT	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Changed V_{CC} stabilization time in footnote #7 from 100 µs to 200 µs Changed I_{CCDR} from 2.0 µA to 2.5 µA Changed typo in Data Retention Characteristics(t_R) from 100 µs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414807	See ECN	ZSD	Changed from Preliminary information to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Removed 35ns Speed Bin Removed "L" version of CY62148EV30 Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 µA to 1 µA and Max. values from 2.5 µA to 7 µA. Changed the AC test load capacitance value from 50pF to 30pF. Changed I_{CCDR} from 2.5 µA to 7 µA. Added I_{CCDR} typical value. Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns. Changed t_{SD} from 22 ns to 25 ns. Updated the package diagram 36-pin VFBGA from *B to *C Added 32-pin SOIC package diagram and pin diagram Updated the ordering information table and replaced the Package Name column with Package Diagram.