

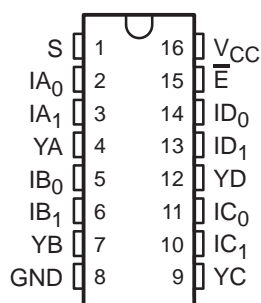
# TS3L110

## QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH DIFFERENTIAL 8-CHANNEL TO 4-CHANNEL MULTIPLEXER/DEMULPLEXER

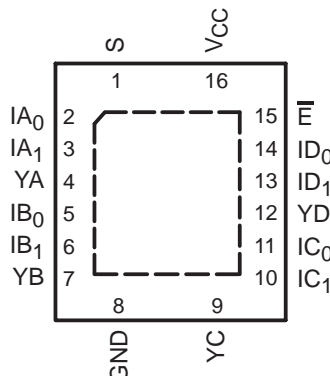
SCDS176 – SEPTEMBER 2004

- Wide Bandwidth (BW = 500 MHz Typ)
- Low Crosstalk ( $X_{TALK} = -30$  dB Typ)
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low and Flat ON-State Resistance ( $r_{on} = 4 \Omega$  Typ,  $r_{on(Flat)} = 1 \Omega$ )
- Switching on Data I/O Ports (0 to 5 V)
- $V_{CC}$  Operating Range From 3 V to 3.6 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Data and Control Inputs Have Undershoot Clamp Diodes
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Suitable for Both 10 Base-T/100 Base-T Signaling

D, DBQ, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



### description/ordering information

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ( $\bar{E}$ ) input. When  $\bar{E}$  is low, the switch is enabled, and the I port is connected to the Y port. When  $\bar{E}$  is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	TS3L110RGYR	TK110
	SOIC – D	Tube	TS3L110D	TS3L110
		Tape and reel	TS3L110DR	
	SSOP (QSOP) – DBQ	Tape and reel	TS3L110DBQR	TK110
	TSSOP – PW	Tube	TS3L110PW	TK110
		Tape and reel	TS3L110PWR	
	TVSOP – DGV	Tape and reel	TS3L110DGVR	TK110

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**description/ordering information (continued)**

This device can be used to replace mechanical relays in LAN applications. This device has low and flat  $r_{on}$ , wide bandwidth, and low crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications. The device can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations. The device is designed for low channel-to-channel skew and low crosstalk.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\bar{E}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

INPUTS		INPUT/OUTPUT YX	FUNCTION
$\bar{E}$	S		
L	L	$IX_0$	$YX = IX_0$
L	H	$IX_1$	$YX = IX_1$
H	X	Z	Disconnect

**PIN DESCRIPTIONS**

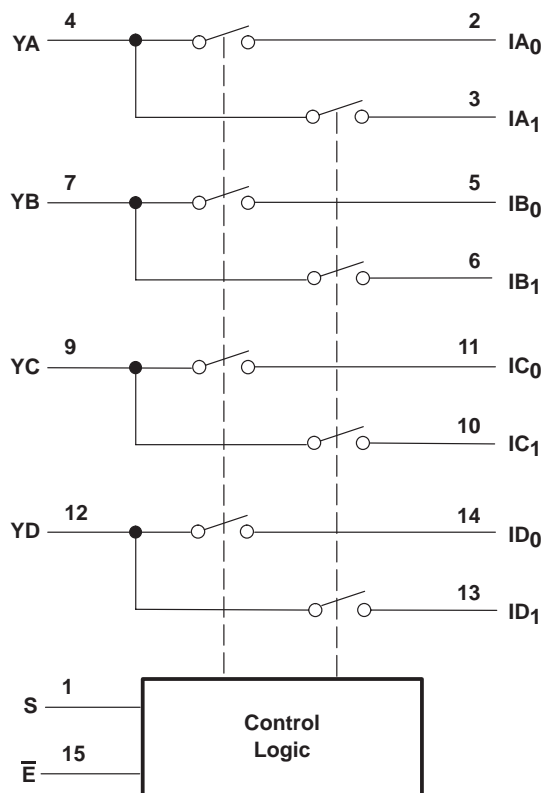
PIN NAME	DESCRIPTION
$IAn-IDn$	Data I/Os
S	Select input
$\bar{E}$	Enable input
$YA-YD$	Data I/Os

**TS3L110**

**QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH  
DIFFERENTIAL 8-CHANNEL TO 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER**

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logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through $V_{CC}$ or GND terminals	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package	73°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): DGV package	120°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.
  6. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 7)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.6	V
$V_{IH}$	High-level control input voltage ( $\bar{E}$ , S)	2	5.5	V
$V_{IL}$	Low-level control input voltage ( $\bar{E}$ , S)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 7: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**TS3L110**  
**QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH**  
**DIFFERENTIAL 8-CHANNEL TO 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER**  
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**electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	$\bar{E}, S$	$V_{CC} = 3.6\text{ V}, I_{IN} = -18\text{ mA}$			-1.8	V
$I_{IH}$	$\bar{E}, S$	$V_{CC} = 3.6\text{ V}, V_{IN} = 5.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	$\bar{E}, S$	$V_{CC} = 3.6\text{ V}, V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0, V_O = 0\text{ to }5.5\text{ V}, V_I = 0$			1	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}, I_{I/O} = 0, \text{ Switch ON or OFF}$		0.7	1.5	mA
$C_{in}$	$\bar{E}, S$	$f = 1\text{ MHz}, V_{IN} = 0$		2.5	3.5	pF
$C_{io}(\text{OFF})$	I port	$V_I = 0, f = 1\text{ MHz}, \text{Outputs open, Switch OFF}$		3.5	5	pF
	Y port	$V_I = 0, f = 1\text{ MHz}, \text{Outputs open, Switch OFF}$		5.5	7	
$C_{io}(\text{ON})$	I or Y port	$V_I = 0, f = 1\text{ MHz}, \text{Outputs open, Switch ON}$		10.5	13	pF
$r_{on}$		$V_{CC} = 3\text{ V}, 1.25\text{ V} \leq V_I \leq V_{CC}, I_I = -10\text{ mA to }-30\text{ mA}$		4	8	$\Omega$
$r_{on}(\text{flat})^\ddagger$		$V_{CC} = 3\text{ V}, V_I = 1.25\text{ V and }V_{CC}, I_I = -10\text{ mA to }-30\text{ mA}$		1		$\Omega$
$\Delta r_{on}^\S$		$V_{CC} = 3\text{ V}, 1.25\text{ V} \leq V_I \leq V_{CC}, I_I = -10\text{ mA to }-30\text{ mA}$		0.9	2	$\Omega$

$V_I, V_O, I_I,$  and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡  $r_{on}(\text{flat})$  is the difference of  $r_{on}$  in a given channel at specified voltages.

§  $\Delta r_{on}$  is the difference of  $r_{on}$  in a given device.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}, R_L = 200\ \Omega, C_L = 10\text{ pF}$  (unless otherwise noted) (see Figures 5 and 6)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{pd}^\P$	I or Y	Y or I		0.25		ns
$t_{PZH}, t_{PZL}$	$\bar{E}$ or S	I or Y	0.5		7	ns
$t_{PHZ}, t_{PLZ}$	$\bar{E}$ or S	I or Y	0.5		5	ns
$t_{sk(p)}^\#$	I or Y	Y or I	0.1	0.2		ns

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

# Skew between opposite transitions of the same output  $|t_{PHL} - t_{PLH}|$ . This parameter is not production tested.

**dynamic characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$X_{TALK}$	$R_L = 100\ \Omega, f = 250\text{ MHz}, \text{ see Figure 7}$		-26		dB
$O_{IRR}$	$R_L = 100\ \Omega, f = 250\text{ MHz}, \text{ see Figure 8}$		-28		dB
BW	$R_L = 100\ \Omega, \text{ see Figure 6}$		500		MHz

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .



## OPERATING CHARACTERISTICS

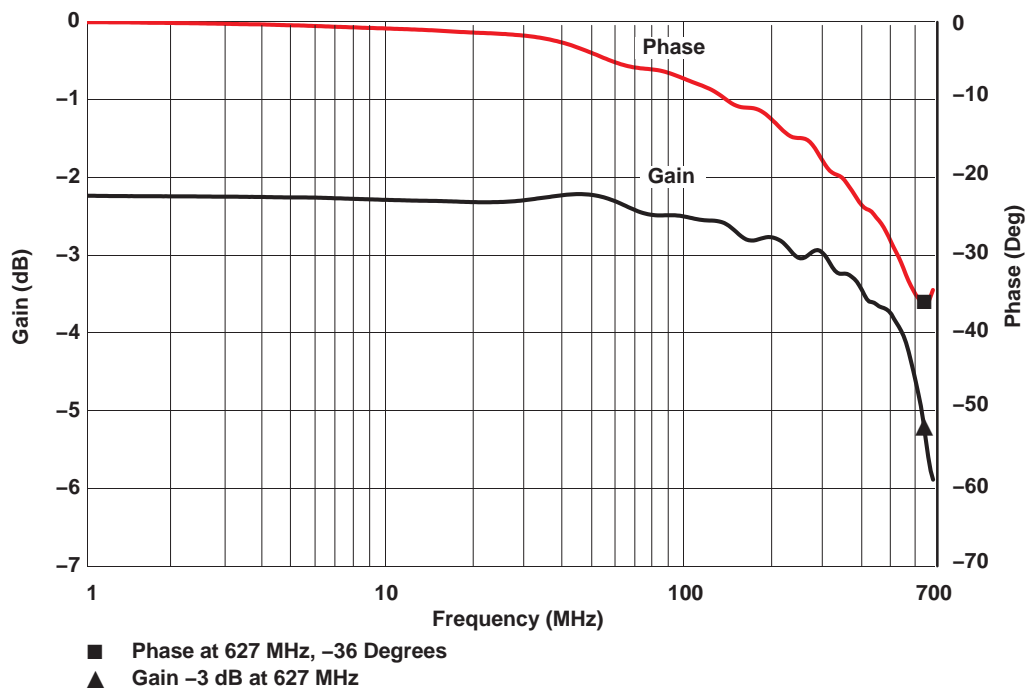


Figure 1. Gain/Phase vs Frequency

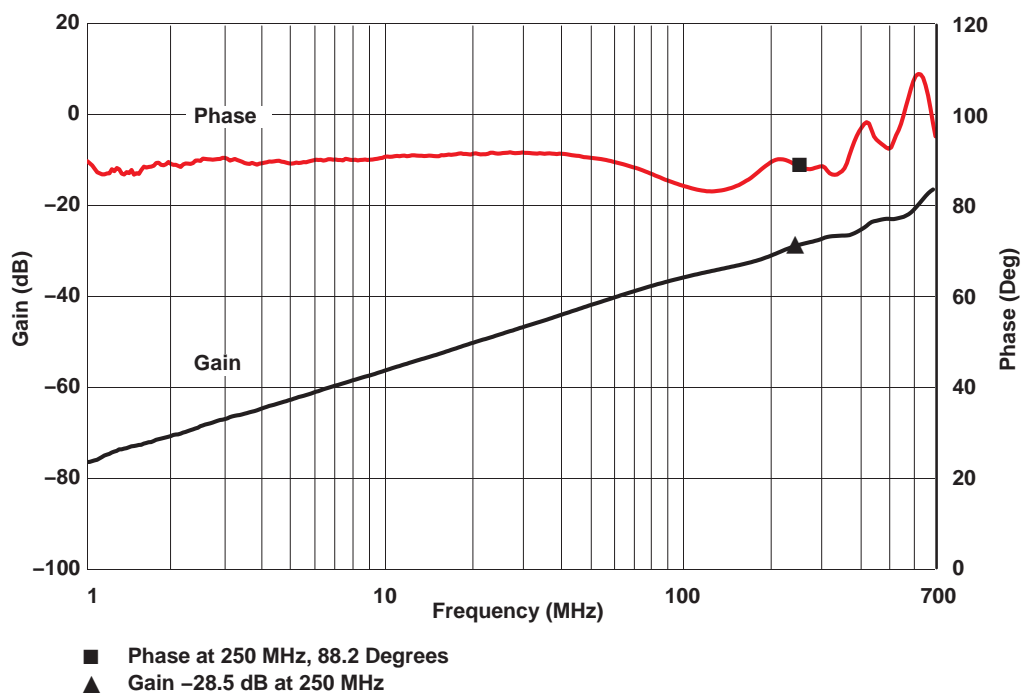


Figure 2. OFF Isolation vs Frequency

### OPERATING CHARACTERISTICS

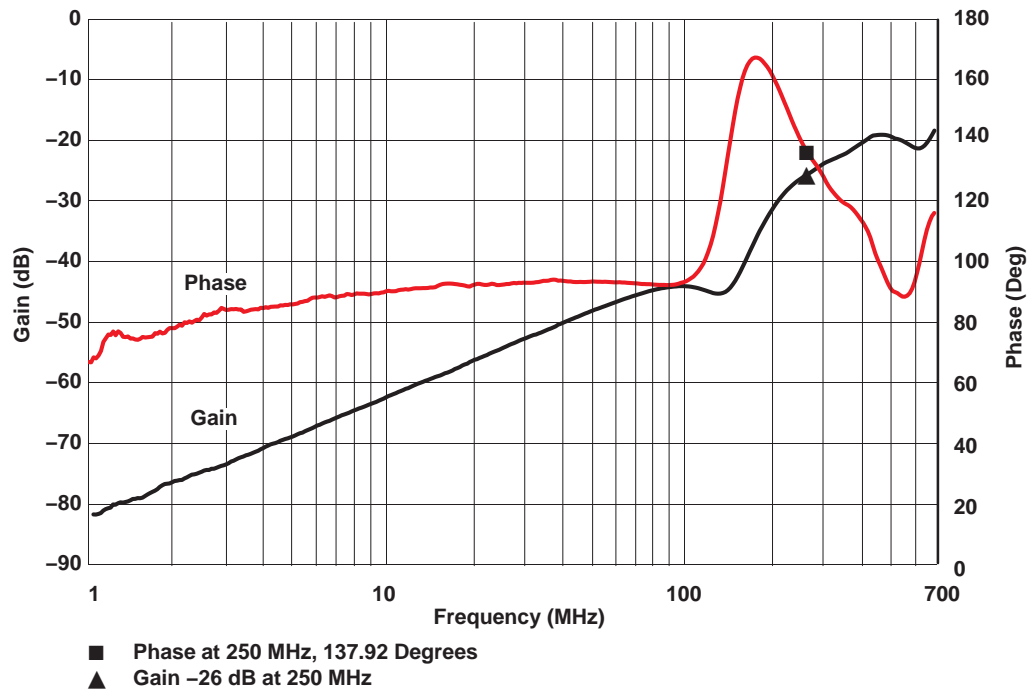


Figure 3. Crosstalk vs Frequency

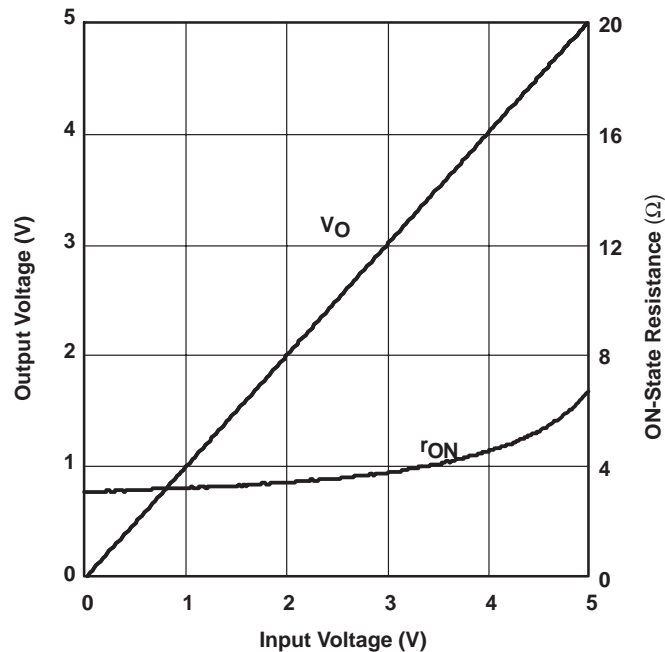
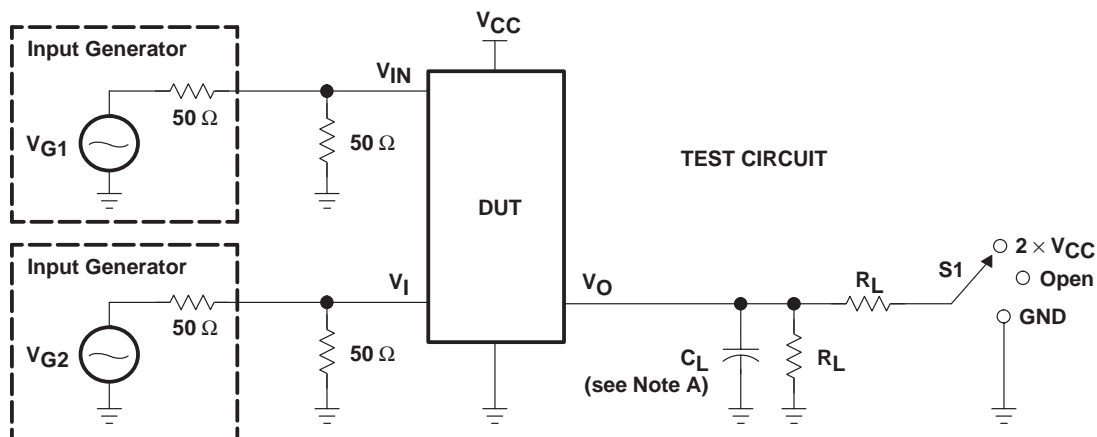
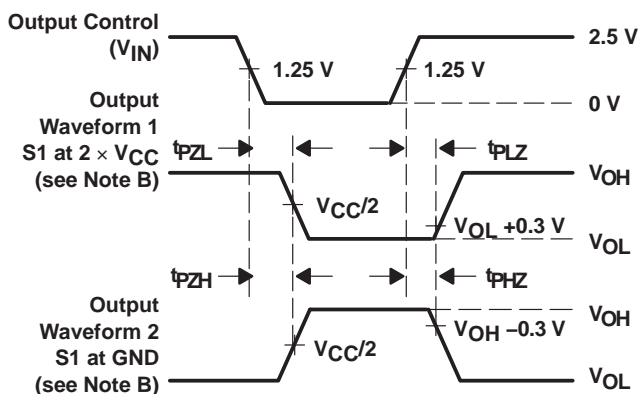


Figure 4. Output Voltage/ON-State Resistance vs Input Voltage

### PARAMETER MEASUREMENT INFORMATION FOR ENABLE AND DISABLE TIMES



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>CC</sub>	10 pF	0.3 V



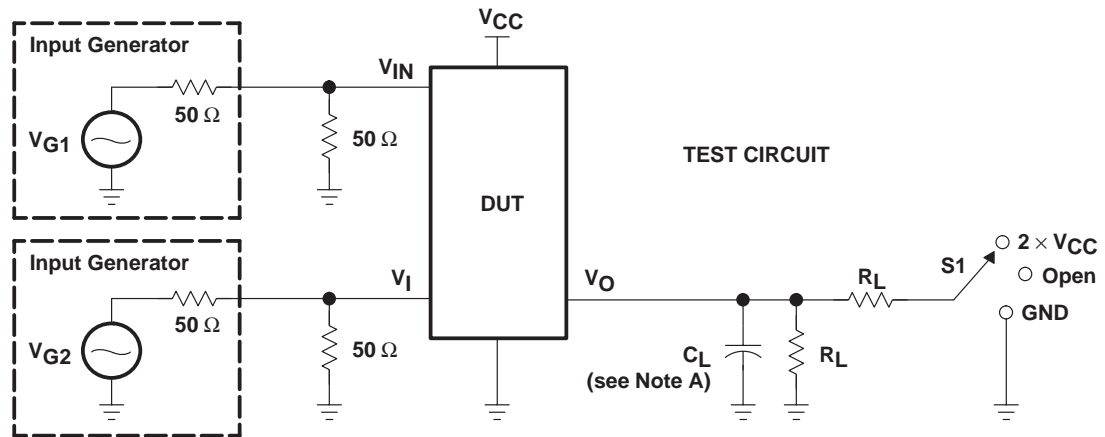
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

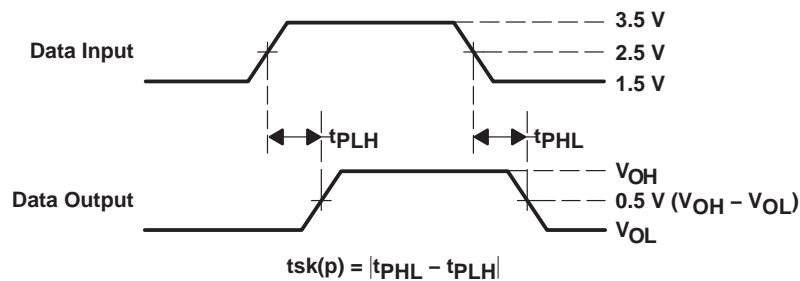
Figure 5. Test Circuit and Voltage Waveforms



**PARAMETER MEASUREMENT INFORMATION  
FOR SKEW**



TEST	VCC	S1	RL	VIN (see Note B)	CL
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	GND	200 Ω	VCC or GND	10 pF

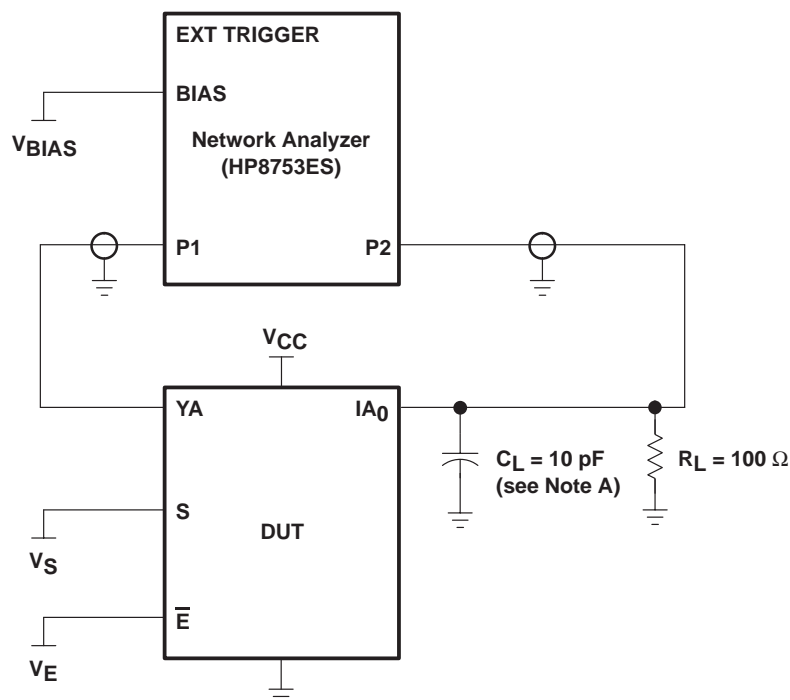


**VOLTAGE WAVEFORMS  
PULSE SKEW ( $t_{sk(p)}$ )**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Switch is ON during the measurement of  $t_{sk(p)}$ , i.e., voltage at  $\bar{E} = 0$  and  $S = V_{CC}$  or GND

**Figure 6. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and jig capacitance.

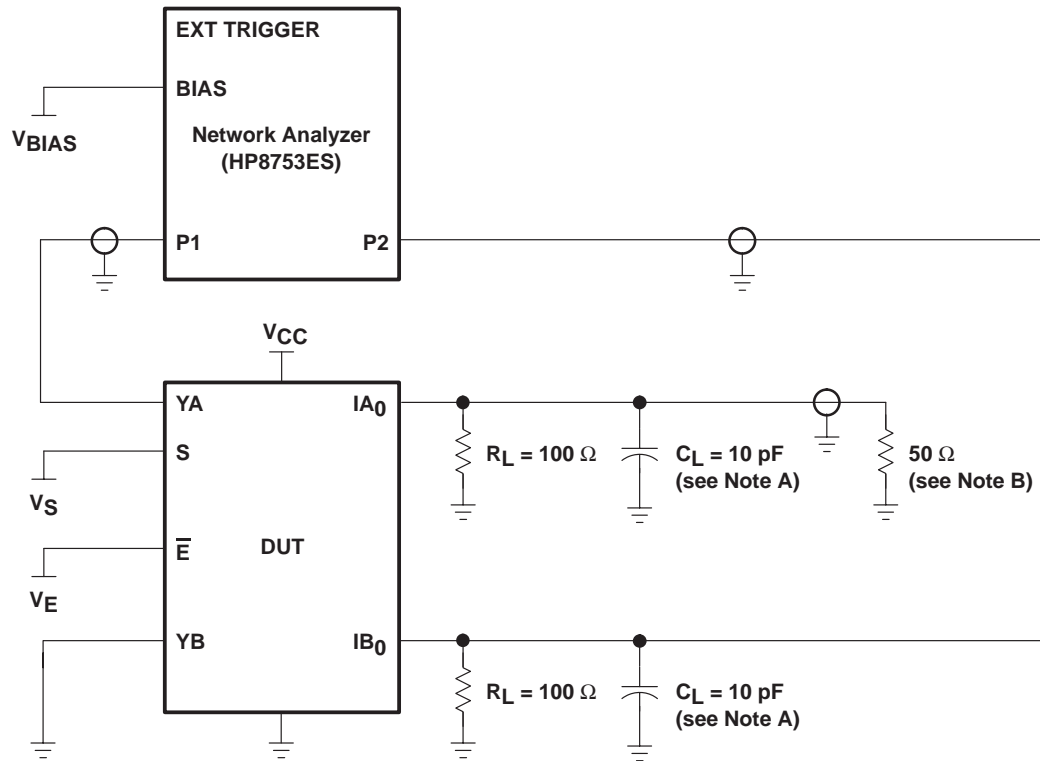
**Figure 7. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_S = 0$ ,  $V_E = 0$ , and YA is the input, the output is measured at  $IA_0$ . All unused analog I/O ports are left open.

### HP8753ES setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35 \text{ V}$   
 ST = 2 s  
 P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

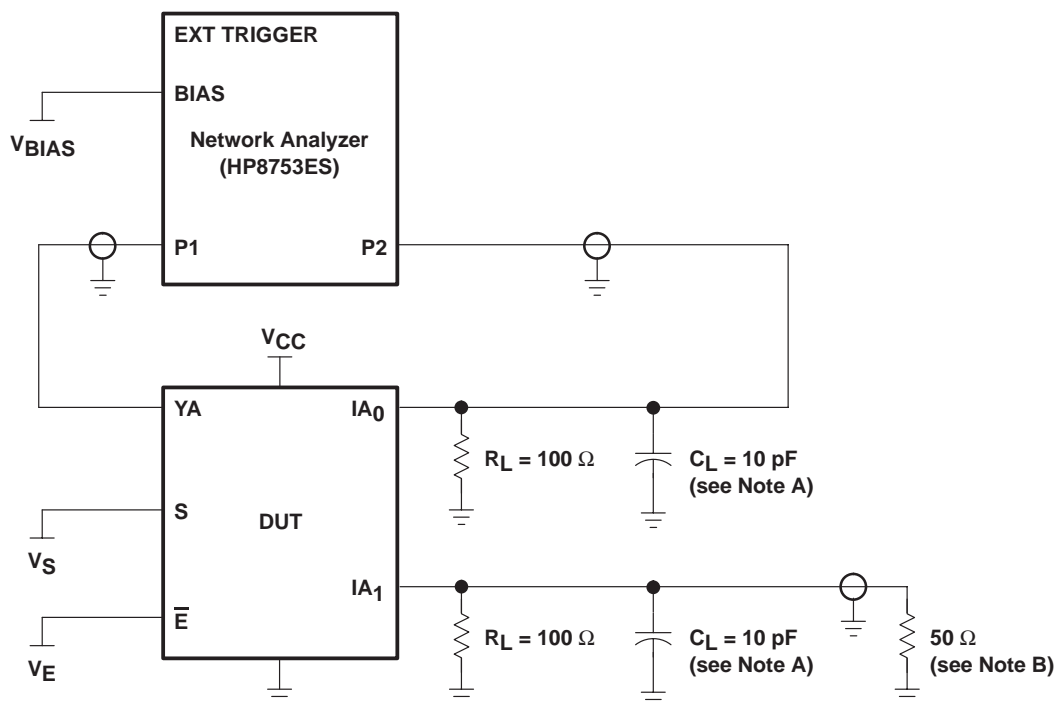
**Figure 8. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_S = 0$ ,  $V_E = 0$ , and YA is the input, the output is measured at  $IB_0$ . All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50- $\Omega$  pulldown resistors.

### HP8753ES setup

Average = 4  
RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
ST = 2 s  
P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 9. Test Circuit for OFF Isolation ( $O_{IRR}$ )**

OFF isolation is measured at the output of the OFF channel. For example, when  $V_S = V_{CC}$ ,  $V_E = 0$ , and YA is the input, the output is measured at  $IA_0$ . All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50- $\Omega$  pulldown resistors.

### HP8753ES setup

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35$  V

ST = 2 s

P1 = 0 dBm

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS3L110D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110DBQR	ACTIVE	SSOP/QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3L110DBQRE4	ACTIVE	SSOP/QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3L110DBQRG4	ACTIVE	SSOP/QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3L110DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L110RGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3L110RGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

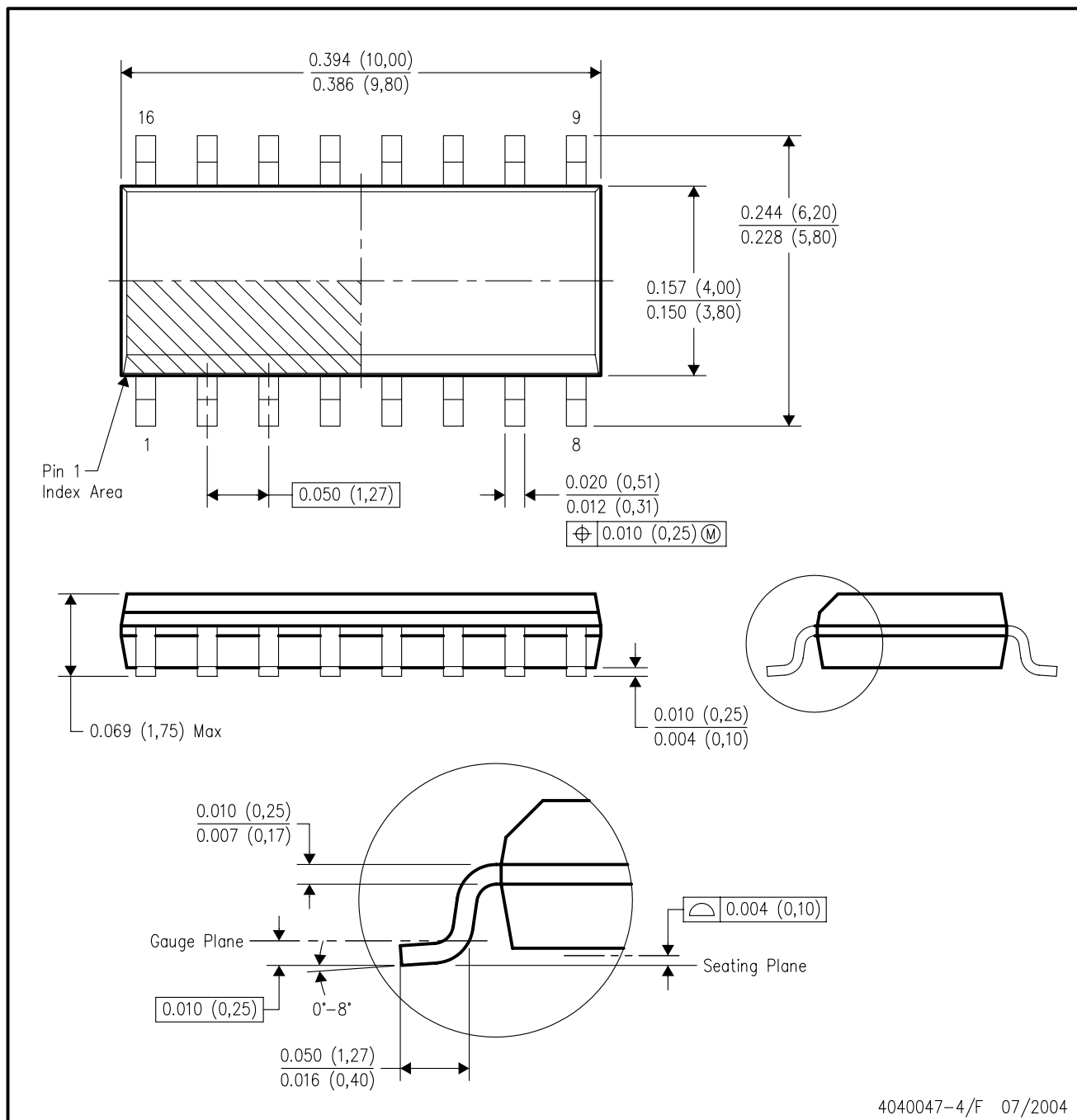
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

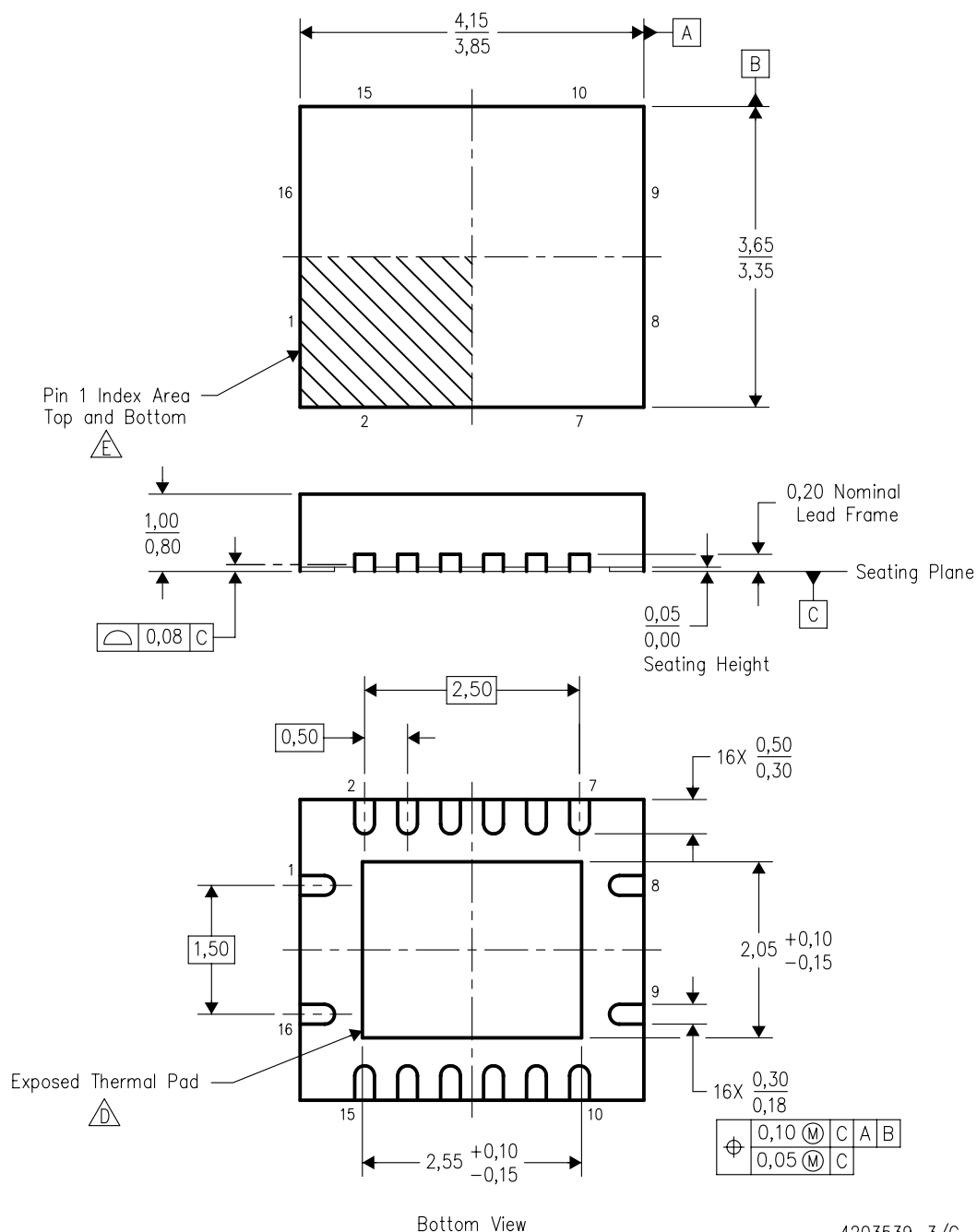


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## RGY (R-PQFP-N16)

## PLASTIC QUAD FLATPACK



4203539-3/G 04/2005

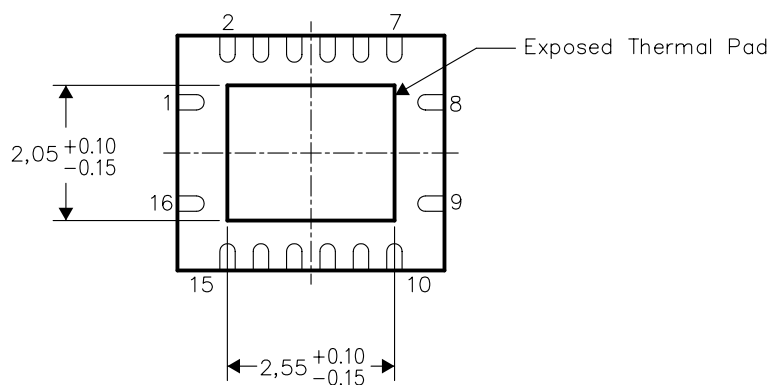
- NOTES:
- |           |  |
|-----------|--|
| A.        | All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.   |
| B.        | This drawing is subject to change without notice.  |
| C.        | QFN (Quad Flatpack No-Lead) package configuration.   |
| <u>D.</u> | The package thermal pad must be soldered to the board for thermal and mechanical performance.  |
| <u>E.</u> | Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.<br>The Pin 1 identifiers are either a molded, marked, or metal feature. |
| F.        | Package complies to JEDEC MO-241 variation BB.   |

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

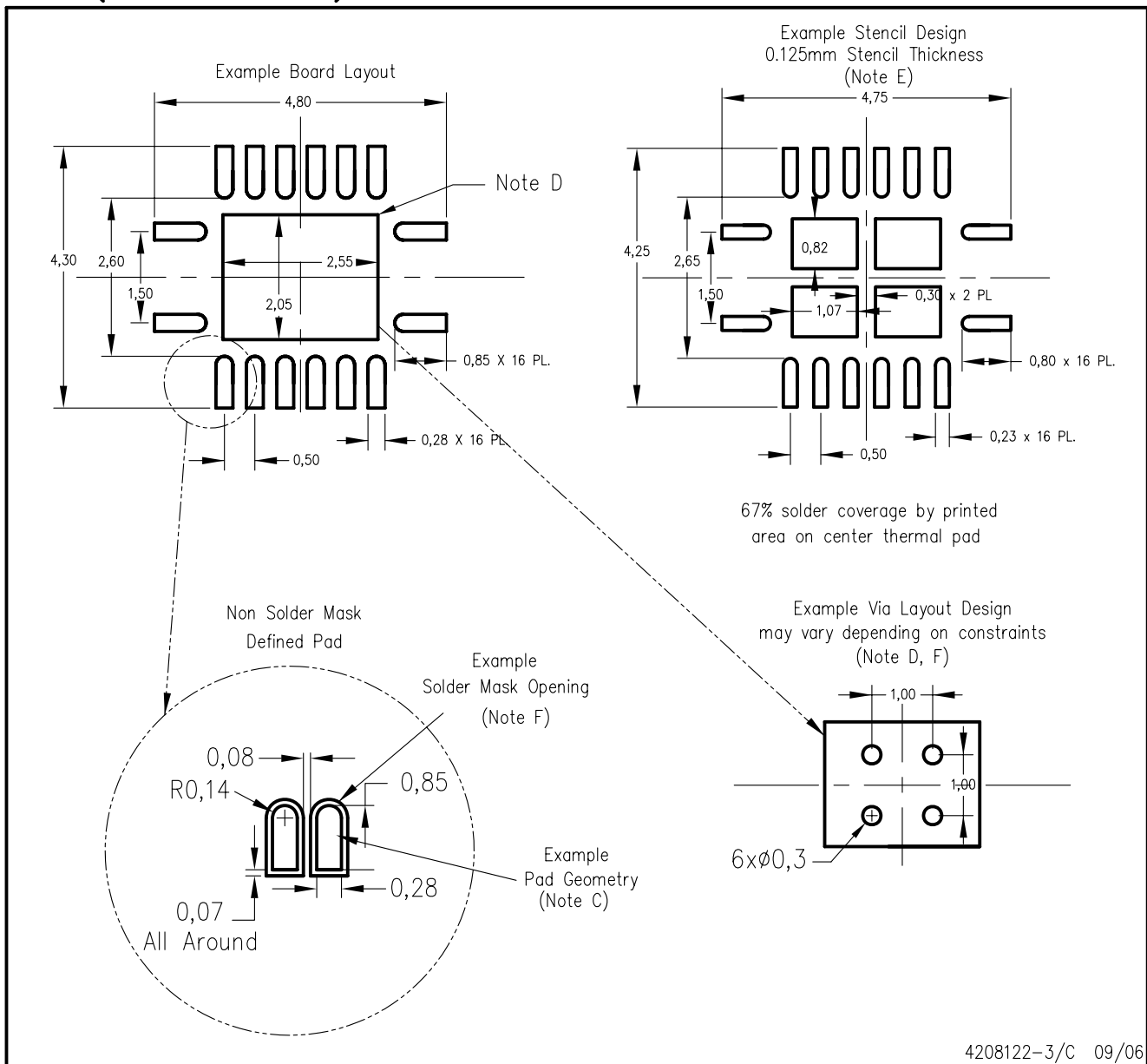


Bottom View

NOTE: All linear dimensions are in millimeters

## Exposed Thermal Pad Dimensions

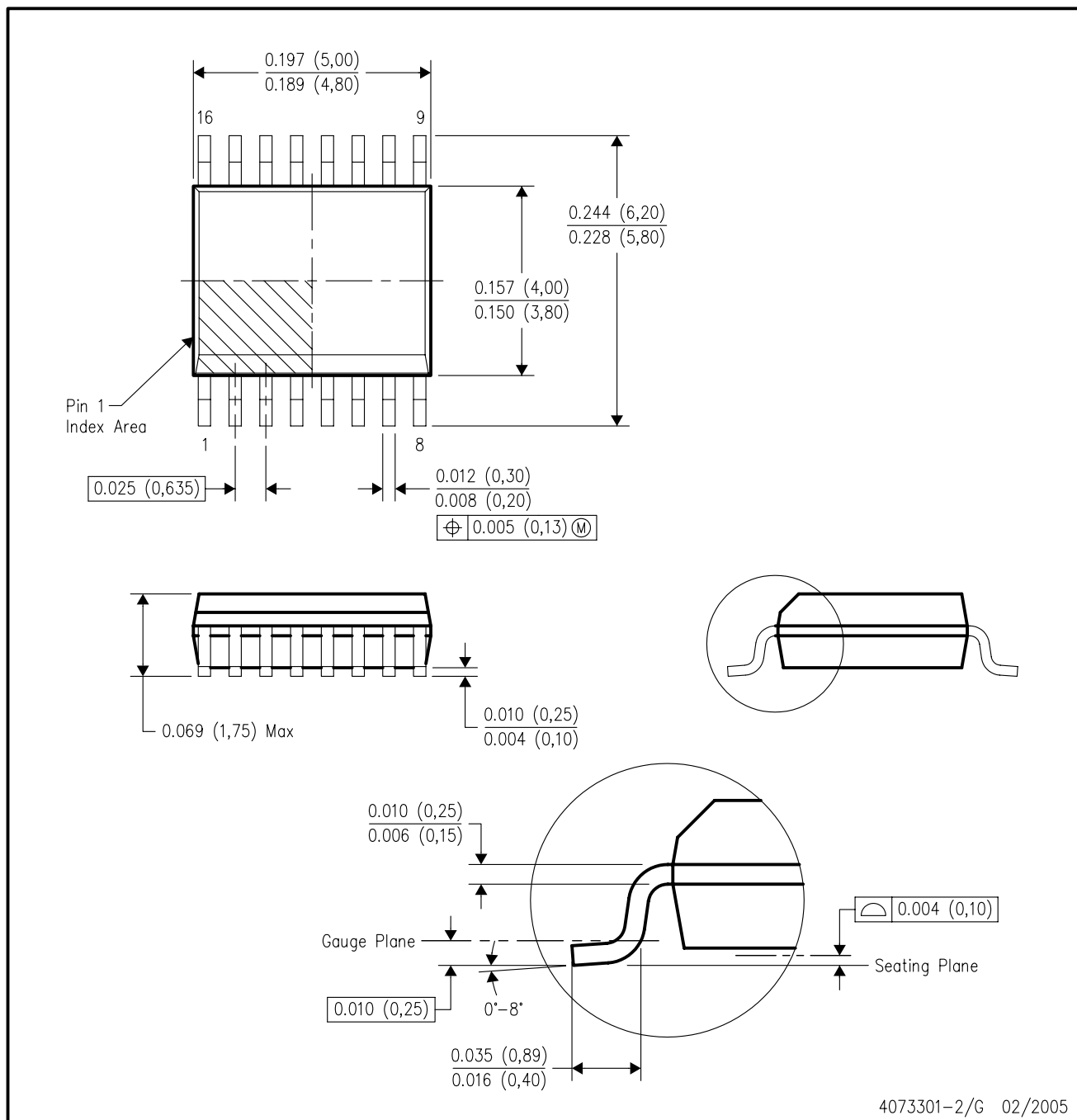
## RGY (R-PQFP-N16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## DBQ (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

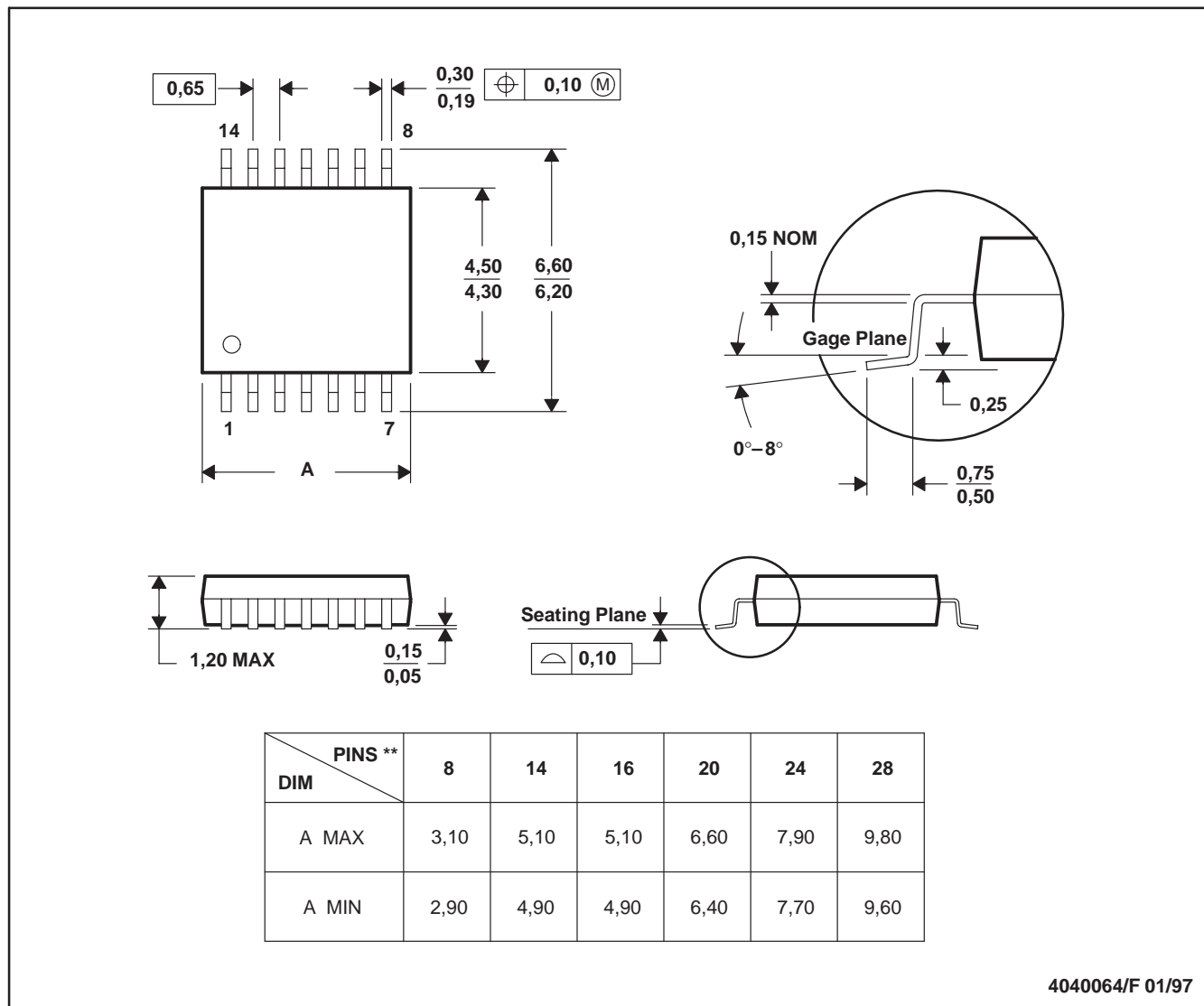


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AB.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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