Interfacing LVDS to PECL, LVPECL, CML, RS-422 and single-ended devices

1. Introduction

Today's high-speed requirement is moving the industry toward high-speed, serial, differential, low-power and point-to-point interface. LVDS offers all of these features. Pericom Semiconductor offers wide range of LVDS drivers, receivers and clock distribution buffers.

This application note discusses the interface between LVDS and PECL, LVPECL, CML, RS-422 and single ended devices using resistor network.

Since the structure of drivers and receivers are different between manufacturers, the circuits provided in this application note are for design reference only. The designer needs to validate the circuit and adjust the values of the resistors and capacitors in the circuits for optimal performance.

2. The Specifications of the Standards

The table below lists the operational voltage levels for the different standards used in this application note.

Table 1. The Specs of LVDS, PECL, LVPECL, CML and RS-422

Parameters	V_{CC}	V_{OH}	V_{OL}	V_{PP}	V_{OS} (voltage offset)
LVDS	3.3V	1.4V	1.0V	350mV to 400mV	1.2V
PECL	5.0V	4.0V	3.2V	800mV to 1000mV	3.6V
LVPECL	3.3V	2.5V	1.5V	800mV to 1000mV	2.0V
CML	5V	5V	4.6V	400mV	4.8V
RS-422	5V	3.4V	0.2V	3.1V	1.8V

3. The Calculation of the Resistor Divider

In order to interface the PECL and LVPECL standards to Pericom LVDS, we will use a resistor divider to shift the different voltage levels.

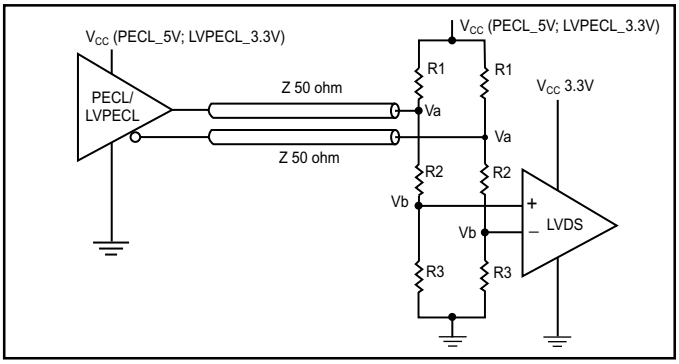

Figure 1. PECL and LVPECL to LVDS interface circuit

The interface in Figure 1 is using voltage divider consisted by R1, R2 and R3. The calculation for the values of R1, R2 and R3 is followed below:

$R1 \parallel (R2 + R3) = Z$
$[(R2 + R3) / (R1 + R2 + R3)] = Va / Vcc$
$R3 / (R1 + R2 + R3) = Vb / Vcc$

Where:
Va – the Vos, 3.6V for SEPC and 2.0V for LVPECL.
Vb – the Vos, 1.2V for LVDS.
Z – 50 ohm.

The gain at Vb is:
$Gain = R3 / (R2 + R3)$

The swing magnitude at Vb is:
Vbs = Vas x gain

Where:
Vas - the swing magnitude at Va.
Vbs - the swing magnitude at Vb.

In real application design, the values of R1, R2 and R3 are different to the calculation results above, due to that the driver's output impedance is not included in the calculation. The driver's output structure and impedance are different between manufacturers thereby the values of R1, R2 and R3 should also be different.

3.1. Three approaches to obtain the resistance values

A. The Empirical Approach

Use the reference values in Table 2 and adjust these values according to approach 2 or 3 below. The interface designer should measure the Vos (the voltage offset) and Vpp (swing magnitude) at Va and Vb to validate the circuit in real application design.

Table 2. The values of R1, R2 and R3 are for reference only

	R1 (ohm)	R2 (ohm)	R3 (ohm)
LVPECL V_{CC}=3.3V	150	40	49
PECL V_{CC}=5V	84	105	35

B. The approach of using simulation tool

Getting the driver's IBIS model from the manufacturer and simulate the interface circuit for the values of R1, R2 and R3. If both the IBIS model and simulation tool are accurate, the simulation should provide the correct values of R1, R2 and R3. Then validate the values from simulation by the real circuit test.

C. The approach of real adjustment

Using the circuit in Figure 2 to adjust the values of R1, R2 & R3.

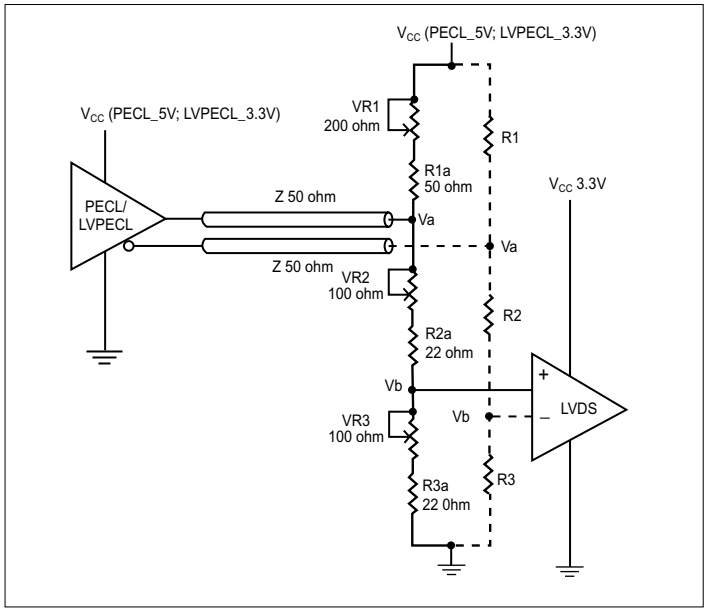

Figure 2. The adjustment circuit
R1 = (VR1 + R1a); R2 = (VR2 + R2a); R3 = (VR3 + R3a)

The R1a, R2a and R3a in Figure 2 are to limit the adjustable range and to prevent the overload current.

When adjusting the circuit, monitoring the signal at Va and Vb using scope, adjust VR1, VR2 and VR3:

a. The Vos (the average voltage in middle of the swing range) at Vb should be in the range of 0.8V to 1.6V for Pericom LVDS receivers. Please refer to the driver spec for the Vos at Va.

b. The swing range at Vb should be in the range of 350mV to 550mV for Pericom receivers. Please refer to the driver spec for the swing magnitude at Va. The swing magnitude at Va may be lower than the driver spec in order to fulfill the swing request at Vb.

c. After the circuit is adjusted, measure the value of VR1 and R1a for R1; VR2 and R2a for R2; VR3 and R3a for R3.

d. It is easier to use lower frequency for the adjustment, 100 khz to 10 MHz is preferred, but please validate the circuit at normal working frequency and adjust again if needed.

Circuit restriction

Due to the extra capacitance and nets added by the interface circuit, the maximum frequency of the interface should be lower than the maximum frequency offered in datasheet. The trace lengths between the driver and receiver are also limited depending on the frequency, the maximum trace length is estimated at 14" for 66 MHz and 2" for 320 MHz.

The trace length is a practical issue and depends on real design.

To reduce the parasitic capacitance, inductance and reflection for higher performance, the traces between the components in the interface circuit should be minimized, the shorter the traces the better. The capacitors, resistors, and diodes used in the interface circuits must be high-speed components with short leads. Chip type packages are preferred.

4. PECL to LVDS

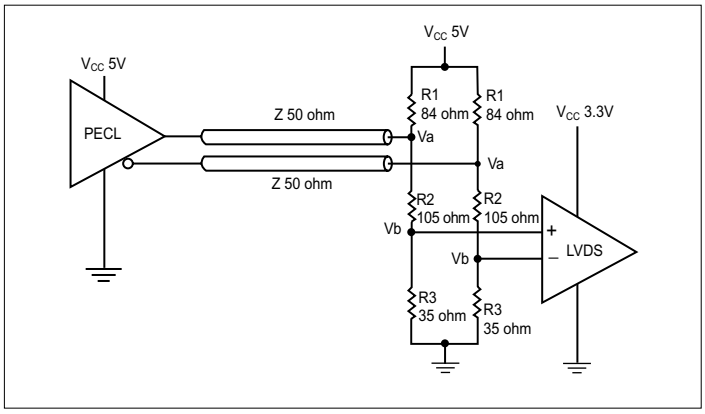

Figure 3. The PECL to LVDS interface circuit

Please refer to Section 3 for the circuit adjustment and restriction.

5. LVDS to PECL

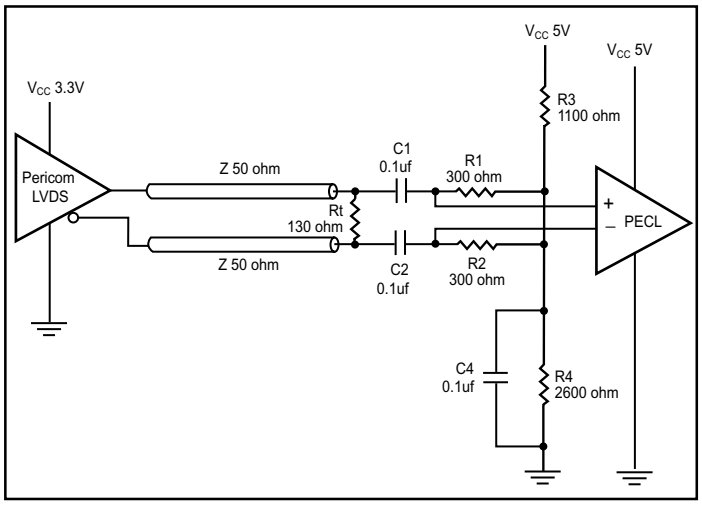

Figure 4. The LVDS to PECL interface circuit

The PECL receiver in Figure 4. has no internal pull-up resistors.

The resistance values in the circuit are for Pericom LVDS driver. Please refer to Section 3 for the circuit adjustment and restriction.

Since this interface is using AC coupling, this interface can only pass the AC signal thereby the signal transferred from the driver to the receiver must be suitable for AC coupling. When the capacitance of C1 and C2 is 0.1uf, the maximum time interval between any signal state switching (high to low or low to high) is 500ns.

6. LVPECL to LVDS

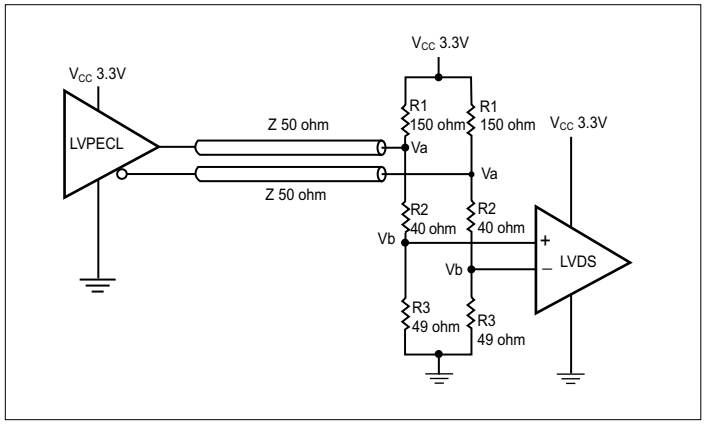

Figure 5. LVPECL to LVDS Interface Circuit

Please refer to Section 3 for the circuit adjustment and restriction.

7. LVDS to LVPECL

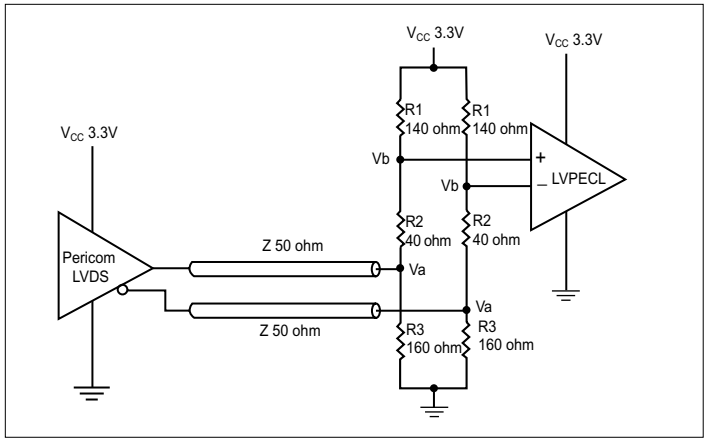

Figure 6. LVDS to LVPECL Interface Circuit

The resistance values in this circuit are for Pericom LVDS driver. The LVPECL receiver in this circuit has no internal pull-up resistors

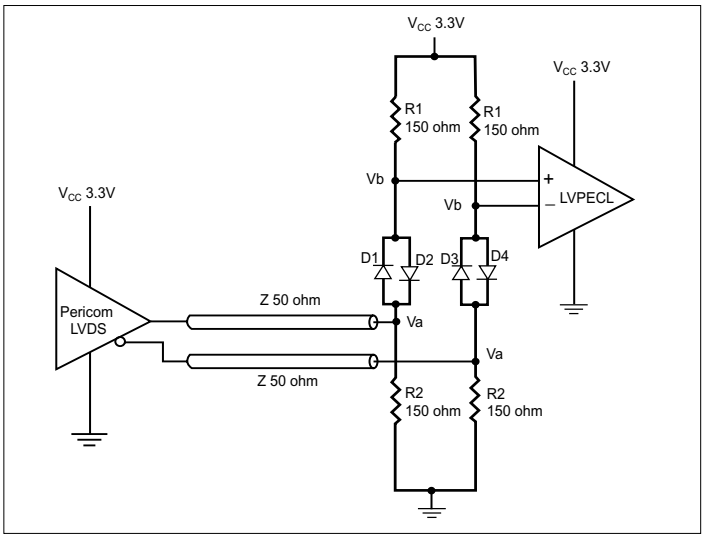

Figure7. LVDS to LVPECL interface using diodes

In Figure 7, the diodes D1, D2, D3 and D4 generate a 0.7V offset between Va and Vb with lower swing attenuation than the circuit in figure 6. Use high-speed diodes with 0.7V forwarding voltage drop, chip diodes are preferred.

The resistance values in this circuit are for Pericom LVDS driver. Please refer to Section 3 for the circuit adjustment and restriction. The LVPECL receiver in this circuit has no internal pull-up resistors.

8. CML to LVDS

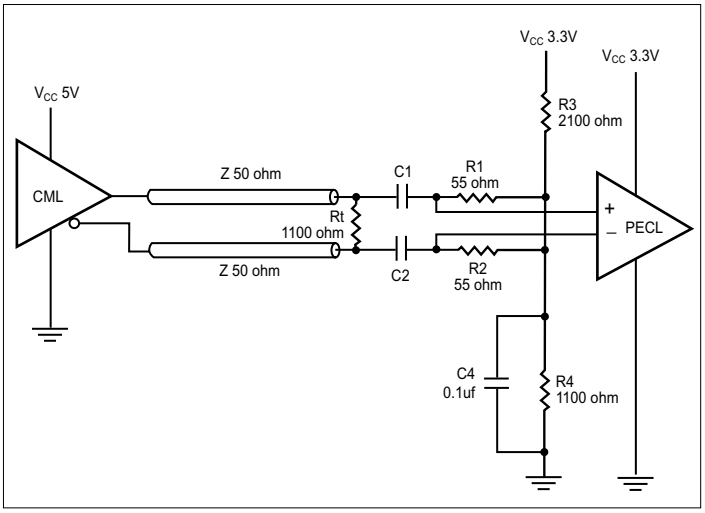

Figure 8. CML to LVDS interface circuit

Please refer to Section 3 for the circuit adjustment and restriction. Since this interface is using AC coupling, this interface can only pass the AC signal thereby the signal transferred from the driver to the receiver must be suitable for AC coupling. When the capacitance of C1 and C2 is 0.1uf, the maximum time interval between any signal state switching (high to low or low to high) is 500ns.

9. LVDS to CML

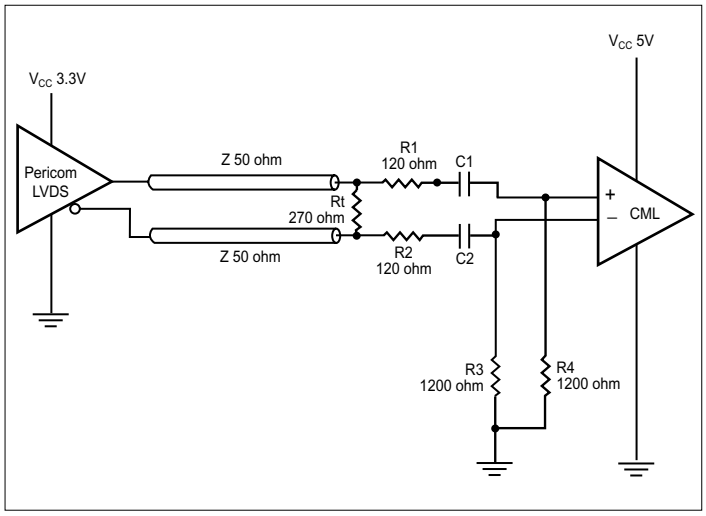

Figure 9. LVDS to CML interface circuit

The resistance values in this circuit are for Pericom LVDS driver. The CML receiver in this circuit has 50 Ohm internal pull-up resistors. Please refer to Section 3 for the circuit adjustment and restriction.

Since this interface is using AC coupling, this interface can only pass the AC signal thereby the signal transferred from the driver to the receiver must be suitable for AC coupling. When the capacitance of C1 and C2 is 0.1uf, the maximum time interval between any signal state switching (high to low or low to high) is 500ns.

10. RS-422 to LVDS

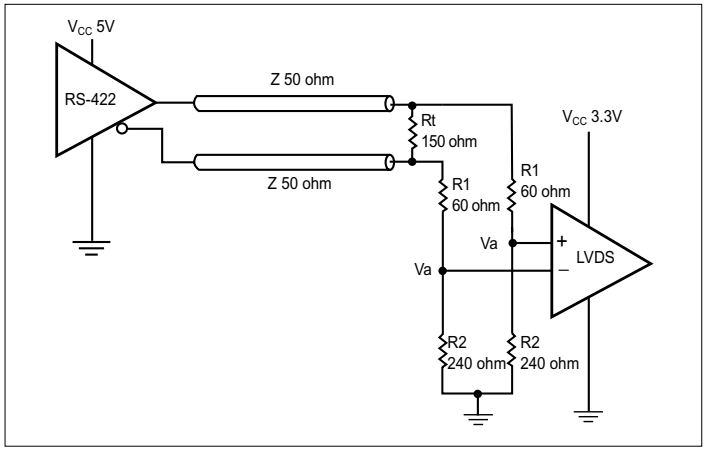

Figure 10. RS-422 to LVDS Interface Circuit

Please refer to Section 3 for the circuit adjustment and restriction.

11. Single-Ended Signal to LVDS

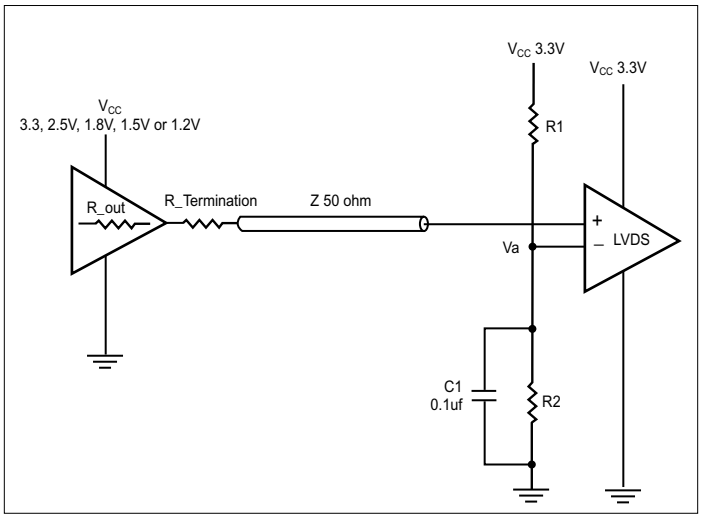

Figure 11. Single-Ended Signal to LVDS

When a single-ended CMOS driver is interfacing to a Pericom LVDS receiver, using the circuit in Figure 11 and the values in Table 3.

Table 3. The values of R1, R2 and Va for Pericom receiver

	Driver Vcc is: 3.3V	Driver Vcc is: 2.5V	Driver Vcc is: 1.8V	Driver Vcc is: 1.5V	Driver Vcc is: 1.2V
Va	1.65V	1.25V	0.9V	0.75V	0.75V
R1 (ohm)	1000	1460	2100	2000	2000
R2 (ohm)	1000	900	790	590	590

Also match the output impedance consisted by R_out and R_termination to the 50 Ohm trace impedance as:

R_out + R_termination = Z 50 Ohm

For example, if the output impedance of the driver is 20 Ohm, we should use 30 Ohm for R_termination, then we have:

20 Ohm + 30 Ohm = 50 Ohm (trace)

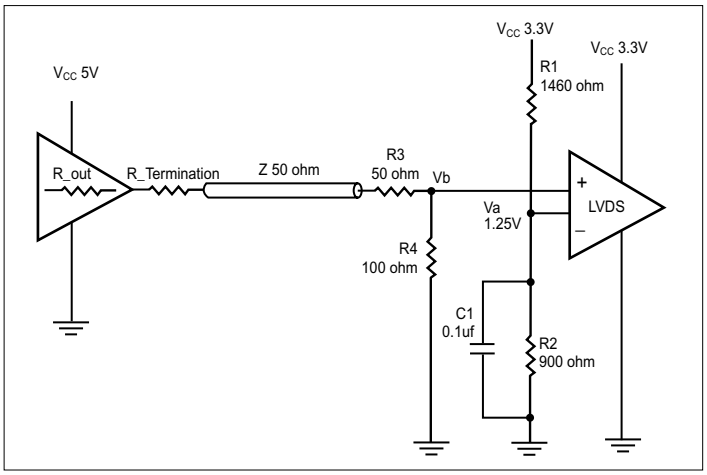

Figure 12. 5V Single-Ended Signal to LVDS

In Figure 12, the resistance value of R_termination is from 0 Ohm to 22 Ohm depending on the signal quality at Vb. Increase the resistance of R_termination if there are overshoot / undershoot at Vb or reduce the resistance of R_termination if the signal edges at Vb are attenuated.

Conclusion

This application note provides the reference circuits for the ease of interfacing different standards to Pericom LVDS devices.

The final validation is essential: due to the driver difference between manufacturers, all the circuits provided in this application note have to be validated by the designer before real application.

Pericom offers wide range of LVDS drivers and receivers and differential clock distribution devices and will support the interface design using Pericom products.