DC to 2.0 GHz Symmetric Multiplier

Preliminary Technical Data

ADL5391

FEATURES

Ultra-Fast Symmetric Multiplier
Function: $V_W = \alpha \times (V_X \times V_Y) / 1V + V_Z$
Unique Design Ensures Absolute XY-Symmetry
Identical X and Y Amplitude/Timing Responses
Adjustable Gain Scaling, α
DC coupled Throughout, 3-dB Bandwidth of 2 GHz
Fully-Differential Inputs, may be used Single-Ended
Low Noise, High Linearity$_7$
Accurate, Temperature Stable Gain Scaling
Single-Supply Operation (4.5 to 5.5 V @ 130mA)
Low Current Power Down Mode
16-lead Chip-Scale Package

APPLICATIONS

Wideband Multiplication and Summing
High-Frequency Analog Modulation
Adaptive Antennas (Diversity/Phased-Array)
Square-Law Detector and True RMS Detector
Accurate Polynomial Function Synthesis

FUNCTIONAL BLOCK DIAGRAM

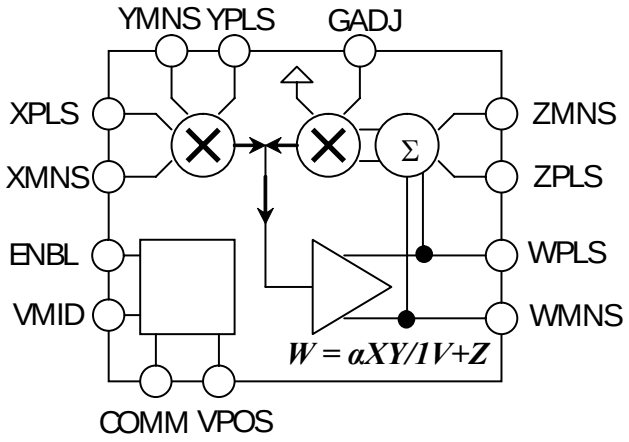

Figure 1.

GENERAL DESCRIPTION

The ADL5391 draws on three decades of experience in advanced analog multiplier products. It provides the same general mathematical function that has been field-proven to provide an exceptional degree of versatility in function synthesis:

$$V_W = \alpha \times (V_X \times V_Y)/1V + V_Z$$

The most significant advance in the ADL5391 is the use of a new multiplier core architecture, which differs markedly from the conventional form that has been in use since 1970. The conventional structure, employing a current-mode, trans-linear core, is fundamentally asymmetric with respect to the X and Y inputs, leading to relative amplitude and timing misalignments that are problematic at high frequencies. The new multiplier core eliminates these misalignments by offering absolutely symmetric signal paths for both X and Y inputs. The Z input allows a signal to be added directly to the output. This can be used to cancel a carrier or to apply a static offset voltage.

The fully differential X, Y and Z input interfaces are operational over a ±2V range-and they can be used in single-ended fashion as well. A user applied input common-mode can be varied from the internally set $V_{PS}/2$ down to ground. These input interfaces each present a differential 500 Ω input impedance up to approximately 700 MHz, decreasing to 50 Ω at 2 GHz. The gain scaling input, GADJ, can be used for fine adjustment of the gain scaling constant (α) about unity.

The differential output can swing ±2V about the Vps/2 common-mode and can be taken in a single-ended fashion as well. The output common-mode is designed to interface directly to the inputs of another ADL5391. Light DC loads can be ground referenced; however, AC-coupling of the outputs is recommended for heavy loads.

The ENBL pin allows the ADL5391 to be disabled quickly to a standby mode. The ADL5391 operates off supply voltages from 4.5 V to 5.5 V while consuming approximately 130 mA.

The ADL5391 is fabricated on Analog Devices' proprietary, high performance 65 GHz SOI complementary SiGe bipolar IC process. It is available in a 16-lead Pb-free LFCSP package and operates over a −40°C to +85°C temperature range. Evaluation boards are available.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

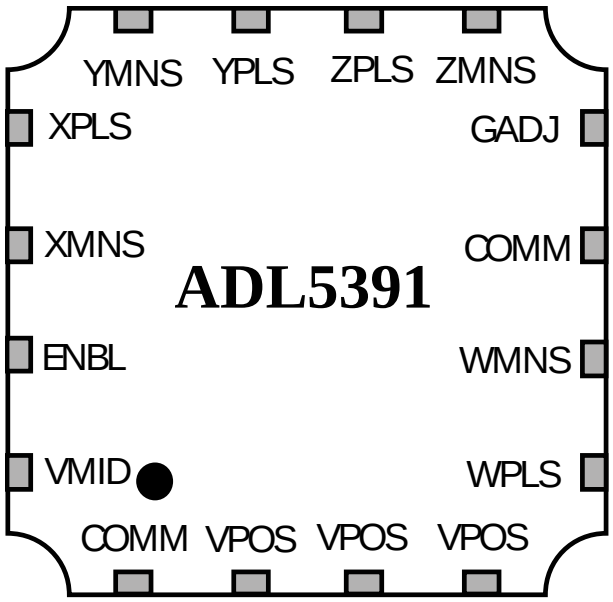

Figure 2. Pin Configuration- 16-Lead Lead Frame Chip Scale Package (LFCSP)

Table 1. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 7	**COMM**	**Device Common. Connect via lowest possible impedance to external circuit common.**
2, 3, 4	**VPOS**	**Positive Supply Voltage. 4.5 V – 5.5 V.**
5, 6	**WPLS, WMNS**	**Differential Outputs. (Is pull-up required?)**
8	**GADJ**	**Denominator Scaling Input**
9, 10	**ZMNS, ZPLS**	**Differential Intercept Inputs. Must be ac-coupled. Differential impedance 50 Ω nominal.**
11, 12	**YPLS, YMNS**	**Differential X-Multiplicand Inputs.**
13, 14	**XPLS, XMNS**	**Differential Y-Multiplicand Inputs.**
15	**ENBL**	**Chip Enable. Pull high to enable.**
16	**VMID**	**Vpos/2 Reference Output. Connect decoupling capacitor to circuit common.**

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_L = 50 Ω, ZPLS=ZMNS= Open, GADJ =Open, unless otherwise noted Transfer Function: **W = XY/1V + Z,** Common mode internally set to 2.5V nonimal

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
MULTIPLICAND INPUTS (X,Y)	**XPLS, XMNS, YPLS, YMNS**				
Differential Voltage Range	differential, Common Mode = 2.5V		2		Vpp
Common Mode Range	For Full Differential Range	0		2.5	V
Offset Voltage	DC		TBD		mV
Differential Input Impedance	f =DC		500		Ώ
	f = 2 GHz		50		
Feedthrough, X or Y	f = 10MHz, X (Y)= 0V, Y (X) = 0dBm, relative to condition where X (Y)=+1V		TBD	-35	dB
	f = 100MHz			-35	
Gain	X=100 MHz and 0dBm, Y=1V		0		dB
CMRR	±1Vp-p, f<1MHz		TBD		dB
~~INTERCEPT~~ OUTPUT OFFSET INPUT (Z)	**ZPLS, ZMNS**				
Differential Voltage Range	Common Mode from 2.5 V down to COMM		2		Vpp
Common Mode Range	For Full Differential Range	0		2.5	V
Gain	From Z to W, F≤10MHz		0		dB
-3 dB Small-Signal Bandwidth			TBD		
Differential Input Impedance	f = DC		500		Ώ
	f = 2GHz		50		
CMRR	±1Vp-p, f<1 MHz		TBD		dB
OUTPUTS (W)	**WPLS, WMNS**				
Differential Voltage Range	No External Common Mode		±2		V
Common Mode Output			2.5		V
Noise Power Spectral Density	X=Y=1V,				dBm/Hz
	f= 10 MHz		-133		
	f= 100 MHz		-133		
	X=Y=0				
	f = 10 MHz		-138		
	f= 100 MHz		-138		
Noise Voltage Spectral Density	X=Y=0, F =10 MHz		10		nV/√Hz
Differential Output Impedance	f = DC		TBD		Ώ
	f = 2GHz		50		
Maximum Current	Sink or source		TBD		mA
DYNAMIC CHARACTERISTICS					
Frequency Range	X, Y, Z to W,	0		2	GHz
	X and Y to W, Z=0				
DC Non-linearity	X(Y)= ±1V, Y(X)= 1V		TBD		%FS
Slew Rate	W from –2.0V to 2.0V		TBD		V/µs
Settling Time					
OIP3	Two tone IP3 test. X (Y) = 100mVp/tone (-10 dBm into 50 ohms), Y(X)=1,				dBm
	f1= 9.9 MHz, f = 10 MHz		29		
	f1= 99 MHz, f2= 100 MHz,		29		
Output 1 dB Compression Point	X(Y) to W, Y(X)= 1V, 10MHz		TBD		dBm
	100MHz				

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE VOLTAGE	**VMID**				
Set-point			$V_{POS}/2$		V
Maximum Source Current	Common-mode for X, Y, Z = 2.5V		50		mA
Output Impedance			TBD		Ω
POWER AND ENABLE	**VPOS, COMM, ENBL**				
Supply Voltage Range		4.5		5.5	V
Total Supply Current	Common-mode for X, Y, Z = 2.5V		130		mA
PSRR					
Disable Current	ENBL = 0V		TBD		mA

ADL5391 EVALUATION BOARD

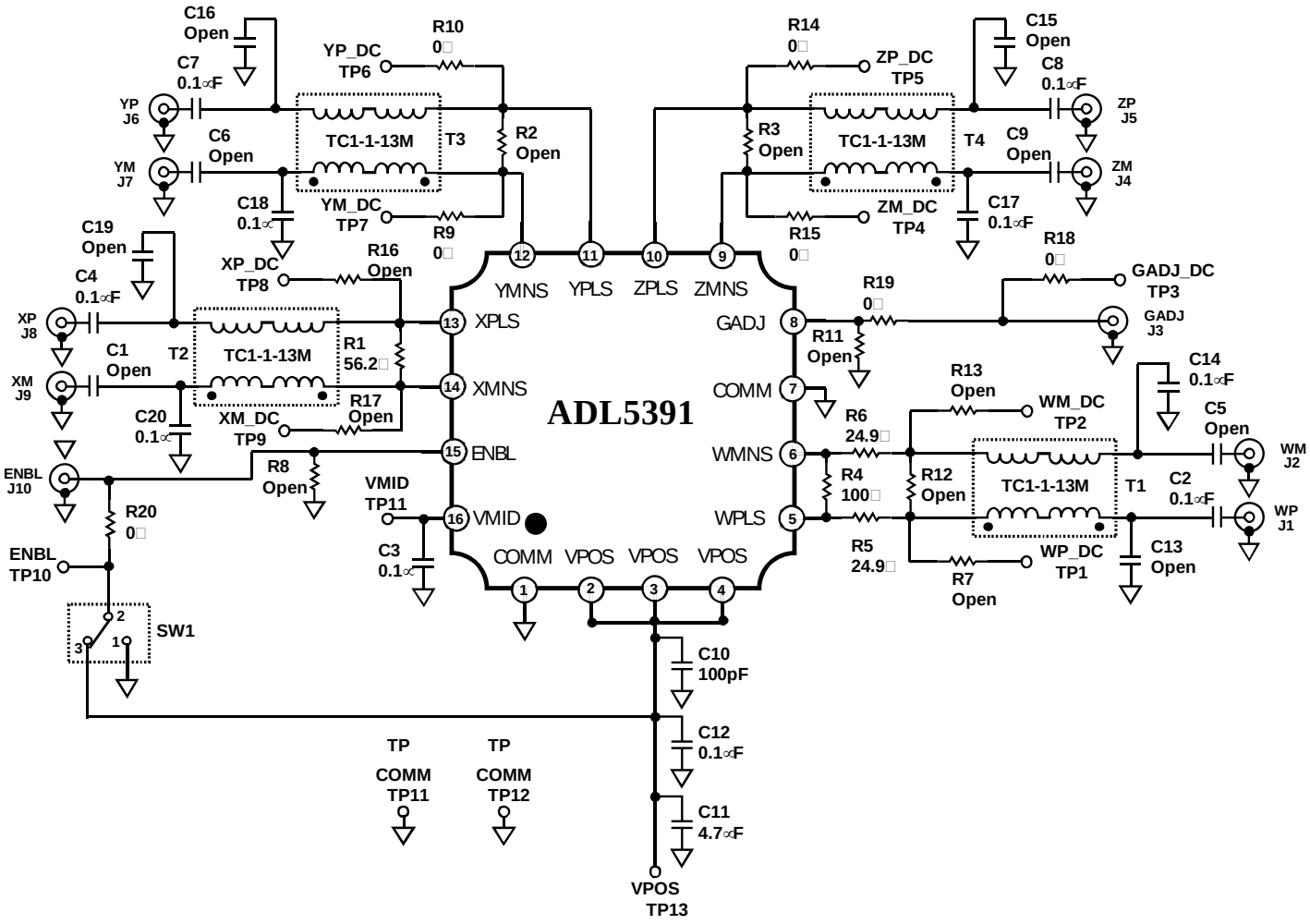

Figure 3. ADL5391-EVALZ Evaluation Board Schematic

Table 3. Evaluation Board Configuration Options

Component	Function	Part Number	Default Value
J1, J5, J6, J8	SMA connectors for single ended high frequency operation. If J5 and J6 are used, R9, R10. R14 and R15 should be removed. R2 and R3 should also be populated in order to match the inputs. If used in broadband operation, C4, C7, C8, and C2 need to be replaced with 0-ohm resistors.		
J2, J4, J7, J9	SMA connectors for broadband differential operation. If these are to be used, baluns should be removed and jumped over using 0-ohm resistors, and C14, C15, C18, and C20 should be removed		
T1, T2, T3, T4	Single ended to differential transformation for high frequency AC operation. If broadband operation is necessary, the baluns can be removed and jumped over using 0-ohm resistors.	TC1-1-13M+ (Mini-Circuits)	T3 and T4 are populated but the Y and Z inputs are set up for DC operation.
	DC Block capacitors		.1 µF 0603 capacitor
C2, C8, C7, C4, C14, C17, C18, C20	DC Block capacitors		.1 µF 0402 capacitor
C5, C9, C6, C1, C13, C15, C16, C19	Not installed DC Block capacitors		Open 0402 capacitor
R18, R15, R14, R10, R9	Snubbing Resistors		0 Ω 0402 Resistors
R19, R20	Snubbing Resistors		0 Ω 0603 Resistors
R16, R17, R7, R13,	Snubbing Resistors		Open 0402 Resistors
C10	Filter Capacitor		100 pF 0402 Capacitor
C12	Filter Capacitor		.1 µF 0402 capacitor
C3	Filter Capacitor		.1 µF 0603 capacitor
C11	Filter Capacitor		4.7 µF 3216 capacitor
R1	Matching Resistor		56.2 Ω 0603 Resistor
R2, R3, R12	Matching Resistor. Input impedance to X, Y, and Z inputs are the same. For the same frequency R1, R2, and R3 should be the same.		Open 0603 Resistor
R6, R5	Matching Resistor		24.9 Ω 0402 Resistor
R4	Matching Resistor		100 Ω 0603 Resistor
R8, R11	Can be used for voltage divider or filtering		Open 0603 Resistor
SW1	Enable switch: Enable = 5V, Disable = 0V		SW1 installed
WM_DC, WP_DC, XM_DC, XP_DC, YM_DC, YP_DC, ZM_DC, ZP_DC	Green Testloop		
VPOS	Red Testloop		
COMM, COMM2	Black Testloop		
ENBL_DC, GADJ_DC, VMID	Yellow Testloop		
DUT	ADL5391	ADL5391ARUZ	

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