Grounding in Mixed Signal PCB

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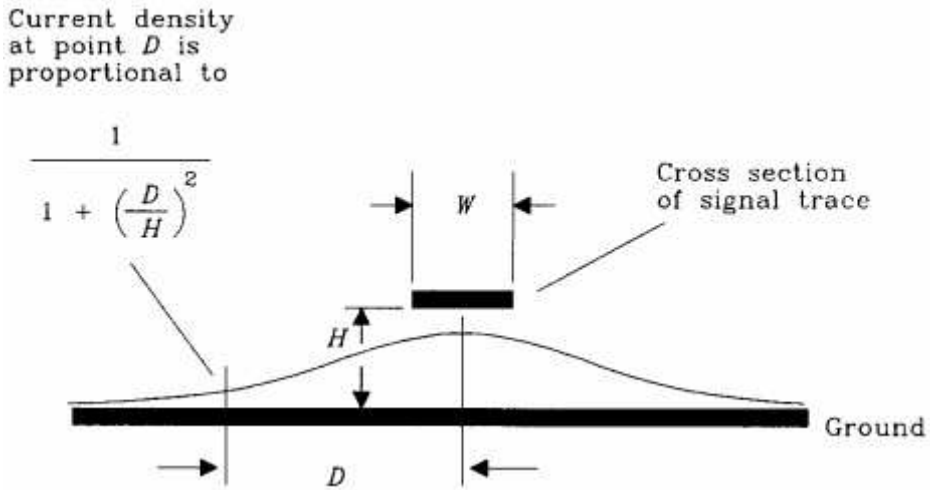
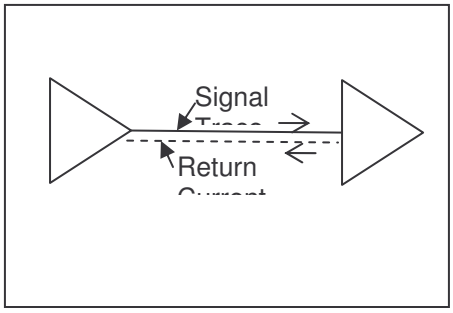
Depending upon your application, there can be signals on your printed circuit board from both analog and digital worlds. And as it happens to be, they cannot stand each other eye-to-eye. The crosstalk and the switching noise from the digital signals can alter the shape and hence, meaning of analog signals. This makes it necessary to shield and isolate sensitive analog signals from noisy digital signals on the PCB.

There are various ways how the board design engineers go about segregating the analog and digital sections on the board. One popular method in practice is to split the reference ground plane in digital and analog portions. The split ground planes here are connected at a single point using a ferrite bead. The method looks good on paper since ferrite beads come handy in limiting the passing of high frequency noise from digital section to analog domain. However, this may give false sense of safety to the board designers.

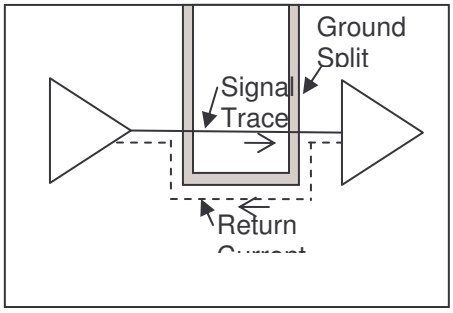
Before we go into the problems that occur because of split grounds, let us revisit the fundamentals of return current. Every electrical signal that runs down a trace on PCB from the driver to the receiver comes back to the driver, in the form of return current. In case of multi-layer boards, this return current flows through the reference plane of that trace that is closest to the trace. Below figure taken from Howard Johnson's high-speed digital design book depicts the current distribution of a return signal on the reference plane of the trace.



As per the above figure, the current distribution of return signal is highest directly beneath the signal trace and gradually decreases as the distance from the trace increases. But if the return signal is not provided a path directly beneath the signal trace, it tries to stay as close to the signal trace as possible. Following figures show the behavior of return signal:



Return current flowing directly beneath the trace in case of solid



Return current flowing around the split in case of slotted ground plane

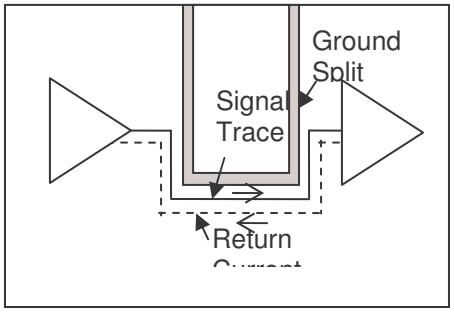
As shown in the above figure, when a signal trace is routed above the split plane, the return signal is forced around the split. This circuitous route increases the loop area (area between the trace and its return current) of the signal. The emissions generated by a particular signal trace are directly related to the loop area. As a result, the splits in ground planes become a factor in increasing the noise instead of decreasing it.

Another problem related to the above scenario is the change in trace impedance. To maintain the constant trace impedance along its entire route, it is necessary that the trace is routed above a solid reference plane. But when the trace is routed above the split as in the case mentioned, the trace impedance changes variably. This results in unwanted reflections in the electrical signals affecting the performance of high rise time systems.

The better approach will be to route traces around the splits so that signal traces are close to their return currents at all times.

But a still better approach will be to use a virtual split instead of actual split to segregate the analog and digital sections of the board. This is how it can be done:

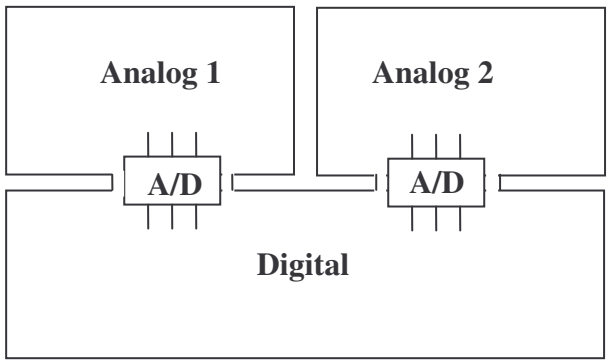
1. While creating the schematic, give different names to the analog and digital grounds. If your design has different analog sections, give different names to the different analog grounds that may exist in your schematic as well, for example video ground and audio ground. This will make sure that the layout engineer can easily differentiate between different analog and digital sections from the netlist.
2. At the time of component placement, take extra care to divide the board between distinct analog and digital sections. This will ensure that digital and analog traces remain in their own real estate.
3. Work with layout engineer to split the ground plane in analog and digital sections based upon the component placement. If there are multiple ground plane layers in the PCB, they should be identical. In no case whatsoever, should the analog ground of one layer should overlap the digital ground of another layer.
4. If there is an ADC in the design, the ground layer split should run across the ADC dividing the ADC between analog and digital area as per its pin assignment.
5. At the time of routing, enforce strict routing discipline to make sure that none of the analog or digital traces crosses the split. Taking example from the previous figure, the trace should be routed around the split to minimize emission and impedance problems.



6. Depending upon the design, there will be few traces that will need to cross over from analog to digital section or vice versa. Assign a quite area in the PCB where all these traces will cross the split in the form of a narrow bridge.

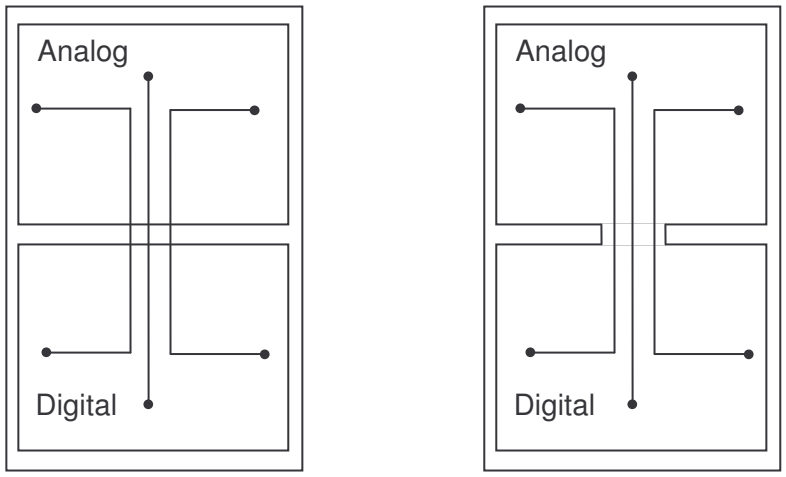
By the time above steps are taken care of, the splits in the ground plane will overrun their use in most of the cases. Once the routing is frozen, you can connect different grounds in the schematic and merge all the different grounds in one single solid reference ground plane. This should work flawlessly for most of the cases.

There will be few cases, where greater isolation is required. This can be because of PCB size constraints or when higher resolution ADC (more than or equal to 14 bits) is used. In such a scenario, maintain the split between analog and digital sections. However, connect the splits solidly to each other directly beneath the ADC. Following figure gives an example of such a case.



Note that even in the above case, the splits are connected to each other solidly instead of using a ferrite bead.

In case if splits are supposed to be maintained, and there are crossover signals that go from one domain to another as mentioned in step 6, provide a bridge in the ground plane directly beneath the region where these traces are crossing over.



At the time of routing

After routing

Keeping above points in mind can save a lot of hassles at the time of EMI testing. May the ground be with you!

References:

1. H.W. Ott, **Noise Reduction Techniques in Electronic Systems, Second Edition**, John Wiley & Sons, Inc., New York, 1988.
2. Howard W. Johnson and Martin Graham, **High-Speed Digital Design**, PTR Prentice Hall, 1993.