- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**

- **Very Low Power Consumption . . . 5 mW Typ**

- **Wide Driver Supply Voltage Range . . . $\pm$4.5 V to $\pm$15 V**

- **Driver Output Slew Rate Limited to 30 V/μs Max**

- **Receiver Input Hysteresis . . . 1000 mV Typ**

- **Push-Pull Receiver Outputs**

- **On-Chip Receiver 1-μs Noise Filter**

- **Functionally Interchangeable With Motorola MC145406 and Texas Instruments TL145406**

- **Package Options Include Plastic Small-Outline (D, DW, NS) Packages and DIPs (N)**

SN65C1406 . . . D PACKAGE
SN75C1406 . . . D, DW, N, OR NS PACKAGE
(TOP VIEW)

V_{DD}	1	16	V_{CC}
1RA	2	15	1RY
1DY	3	14	1DA
2RA	4	13	2RY
2DY	5	12	2DA
3RA	6	11	3RY
3DY	7	10	3DA
V_{SS}	8	9	GND
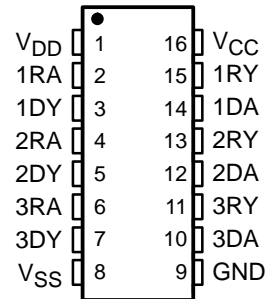
description

The SN65C1406 and SN75C1406 are low-power BiMOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices are designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs, and the receivers have filters that reject input noise pulses shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1406 and SN75C1406 are designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from –40°C to 85°C. The SN75C1406 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

	PACKAGED DEVICES			
T_A	SMALL OUTLINE (D)	SMALL OUTLINE (DW)	PLASTIC DIP (N)	PLASTIC SMALL OUTLINE (NS)
–40°C to 85°C	SN65C1406D	—	—	—
0°C to 70°C	SN75C1406D	SN75C1406DW	SN75C1406N	SN75C1406NS

The D, DW, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., SN75C1406DR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

logic diagram (positive logic)

Typical of Each Receiver

RA ——— 2, 4, 6 ———◯▷ 15, 13, 11 ——— RY

Typical of Each Driver

DY ——— 3, 5, 7 ———▷◯ 14, 12, 10 ——— DA

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265
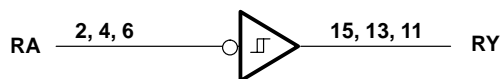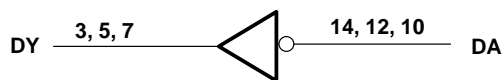
schematics of inputs and outputs

EQUIVALENT DRIVER INPUT

Input DA

Internal 1.4-V Reference

V_{DD}

V_{SS}

GND

EQUIVALENT DRIVER OUTPUT

VDD

160 Ω

74 Ω

Output DY

72 Ω

V_{SS}

EQUIVALENT RECEIVER INPUT

Input RA

3.4 kΩ

1.5 kΩ

ESD Protection

ESD Protection

530 Ω

GND

EQUIVALENT RECEIVER OUTPUT

V_{CC}

Output RY

GND
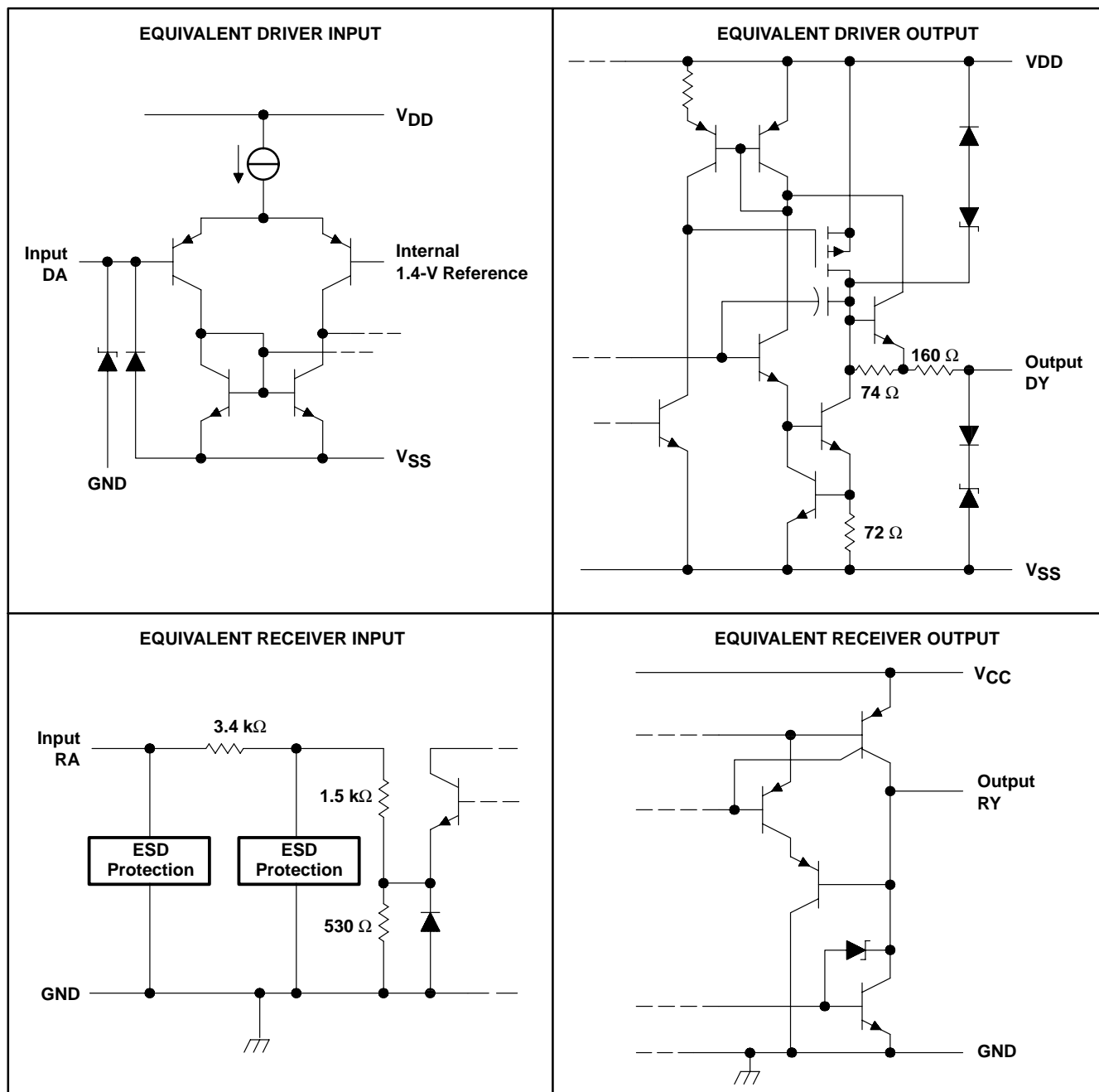
All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{DD} (see Note 1) . . . . 15 V

V_{SS} . . . . −15 V

V_{CC} . . . . 7 V

Input voltage range, V_I: Driver . . . . V_{SS} to V_{DD}

Receiver . . . . −30 V to 30 V

Output voltage range, V_O: Driver . . . . (V_{SS} − 6 V) to (V_{DD} + 6 V)

Receiver . . . . −0.3 V to (V_{CC} + 0.3 V)

Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 73°C/W

DW package . . . . 57°C/W

N package . . . . 67°C/W

NS package . . . . 64°C/W

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

Storage temperature range, T_{stg} . . . . −65°C to 150 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	12	15	V
V_{SS}	Supply voltage		−4.5	−12	−15	V
V_{CC}	Supply voltage		4.5	5	6	V
V_I	Input voltage	Driver	V_{SS}+2		V_{DD}	V
		Receiver			±25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output curren				3.2	mA
T_A	Operating free-air temperature	SN65C1406	−40		85	°C
		SN75C1406	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 0.8 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
				V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 3)	V_{IH} = 2 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
				V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				1	µA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1	µA
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	−7.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{DD},	See Figure 1	7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		115	250	µA
				V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	µA
				V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_O	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, See Note 4	V_O = −2 V to 2 V,		300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
4. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output¶	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3	0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output¶	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3	0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
t_{THL}	Transition time, high- to low-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3	4	10	30	V/µs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform
# Measured between 3-V and −3-V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low

TEXAS INSTRUMENTS

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V $\pm$ 10% (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5			1.7	2	2.55	V
V_{IT-}	Negative-going input threshold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis voltage (V_{IT+}−V_{IT-})				600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA,	See Figure 5 and Note 5		3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V		2.8	4.4		
			V_{CC} = 5 V		3.8	4.9		
			V_{CC} = 5.5 V		4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA,	See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 2.5 V			3.6	4.6	8.3	mA
		V_I = 3 V			0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −2.5 V			−3.6	−5	−8.3	mA
		V_I = −3 V			−0.43	−0.55	−1	
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.75 V, V_O = 0,	See Figure 4			−8	−15	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = V_{CC}, V_O = V_{CC},	See Figure 4			13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V			320	450	μA
			V_{DD} = 12 V, V_{SS} = −12 V			320	450	

† All typical values are at T_A = 25°C.
NOTE 5: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs remain in the high state.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V $\pm$ 10% (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6			3	4	μs
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6			3	4	μs
t_{TLH}	Transition time, low- to high-level output‡	C_L = 50 pF, R_L = 5 kΩ, See Figure 6			300	450	ns
t_{THL}	Transition time, high- to low-level output‡	C_L = 50 pF, R_L = 5 kΩ, See Figure 6			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§	C_L = 50 pF, R_L = 5 kΩ		1		4	μs

‡ Measured between 10% and 90% points of output waveform
§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

TEXAS
INSTRUMENTS

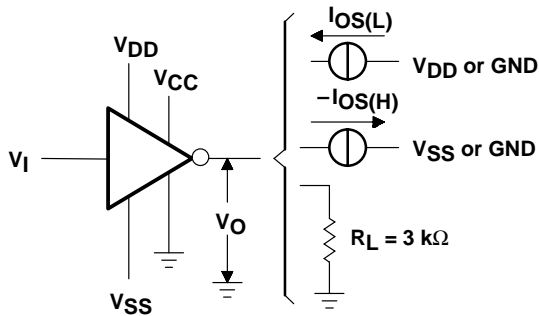## PARAMETER MEASUREMENT INFORMATION

Figure 1. Driver Test Circuit
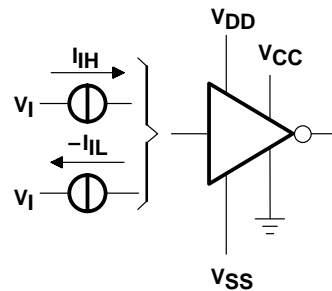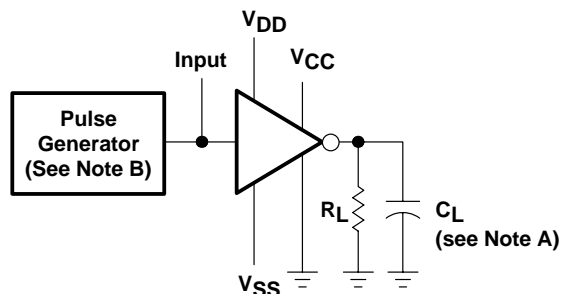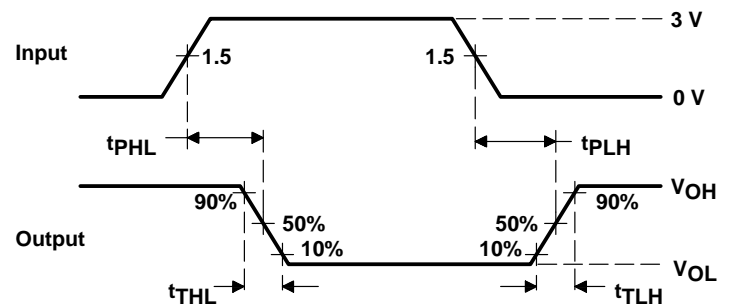V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

Figure 2. Driver Test Circuit, I_{IL}, I_{IH}

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.

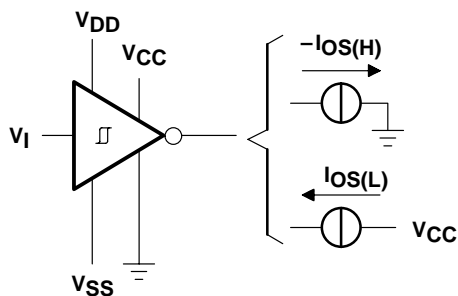**Figure 3. Driver Test Circuit and Voltage Waveforms**

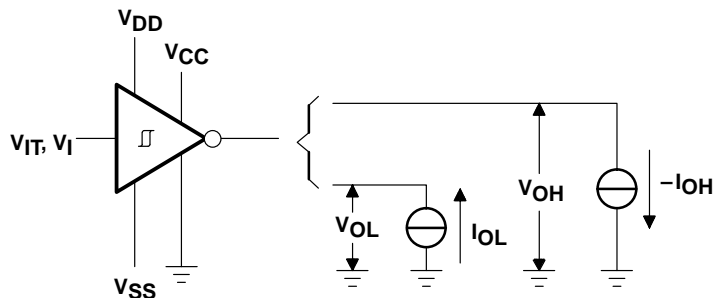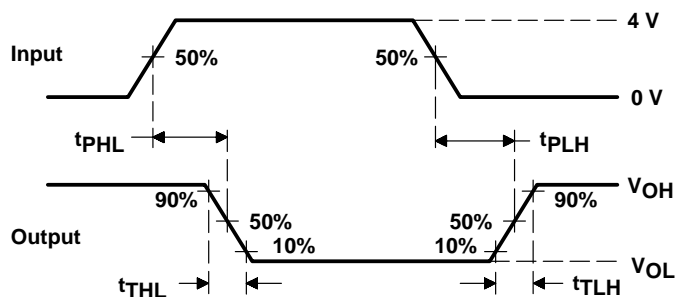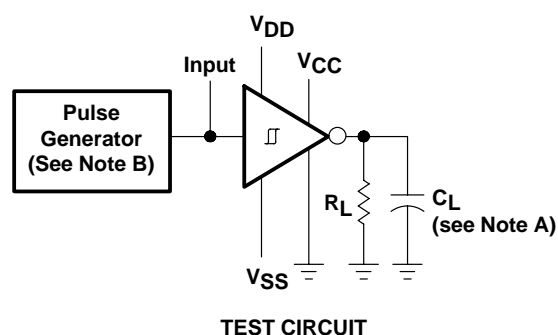**Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$**

Figure 5. Receiver Test Circuit, V_{IT}, V_{OL}, V_{OH}

![Texas Instruments logo] **TEXAS INSTRUMENTS**

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: C. C_L includes probe and jig capacitance.
D. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.

Figure 6. Receiver Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

The TIA/EIA-232-F specification is for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. Many TIA/EIA-232-F devices will operate at higher data rates with lower capacitive loads (short cables). For reliable operation at greater than 20 kbit/s, the designer needs to have control of both ends of the cable. By mixing different types of TIA/EIA-232-F devices and cable lengths, errors can occur at higher frequencies (above 20 kbit/s). When operating within the TIA/EIA-232-F requirements of less than 20 kbit/s and with compliant line circuits, interoperability is assured. For applications operating above 20 kbit/s, the design engineer should consider devices and system designs that meet the TIA/EIA-232-F requirements.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65C1406D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65C1406DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65C1406DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65C1406DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65C1406N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN75C1406D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75C1406DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C1406DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C1406DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C1406DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C1406N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C1406NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C1406NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C1406NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
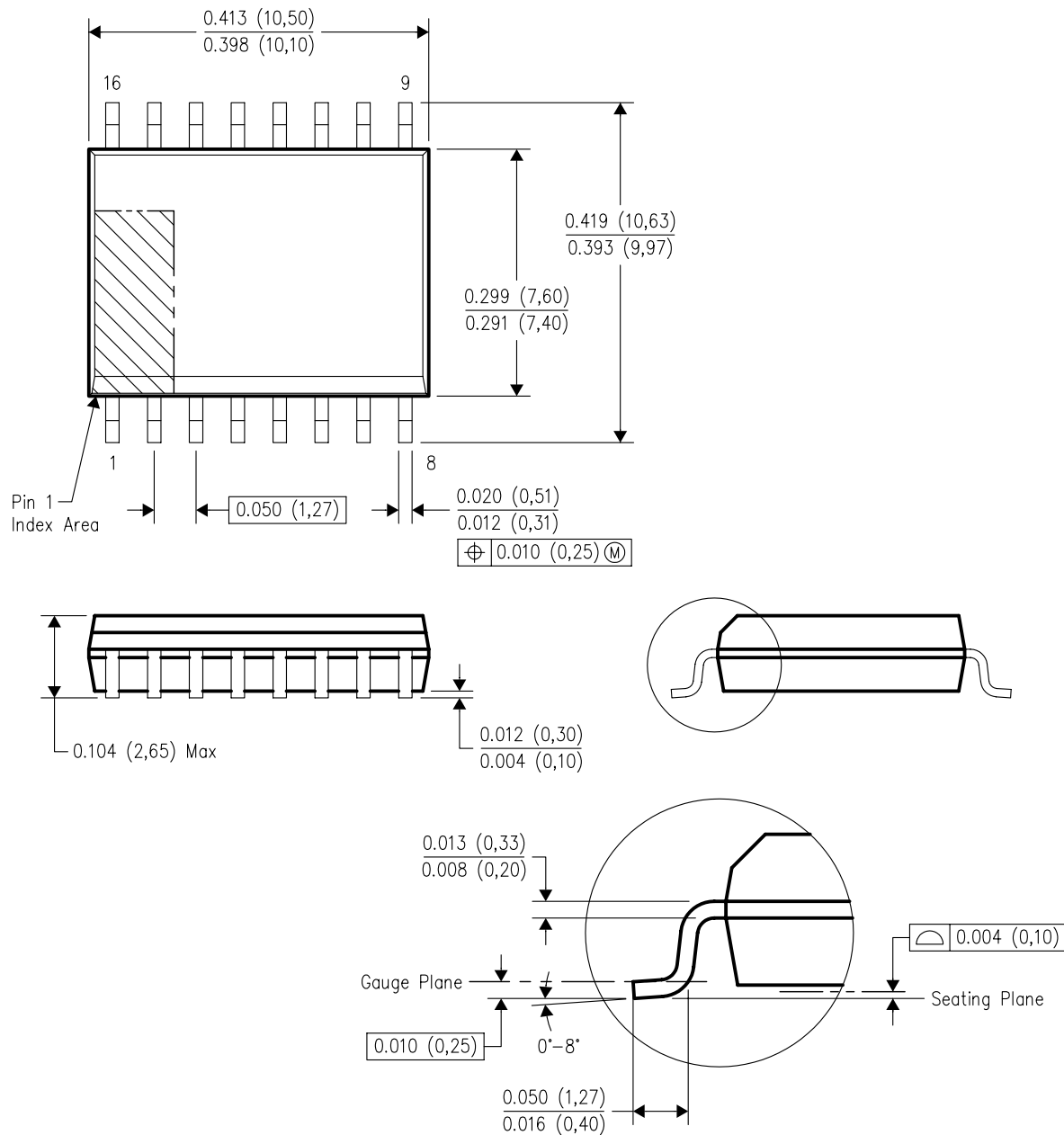   D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F   07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS−012 variation AC.

DW (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−2/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

MECHANICAL DATA

NS (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
              B. This drawing is subject to change without notice.
              C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                            Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated