USB Blaster Emulation with HPSDR Ozy

The idea is to use the FX2 chip and the Cyclone II FPGA on Ozy to emulate the Altera USB Blaster so that FPGAs on the other boards sitting on the Atlas bus slots can be easily programmed.

The USB Blaster emulation has already been attempted and the code is available under the GNU GPL, thanks to the great work done by kolja waschk <usbjtag@ixo.de>. The projected is hosted at <http://www.ixo.de/info/usb_jtag/>.

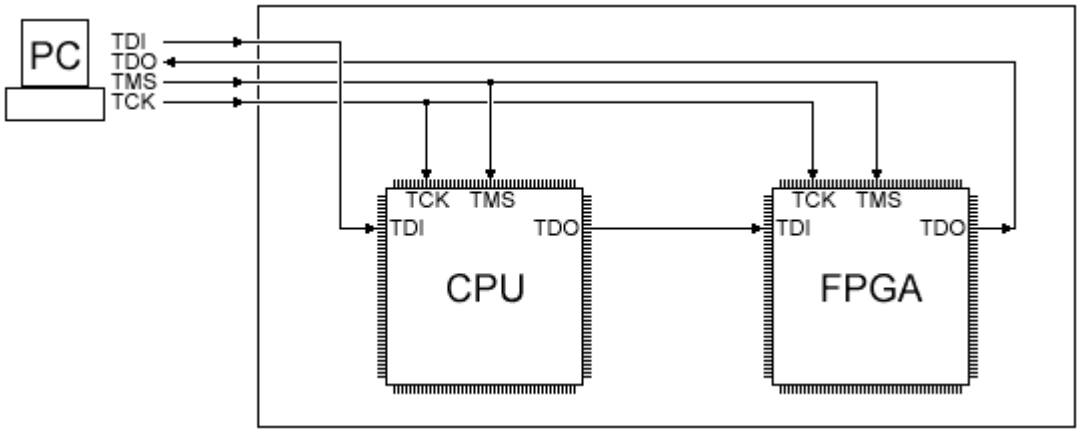
This code has been ported to the Ozy board and we use the following 4 pins for the JTAG pins.

FX2 Port	JTAG signal
B0	TDI
B1	TDO
B2	TCK
B3	TMS

The following Atlas lines are used for JTAG use:

Atlas line	JTAG signal
A23	TMS
A24	TCK
A25	SDOBACK
A27	TDO (in)
A29	TDI

Now, JTAG chaining works as shown in the below diagram. Picture used from the fpga4fun website *without* permission and is copyrighted by fpga4fun.com KNJN LLC.



As we see, the TDO goes into the TDI of the next device in the chain. To facilitate the chaining of devices, the designers of HPSDR Atlas have routed the A27 line of N^{th} slot to the A29 line of the $(N+1)^{th}$ slot. The last board plugged in should have a jumper which routes the TDO pin and connects it to the SDOBACK signal. So the only requirement here is that the boards should be in the adjuscent slots in the increasing order, otherwise the chain gets broken.

Now in the Cyclone II FPGA on Ozy, we take the FX2 JTAG emulation signals and route the signals into the appropriate Atlas lines.

Here is the routing table as performed by the FPGA code.

Atlas Line	FX2 pin
A23 (input)	B3 (output)
A24 (input)	B2 (output)
A25 (output)	B1 (input)
A27 (input)	B0 (output)

Let us take an example where Ozy is sitting in slot N and Janus in slot (N+1) and we have the jumper connecting TDO and SDOBACK on Janus in place. Apart from TMS and TCK, we put out the FX2 TDI signal (B.0) into the TDO line of Atlas (A27) slot N, which gets crossed into TDI of the slot (N +1). The TDO of slot (N+1) gets connected to SDOBACK line (A25) which is read into the FX2 port B.1.

To get the Ozy blaster working, do the following steps.

1. Load the standard OzyJanus firmware into Ozy.
2. Load Ozy SDR1000 FPGA configuration (RBF).
3. Load the FPGA configuration (RBF) at <svn://206.216.146.154/svn/repos_sdr_hpsdr/trunk/vu3rdd/trunk/vu3rdd/usb_blaster_fpga>.
4. Load the FX2 firmware std.ihx from the SVN at <svn://206.216.146.154/svn/repos_sdr_hpsdr/trunk/vu3rdd/usb_jtag/firmware>.

This should load the drivers for Altera USB Blaster. Now fire up your Quartus and hack away!