

Recent Developments in Low Cost Digital Receivers at OSU

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Key Technologies

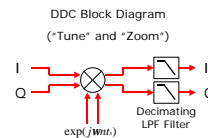
AD Converters

- Real Sampling
 - AD6640 (\$60)
 - 65 MSPS
 - Single 12-bit
 - SFDR -80dB
- Complex Sampling
 - AD9281 (\$5)
 - 28 MSPS
 - Dual 8-bit
 - SFDR -65dB



Digital Down Conversion

- AD6620 Digital Receive Signal Proc.
- Programmable bandwidth and decimation
- Digitally tunable (no I-Q imbalance)
- Low cost \$20 component
- Input can be real or complex (up to 16-bit)
- Complex 16-bit output



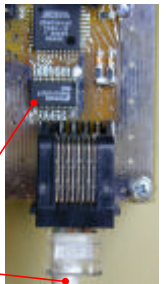
Reconfigurable FPGA's

- Uses:
 - LVDS glue logic
 - I-Q correction
 - DSP operations
 - Clock control
 - Interfacing
 - Signal conditioning
 - Possible DDC functionality
- 2.5V, 3.3V, 5.0V
- Low cost
 - EPM7064 \$6.30
 - EPM7128 \$14.00
 - EP1K30 \$12.50



LVDS Communication

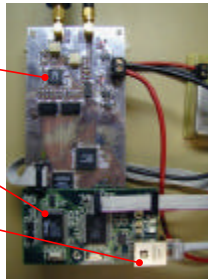
- LVDS - Low Voltage Differential Signaling
- 10-bit parallel input at 66MHz (660Mbps)
- Distances up to 10m
- Low EMI
- Low power (Rx & Tx 500mW)
- Low cost components DS72LV1023/1224 \$14 each
- Low cost CAT-5 cable (8 wire - 2 wires used)



Technology Demonstrations

#1: ADC-DDC-FIFO- C-Ethernet

- Real sampling at 12-bit 65 MSPS
- 256k sample FIFO captures output
- Onboard C (Rabbit Controller) Programs DDC
- Data transferred via Ethernet (10Mb/s)
- \$250 each.



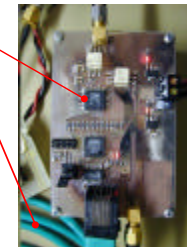
#2: ADC-DDC-LVDS- C

- Real sampling at 12-bit 65 MSPS
- Designed to sit in a back plane
- C (Rabbit) controls each DDC
- Low bandwidth LVDS output
- \$150 each.



#3: ADC-LVDS

- Real sampling at:
 - 10-bit 65 MSPS
 - 12-bit 32 MSPS
- 8-wire Cat-5 cable can also contain:
 - Power
 - LVDS ADC clock
 - Mode (10/12-bit)
- Compatible with #4 cable
- 325mA@6V
- \$100 each



Acknowledgments

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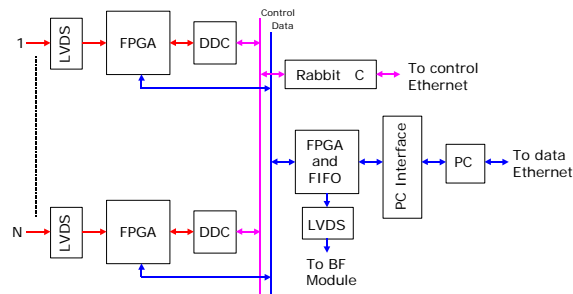
Scalable Array Receiver

#4: Complex DC-ADC-LVDS

- Onboard high pass 900MHz filter and LNA
- Tunable range of 950-2150MHz using MAX2105 direct conversion receiver (\$7)
- Complex Sampling at 20 MSPS using matched dual 8-bit ADC
- 8-wire Cat-5 cable contains:
 - Power (12V)
 - LVDS ADC clock
 - Digital AGC gain
 - Continuous 2x8-bit LVDS Output (16MHz of BW)
- 400mA@12V
- \$130 each

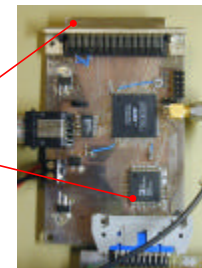


A New Array Processing Architecture



Array Receiver/Multiplexer Prototype

- LVDS receiver (can be complex or real)
- ACEX FPGA can contain:
 - High speed (80Mbytes/s) PCI-DIO-32HS interface to PC
 - Digital IQ correction
 - DDC interface
- Outputs could be:
 - Down converted data
 - Multiplexed data output
 - Beamformer output
- \$130 per digital backend



Conclusions

- Cost effective direct IQ conversion has high potential for array applications. (32 antenna system \$20k)
- LVDS in combination with small FPGAs form a high-speed, low-cost, flexible communications media.
- High BW sampling at antenna increases post-processing potential in back-end.
- Small, cost effective, FPGAs enable DSP operations on each antenna output.
- AD6620 DDC cost effective BW reducer. (Could be part of the FPGA firmware)