PEX 8111BB
PCI Express-to-PCI Bridge
Data Book

Version 1.1

December 2005

Website www.plxtech.com
Technical Support www.plxtech.com/support/
Phone 408 774-9060
800 759-3735
FAX 408 774-2169

Revision History

Revision	Date	Description of Changes
1.0	November, 2005	Initial Production release Silicon Revision BB.
1.1	December, 2005	Table 16-2 – Corrected JTAG IDCODE values in Version column. Table 17-1 – Removed "Ambient Temperature" row. Table 18-2 – Corected 161-Ball FBGA Package ball pitch dimension. Global (2 places) – Changed "PCI Express host" to "PCI Express Root Complex." Section 5.1.1.2 – Added note regarding *No Snoop* and *Relaxed Ordering* bits. Register 14-56, (Offset 68h; DEVCTL) PCI Express Device Control, Bits [3:0] – Added "Valid only in Forward Bridge mode" to bit descriptions. Register 14-82, (Offset 101Ch; POWER) Power – Added "(Forward Bridge Mode Only" to register title. Figure 18-3 – Corrected title.

Order Number: 8111-SIL-DB-P1-1.1

Preface

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Scope

This document describes the PEX 8111 bridge operation and provides operational data for customer use.

Intended Audience

This data book provides the functional details of PLX Technology PEX 8111 for both hardware designers and software/firmware engineers. This data book assumes that the reader has access to and is familiar with the documents referenced below.

Supplemental Documentation

This data book assumes that the reader is familiar with the documents referenced below.

- PCI Special Interest Group (PCI SIG)

  5440 SW Westgate Drive #217, Portland, OR 97221 USA

  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com

  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  - *PCI Bus Power Management Interface Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- The Institute of Electrical and Electronics Engineers, Inc.

  445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA

  Tel: 800 678-4333 (domestic only) or 732 981-0060, Fax: 732 981-1721, http://www.ieee.org

  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  - *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*

Supplemental Documentation Abbreviations

Note: *In this data book, shortened titles are provided to the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Mgmt. r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PCI Express r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express-to-PCI/ PCI-X Bridge r1.0	*PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*

Data Assignment Conventions

Data Width	PEX 8111 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	DWORD/DWord/Dword
8 bytes (64 bits)	QWORD/QWord/Qword

Terms and Abbreviations

The following table lists common terms and abbreviations used in this document. Terms and abbreviations defined in the *PCI Express r1.0a* are not included in this table.

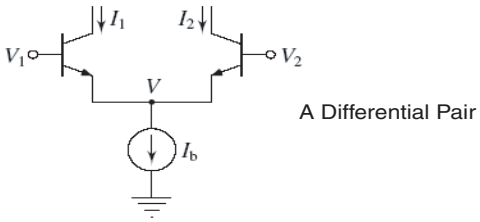
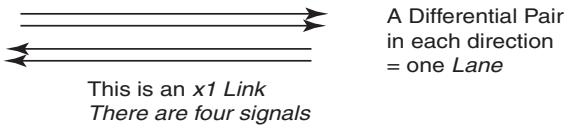
Terms and Abbreviations

Acronym	Definition
#	Indicates an Active-Low signal.
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges the signal receipt.
ADB	Allowable Disconnect Boundary.
ADQ	Allowable Disconnect Quantity. In PCI Express, the ADQ is a buffer size. Used to indicate memory requirements or reserves.
BAR	Base Address Register.
Byte	8-bit quantity of data.
CA	Completion with Completer Abort status.
CFG	Access initiated by PCI Configuration transactions on the primary bus.
Clock cycle	One period of the PCI Bus clock.
Completer	Device addressed by a *requester*.
CRS	Configuration Retry Status.
CSR	Configuration Status register; Control and Status register; Command and Status register
DAC	Dual Address cycle. A PCI transaction wherein a 64-bit address is transferred across a 32-bit data path in two Clock cycles.
Destination Bus	Target of a transaction that crosses a bridge is said to reside on the destination bus.
DLLP	Data Link Layer Packet (originates at the Data Link Layer); can contain Flow Control (FCx DLLPs) acknowledge packets (ACK and NAK DLLPs); and power management (PMx DLLPs).
Downstream	Transactions that are forwarded from the primary bus to the secondary bus of a bridge are said to be flowing downstream.
DWORD	32-bit quantity of data.
ECRC	End-to-end Cyclic Redundancy Check (CRC)
EE	Access initiated by the Serial EEPROM Controller during initialization.
Endpoints	Devices, other than the Root Complex and switches, that are requesters or completers of PCI Express transactions. • Endpoints may be PCI Express endpoints or ***legacy*** endpoints. • ***Legacy*** endpoints can support I/O and Locked transaction semantics. PCI Express endpoints do not support I/O and Locked transaction semantics.
FCP	Flow Control Packet devices on each link exchange FCPs, which carry *header* and *data payload* credit information for one of three packet types – Posted Requests, Non-Posted Requests, and Completions.
Forward Bridge mode	The primary bus is closest to the PCI Express Root Complex.
host	Computer that provides services to computers that connect to it on a network. Considered to be in charge of the other devices connected to the bus.

Terms and Abbreviations *(Cont.)*

Acronym	Definition
HwInit	Hardware initialized register or register bit. The register bits are initialized by a PEX 8111 hardware initialization mechanism or PEX 8111 Serial EEPROM register initialization feature. Register bits are Read-Only after initialization and are reset only with a Cold or Warm reset.
I	CMOS Input.
I/O	CMOS Bi-Directional Input Output.
Lane	Differential signal pair in each direction.
Layers	PCI Express defines three layers: • ***Transaction Layer*** – The primary function of the Transaction Layer is assembly and disassembly of TLPs. The major components of a transaction layer packet (TLP) are Header, Data Payload, and an optional Digest Field. • ***Data Link Layer*** – The primary task of the Data Link Layer is to provide link management and data integrity, including error detection and correction. This layer defines the data control for PCI Express. • ***Physical Layer*** – The primary value to users is that this layer appears to the upper layers to be PCI. It connects the lower protocols to the upper layers.
MM	Access initiated by PCI Memory transactions on the primary or secondary bus, using the address range defined by **PCI Base Address 0**.
MSI	Message Signaled Interrupt.
NAK	Negative Acknowledge.
Non-Posted Transaction	A Memory Read, I/O Read or Write, or Configuration Read or Write that returns a completion to the master.
NS	No Snoop.
O	CMOS Output.
OD	Open Drain.
Originating Bus	Master of a transaction that crosses a bridge is said to reside on the originating bus.
Packet Types	There are three packet types: • ***TLP***, Transaction Layer Packet • ***DLLP***, Data Link Layer Packet • ***PLP***, Physical Layer Packet
PCI	PCI Compliant
PCI	Peripheral Component Interconnect. A PCI Bus is a high-performance bus that is 32 bits or 64 bits wide. It is designed to be used with devices that contain high-bandwidth requirements (*such as*, the display subsystem). It is an I/O bus that retains the ability to be dynamically configured.
PCI Master (Initiator)	Drives the Address phase and transaction boundary (FRAME#). Initiates a transaction and drives data handshaking (IRDY#) with the target.
PCI Target	Claims the transaction by asserting DEVSEL# and handshakes the transaction (TRDY#) with the initiator.
PCI Transaction	Read, Write, Read Burst, or Write Burst operation on the PCI Bus. Includes an Address phase, followed by one or more Data phases.
PCI Transfer	During a transfer, data is moved from the source to the destination on the PCI Bus. TRDY# and IRDY# assertion indicates a Data transfer.
PCIE	PCI Express.

Terms and Abbreviations *(Cont.)*

Acronym	Definition
Port	Interface between a PCI Express component and the ***link***. Consists of transmitters and receivers. • An ***ingress*** port receives a packet. • An ***egress*** port transmits a packet. • A ***link*** is a physical connection between two devices that consists of x*N* ***lanes***. • An x1 link consists of one Transmit and one Receive signal, where each signal is a differential pair. This is one lane. There are four lines or signals in an x1 link.  
Posted Transaction	Memory write that does not return a completion to the master.
Primary Bus	Bus closest to the PCI Express Root Complex (Forward Bridge mode) or the PCI host CPU (Reverse Bridge mode).
PU	Signal is internally pulled up.
QoS	Quality of Service.
RC	Root Complex.
RCB	Read Boundary Completion.
Request packet	A *non-posted request packet* sent by a requester has a completion packet returned by the associated completer. A *posted request packet* sent by a requester has no completion packet returned by the completer.
Requester	Device that originates a transaction or puts a transaction sequence into the PCI Express fabric.
Reverse Bridge Mode	The primary bus is closest to the PCI host CPU.
RO	Read-Only register or register bit. Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8111 hardware initialization mechanism or PEX 8111 Serial EEPROM register initialization feature.
RO	Relaxed Ordering.
RsvdP	***Reserved*** and Preserved. ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve value read for writes to bits.
RsvdZ	***Reserved*** and Zero. ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.

Terms and Abbreviations *(Cont.)*

Acronym	Definition
RW	Read-Write register. Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	Read-Only Status. Write 1 to clear status register. Register bits indicate status when read; a set bit indicating a status event is cleared by writing 1. Writing 0 to RW1C bits has no effect.
RX	Received Packet.
SC	Successful Completion.
Secondary Bus	The bus farthest from the PCI Express Root Complex (Forward Bridge mode) or the PCI host CPU (Reverse Bridge mode).
STRAP	Strapping pads (*such as*, BAR0ENB#, FORWARD, and EXTARB) must be connected to H or L on the board.
STS	Sustained Three-State Output, Driven High for One CLK before Float.
TC	Traffic Class.
TLP	Translation Layer Packet.
TP	Totem Pole.
TS	Three-State Bi-Directional.
TX	Transmitted Packet.
Upstream	Transactions that are forwarded from the secondary bus to the primary bus of a bridge are said to be flowing upstream.
UR	Unsupported Request.
VC	Virtual Channel.
WO	Write-Only register. Used to indicate that a register is written by the Serial EEPROM Controller.
Word	16-bit quantity of data.

Contents

Registers

Chapter 1 Introduction

1.1 Features

- Standards Compliant
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1 (PCI-to-PCI Bridge r1.1)*
  - *PCI Bus Power Management Interface Specification, Revision 1.1 (PCI Power Mgmt. r1.1)*
  - *PCI Express Base Specification, Revision 1.0a (PCI Express r1.0a)*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 (PCI ExpressBridge r1.0)*
- Forward and reverse transparent bridging between the PCI Express and PCI Buses
- PCI Express Single-Lane Port (one virtual channel)
- PCI Express 2.5 Gbps per direction
- PCI Express full Split Completion protocol
- 32-bit 66 MHz PCI Bus
- Internal PCI Arbiter supporting up to 4 external PCI Masters
- SPI serial EEPROM port
- Internal 8-KB shared RAM available to the PCI Express and PCI Buses
- Four GPIO balls
- Low-power CMOS in 144-ball PBGA or161-ball FBGA package
- 1.5V PCI Express interface operating voltage, 3.3V I/O, 5V tolerant PCI

1.2 Overview

The ExpressLane® PEX 8111 PCI Express-to-PCI Bridge allows for the use of ubiquitous PCI silicon with the high-performance PCI Express Network. As PCI Express systems proliferate, there remain many applications that do not need the extensive bandwidth nor performance features of PCI Express. With the PEX 8111, many existing chips and entire subsystems can be used, without modification, with PCI Express motherboards.

1.2.1 PCI Express Endpoint Interface

- Full 2.5 Gbps per direction
- Single lane and single virtual channel operation
- Compatible with multi-lane and multi-virtual channel PCI Express chips
- Packetized serial traffic with PCI Express Split Completion protocol
- Data Link Layer CRC generator and checker
- Automatic Retry of bad packets
- Integrated low-voltage differential drivers
- 8b/10b signal encoding
- In-band interrupts and messages
- Message Signaled Interrupt (MSI) support

1.2.2 PCI Bus Interface

- *PCI r3.0*-compliant 32-bit, 66 MHz PCI interface
- PCI Master Controller allows PCI Express access to PCI target devices
- PCI Target Controller
  - Allows full transparent access to PCI Express resources
  - Allows Memory-Mapped access to shared RAM and Configuration registers
- PCI Arbiter supports up to four external PCI Bus Masters
- Power Management registers and PCI backplane PME# signal support
- Message Signaled Interrupts (MSI) support

1.2.3 Configuration Registers

- All internal registers are accessible from the PCI Express or PCI Buses
- All internal registers are set up through an external serial EEPROM
- Internal registers allow writes to and reads from an external serial EEPROM
- Internal registers allow control of GPIO balls

1.2.4 Data Transfer Pathways

- PCI transparent bridge access to PCI Express
- PCI Memory-Mapped Single access to internal Configuration registers
- PCI Memory-Mapped Single/Burst access to internal shared RAM
- Indexed Addressing Capability registers (offsets 84h and 88h)
- PCI Configuration access to PCI Configuration registers (Reverse Bridge mode only)
- PCI Express transparent bridge access to PCI Bus targets
- PCI Express Memory-Mapped Single access to internal Configuration registers
- PCI Express Memory-Mapped Single/Burst access to internal shared RAM
- PCI Express Configuration access to PCI Configuration registers (Forward Bridge mode only)

1.3 Block Diagrams

Figure 1-1. PEX 8111 Block Diagram

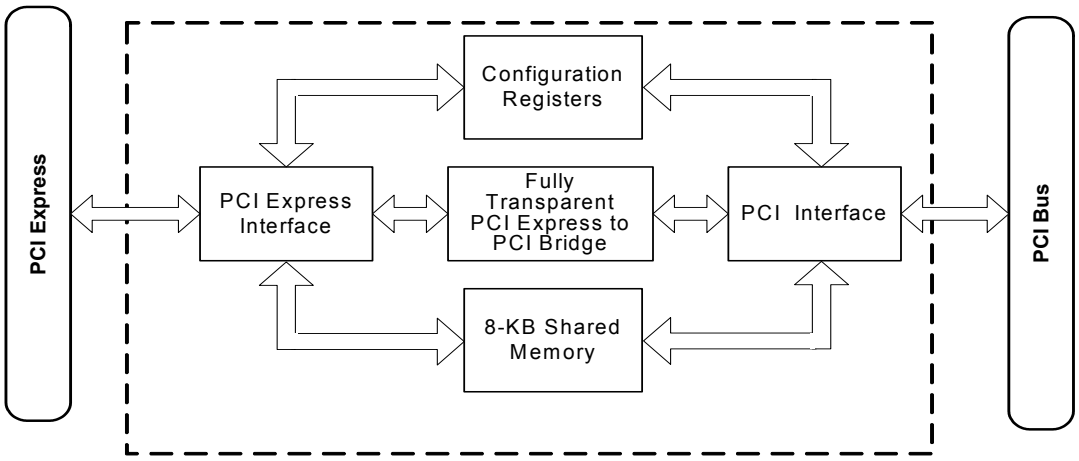


Figure 1-2. PEX 8111 Typical Forward Bridge Block Diagram

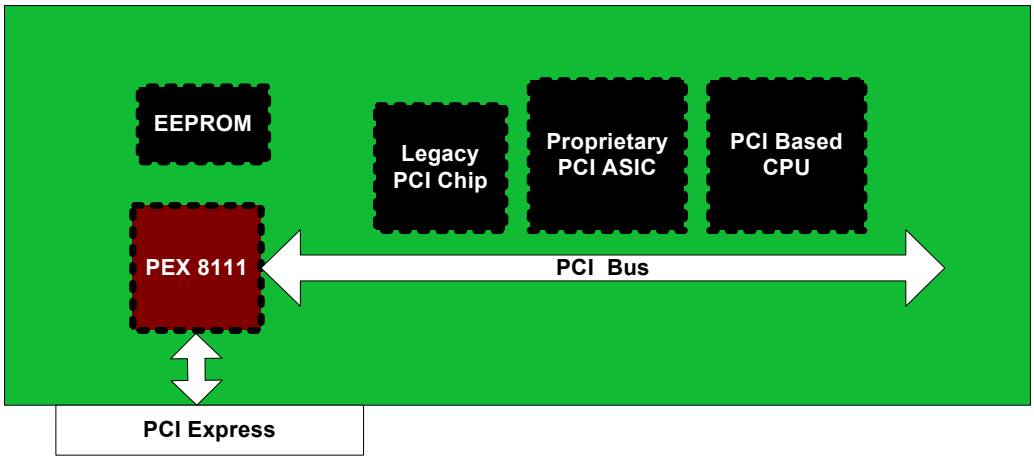
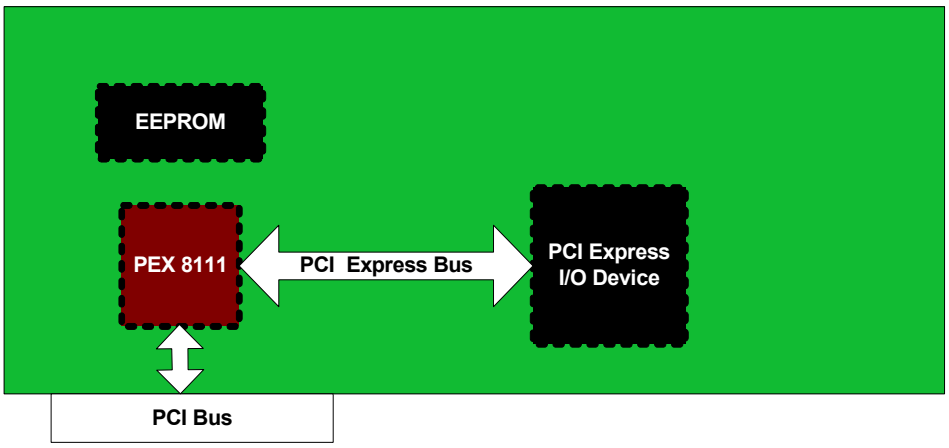


Figure 1-3. PEX 8111 Typical Reverse Bridge Block Diagram



Chapter 2 Ball Descriptions

2.1 Ball Description Abbreviations

Table 2-1. Ball Description Abbreviations (PBGA and FBGA Packages)

Abbreviation	3Description
#	Active low
DIFF	PCI Express Differential buffer
I	Input
I/O	Bi-Directional
O	Output
OD	Open Drain
PCI	PCI-Compatible buffer, 26-mA drive
PD	50K-Ohm Pull-Down resistor
PU	50K-Ohm Pull-Up resistor
S	Schmitt Trigger
STS	Sustained Three-State, driven inactive one Clock cycle before float
TP	Totem Pole
TS	Three-State

2.2 PCI Signal Pull-Up Resistors (Reverse Bridge Mode Only)

The PCI balls listed in this chapter are generic primary and secondary PCI interface pins that do not have internal resistors. When designing motherboards, system slot boards, adapter boards, backplanes, and so forth, the termination of these pins must follow the guidelines detailed in the *PCI r3.0*. The following guidelines are not exhaustive and should be read in conjunction with the appropriate *PCI r3.0* sections.

PCI Control signals require a pull-up resistor on the motherboard, to ensure that these signals are always at valid values when a PCI Bus agent is not driving the bus. For a 32-bit PCI Bus, these Control signals include the following:

- DEVSEL#
- FRAME#
- INT[D:A]#
- IRDY#
- PERR#
- SERR#
- STOP#
- TRDY#

The 32-bit point-to-point and shared bus signals do not require pull-up resistors, as bus parking ensures that these signals remain stable. The INT[D:A]# balls require pull-up resistors, regardless of whether they are used. Depending on the application, M66EN can also require a pull-up resistor. The value of these pull-up resistors depends on the bus loading. The *PCI r3.0* provides formulas for calculating the resistor values. When making adapter board devices where the PEX 8111 port is wired to the PCI connector, pull-up resistors are not required because they are pre-installed on the motherboard. Based on the above, in an embedded design, pull-up resistors can be required for PCI control signals on the bus.

2.3 Ball Description – 144-Ball PBGA Package

Table 2-2. Power and Ground (46 balls) (144-Ball PBGA Package)

Signal	Type	Balls	Description
AVDD	Power	E7	**Analog Supply Voltage** Connect to the +1.5V power supply.
AVSS	Ground	C7	**Analog Ground** Connect to ground.
GND	Ground	A12, B4, C3, C11, D9, E6, F12, G5, H4, H7, J4, J8, K2, K10	**Ground** Connect to ground.
VDD_P	Power	D5	**PLL Supply Voltage** Connect to the +1.5V filtered PLL power supply.
VDD_R	Power	A7	**Receiver Supply Voltage** Connect to the +1.5V power supply.
VDD_T	Power	A5	**Transmitter Supply Voltage** Connect to the +1.5V power supply.
VDD1.5	Power	C10, D4, F6, F8, G6, G7, J9, K3	**PCI Express Interface Supply Voltage** Connect to the +1.5V power supply.
VDD3.3	Power	B3, B11, L2, M10	**I/O Supply Voltage** Connect to the +3.3V power supply.
VDD5	Power	F5, G8, H6	**PCI I/O Clamp Voltage** Connect to the +5.0V power supply for PCI buffers. In a 3.3V PCI environment, connect to the 3.3V power supply.
VDDQ	Power	E5, F9, G4, H5, H8, J7	**I/O Supply Voltage** Connect to the +3.3V power supply for PCI buffers.
VSS_C	Ground	D7	**Common Ground** Connect to ground.
VSS_P0	Ground	D6	**PLL Ground** Connect to ground.
VSS_P1	Ground	C6	**PLL Ground** Connect to ground.
VSS_R	Ground	B8	**Receiver Ground** Connect to ground.
VSS_RE	Ground	F7	**Receiver Ground** Connect to ground.
VSS_T	Ground	C5	**Transmitter Ground** Connect to ground.

Table 2-3. PCI Express Balls (9 balls) (144-Ball PBGA Package)

Signal	Type	Balls	Description
PERn0	I DIFF	B7	**Receive Minus** PCI Express Differential Receive signal.
PERp0	I DIFF	A8	**Receive Plus** PCI Express Differential Receive signal.
PERST#	I/O 6 mA 3.3V	B12	**PCI Express Reset** In Forward Bridge mode, PERST# is an input. Resets the entire chip when asserted. In Reverse Bridge mode, PERST# is an output. Asserted when a PCI reset is detected.
PETn0	O DIFF	A4	**Transmit Minus** PCI Express Differential Transmit signal.
PETp0	O DIFF	B5	**Transmit Plus** PCI Express Differential Transmit signal.
REFCLK-	I DIFF	B6	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz spread spectrum reference clock. Connected to the PCI Express Bus REFCLK- ball in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
REFCLK+	I DIFF	A6	**PCI Express Clock Input Plus** PCI Express differential, 100-MHz spread spectrum reference clock. Connected to the PCI Express Bus REFCLK+ ball in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
WAKEIN#	I 3.3V	C12	**Wake In Signal** In Reverse Bridge mode, WAKEIN# is an input, and indicates that the PCI Express Device requested a wakeup while the link remains in the L2 state.
WAKEOUT#	OD 6 mA 3.3V	A9	**Wake Out Signal** In Forward Bridge mode, WAKEOUT# is an Open Drain output, which is asserted when PMEIN# is asserted and the link remains in the L2 state.

Table 2-4. PCI Balls (63 balls) (144-Ball PBGA Package)

Signal	Type	Balls	Description
AD[31:0]	I/O TS PCI	J10, J12, J11, K12, L9, M9, K8, L8, K7, L7, M7, J6, K6, M6, L6, J5, H2, H1, G3, G2, G1, F4, F3, F2, E4, E3, E2, E1, D2, D1, C1, D3	**Address/Data Bus** The PCI address and data are multiplexed onto the same bus. During the Address phase, AD[31:0] contain the physical address of the transfer. During the Data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and Read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M8, K5, H3, F1	**Command/Byte Enable Bus** The Bus command and Byte Enables are multiplexed onto the same bus. During the Address phase, CBE[3:0]# contain the Bus command. During the Data phase, CBE[3:0]# contain the Byte Enables. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]). **CBE[3:0]# — Command** 0000b — Interrupt Acknowledge 0001b — Special cycle 0010b — I/O Read 0011b — I/O Write 0100b, 0101b — ***Reserved*** 0110b — Memory Read 0111b — Memory Write 1000b, 1001b — ***Reserved*** 1010b — Configuration Read 1011b — Configuration Write 1100b — Memory Read Multiple 1101b — Dual Address Cycle 1110b — Memory Read Line 1111b — Memory Write and Invalidate
DEVSEL#	I/O STS PCI PU (Reverse Bridge mode only)	K4	**Device Select** Indicates that the target (bus slave) decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus was selected.
FRAME#	I/O STS PCI PU (Reverse Bridge mode only)	M5	**Frame** Driven by the initiator. Indicates access start and duration. When FRAME# is first asserted, the Address phase is indicated. When FRAME# is de-asserted, the transaction remains in the last Data phase.
GNT[3:0]#	I/O TS PCI	E11, F11, G9, G10	**Bus Grant** Indicates that the central arbiter granted the bus to an agent. When the internal PCI arbiter is enabled, GNT[3:0]# are outputs used to grant the bus to external devices. When the internal PCI arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8111. GNT[3:1]# are placed into high-impedance state.
IDSEL	I PCI	K9	**Initialization Device Select** Used as a Chip Select during Configuration Read and Write cycles. Each PCI slot or device typically contains an IDSEL connected to a signal address line, allowing the PCI host to select individual sets of Configuration registers. IDSEL is used only in Reverse Bridge mode. In Forward Bridge mode, IDSEL is grounded or pulled up to 3.3V.

Table 2-4. PCI Balls (63 balls) (144-Ball PBGA Package) *(Cont.)*

Signal	Type	Balls	Description
INTA#, INTB#, INTC#, INTD#	I/O OD PCI PU (Reverse Bridge mode only)	E12, E9, D11, E10	**Interrupt** Asserted to request an interrupt. After assertion, must remain asserted until the device driver clears it. INT*x*# is level-sensitive and asynchronous to the CLK. In Forward Bridge mode, INT*x*# is an input from PCI devices. All INT*x*# signals are mapped into Assert_INT*x* and Deassert_INT*x* messages on the PCI Express Bus. In Reverse Bridge mode, INTI# is an output to the PCI Central Resource Function. All Assert_INT*x* and Deassert_INT*x* PCI Express messages are translated to INT*x*# transitions on the PCI Bus.
IRDY#	I/O STS PCI PU (Reverse Bridge mode only)	L5	**Initiator Ready** Indicates that the initiator (bus master) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	M3	**Lock Atomic Operation** Indicates an atomic operation to a bridge that may require multiple transactions to complete. An output in Forward Bridge mode and an input in Reverse Bridge mode.
M66EN	I PCI	D10	**66 MHz Enable** Indicates whether the PCI Bus is operating at 33 or 66 MHz. When low, and the PCLKO divider is 3, the PCLKO ball oscillates at 33 MHz with a 50% Duty cycle. When high, and the PCLKO divider is 3, the PCLKO ball oscillates at 66 MHz with a 33% Duty cycle. Read using the **PCI Control** register *M66EN* bit. Must be grounded in 33 MHz systems.
PAR	I/O TS PCI	J1	**Parity** Even parity is generated across AD[31:0], and CBE[3:0]#. *That is*, the number of ones (1) on AD[31:0], CBE[3:0]#, and PAR is an even number. PAR is valid one clock after the Address phase. For Data phases, PAR is valid one clock after IRDY# is asserted on Write cycles, and one clock after TRDY# is asserted on Read cycles. PAR maintains the same timing as AD[31:0], except it is delayed by one Clock cycle. The bus initiator drives PAR for Address and Write Data phases, and the target drives PAR for Read Data phases.
PCIRST#	I/O OD PCI	F10	**PCI Reset** In Forward Bridge mode, PCIRST# is driven when a PCI Express reset is detected, or when the **Bridge Control** register *Secondary Bus Reset* bit is set. In Reverse Bridge mode, PCIRST# is an input that resets the entire chip. Reset is asserted and de-asserted asynchronously to CLK, and is used to bring a PCI device to an initial state. All PCI signals are asynchronously placed into a high-impedance state during reset.
PCLKI	I PCI	D12	**PCI Clock Input** All PCI signals, except RST# and interrupts, are sampled on the rising edge of PCLKI. Frequency varies from 0 to 66 MHz. Must oscillate during the serial EEPROM initialization sequence.
PERR#	I/O STS PCI PU (Reverse Bridge mode only)	J3	**Parity Error** Indicates that a Data Parity error occurred. Driven active by the receiving agent two clocks following the data that contained bad parity.
PMEIN#	I S PCI	H12	**Power Management Event In** Valid only in Forward Bridge mode. Input used to monitor requests to change the system's power state.

Table 2-4. PCI Balls (63 balls) (144-Ball PBGA Package) *(Cont.)*

Signal	Type	Balls	Description
PMEOUT#	OD 24 mA 3.3V	L12	**Power Management Event Out** Valid only in Reverse Bridge mode. Open-drain output used to request a change in the power state. PMEOUT# is ***not*** 5V tolerant. When used in a system with a 5V pull-up resistor on the PCI backplane PME# signal, an external voltage translation circuit is required.
REQ[3:0]#	I/O TS PCI	H11, G12, H9, G11	**Bus Request** Indicates that an agent requires use of the bus. When the internal PCI arbiter is enabled, REQ[3:0]# are inputs used to service external bus requests. When the internal PCI arbiter is disabled, REQ0# is an output used to request bus control, and REQ[3:1]# are unused inputs.
SERR#	I/O OD PCI PU (Reverse Bridge mode only)	J2	**System Error** Indicates that an Address Parity error, Data Parity error on the special cycle command, or other catastrophic error occurred. Driven active for one PCI clock period, and is synchronous to the CLK. Driven only in Reverse Bridge mode.
STOP#	I/O STS PCI PU (Reverse Bridge mode only)	L4	**Stop** Indicates that the target (bus slave) is requesting that the master stop the current transaction. After STOP# is asserted, STOP# must remain asserted until FRAME# is de-asserted, whereupon STOP# must be de-asserted. Also, DEVSEL# and TRDY# cannot be changed until the current Data phase completes. STOP# must be de-asserted in the clock following the completion of the last Data phase, and must be placed into a high-impedance state in the next clock. Data is transferred when both IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI PU (Reverse Bridge mode only)	M4	**Target Ready** Indicates that the target (bus slave) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.

Table 2-5. Clocks, Reset, and Miscellaneous (14 balls) (144-Ball PBGA Package)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	E8	**PCI Base Address 0 Register Enable** When low, the **PCI Base Address 0** register is enabled. When high, the **PCI Base Address 0** register is enabled by the **Device-Specific Control** register *PCI Base Address 0 Enable* bit.
EECLK	O 3 mA TP 3.3V	B2	**Serial EEPROM Clock** Provides the clock to the serial EEPROM. Frequency is determined by the **Serial EEPROM Clock Frequency** register, and varies from 2 to 25 MHz.
EECS#	O 3 mA TP 3.3V	C4	**Serial EEPROM Chip Select** Active-low Chip Select.
EERDDATA	I 3.3V	A1	**Serial EEPROM Read Data** Used to read data from the device. A 47K-Ohm pull-up resistor is required.
EEWRDATA	O 3 mA TP 3.3V	A2	**Serial EEPROM Write Data** Used to write data to the device.
EXTARB	I 3.3V	K11	**External Arbiter Enable** When low, the internal PCI arbiter services requests from an external PCI device. When high, the PEX 8111 requests the PCI Bus from an external arbiter.
FORWARD	I 3.3V PU	L11	**Bridge Select** When low, the PEX 8111 acts as a PCI-to-PCI Express Bridge (reverse bridge). When high, the PEX 8111 acts as a PCI Express-to-PCI Bridge (forward bridge).
GPIO[3:0]	I/O 12 mA 3.3V PU	A11, B10, A10, C9	**General Purpose I/O** Program as an Input or Output general-purpose ball. Internal device status is also an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **General-Purpose I/O Control** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is low at the trailing edge of RESET#, the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. When GPIO3 is low at the trailing edge of RESET#, the **TLP Controller Configuration 0** register *Delay Link Training* bit is set.
NC1	–	C2	**No Connect** Must remain open.

Table 2-5. Clocks, Reset, and Miscellaneous (14 balls) (144-Ball PBGA Package) *(Cont.)*

Signal	Type	Balls	Description
PCLKO	O 26 mA TP PCI	H10	**PCI Clock Output** Buffered clock output from the internal 100-MHz reference clock, with the frequency depending on the **Device Initialization** register *PCLKO Clock Frequency* field. Signal frequency is 66 MHz when M66EN is high. PCLKO is always driven and oscillates when one of the following occurs: • PCI Express REFCLK-/+ input pins are active. • PCLKO clock divider in **Device Initialization** register is non-zero. • Internal AGEP_RST_B_ signal to Pixie is de-asserted. AGEP_RST_B_ is asserted for: – Pin reset – Power Management reset
PWR_OK	O 6 mA 3.3V	B9	**Power OK** Valid only in Forward Bridge mode. When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the **Power** register, PWR_OK is asserted.

Table 2-6. Test Balls (12 balls) (144-Ball PBGA Package)

Signal	Type	Balls	Description
BTON	I	M11	**Test Enable** Connect to ground for normal operation.
BUNRI	I	D8	**Test Mode Select** Connect to ground for normal operation.
SMC	I	K1	**Scan Path Mode Control** Connect to ground for normal operation.
TCK	I	M2	**Test Clock** Joint Test Action Group (JTAG) test clock. Sequences the TAP controller as well as all PEX 8111 JTAG registers. Ground when JTAG is not used.
TDI	I PU	L3	**Test Data Input** Serial data input to all JTAG instruction and data registers. The Test Access Port (TAP) controller state, as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. Hold open when JTAG is not used.
TDO	O 12 mA 3.3V TS	L1	**Test Data Output** Serial data output for all JTAG instruction and data registers. The TAP controller state, as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed as the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. Placed into a high-impedance state at all other times. Hold open when JTAG is not used.
TEST	I	A3	**Test Mode Select** Connect to ground for normal operation.
TMC	I	C8	**Test Mode Control** Connect to ground for normal operation.
TMC1	I	B1	**IDDQ Test Control Input** Connect to ground for normal operation.
TMC2	I	M1	**I/O Buffer Control** Connect to ground for normal operation.
TMS	I PU	M12	**Test Mode Select** Mode input signal to the TAP Controller. The TAP controller is a 16-state FSM that provides the control logic for JTAG. The TMS state at the rising edge of TCK determines the sequence of states for the TAP controller. Hold open when JTAG is not used.
TRST#	I PU	L10	**Test Reset** Resets the JTAG TAP controller when driven to ground. Ground when JTAG is not used.

2.3.1 Physical Ball Assignment – 144-Ball PBGA Package

Figure 2-1. 144-Ball PBGA Physical Ball Assignment – Bottom View

M	L	K	J	H	G	F	E	D	C	B	A	
TMS	PMEOUT#	AD28	AD30	PMEIN#	REQ2#	GND	INTA#	PCLKI	WAKEIN#	PERST#	GND	12
BTON	FORWARD	EXTARB	AD29	REQ3#	REQ0#	GNT2#	GNT3#	INTC#	GND	VDD3.3	GPIO3	11
VDD3.3	TRST#	GND	AD31	PCLKO	GNT0#	PCIRST#	INTD#	M66EN	VDD1.5	GPIO2	GPIO1	10
AD26	AD27	IDSEL	VDD1.5	REQ1#	GNT1#	VDDQ	INTB#	GND	GPIO0	PWR_OK	WAKEOUT#	9
CBE3#	AD24	AD25	GND	VDDQ	VDD5	VDD1.5	BAR0ENB#	BUNRI	TMC	VSS_R	PERp0	8
AD21	AD22	AD23	VDDQ	GND	VDD1.5	VSS_RE	AVDD	VSS_C	AVSS	PERn0	VDD_R	7
AD18	AD17	AD19	AD20	VDD5	VDD1.5	VDD1.5	GND	VSS_P0	VSS_P1	REFCLK-	REFCLK+	6
FRAME#	IRDY#	CBE2#	AD16	VDDQ	GND	VDD5	VDDQ	VDD_P	VSS_T	PETp0	VDD_T	5
TRDY#	STOP#	DEVSEL#	GND	GND	VDDQ	AD10	AD7	VDD1.5	EECS#	GND	PETn0	4
LOCK#	TDI	VDD1.5	PERR#	CBE1#	AD13	AD9	AD6	AD0	GND	VDD3.3	TEST	3
TCK	VDD3.3	GND	SERR#	AD15	AD12	AD8	AD5	AD3	NC1	EECLK	EEWRDATA	2
TMC2	TDO	SMC	PAR	AD14	AD11	CBE0#	AD4	AD2	AD1	TMC1	EERDDATA	1

2.3.2 Ball Tables – 144-Ball PBGA Package

Table 2-7. Grid Order (144-Ball PBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
A1	EERDDATA	D1	AD2	G1	AD11	K1	SMC
A2	EEWRDATA	D2	AD3	G2	AD12	K2	GND
A3	TEST	D3	AD0	G3	AD13	K3	VDD1.5
A4	PETn0	D4	VDD1.5	G4	VDDQ	K4	DEVSEL#
A5	VDD_T	D5	VDD_P	G5	GND	K5	CBE2#
A6	REFCLK+	D6	VSS_P0	G6	VDD1.5	K6	AD19
A7	VDD_R	D7	VSS_C	G7		K7	AD23
A8	PERp0	D8	BUNRI	G8	VDD5	K8	AD25
A9	WAKEOUT#	D9	GND	G9	GNT1#	K9	IDSEL
A10	GPIO1	D10	M66EN	G10	GNT0#	K10	GND
A11	GPIO3	D11	INTC#	G11	REQ0#	K11	EXTARB
A12	GND	D12	PCLKI	G12	REQ2#	K12	AD28
B1	TMC1	E1	AD4	H1	AD14	L1	TDO
B2	EECLK	E2	AD5	H2	AD15	L2	VDD3.3
B3	VDD3.3	E3	AD6	H3	CBE1#	L3	TDI
B4	GND	E4	AD7	H4	GND	L4	STOP#
B5	PETp0	E5	VDDQ	H5	VDDQ	L5	IRDY#
B6	REFCLK-	E6	GND	H6	VDD5	L6	AD17
B7	PERn0	E7	AVDD	H7	GND	L7	AD22
B8	VSS_R	E8	BAR0ENB#	H8	VDDQ	L8	AD24
B9	PWR_OK	E9	INTB#	H9	REQ1#	L9	AD27
B10	GPIO2	E10	INTD#	H10	PCLKO	L10	TRST#
B11	VDD3.3	E11	GNT3#	H11	REQ3#	L11	FORWARD
B12	PERST#	E12	INTA#	H12	PMEIN#	L12	PMEOUT#
C1	AD1	F1	CBE0#	J1	PAR	M1	TMC2
C2	NC1	F2	AD8	J2	SERR#	M2	TCK
C3	GND	F3	AD9	J3	PERR#	M3	LOCK#
C4	EECS#	F4	AD10	J4	GND	M4	TRDY#
C5	VSS_T	F5	VDD5	J5	AD16	M5	FRAME#
C6	VSS_P1	F6	VDD1.5	J6	AD20	M6	AD18
C7	AVSS	F7	VSS_RE	J7	VDDQ	M7	AD21
C8	TMC	F8	VDD1.5	J8	GND	M8	CBE3#
C9	GPIO0	F9	VDDQ	J9	VDD1.5	M9	AD26
C10	VDD1.5	F10	PCIRST#	J10	AD31	M10	VDD3.3
C11	GND	F11	GNT2#	J11	AD29	M11	BTON
C12	WAKEIN#	F12	GND	J12	AD30	M12	TMS

Table 2-8. Signal Order (144-Ball PBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
D3	AD0	F1	CBE0#	E9	INTB#	M1	TMC2
C1	AD1	H3	CBE1#	D11	INTC#	M12	TMS
D1	AD2	K5	CBE2#	E10	INTD#	M4	TRDY#
D2	AD3	M8	CBE3#	L5	IRDY#	L10	TRST#
E1	AD4	K4	DEVSEL#	M3	LOCK#	D5	VDD_P
E2	AD5	B2	EECLK	C2	NC1	A7	VDD_R
E3	AD6	C4	EECS#	D10	M66EN	A5	VDD_T
E4	AD7	A1	EERDDATA	E8	BAR0ENB#	C10	VDD1.5
F2	AD8	A2	EEWRDATA	J1	PAR	D4	
F3	AD9	K11	EXTARB	F10	PCIRST#	F6	
F4	AD10	L11	FORWARD	D12	PCLKI	F8	
G1	AD11	M5	FRAME#	H10	PCLKO	G6	
G2	AD12	A12	GND	B7	PERn0	G7	
G3	AD13	B4		A8	PERp0	J9	
H1	AD14	C3		J3	PERR#	K3	
H2	AD15	C11		B12	PERST#	B3	VDD3.3
J5	AD16	D9		A4	PETn0	B11	
L6	AD17	E6		B5	PETp0	L2	
M6	AD18	F12		H12	PMEIN#	M10	
K6	AD19	G5		L12	PMEOUT#	F5	VDD5
J6	AD20	H4		B9	PWR_OK	G8	
M7	AD21	H7		B6	REFCLK-	H6	
L7	AD22	J4		A6	REFCLK+	E5	VDDQ
K7	AD23	J8		G11	REQ0#	F9	
L8	AD24	K2		H9	REQ1#	G4	
K8	AD25	K10		G12	REQ2#	H5	
M9	AD26	G10	GNT0#	H11	REQ3#	H8	
L9	AD27	G9	GNT1#	J2	SERR#	J7	
K12	AD28	F11	GNT2#	K1	SMC	D7	VSS_C
J11	AD29	E11	GNT3#	L4	STOP#	D6	VSS_P0
J12	AD30	C9	GPIO0	M2	TCK	C6	VSS_P1
J10	AD31	A10	GPIO1	L3	TDI	B8	VSS_R
E7	AVDD	B10	GPIO2	L1	TDO	F7	VSS_RE
C7	AVSS	A11	GPIO3	A3	TEST	C5	VSS_T
M11	BTON	K9	IDSEL	C8	TMC	C12	WAKEIN#
D8	BUNRI	E12	INTA#	B1	TMC1	A9	WAKEOUT#

2.4 Ball Description – 161-Ball FBGA Package

Table 2-9. Power and Ground (46 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
AVDD	Power	C8	**Analog Supply Voltage** Connect to the +1.5V power supply.
AVSS	Ground	C6	**Analog Ground** Connect to ground.
GND	Ground	A4, C13, D5, D12, E4, E11, F11, J2, K4, K11, L4, M6, N9, P12	**Ground** Connect to ground.
VDD_P	Power	B6	**PLL Supply Voltage** Connect to the +1.5V filtered PLL power supply.
VDD_R	Power	C7	**Receiver Supply Voltage** Connect to the +1.5V power supply.
VDD_T	Power	D6	**Transmitter Supply Voltage** Connect to the +1.5V power supply.
VDD1.5	Power	B10, C1, C14, G2, G13, L3, L11, N7	**PCI Express Interface Supply Voltage** Connect to the +1.5V power supply.
VDD3.3	Power	B4, C11, L10, N3	**I/O Supply Voltage** Connect to the +3.3V power supply.
VDD5	Power	G3, H13, L7	**PCI I/O Clamp Voltage** Connect to the +5.0V power supply for PCI buffers. In a 3.3V PCI environment, connect VDD5 to the 3.3V power supply.
VDDQ	Power	F4, G12, H4, J12, L8, N5	**I/O Supply Voltage** Connect to the +3.3V power supply for PCI buffers.
VSS_C	Ground	D9	**Common Ground** Connect to ground.
VSS_P0	Ground	D7	**PLL Ground** Connect to ground.
VSS_P1	Ground	D8	**PLL Ground** Connect to ground.
VSS_R	Ground	A9	**Receiver Ground** Connect to ground.
VSS_RE	Ground	B8	**Receiver Ground** Connect to ground.
VSS_T	Ground	A5	**Transmitter Ground** Connect to ground.

Table 2-10. PCI Express Balls (9 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
PERn0	I DIFF	B9	**Receive Minus** PCI Express Differential Receive signal.
PERp0	I DIFF	A8	**Receive Plus** PCI Express Differential Receive signal.
PERST#	I/O 6 mA 3.3V	C12	**PCI Express Reset** In Forward Bridge mode, PERST# is an input. Resets the entire chip when asserted. In Reverse Bridge mode, PERST# is an output. Asserted when a PCI reset is detected.
PETn0	O DIFF	B5	**Transmit Minus** PCI Express Differential Transmit signal.
PETp0	O DIFF	A6	**Transmit Plus** PCI Express Differential Transmit signal.
REFCLK-	I DIFF	A7	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz spread spectrum reference clock. REFCLK- is connected to the PCI Express bus REFCLK- ball in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
REFCLK+	I DIFF	B7	**PCI Express Clock Input Plus** PCI Express differential, 100 MHz spread spectrum reference clock. REFCLK+ is connected to the PCI Express bus REFCLK+ ball in Forward Bridge mode, and to an external differential clock driver in Reverse Bridge mode.
WAKEIN#	I 3.3V	D14	**Wake In Signal** In Reverse Bridge mode, WAKEIN# is an input, and indicates that the PCI Express Device requested a wakeup while the link remains in the L2 state.
WAKEOUT#	OD 6 mA 3.3V	A11	**Wake Out Signal** In Forward Bridge mode, WAKEOUT# is an Open Drain output, and asserted when PMEIN# is asserted and the link remains in the L2 state.

Table 2-11. PCI Balls (63 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
AD[31:0]	I/O TS PCI	L13, J11, K12, L12, M10, P11, P10, P9, L9, N8, P8, M8, M7, L6, N6, P7, K2, J3, J1, H2, H3, H1, G4, F3, F2, F1, E2, E3, E1, D3, D1, D2	**Address/Data Bus** The PCI address and data are multiplexed onto the same bus. During the Address phase, AD[31:0] contain the physical address of the transfer. During the Data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and Read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M9, P6, K1, G1	**Command/Byte Enable Bus** The Bus command and Byte Enables are multiplexed onto the same bus. During the Address phase, CBE[3:0]# contain the Bus command. During the Data phase, CBE[3:0]# contain the Byte Enables. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]). **CBE[3:0]# — Command** 0000b — Interrupt Acknowledge 0001b — Special cycle 0010b — I/O Read 0011b — I/O Write 0100b, 0101b — ***Reserved*** 0110b — Memory Read 0111b — Memory Write 1000b, 1001b — ***Reserved*** 1010b — Configuration Read 1011b — Configuration Write 1100b — Memory Read Multiple 1101b — Dual Address Cycle 1110b — Memory Read Line 1111b — Memory Write and Invalidate
DEVSEL#	I/O STS PCI PU (Reverse Bridge mode only)	M4	**Device Select** Indicates that the target (bus slave) decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus was selected.
FRAME#	I/O STS PCI PU (Reverse Bridge mode only)	L5	**Frame** Driven by the initiator, and indicates the access start and duration. When FRAME# is first asserted, the Address phase is indicated. When FRAME# is de-asserted, the transaction remains in the last Data phase.
GNT[3:0]#	I/O TS PCI	F12, G11, J13, J14	**Bus Grant** Indicates that the central arbiter granted the bus to an agent. When the internal PCI arbiter is enabled, GNT[3:0]# are outputs used to grant the bus to external devices. When the internal PCI arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8111, and GNT[3:1]# are placed into a high-impedance state.
IDSEL	I PCI	N10	**Initialization Device Select** Used as a Chip Select during Configuration Read and Write cycles. Each PCI slot or device typically contains an IDSEL connected to a signal address line, allowing the PCI host to select individual sets of Configuration registers. Used in Reverse Bridge mode. In Forward Bridge mode, ground or pull up to 3.3V.

Table 2-11. PCI Balls (63 balls) (161-Ball FBGA Package) *(Cont.)*

Signal	Type	Balls	Description
INTA#, INTB#, INTC#, INTD#	I/O OD PCI PU (Reverse Bridge mode only)	F14, F13, E14, E13	**Interrupt** Asserted to request an interrupt. After assertion, must remain asserted until the device driver clears it. INT*x*# is level-sensitive and asynchronous to the CLK. In Forward Bridge mode, INT*x*# is an input from PCI devices. All INT*x*# signals are mapped into Assert_INT*x* and Deassert_INT*x* messages on the PCI Express Bus. In Reverse Bridge mode, INT*x*# is an output to the PCI Central Resource Function. All Assert_INT*x* and Deassert_INT*x* PCI Express messages are translated to INT*x*# transitions on the PCI Bus.
IRDY#	I/O STS PCI PU (Reverse Bridge mode only)	P5	**Initiator Ready** Indicates that the initiator (bus master) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	P4	**Lock Atomic Operation** Indicates an atomic operation to a bridge that may require multiple transactions to complete. Output in Forward Bridge mode and input in Reverse Bridge mode.
M66EN	I PCI	D13	**66 MHz Enable** Indicates whether the PCI Bus is operating at 33 or 66 MHz. When low, and the PCLKO divider is 3, the PCLKO ball oscillates at 33 MHz with a 50% Duty cycle. When high, and the PCLKO divider is 3, the PCLKO ball oscillates at 66 MHz with a 33% Duty cycle. Read M66EN using the **PCI Control** register *M66EN* bit. Must be grounded in 33 MHz systems.
PAR	I/O TS PCI	J4	**Parity** Even parity is generated across AD[31:0], and CBE[3:0]#. *That is*, the number of ones (1) on AD[31:0], CBE[3:0]#, and PAR is an even number. PAR is valid one clock after the Address phase. For Data phases, PAR is valid one clock after IRDY# is asserted on Write cycles, and one clock after TRDY# is asserted on Read cycles. PAR maintains the same timing as AD[31:0], except it is delayed by one Clock cycle. The bus initiator drives PAR for Address and Write Data phases, and the target drives PAR for Read Data phases.
PCIRST#	I/O OD PCI	G14	**PCI Reset** In Forward Bridge mode, driven when a PCI Express reset is detected, or the **Bridge Control** register *Secondary Bus Reset* bit is set. In Reverse Bridge mode, PCIRST# is an input that resets the entire chip. Reset is asserted and de-asserted asynchronously to CLK, and used to bring a PCI device to an initial state. All PCI signals are asynchronously placed into a high-impedance state during reset.
PCLKI	I PCI	E12	**PCI Clock Input** All PCI signals, except RST# and interrupts, are sampled on the rising edge of PCLKI. Frequency varies from 0 to 66 MHz. Must oscillate during the serial EEPROM initialization sequence.
PERR#	I/O STS PCI PU (Reverse Bridge mode only)	L2	**Parity Error** Indicates that a Data Parity error occurred. Driven active by the receiving agent two clocks following the data that contained bad parity.

Table 2-11. PCI Balls (63 balls) (161-Ball FBGA Package) *(Cont.)*

Signal	Type	Balls	Description
PMEIN#	I S PCI	L14	**Power Management Event In** Valid only in Forward Bridge mode. Input used to monitor requests to change the system power state.
PMEOUT#	OD 24 mA 3.3V	M14	**Power Management Event Out** Valid only in Reverse Bridge mode. Open-drain output used to request a change in the power state. PMEOUT# is ***not*** 5V tolerant. When used in a system with a 5V pull-up resistor on the PCI backplane PME# signal, an external voltage translation circuit is required.
REQ[3:0]#	I/O TS PCI	H11, H12, K13, K14	**Bus Request** Indicates that an agent requires use of the bus. When the internal PCI arbiter is enabled, REQ[3:0]# are inputs used to service external bus requests. When the internal PCI arbiter is disabled, REQ0# is an output used to request bus control, and REQ[3:1]# are unused inputs.
SERR#	I/O OD PCI PU (Reverse Bridge mode only)	L1	**System Error** Indicates that an Address Parity error, Data Parity error on the special cycle command, or other catastrophic error occurred. Driven active for one PCI clock period, and is synchronous to the CLK. Driven only in Reverse Bridge mode.
STOP#	I/O STS PCI PU (Reverse Bridge mode only)	N4	**Stop** Indicates that the target (bus slave) is requesting that the master stop the current transaction. After STOP# is asserted, it must remain asserted until FRAME# is de-asserted, whereupon STOP# must be de-asserted. Also, DEVSEL# and TRDY# cannot be changed until the current data phase completes. STOP# must be de-asserted in the clock following the completion of the last Data phase, and must be placed into a high-impedance state in the next clock. Data is transferred when both IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI PU (Reverse Bridge mode only)	M5	**Target Ready** Indicates that the target (bus slave) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.

Table 2-12. Clocks, Reset, and Miscellaneous (31 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	A10	**PCI Base Address 0 Register Enable** When low, the **PCI Base Address 0** register is enabled. When high, the **PCI Base Address 0** register is enabled by the **Device-Specific Control** register *PCI Base Address 0 Enable* bit.
EECLK	O 3 mA TP 3.3V	C2	**Serial EEPROM Clock** Provides the clock to the serial EEPROM. Frequency is determined by the **Serial EEPROM Clock Frequency** register, and varies from 2 to 25 MHz.
EECS#	O 3 mA TP 3.3V	C5	**Serial EEPROM Chip Select** Active-low Chip Select.
EERDDATA	I 3.3V	B3	**Serial EEPROM Read Data** Used to read data from the device. A 47K-Ohm pull-up resistor is required.
EEWRDATA	O 3 mA TP 3.3V	A3	**Serial EEPROM Write Data** Used to write data to the device.
EXTARB	I 3.3V	M12	**External Arbiter Enable** When low, the internal PCI arbiter services requests from an external PCI device. When high, the PEX 8111 requests the PCI Bus from an external arbiter.
FORWARD	I 3.3V PU	M13	**Bridge Select** When low, the PEX 8111 acts as a PCI-to-PCI Express Bridge (reverse bridge). When high, the PEX 8111 acts as a PCI Express-to-PCI Bridge (forward bridge).
GPIO[3:0]	I/O 12 mA 3.3V PU	B12, D11, A12, C10	**General Purpose I/O** Program as an input or output general-purpose ball. Internal device status also retains the ability to be an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **General-Purpose I/O Control** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is low at the trailing edge of RESET#, the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. When GPIO3 is low at the trailing edge of RESET#, the **TLP Controller Configuration 0** register *Delay Link Training* bit is set.
NC	–	A1, A2, A13, A14, B1, B2, B13, B14, E5, N1, N2, N13, N14, P1, P2, P13, P14	**No Connect** Never used. Must remain open.

Table 2-12. Clocks, Reset, and Miscellaneous (31 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
NC1	–	C3	**No Connect** Must remain open.
PCLKO	O 26 mA TP PCI	H14	**PCI Clock Output** Buffered clock output from the internal 100-MHz reference clock, with the frequency depending on the **Device Initialization** register *PCLKO Clock Frequency* field. Signal frequency is 66 MHz when M66EN is high. PCLKO is always driven and oscillates when one of the following occurs: • PCI Express REFCLK-/+ input pins are active • PCLKO clock divider in **Device Initialization** register is non-zero • Internal AGEP_RST_B_ signal to Pixie is de-asserted. AGEP_RST_B_ is asserted for: – Pin reset – Power Management reset
PWR_OK	O 6 mA 3.3V	B11	**Power OK** Valid only in Forward Bridge mode. When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the **Power** register, PWR_OK is asserted.

Table 2-13. Test Balls (12 balls) (161-Ball FBGA Package)

Signal	Type	Balls	Description
BTON	I	M11	**Test Enable** Connect to ground for normal operation.
BUNRI	I	C9	**Test Mode Select** Connect to ground for normal operation.
SMC	I	K3	**Scan Path Mode Control** Connect to ground for normal operation.
TCK	I	M2	**Test Clock** JTAG test clock. Sequences the TAP controller, as well as all PEX 8111 JTAG registers. Ground when JTAG is not used.
TDI	I PU	P3	**Test Data Input** Serial data input to all JTAG instruction and data registers. The TAP controller state, as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. Hold open when JTAG is not used.
TDO	O 12 mA TS 3.3V	M3	**Test Data Output** Serial data output for all JTAG instruction and data registers. The TAP controller state, as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed as the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. Placed into a high-impedance state at all other times. Hold open when JTAG is not used.
TEST	I	C4	**Test Mode Select** Connect to ground for normal operation.
TMC	I	D10	**Test Mode Control** Connect to ground for normal operation.
TMC1	I	D4	**IDDQ Test Control Input** Connect to ground for normal operation.
TMC2	I	M1	**I/O Buffer Control** Connect to ground for normal operation.
TMS	I PU	N12	**Test Mode Select** Mode input signal to the TAP Controller. The TAP controller is a 16-state FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. Hold open when JTAG is not used.
TRST#	I PU	N11	**Test Reset** Resets the JTAG TAP controller when driven to ground. Ground when JTAG is not used.

2.4.1 Physical Ball Assignment – 161-Ball FBGA Package

Figure 2-2. 161-Ball FBGA Physical Ball Assignment – Bottom View

P	N	M	L	K	J	H	G	F	E	D	C	B	A	
NC	NC	PMEOUT#	PMEIN#	REQ0#	GNT0#	PCLKO	PCIRST#	INTA#	INTC#	WAKEIN#	VDD1.5	NC	NC	14
NC	NC	FORWARD	AD31	REQ1#	GNT1#	VDD5	VDD1.5	INTB#	INTD#	M66EN	GND	NC	NC	13
GND	TMS	EXTARB	AD28	AD29	VDDQ	REQ2#	VDDQ	GNT3#	PCLKI	GND	PERST#	GPIO3	GPIO1	12
AD26	TRST#	BTON	VDD1.5	GND	AD30	REQ3#	GNT2#	GND	GND	GPIO2	VDD3.3	PWR_OK	WAKEOUT#	11
AD25	IDSEL	AD27	VDD3.3							TMC	GPIO0	VDD1.5	BAR0ENB#	10
AD24	GND	CBE3#	AD23							VSS_C	BUNRI	PERn0	VSS_R	9
AD21	AD22	AD20	VDDQ							VSS_P1	AVDD	VSS_RE	PERp0	8
AD16	VDD1.5	AD19	VDD5							VSS_P0	VDD_R	REFCLK+	REFCLK-	7
CBE2#	AD17	GND	AD18							VDD_T	AVSS	VDD_P	PETp0	6
IRDY#	VDDQ	TRDY#	FRAME#						NC	GND	EECS#	PETn0	VSS_T	5
LOCK#	STOP#	DEVSEL#	GND	GND	PAR	VDDQ	AD9	VDDQ	GND	TMC1	TEST	VDD3.3	GND	4
TDI	VDD3.3	TDO	VDD1.5	SMC	AD14	AD11	VDD5	AD8	AD4	AD2	NC1	EERDDATA	EEWRDATA	3
NC	NC	TCK	PERR#	AD15	GND	AD12	VDD1.5	AD7	AD5	AD0	EECLK	NC	NC	2
NC	NC	TMC2	SERR#	CBE1#	AD13	AD10	CBE0#	AD6	AD3	AD1	VDD1.5	NC	NC	1

Bottom View

(PEX 8111)

2.4.2 Ball Tables – 161-Ball FBGA Package

Table 2-14. Grid Order (161-Ball FBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
A1	NC	C14	VDD1.5	H2	AD12	M5	TRDY#
A2		D1	AD1	H3	AD11	M6	GND
A3	EEWRDATA	D2	AD0	H4	VDDQ	M7	AD19
A4	GND	D3	AD2	H11	REQ3#	M8	AD20
A5	VSS_T	D4	TMC1	H12	REQ2#	M9	CBE3#
A6	PETp0	D5	GND	H13	VDD5	M10	AD27
A7	REFCLK-	D6	VDD_T	H14	PCLKO	M11	BTON
A8	PERp0	D7	VSS_P0	J1	AD13	M12	EXTARB
A9	VSS_R	D8	VSS_P1	J2	GND	M13	FORWARD
A10	BAR0ENB#	D9	VSS_C	J3	AD14	M14	PMEOUT#
A11	WAKEOUT#	D10	TMC	J4	PAR	N1	NC
A12	GPIO1	D11	GPIO2	J11	AD30	N2	
A13	NC	D12	GND	J12	VDDQ	N3	VDD3.3
A14		D13	M66EN	J13	GNT1#	N4	STOP#
B1		D14	WAKEIN#	J14	GNT0#	N5	VDDQ
B2		E1	AD3	K1	CBE1#	N6	AD17
B3	EERDDATA	E2	AD5	K2	AD15	N7	VDD1.5
B4	VDD3.3	E3	AD4	K3	SMC	N8	AD22
B5	PETn0	E4	GND	K4	GND	N9	GND
B6	VDD_P	E5	NC	K11		N10	IDSEL
B7	REFCLK+	E11	GND	K12	AD29	N11	TRST#
B8	VSS_RE	E12	PCLKI	K13	REQ1#	N12	TMS
B9	PERn0	E13	INTD#	K14	REQ0#	N13	NC
B10	VDD1.5	E14	INTC#	L1	SERR#	N14	
B11	PWR_OK	F1	AD6	L2	PERR#	P1	
B12	GPIO3	F2	AD7	L3	VDD1.5	P2	
B13	NC	F3	AD8	L4	GND	P3	TDI
B14		F4	VDDQ	L5	FRAME#	P4	LOCK#
C1	VDD1.5	F11	GND	L6	AD18	P5	IRDY#
C2	EECLK	F12	GNT3#	L7	VDD5	P6	CBE2#
C3	NC1	F13	INTB#	L8	VDDQ	P7	AD16
C4	TEST	F14	INTA#	L9	AD23	P8	AD21
C5	EECS#	G1	CBE0#	L10	VDD3.3	P9	AD24
C6	AVSS	G2	VDD1.5	L11	VDD1.5	P10	AD25
C7	VDD_R	G3	VDD5	L12	AD28	P11	AD26
C8	AVDD	G4	AD9	L13	AD31	P12	GND

Table 2-14. Grid Order (161-Ball FBGA Package) *(Cont.)*

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
C9	BUNRI	G11	GNT2#	L14	PMEIN#	P13	NC
C10	GPIO0	G12	VDDQ	M1	TMC2	P14	
C11	VDD3.3	G13	VDD1.5	M2	TCK		
C12	PERST#	G14	PCIRST#	M3	TDO		
C13	GND	H1	AD10	M4	DEVSEL#		

Table 2-15. Signal Order (161-Ball FBGA Package)

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
D2	AD0	C2	EECLK	B1		M3	TDO
D1	AD1	C5	EECS#	B2		C4	TEST
D3	AD2	B3	EERDDATA	B13		D10	TMC
E1	AD3	A3	EEWRDATA	B14		D4	TMC1
E3	AD4	M12	EXTARB	E5		M1	TMC2
E2	AD5	M13	FORWARD	N1		N12	TMS
F1	AD6	L5	FRAME#	N2	NC	M5	TRDY#
F2	AD7	A4		N13		N11	TRST#
F3	AD8	C13		N14		B6	VDD_P
G4	AD9	D5		P1		C7	VDD_R
H1	AD10	D12		P2		D6	VDD_T
H3	AD11	E4		P13		B10	VDD1.5
H2	AD12	E11		P14		C1	
J1	AD13	F11	GND	C3	NC1	C14	
J3	AD14	J2		D13	M66EN	G2	
K2	AD15	K4		A10	BAR0ENB#	G13	
P7	AD16	K11		J4	PAR	L3	
N6	AD17	L4		G14	PCIRST#	L11	
L6	AD18	M6		E12	PCLKI	N7	
M7	AD19	N9		H14	PCLKO	B4	VDD3.3
M8	AD20	P12		B9	PERn0	C11	
P8	AD21	J14	GNT0#	A8	PERp0	L10	
N8	AD22	J13	GNT1#	L2	PERR#	N3	
L9	AD23	G11	GNT2#	C12	PERST#	G3	VDD5
P9	AD24	F12	GNT3#	B5	PETn0	H13	
P10	AD25	C10	GPIO0	A6	PETp0	L7	

Table 2-15. Signal Order (161-Ball FBGA Package) *(Cont.)*

Grid	Signal	Grid	Signal	Grid	Signal	Grid	Signal
P11	AD26	A12	GPIO1	L14	PMEIN#	F4	VDDQ
M10	AD27	D11	GPIO2	M14	PMEOUT#	G12	
L12	AD28	B12	GPIO3	B11	PWR_OK	H4	
K12	AD29	N10	IDSEL	A7	REFCLK-	J12	
J11	AD30	F14	INTA#	B7	REFCLK+	L8	
L13	AD31	F13	INTB#	K14	REQ0#	N5	
C8	AVDD	E14	INTC#	K13	REQ1#	D9	VSS_C
C6	AVSS	E13	INTD#	H12	REQ2#	D7	VSS_P0
M11	BTON	P5	IRDY#	H11	REQ3#	D8	VSS_P1
C9	BUNRI	P4	LOCK#	L1	SERR#	A9	VSS_R
G1	CBE0#	A1	NC	K3	SMC	B8	VSS_RE
K1	CBE1#	A2		N4	STOP#	A5	VSS_T
P6	CBE2#	A13		M2	TCK	D14	WAKEIN#
M9	CBE3#	A14		P3	TDI	A11	WAKEOUT#
M4	DEVSEL#						

Chapter 3 Reset Summary

3.1 Forward Bridge Mode

Table 3-1 delineates which device resources are reset when each of the forward bridge reset sources are asserted.

Table 3-1. Forward Bridge Reset

Reset Sources	Device Resources			
	PCI Express Interface Logic	PCI Interface Logic	PCI RST# Ball	Configuration Registers
PCI Express PERST# ball	X	X	X	X
PCI Express Link Down	X	X	X	X[a]
PCI Express Hot Reset	X	X	X	X[a]
Secondary Bus Reset bit	–	X	X	–
D3 to D0 Power Management Reset	X	X	X	X

a. **General-Purpose I/O Control** register is not reset for Link Down nor Hot Reset.

b. "X" is "Don't Care."

c. "–" is "Not Applicable."

3.2 Reverse Bridge Mode

Table 3-2 delineates which device resources are reset when each of the reverse bridge reset sources are asserted.

Table 3-2. Reverse Bridge Reset

Reset Sources	Device Resources				
	PCI Express Interface Logic	PCI Interface Logic	PCI PERST# Ball	PCI Express Hot Reset	Configuration Registers
PCI RST# ball	X	X	X	X	X
Secondary Bus Reset bit	X	–	–	X	–
D3 to D0 Power Management Reset	X	X	–	X	X

3.3 Initialization Summary

Certain PEX 8111 initialization sequences are described below:

- No serial EEPROM, blank serial EEPROM, or invalid serial EEPROM
  - When the EERDDATA ball is always high, then an invalid serial EEPROM is detected. In this case, the default PCI Device ID (8111h) is selected. A 47K-Ohm pull-up resistor ensures that EERDDATA is high when no serial EEPROM is installed.
  - Enable the PCI Express and PCI interfaces, using default register values.
- Valid serial EEPROM with Configuration register data
  - Enable the PCI Express and PCI interfaces, using register values loaded from the serial EEPROM. The **Device Initialization** register *PCI Express Enable* or *PCI Enable* bit should be the last bit set by the serial EEPROM.

Chapter 4 Initialization

4.1 Forward Bridge Initialization

The actions that the PEX 8111 takes upon receipt of certain reset events and interface initialization requirements are described in the following sections.

4.1.1 Forward Bridge Reset Behavior

There are three types of reset that the PEX 8111 receives over the PCI Express primary interface:

- Physical layer resets that are platform specific and referred to as *Fundamental Resets* (cold/warm reset)
- PCI Express Physical Layer mechanism (Hot Reset)
- PCI Express Data Link transitioning to the Down state of primary interface

These three primary interface reset sources are each described in the sections that follow. All primary interface reset events initiate a Secondary Bus Reset which resets the PCI Bus. In addition to primary interface reset sources, the PEX 8111 supports a PCI Bus reset by way of the **Bridge Control** register.

When attempting a Configuration access to devices on the PCI Bus behind the PEX 8111, the timing parameter *Trhfa* (2^{25} PCI clocks) must be respected after reset.

4.1.1.1 Fundamental Reset (Cold/Warm Reset)

The PEX 8111 uses the PCI Express PERST# signal as a fundamental reset input. When PERST# assertion follows the power-on event, it is referred to as a *cold reset*. The PCI Express system also generates this signal without removing power; which is referred to as a *warm reset*. The PEX 8111 treats cold and warm resets without distinction. The PEX 8111 state machines are asynchronously reset, and the Configuration registers are initialized to their default values when PERST# is asserted. The PEX 8111 also places its PCI outputs into a high-impedance state, unless it is configured as the PCI Bus parking agent.

The PEX 8111 propagates the warm/cold reset from its primary interface to PCI reset on the secondary interface. The PCI RST# signal is asserted while PERST# is asserted. During a cold reset, PCI RST# is asserted for at least 100 µs after the power levels are valid. During other types of PCI resets, PCI RST# is asserted for at least 1 ms.

4.1.1.2 Primary Reset Due to Physical Layer Mechanism (Hot Reset)

PCI Express supports the Link Training Control Reset (a training sequence with the Hot Reset bit set), or Hot Reset, for propagating Reset Requests downstream. When the PEX 8111 receives a Hot Reset on its PCI Express primary interface, it propagates that reset to the PCI RST# signal. In addition, the PEX 8111 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. Software is responsible for ensuring that the Link Reset assertion and de-assertion messages are timed such that the bridge adheres to proper reset assertion and de-assertion durations on the PCI RST# signal.

4.1.1.3 Primary Reset Due to Data Link Down

When the PEX 8111 PCI Express primary interface remains in normal operation and, for whatever reason, the Link is down, the Transaction and Data Link Layers enter the DL_Down state. The PEX 8111 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. In addition, the entry of the primary interface of the PEX 8111 into DL_Down status initiates a reset of the PCI Bus, using the PCI RST# signal.

4.1.1.4 Secondary Bus Reset by way of Bridge Control Register

A PCI secondary interface reset is initiated by setting the **Bridge Control** register *Secondary Bus Reset* bit. This targeted reset is used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration. A write to the *Secondary Bus Reset* bit forces the assertion of the secondary interface PCI Reset (RST#) signal without affecting the primary interface or Configuration Space registers. Moreover, the logic associated with the secondary interface is re-initialized and transaction buffers associated with the secondary interface are cleared.

RST# is asserted when the *Secondary Bus Reset* bit is set; therefore, software must take care to observe proper PCI reset timing requirements. Software is responsible for ensuring that the PEX 8111 does not receive transactions that require forwarding to the secondary interface while *Secondary Bus Reset* bit is set.

4.1.1.5 Bus Parking during Reset

The PEX 8111 drives the secondary interface PCI Bus AD[31:0], CBE[3:0]#, and PAR signals to a logic low level (zero) when the secondary interface RST# is asserted.

4.2 Reverse Bridge Initialization

4.2.1 Reverse Bridge Reset Behavior

A PCI Express Hot Reset (PCI Express Link Training Sequence) is generated for the following cases:

- **Bridge Control** register *Secondary Bus Reset* bit is set
- Power management state transitions from D3 to D0

PCI RST# assertion causes the PCI Express sideband Reset signal (PERST#) to assert.

4.2.2 Reverse Bridge Secondary Bus Reset by way of Bridge Control Register

A PCI Express secondary interface reset is initiated by setting the **Bridge Control** register *Secondary Bus Reset* bit. This targeted reset is used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration.

A write to the *Secondary Bus Reset* bit causes a PCI Express Link Reset Training Sequence to transmit without affecting the primary interface or Configuration Space registers. Moreover, the logic associated with the secondary interface is re-initialized and transaction buffers associated with the secondary interface are cleared.

Chapter 5 Interrupts

5.1 Forward Bridge PCI Interrupts

In Forward Bridge mode, the PCI INT*x*# signals are inputs to the PEX 8111. The interrupt is routed to the PCI Express Bus, using virtual wire interrupt messages. The PCI Express supports the INT*x* virtual wire interrupt feature for legacy systems that still support the PCI INT*x*# interrupt signals. PCI INT*x*# interrupts are "virtualized" in PCI Express using Assert_INT*x* and Deassert_INT*x* messages, where *x* is A, B, C, or D for the respective PCI INT*x*# interrupt signals defined in the *PCI r3.0*. This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INT*x* and Deassert_INT*x* messages transmitted on the PCI Express link capture the asserting/de-asserting edge of the respective PCI INT*x*# signal.

The Requester ID used in the PCI Express Assert_INT*x* and Deassert_INT*x* messages transmitted by the PEX 8111 (irrespective of whether the source is internal or external to the bridge) equals the bridge primary interface Bus and Device Numbers. The Function Number sub-field is cleared to 0.

5.1.1 Forward Bridge Internally Generated Interrupts

The following internal events are programmed to generate an interrupt:

- Serial EEPROM transaction completed
- Any GPIO bit that is programmed as an input
- **Mailbox** register written

When one of these interrupts occurs, an interrupt is produced using one of two methods described in the following two sections.

5.1.1.1 Virtual Wire Interrupts

When MSI is disabled, virtual wire interrupts are used to support internal interrupt events. Internal interrupt sources are masked by the **PCI Command** register *Interrupt Disable* bit and routed to one of the virtual interrupts using the **PCI Interrupt Pin** register. PCI Express Assert_INT*x* and Deassert_INT*x* messages are not masked by the **PCI Command** register *Bus Master Enable* bit. The internal interrupt is processed the same as the corresponding PCI interrupt signal.

5.1.1.2 Message Signaled Interrupts

The PCI Express Bus supports interrupts using Message Signaled Interrupts (MSI). With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8111 uses the 64-bit Message Address version of the MSI capability structure and clears the *No Snoop* and *Relaxed Ordering* bits in the Requester Attributes. There are Address and Data Configuration registers associated with the MSI feature – **Message Signaled Interrupts Address**, **Message Signaled Interrupts Upper Address**, and **Message Signaled Interrupts Data**. When an internal interrupt event occurs, the value in the **Message Signaled Interrupts Data** Configuration register is written to the PCI Express address specified by the **MSI Address** Configuration registers.

The MSI feature is enabled by the **Message Signaled Interrupts Control** register *MSI Enable* bit. When MSI is enabled, the virtual wire interrupt feature is disabled. MSI interrupts are generated independently of the **PCI Command** register *Interrupt Disable* bit. MSI interrupts are gated by the **PCI Command** register *Bus Master Enable* bit.

Note: *The No Snoop and Relaxed Ordering bits are cleared because the PEX 8111 does not support these features.*

5.2 Reverse Bridge PCI Interrupts

In Reverse Bridge mode, the PCI INT*x*# signals are outputs from the PEX 8111. Each INT*x*# signal is asserted or de-asserted when the corresponding PCI Express Assert_INT*x* or Deassert_INT*x* message is received. The INT*x*# signals are asserted independently of the **PCI Command** register *Interrupt Disable* bit, and only when the PEX 8111 remains in power state D0.

5.2.1 Reverse Bridge Internally Generated Interrupts

The following internal events are programmed to generate an interrupt:

- Serial EEPROM transaction completed
- Any GPIO bit that is programmed as an input
- **Mailbox** register written

When one of these interrupts occurs, an interrupt is produced using one of two methods described in the following two sections.

5.2.1.1 INT*x*# Signals

When an internal interrupt event occurs, it causes a PCI INT*x*# signal to assert. Internal interrupt sources are masked by the **PCI Command** register *Interrupt Disable* bit and are routed to one of the INT*x*# signals, using the **PCI Interrupt Pin** register. The INT*x*# signals are asserted only when Message Signaled Interrupts are disabled.

5.2.1.2 Message Signaled Interrupts

The PCI Bus supports interrupts using Message Signaled Interrupts (MSI). With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8111 uses the 64-bit Message Address version of the MSI capability structure. There are Address and Data Configuration registers associated with the MSI feature – **Message Signaled Interrupts Address**, **Message Signaled Interrupts Upper Address**, and **Message Signaled Interrupts Data**. When an internal interrupt event occurs, the value in the **Message Signaled Interrupts Data** Configuration register is written to the PCI Express address specified by the **MSI Address** Configuration registers.

The MSI feature is enabled by the **Message Signaled Interrupts Control** register *MSI Enable* bit. When MSI is enabled, the INT*x*# interrupt signals for internally generated interrupts are disabled. MSI interrupts are generated independently of the **PCI Command** register *Interrupt Disable* bit. MSI interrupts are gated by the **PCI Command** register *Bus Master Enable* bit.

Chapter 6 Serial EEPROM Controller

6.1 Overview

The PEX 8111 provides an interface to SPI (Serial Peripheral Interface)-compatible serial EEPROMs. This interface consists of a Chip Select, Clock, Write Data, and Read Data balls, and operates at up to 25 MHz. Compatible 128-byte serial EEPROMs include the Atmel AT25010A, Catalyst CAT25C01, and ST Microelectronics M95010W. The PEX 8111 supports up to a 16 MB serial EEPROM, utilizing 1-, 2-, or 3-byte addressing. The PEX 8111 automatically determines the appropriate addressing mode.

6.2 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the following format.

Table 6-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	Refer to Table 6-2	Serial EEPROM Format Byte
2h	REG BYTE COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG BYTE COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
10h	REGADDR (LSB)	2nd Configuration Register Address (LSB)
11h	REGADDR (MSB)	2nd Configuration Register Address (MSB)
12h	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
13h	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
14h	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
15h	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
……		
REG BYTE COUNT + 4	MEM BYTE COUNT (LSB)	Shared memory Byte Count (LSB)
REG BYTE COUNT + 5	MEM BYTE COUNT (MSB)	Shared memory Byte Count (MSB)
REG BYTE COUNT + 6	SHARED MEM (Byte 0)	1st byte Shared memory
REG BYTE COUNT + 7	SHARED MEM (Byte 1)	2nd byte of Shared memory
……		
FFFFh	SHARED MEM (Byte *n*)	Last byte of Shared memory

Table 6-2 delineates the Serial EEPROM Format Byte organization.

Table 6-2. Serial EEPROM Format Byte

Bits	Description
0	**Configuration Register Load** When cleared, and REG BYTE COUNT is non-zero, the Configuration data is read from the serial EEPROM and discarded. When set, Configuration registers are loaded from the serial EEPROM. The first Configuration Register address is located at bytes 3 and 4 in the serial EEPROM.
1	**Shared Memory Load** When set, shared memory is loaded from the serial EEPROM, starting at location REG BYTE COUNT + 6. The byte number to load is determined by the value in serial EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5.
7:2	***Reserved***

6.3 Initialization

After the device reset is de-asserted, the serial EEPROM internal status register is read to determine whether a serial EEPROM is installed. A pull-up resistor on the EERDDATA ball produces a value of FFh when there is no serial EEPROM installed. When a serial EEPROM is detected, the first byte (validation signature) is read. when a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8111. The serial EEPROM address width is determined while this first byte is read. When the first byte is not 5Ah, then the serial EEPROM is blank, or programmed with invalid data. In this case, the PCI Express and PCI interfaces are enabled for a default enumeration. Also, the **Serial EEPROM Control** register *Serial EEPROM Address Width* field reports a value of 00b (undetermined width).

When the serial EEPROM contains valid data, the second byte (Serial EEPROM Format Byte) is read to determine which serial EEPROM sections are loaded into the PEX 8111 Configuration registers and memory.

Bytes 2 and 3 determine the number of serial EEPROM locations containing Configuration register addresses and data. Each Configuration register entry consists of two bytes of register address (bit 12 low selects the PCI Configuration registers, and bit 12 high selects the Memory-Mapped Configuration registers) and four bytes of register Write data. When bit 1 of the Serial EEPROM Format Byte is set, locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5 are read to determine the number of bytes to transfer from the serial EEPROM into shared memory.

The REG BYTE COUNT must be a multiple of 6 and MEM BYTE COUNT must be a multiple of 4.

The EECLK ball frequency is determined by the **Serial EEPROM Clock Frequency** register *Serial EEPROM Clock Frequency* field. The default clock frequency is 2 MHz. At this clock rate, it takes about 24 µs per DWORD during Configuration register or shared memory initialization. For faster loading of large serial EEPROMs that support a faster clock, direct the first Configuration register load from the serial EEPROM to the **Serial EEPROM Clock Frequency** register.

Note: *When operating in Reverse Bridge mode, ensure that the serial EEPROM sets the* **Device Initialization** *register PCI Enable bit. When operating in Forward Bridge mode, ensure that the serial EEPROM sets the* **Device Initialization** *register PCI Express Enable bit.*

6.4 Serial EEPROM Random Read/Write Access

A PCI Express or PCI Bus master uses the **Serial EEPROM Control (EECTL)** register to access the serial EEPROM. This register contains 8-bit Read and Write Data fields, Read and Write Start signals, and related Status bits.

The following "C" routines demonstrate the firmware protocol required to access the serial EEPROM through the **Serial EEPROM Control** register. An interrupt is usually generated when the **Serial EEPROM Control** register *Serial EEPROM Busy* bit goes from true to false.

6.4.1 Serial EEPROM Opcodes

```
READ_STATUS_EE_OPCODE = 5
WREN_EE_OPCODE = 6
WRITE_EE_OPCODE = 2
READ_EE_OPCODE = 3
```

6.4.2 Serial EEPROM Low-Level Access Routines

```
int EE_WaitIdle()
{
    int eeCtl, ii;
    for (ii = 0; ii < 100; ii++)
     {
        PEX 8111Read(EECTL, eeCtl);      /* read current value in EECTL */
        if ((eeCtl & (1 << EEPROM_BUSY)) == 0) /* loop until idle */
            return(eeCtl);
    }
    PANIC("EEPROM Busy timeout!\n");
}
void EE_Off()
{
    EE_WaitIdle();                        /* make sure EEPROM is idle */
    PEX 8111Write(EECTL, 0);              /* turn off everything (especially
EEPROM_CS_ENABLE)*/
}
int EE_ReadByte()
{
    int eeCtl = EE_WaitIdle();            /* make sure EEPROM is idle */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_READ_START);
    PEX 8111Write(EECTL, eeCtl);          /* start reading */
    eeCtl = EE_WaitIdle();                /* wait until read is done */
    return((eeCtl >> EEPROM_READ_DATA) & 0xff); /* extract read data from
EECTL */
}
void EE_WriteByte(int val)
{
    int eeCtl = EE_WaitIdle();            /* make sure EEPROM is idle */
    eeCtl &= ~(0xff << EEPROM_WRITE_DATA);/* clear current WRITE value */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_WRITE_START) |
             ((val & 0xff) << EEPROM_WRITE_DATA);
    PEX 8111Write(EECTL, eeCtl);
}
```

6.4.3 Serial EEPROM Read Status Routine

```
...
EE_WriteByte(READ_STATUS_EE_OPCODE);      /* read status opcode */
status = EE_ReadByte();                   /* get EEPROM status */
EE_Off();                                 /* turn off EEPROM */
...
```

6.4.4 Serial EEPROM Write Data Routine

```
...
EE_WriteByte(WREN_EE_OPCODE);          /* must first write-enable */
EE_Off();                              /* turn off EEPROM */
EE_WriteByte(WRITE_EE_OPCODE);         /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM       /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);               /* send next byte of address */
EE_WriteByte(addr);                    /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    EE_WriteByte(buffer[ii]);          /* send data to be written */
}
EE_Off();                              /* turn off EEPROM */
...
```

6.4.5 Serial EEPROM Read Data Routine

```
...
EE_WriteByte(READ_EE_OPCODE);          /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM       /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);               /* send next byte of address */
EE_WriteByte(addr);                    /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
   buffer[ii] = EE_ReadByte(buffer[ii]);   /* store read data in buffer */
}
EE_Off();                              /* turn off EEPROM */
```

Chapter 7 Address Spaces

7.1 Introduction

The PEX 8111 supports the following Address spaces:

- PCI-compatible Configuration (00h to FFh; 256 bytes)
- PCI Express Extended Configuration (100h to FFFh)
- I/O (32-bit)
- Memory (32-bit Non-Prefetchable)
- Prefetchable Memory (64-bit)

The first two spaces are used for accessing Configuration registers. (Refer to Chapter 8, "Configuration Transactions," for details.)

PCI Express Extended Configuration space (100h to FFFh) is supported only in Forward Bridge mode.

Table 7-1 lists which bus is primary or secondary for the PEX 8111 Forward and Reverse Bridge modes.

The other three Address spaces determine which transactions are forwarded from the primary to secondary bus, and from the secondary to primary bus. The Memory and I/O ranges are defined by a set of **Base** and **Limit** registers in the Configuration Header. Transactions falling within the ranges defined by the **Base** and **Limit** registers are forwarded from the primary to secondary bus. Transactions falling outside these ranges are forwarded from the secondary to primary bus.

The PEX 8111 does not perform Address Translation (flat address space) when transactions cross the bridge.

Table 7-1. Primary and Secondary Bus Definitions for Forward and Reverse Bridge Modes

Bridge Mode	Primary Bus	Secondary Bus
Forward Bridge	PCI Express	PCI
Reverse Bridge	PCI	PCI Express

7.2 I/O Space

The I/O Address space determines whether to forward I/O Read or I/O Write transactions across the bridge. PCI Express uses the 32-bit Short Address Format (DWORD-aligned) for I/O transactions.

7.2.1 Enable Bits

The bridge response to I/O transactions is controlled by five Configuration register bits:

- **PCI Command** register *I/O Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *ISA Enable* bit
- **Bridge Control** register *VGA Enable* bit
- **Bridge Control** register *VGA 16-Bit Decode* bit

The *I/O Space Enable* bit must be set for I/O transactions to be forwarded downstream. When cleared:

- All I/O transactions on the secondary bus are forwarded to the primary bus
- Forward Bridge mode – All primary interface I/O requests are completed with Unsupported Request status
- Reverse Bridge mode – All I/O transactions are ignored (no DEVSEL# assertion) on the primary (PCI) bus

The *Bus Master Enable* bit must be set for I/O transactions to be forwarded upstream. When cleared:

- Forward Bridge mode – All I/O transactions on the secondary (PCI) bus are ignored
- Reverse Bridge mode – All I/O requests on the secondary (PCI Express) bus are completed with Unsupported Request status

The *ISA Enable* bit is discussed in Section 7.2.3, "ISA Mode." The *VGA Enable* and *VGA 16-Bit Decode* bits are discussed in Section 7.2.4, "VGA Mode."

7.2.2 I/O Base and Limit Registers

The following **I/O Base** and **Limit** Configuration registers are used to determine whether to forward I/O transactions across the bridge:

- **I/O Base** (upper four bits of 8-bit register correspond to Address bits [15:12])
- **I/O Base Upper 16 Bits** (16-bit register corresponds to Address bits [31:16])
- **I/O Limit** (upper four bits of 8-bit register correspond to Address bits [15:12])
- **I/O Limit Upper 16 Bits** (16-bit register correspond to Address bits [31:16])

The I/O base consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit **I/O Base** register define bits [15:12] of the I/O Base address. The lower four bits of the 8-bit register determine the I/O address capability of this device. The 16 bits of the **I/O Base Upper 16 Bits** register define bits [31:16] of the I/O Base address.

The I/O limit consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit **I/O Limit** register define bits [15:12] of the I/O Limit address. The lower four bits of the 8-bit register determine the I/O address capability of this device, and reflect the value of the same field in the **I/O Base** register. The 16 bits of the **I/O Limit Upper 16 Bits** register define bits [31:16] of the I/O Limit address.

Because Address bits [11:0] are not included in the Address space decoding, the I/O Address range maintains a granularity of 4 KB and is always aligned to a 4-KB boundary. The maximum I/O range is 4 GB.

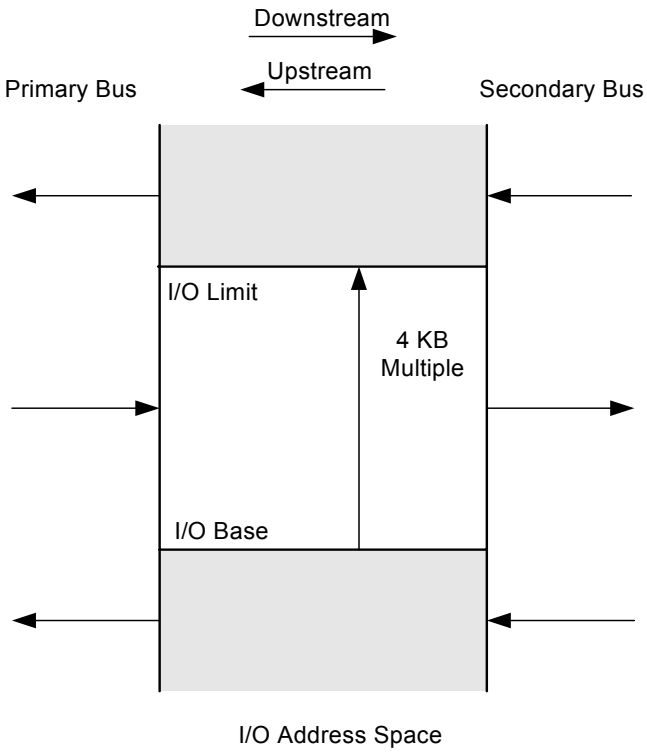
I/O transactions on the primary bus that fall within the range defined by the **I/O Base** and **Limit** registers are forwarded downstream to the secondary bus, and I/O transactions on the secondary bus that are within the range are ignored.

I/O transactions on the primary bus that do not fall within the range defined by the **I/O Base** and **Limit** registers are ignored, and I/O transactions on the secondary bus that do not fall within the range are forwarded upstream to the primary bus.

Figure 7-1 illustrates I/O forwarding.

For 16-bit I/O addressing, when the **I/O Base** retains a value greater than the **I/O Limit**, the I/O range is disabled. For 32-bit I/O addressing, when the I/O base specified by the **I/O Base** and **I/O Base Upper 16 Bits** registers retains a value greater than the I/O limit specified by the **I/O Limit** and **I/O Base Upper 16 Bits** registers, the I/O range is disabled. In these cases, all I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

Figure 7-1. I/O Forwarding



7.2.3 ISA Mode

The **Bridge Control** register *ISA Enable* bit supports I/O forwarding in a system that contains an ISA Bus. The *ISA Enable* bit only affects I/O addresses that are within the range defined by the **I/O Base** and **Limit** registers, and are in the first 64 KB of the I/O Address space.

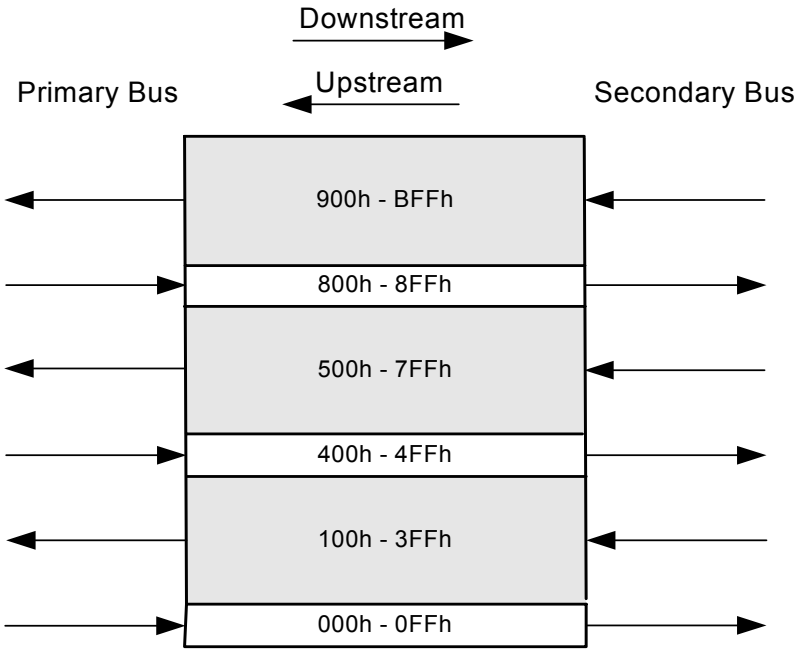
When the *ISA Enable* bit is set, the bridge does not forward downstream I/O transactions on the primary bus that are in the top 768 bytes of each 1-KB block within the first 64 KB of Address space. Only transactions in the bottom 256 bytes of each 1-KB block are forwarded downstream. When the *ISA Enable* bit is clear, all addresses within the range defined by the **I/O Base** and **Limit** registers are forwarded downstream. I/O transactions with addresses above 64 KB are forwarded according to the range defined by the **I/O Base** and **Limit** registers.

When the *ISA Enable* bit is set, the bridge forwards upstream I/O transactions on the secondary bus that are in the top 768 bytes of each 1-KB block within the first 64 KB of Address space, although the address is within the I/O base and limit. All other transactions on the secondary bus are forwarded upstream when they fall outside the range defined by the **I/O Base** and **Limit** registers. When the *ISA Enable* bit is clear, all secondary bus I/O addresses outside the range defined by the **I/O Base** and **Limit** registers are forwarded upstream.

As with all upstream I/O transactions, the **PCI Command** register *Bus Master Enable* bit must be set to enable upstream forwarding.

Figure 7-2 illustrates I/O forwarding with the *ISA Enable* bit set.

Figure 7-2. I/O Forwarding with the *ISA Enable* Bit Set



7.2.4 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Register accesses to be forwarded downstream from the primary to secondary bus, independent of the **I/O Base** and **Limit** registers.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O address decoding, and is applicable when the *VGA Enable* bit is set.

The *VGA Enable* and *VGA 16-Bit Decode* bits control the following VGA I/O addresses:

- 10-bit addressing – Address bits [9:0] = 3B0h through 3BBh, and 3C0h through 3DFh
- 16-bit addressing – Address bits [15:0] = 3B0h through 3BBh, and 3C0h through 3DFh

These ranges apply only to the first 64 KB of I/O Address space.

7.2.4.1 VGA Palette Snooping

Separate VGA palette snooping is not supported by PCI Express-to-PCI bridges; however, the PEX 8111 supports palette snooping in Reverse Bridge mode. In Forward Bridge mode, the **Bridge Control** register *VGA Enable* bit determines whether VGA Palette accesses are forwarded from PCI Express-to-PCI. The **PCI Command** register *VGA Palette Snoop* bit is forced to 0 in Forward Bridge mode.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O palette snooping address decoding, and is applicable when the *VGA Palette Snoop* bit is set.

The *VGA Palette Snoop* and *VGA 16-Bit Decode* bits control the following VGA I/O Palette Snoop addresses:

- 10-bit addressing – Address bits [9:0] = 3C6h, 3C8h, and 3C9h
- 16-bit addressing – Address bits [15:0] = 3C6h, 3C8h, and 3C9h

The PEX 8111 supports the following three modes of palette snooping:

- Ignore VGA palette accesses when there are no graphics agents downstream that need to snoop or respond to VGA Palette Access cycles (reads or writes)
- Positively decode and forward VGA palette writes when there are graphics agents downstream of the PEX 8111 that require to snoop palette writes (reads are ignored)
- Positively decode and forward VGA palette reads and writes when there are graphics agents downstream that require to snoop or respond to VGA Palette Access cycles (reads or writes)

The **Bridge Control** register *VGA Enable* bit and **PCI Command** register *VGA Palette Snoop* bit select the bridge response to Palette accesses, as delineated in Table 7-2.

Table 7-2. Bridge Response to Palette Access

VGA Enable	VGA Palette Snoop	Response to Palette Accesses
0	0	Ignore all Palette accesses
0	1	Positively decode Palette writes (ignore reads)
1	X	Positively decode Palette reads and writes

Note: *X is "Don't Care."*

7.3 Memory-Mapped I/O Space

The Memory-Mapped I/O Address space determines whether to forward Non-Prefetchable Memory Read or Write transactions across the bridge. Map devices that experience side effects during reads, *such as* FIFOs, into this space. For PCI-to-PCI Express reads, prefetching occurs in this space only when the Memory Read Line or Memory Read Multiple commands are issued on the PCI Bus. For PCI Express-to-PCI reads, the byte number to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this Address space are limited to a 32-bit range.

7.3.1 Enable Bits

The bridge response to Memory-Mapped I/O transactions is controlled by three Configuration register bits:

- **PCI Command** register *Memory Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *VGA Enable* bit

The *Memory Space Enable* bit must be set for Memory transactions to be forwarded downstream. When cleared:

- All Memory transactions on the secondary bus are forwarded to the primary bus
- Forward Bridge mode – All Non-Posted Memory Requests are completed with an Unsupported Request status, and Posted Write data is discarded
- Reverse Bridge mode – All Memory transactions are ignored on the primary (PCI) bus

The *Bus Master Enable* bit must be set for Memory transactions to be forwarded upstream. When cleared:

- Forward Bridge mode – All Memory transactions on the secondary (PCI) bus are ignored
- Reverse Bridge mode – All Non-Posted Memory Requests on the secondary (PCI Express) bus are completed with an Unsupported Request status, and Posted Write data is discarded

The *VGA Enable* bit is discussed in Section 7.3.3, "VGA Mode."

7.3.2 Memory Base and Limit Registers

The following **Memory Base** and **Limit** Configuration registers are used to determine whether to forward Memory-Mapped I/O transactions across the bridge:

- **Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])

Bits [15:4] of the **Memory Base** register define bits [31:20] of the Memory-Mapped I/O Base address. Bits [15:4] of the **Memory Limit** register define bits [31:20] of the Memory-Mapped I/O Limit address. Bits [3:0] of each register are hardwired to 0h.

Because Address bits [19:0] are not included in the Address space decoding, the Memory-Mapped I/O Address range retains a granularity of 1 MB and is always aligned to a 1-MB boundary. The maximum Memory-Mapped I/O range is 4 GB.

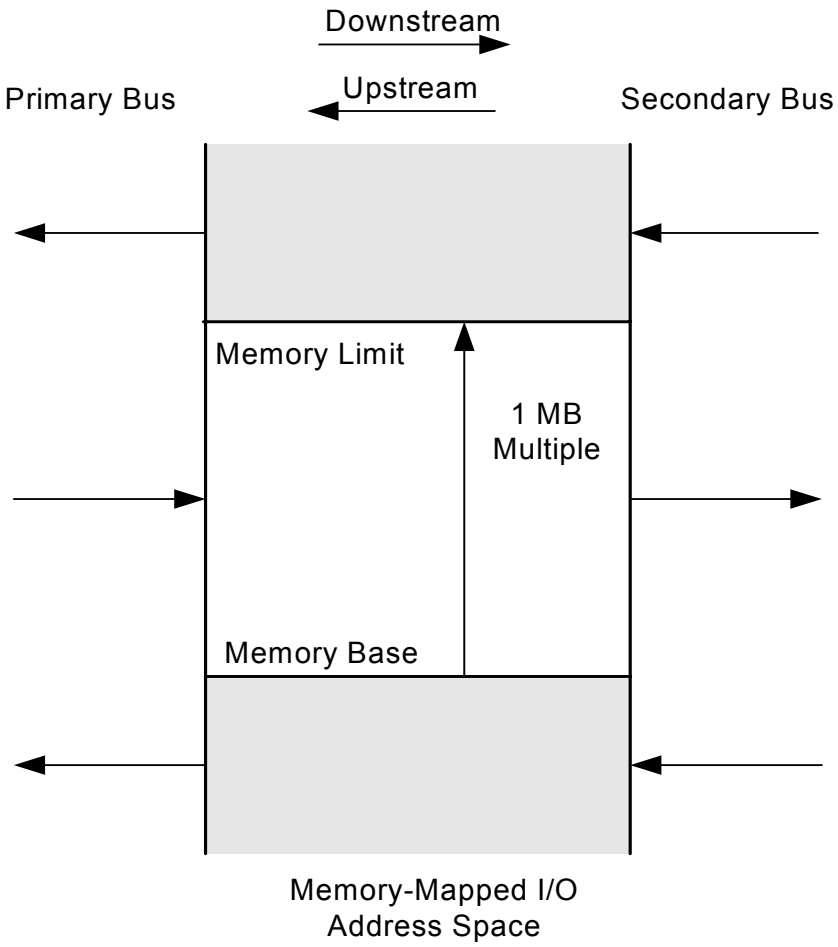
Memory transactions that fall within the range defined by the **Memory Base** and **Limit** registers are forwarded downstream from the primary to secondary bus, and Memory transactions on the secondary bus that are within the range are ignored.

Memory transactions that do not fall within the range defined by the **Memory Base** and **Limit** registers are ignored on the primary bus, and forwarded upstream from the secondary bus (provided they are not in the Address range defined by the set of **Prefetchable Memory Address** registers or forwarded downstream by the VGA mechanism).

Figure 7-3 illustrates Memory-Mapped I/O forwarding.

When the **Memory Base** is programmed to retain a value greater than the **Memory Limit**, then the Memory-Mapped I/O range is disabled. In this case, all Memory transaction forwarding is determined by the **Prefetchable Base** and **Limit** registers and the **Bridge Control** register *VGA Enable* bit.

Figure 7-3. Memory-Mapped I/O Forwarding



7.3.3 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Frame Buffer accesses to be forwarded downstream from the primary to secondary bus, independent of the **Memory Base** and **Limit** registers.

The *VGA Enable* bit controls VGA Memory addresses 0A0000h through 0BFFFFh.

7.4 Prefetchable Space

The Prefetchable Address space determines whether to forward Prefetchable Memory Read or Write transactions across the bridge. Map devices that do not experience side effects during reads into this space.

- For PCI-to-PCI Express reads, prefetching occurs in this space for all Memory Read commands (Memory Read, Memory Read Line, and Memory Read Multiple) issued on the PCI Bus
- For Memory Read commands, the **Device-Specific Control** register *Blind Prefetch Enable* bit must be set for prefetching to occur
- For PCI Express-to-PCI reads, the byte number to read is determined by the Memory Read Request; therefore, prefetching does not occur

7.4.1 Enable Bits

The bridge response to Prefetchable Address space is controlled by three Configuration register bits:

- **PCI Command** register *Memory Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *VGA Enable* bit

For further details, refer to Section 7.3.1.

7.4.2 Prefetchable Base and Limit Registers

The following **Prefetchable Memory Base** and **Limit** Configuration registers are used to determine whether to forward Prefetchable Memory transactions across the bridge:

- **Prefetchable Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Base Upper 32 Bits** (32-bit register corresponds to Address bits [63:32])
- **Prefetchable Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Limit Upper 32 Bits** (32-bit register corresponds to Address bits [63:32])

Bits [15:4] of the **Prefetchable Memory Base** register define bits [31:20] of the Prefetchable Memory Base address. Bits [15:4] of the **Prefetchable Memory Limit** register define bits [31:20] of the prefetchable memory limit. For 64-bit addressing, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are also used to define the space.

Because Address bits [19:0] are not included in the Address space decoding, the Prefetchable Memory Address range retains a granularity of 1 MB and is always aligned to a 1-MB boundary. The maximum Prefetchable Memory range is 4 GB with 32-bit addressing, and 2^{61} bytes with 64-bit addressing.

Memory transactions that fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are forwarded downstream from the primary to secondary bus, and Memory transactions on the secondary bus that are within the range are ignored.

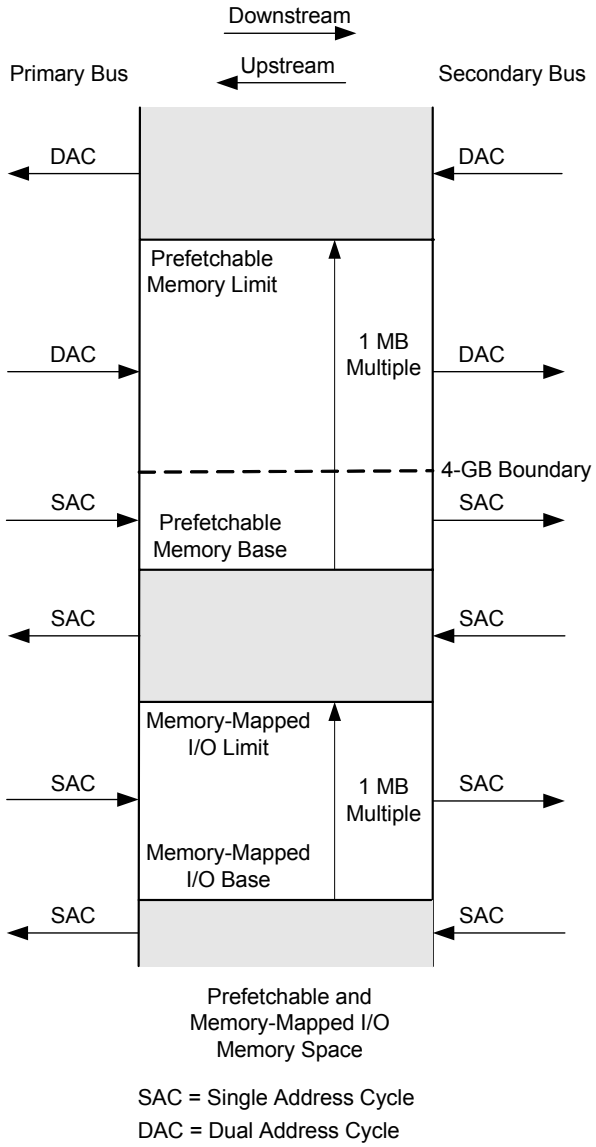
Memory transactions that do not fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are ignored on the primary bus, and forwarded upstream from the secondary bus (provided they are not in the Address range defined by the set of Memory-Mapped I/O Address registers or forwarded downstream by the VGA mechanism).

When the **Prefetchable Memory Base** is programmed to a value greater than the **Prefetchable Memory Limit**, then the Prefetchable Memory range is disabled. In this case, all Memory transaction forwarding is determined by the **Memory Base** and **Limit** registers and the **Bridge Control** register *VGA Enable* bit.

Consider the four **Prefetchable Memory Base** and **Limit** registers when disabling the Prefetchable range.

Figure 7-4 illustrates both Memory-Mapped I/O and Prefetchable Memory forwarding. In the illustration, Dual Address cycles (DAC) indicate 64-bit addressing.

Figure 7-4. Memory-Mapped I/O and Prefetchable Memory Forwarding



7.4.3 64-Bit Addressing

Unlike Memory-Mapped I/O memory that must be below the 4-GB boundary, prefetchable memory is located below, above, or span the 4-GB boundary. Memory locations above the 4-GB boundary must be accessed using 64-bit addressing. PCI Express Memory transactions that use the Short Address (32-bit) format target the non-Prefetchable Memory space, or a Prefetchable Memory window below the 4-GB boundary. PCI Express Memory transactions that use the Long Address (64-bit) format target locations anywhere in the 64-bit Memory space.

PCI Memory transactions that use Single Address cycles only target locations below the 4-GB boundary. PCI Memory transactions that use Dual Address cycles target locations anywhere in the 64-bit Memory space. The first Address phase of Dual Address transactions contains the lower 32 bits of the address, and the second Address phase contains the upper 32 bits of the address. When the upper 32 bits of the address are zero (0h), a Single Address transaction is always performed.

7.4.3.1 Forward Bridge Mode

Below 4-GB Boundary

If the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both cleared to 0, addresses above the 4-GB boundary are ***not supported***. In Forward Bridge mode, if a PCI Express Memory transaction is detected with an address above 4 GB, the transaction is completed with Unsupported Request status. All Dual Address transactions on the PCI Bus are forwarded upstream to the PCI Express Bus.

Above 4-GB Boundary

If the Prefetchable memory is located entirely above the 4-GB boundary, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both set to non-zero values. If a PCI Express Memory transaction is detected with an address below 4 GB, the transaction is completed with Unsupported Request status, and all single address transactions on the PCI Bus are forwarded upstream to the PCI Express Bus (unless the transactions fall within the Memory-Mapped I/O or VGA Memory range). A PCI Express Memory transaction above the 4-GB boundary, that falls within the range defined by the **Prefetchable Memory Base**, **Prefetchable Memory Base Upper 32 Bits**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper 32 Bits** registers, is forwarded downstream and becomes a Dual Address cycle on the PCI Bus. If a Dual Address cycle is detected on the PCI Bus that is outside the range defined by these registers, it is forwarded upstream to the PCI Express Bus. If a PCI Express Memory transaction above the 4-GB boundary does not fall within the range defined by these registers, it is completed with Unsupported Request status. If a PCI Dual Address cycle falls within the range determined by these registers, it is ignored.

Spans 4-GB Boundary

If the Prefetchable memory spans the 4-GB boundary, the **Prefetchable Memory Base Upper 32 Bits** register is cleared to 0, and the **Prefetchable Memory Limit Upper 32 Bits** register is set to a non-zero value. If a PCI Express Memory transaction is detected with an address below the 4-GB boundary, and is greater than or equal to the Prefetchable Memory Base address, then the transaction is forwarded downstream. A single address transaction on the PCI Bus is forwarded upstream to the PCI Express Bus, if the address is less than the Prefetchable Memory Base address. If a PCI Express Memory transaction above the 4-GB boundary is less than or equal to the **Prefetchable Memory Limit** register, it is forwarded downstream to the PCI Bus as a Dual Address cycle. If a Dual Address cycle on the PCI Bus is less than or equal to the **Prefetchable Memory Limit** register, it is ignored. If a PCI Express memory transaction above the 4-GB boundary is greater than the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status. If a Dual Address cycle on the PCI Bus is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Express Bus.

7.4.3.2 Reverse Bridge Mode

Below 4-GB Boundary

If **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both cleared to 0, then addresses above the 4-GB boundary are ***not supported***. In Reverse Bridge mode, if a Dual Address transaction on the PCI Bus is detected, the transaction is ignored. If a PCI Express Memory transaction is detected with an address above the 4-GB boundary, it is forwarded upstream to the PCI Bus as a Dual Address cycle.

Above 4-GB Boundary

If the Prefetchable memory is located entirely above the 4-GB boundary, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both set to non-zero values. The PEX 8111 ignores all Single Address Memory transactions on the PCI Bus, and forwards all PCI Express Memory transactions with addresses below the 4-GB boundary upstream to the PCI Bus (unless they fall within the Memory-Mapped I/O or VGA Memory range).

A Dual Address transaction on the PCI Bus that falls within the range defined by the **Prefetchable Memory Base**, **Prefetchable Memory Base Upper 32 Bits**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper 32 Bits** registers is forwarded downstream to the PCI Express Bus. If a PCI Express Memory transaction is above the 4-GB boundary and falls outside the range defined by these registers, it is forwarded upstream to the PCI Bus as a Dual Address cycle. Dual Address transactions on the PCI Bus that do not fall within the range defined by these registers are ignored. If a PCI Express Memory transaction above the 4-GB boundary falls within the range defined by these registers, it is completed with Unsupported Request status.

Spans 4-GB Boundary

If the Prefetchable memory spans the 4-GB boundary, the **Prefetchable Memory Base Upper 32 Bits** is cleared to 0, and the **Prefetchable Memory Limit Upper 32 Bits** register is set to a non-zero value. If a PCI Single Address cycle is greater than or equal to the Prefetchable Memory Base address, then the transaction is forwarded downstream to the PCI Express Bus. If a PCI Express Memory transaction is detected with an address below the 4-GB boundary, and is less than the Prefetchable Memory Base address, then the transaction is forwarded upstream to the PCI Bus. If a Dual Address PCI transaction is less than or equal to the Prefetchable memory limit register, it is forwarded downstream to the PCI Express Bus. If a PCI Express Memory transaction above the 4-GB boundary is less than or equal to the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status. If a Dual Address PCI transaction is greater than the **Prefetchable Memory Limit** register, it is ignored. If a PCI Express Memory transaction above the 4-GB boundary is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Bus as a Dual Address cycle.

When a PCI Express Memory transaction above 4 GB is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Bus as a Dual Address cycle.

7.4.4 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Frame Buffer accesses to be forwarded downstream from the primary to secondary bus, independent of the **Prefetchable Memory Base** and **Limit** registers.

The *VGA Enable* bit controls VGA Memory addresses 0A0000h through 0BFFFFh.

Chapter 8 Configuration Transactions

8.1 Introduction

Configuration Requests are initiated only by the Root Complex in a PCI Express-based system, or by the Central Resource Function in a PCI-based system. Devices in a PCI Express or PCI system maintain a Configuration space that is accessed using Type 0 or Type 1 Configuration transactions:

- Type 0 Configuration transactions are used to access internal PEX 8111 Configuration registers
- Type 1 Configuration transactions are used to access PEX 8111 devices that reside downstream

The Configuration address is formatted as follows.

Table 8-1. PCI Express

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	***Rsvd***	Extended Register Address	Register Address	***Rsvd***

Table 8-2. PCI Type 0 (at Initiator)

31 16	15 11	10 8	7 2	1 0
Single bit decoding of Device Number	***Rsvd***	Function Number	Register Number	0 0

Table 8-3. PCI Type 0 (at Target)

31 11	10 8	7 2	1 0
Rsvd	Function Number	Register Number	0 0

Table 8-4. PCI Type 1

31 24	23 16	15 11	10 8	7 2	1 0
Rsvd	Bus Number	Device Number	Function Number	Register Number	0 1

8.2 Type 0 Configuration Transactions

The PEX 8111 only responds to Type 0 Configuration transactions on its primary bus that address the PEX 8111 configuration space. A Type 0 Configuration transaction is used to configure the PEX 8111, and is not forwarded downstream to the secondary bus. The PEX 8111 ignores Type 0 Configuration transactions on the secondary bus. Type 0 Configuration transactions always result in the transfer of 1 DWORD.

When Configuration Write data is poisoned, the data is discarded, and a Non-Fatal Error message is generated, when enabled.

8.3 Type 1 Configuration Transactions

Type 1 Configuration transactions are used for device configuration in a hierarchical bus system. Bridges and switches are the only types of devices that respond to a Type 1 Configuration transaction. Type 1 Configuration transactions are used when the transaction is intended for a device residing on a bus other than the one where the Type 1 request is issued.

The *Bus Number* field in a Configuration transaction request specifies a unique bus in the hierarchy on which transaction targets reside. The bridge compares the specified Bus Number with two PEX 8111 Configuration registers – **Secondary Bus Number** and **Subordinate Bus Number** – to determine whether to forward a Type 1 Configuration transaction across the bridge.

When a Type 1 Configuration transaction is received on the primary interface, the following tests are applied, in sequence, to the *Bus Number* field to determine how the transaction must be handled:

- If the *Bus Number* field is equal to the **Secondary Bus Number** register value, and the conditions for converting the transaction into a special cycle transaction are met, the PEX 8111 forwards the Configuration Request to the secondary bus as a special cycle transaction. When the conditions are not met, the PEX 8111 forwards the Configuration Request to the secondary bus as a Type 0 Configuration transaction.
- If the *Bus Number* field is not equal to the **Secondary Bus Number** register value, but is within the range of the **Secondary Bus Number** and **Subordinate Bus Number** (inclusive) registers, the Type 1 Configuration Request is specifying a bus located behind the bridge. In this case, the PEX 8111 forwards the Configuration Request to the secondary bus as a Type 1 Configuration transaction.
- If the *Bus Number* field does not satisfy the above criteria, the Type 1 Configuration Request is specifying a bus that is not located behind the bridge. In this case, the Configuration Request is invalid:
  - If the primary interface is PCI Express, a completion with Unsupported Request status is returned
  - If the primary interface is PCI, the Configuration Request is ignored, resulting in a Master Abort

8.4 Type 1-to-Type 0 Conversion

The PEX 8111 performs a Type 1-to-Type 0 conversion when the Type 1 transaction is generated on the primary bus and is intended for a device directly attached to the secondary bus. The PEX 8111 must convert the Type 1 Configuration transaction to Type 0, thereby allowing the device to respond to it.

Type 1-to-Type 0 conversions are performed only in the downstream direction. The PEX 8111 generates Type 0 Configuration transactions only on the secondary interface, never on the primary interface.

8.4.1 Forward Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Express Bus to a Type 0 transaction on the PCI Bus, when the following are true:

- Type 1 Configuration Request *Bus Number* field is equal to the **Secondary Bus Number** register value.
- Conditions for conversion to a special cycle transaction are not met.

The PEX 8111 then performs the following on the secondary interface:

1. Clears Address bits AD[1:0] to 00b.
2. Derives Address bits AD[7:2] from the Configuration Request *Register Address* field.
3. Derives Address bits AD[10:8] from the Configuration Request *Function Number* field.
4. Clears Address bits AD[15:11] to 0h.
5. Decodes the *Device Number* field and asserts a single Address bit in the range AD[31:16] during the Address phase.
6. Verifies that the Configuration Request *Extended Register Address* field is zero (0h). When the value is non-zero, the PEX 8111 does not forward the transaction, and treats it as an Unsupported Request on the PCI Express Bus, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

8.4.2 Reverse Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Bus to a Type 0 transaction on the PCI Express Bus, when the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- Type 1 Configuration Request *Bus Number* field (AD[23:16]) is equal to the **Secondary Bus Number** register value.
- Bus command on CBE[3:0]# is a Configuration read or write.
- Type 1 Configuration Request *Device Number* field (AD[15:11]) is zero (0h). When the value is non-zero, the transaction is ignored, resulting in a Master Abort.

The PEX 8111 then creates a PCI Express Configuration Request, according to the following:

1. Sets the request *Type* field to Configuration Type 0.
2. Sets the *Register Address* field [7:2] from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Sets the *Function Number* field [18:16] from the Configuration Request *Function Number* field.
5. Clears the *Device Number* field [23:19] from the Configuration Request *Device Number* field (forced to 0h).
6. Sets the *Bus Number* field [31:24] from the Configuration Request *Bus Number* field.

Type 1-to-Type 0 transactions are performed as Non-Posted (Delayed) transactions.

8.5 Type 1-to-Type 1 Forwarding

Type 1-to-Type 1 transaction forwarding provides a hierarchical configuration mechanism when two or more levels of bridges are used. When the PEX 8111 detects a Type 1 Configuration transaction intended for a PCI Bus downstream from the secondary bus, it forwards the transaction unchanged to the secondary bus.

In this case, the transaction target does not reside on the PEX 8111 secondary interface; however, is located on a bus segment further downstream. Ultimately, this transaction is converted to a Type 0 or special cycle transaction by a downstream bridge.

8.5.1 Forward Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Express Bus to a Type 1 transaction on the PCI Bus when the following are true:

- Type 1 Configuration transaction is detected on the PCI Express.
- Value specified by the *Bus Number* field is within the range of bus numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive).

The PEX 8111 then performs the following on the secondary interface:

1. Generates Address bits AD[1:0] as 01b.
2. Generates the PCI Register Number, Function Number, Device Number, and Bus Number from the PCI Express Configuration Request *Register Address*, *Function Number*, *Device Number*, and *Bus Number* fields, respectively.
3. Generates Address bits AD[31:24] as 0h.
4. Verifies that the Configuration Request *Extended Register Address* field is 0h. When the value is non-zero, the PEX 8111 does not forward the transaction, and returns a completion with Unsupported Request status on the PCI Express Bus, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted transactions.

8.5.2 Reverse Bridge Mode

The PEX 8111 forwards a Type 1 transaction on the PCI Bus to a Type 1 transaction on the PCI Express Bus when the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- Value specified by the *Bus Number* field is within the range of bus numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive).
- Bus command on CBE[3:0]# is a Configuration read or write.

The PEX 8111 then creates a PCI Express Configuration Request, according to the following:

1. Sets the Configuration Request *Type* field to Configuration Type 1.
2. Sets the *Register Address* field [7:2] from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Sets the *Function Number* field [18:16] from the Configuration Request *Function Number* field.
5. Sets the *Device Number* field [23:19] from the Configuration Request *Device Number* field.
6. Sets the *Bus Number* field [31:24] from the Configuration Request *Bus Number* field.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted (Delayed) transactions.

8.6 Type 1-to-Special Cycle Forwarding

The Type 1 Configuration Mechanism is used to generate special cycle transactions in hierarchical systems. Special cycle transactions are ignored by the PEX 8111 acting as a target, and are not forwarded across the bridge.

In Forward Bridge mode, special cycle transactions are only generated in the downstream direction (PCI Express-to-PCI).

In Reverse Bridge mode, special cycle transactions are also generated in the downstream direction (PCI-to-PCI Express).

A Type 1 Configuration Write Request on the PCI Express Bus is converted to a special cycle on the PCI Bus when the following conditions are met:

- Type 1 Configuration Request *Bus Number* field is equal to the **Secondary Bus Number** register value.
- *Device Number* field is all ones (1h)
- *Function Number* field is all ones (1h)
- *Register Address* field is all zeros (0h)
- *Extended Register Address* field is all zeros (0h)

When the PEX 8111 initiates the transaction on the PCI Bus, the Bus command is converted from a Configuration write to a special cycle. The Address and Data fields are forwarded, unchanged, from the PCI Express-to-PCI Bus. Target devices that recognize the special cycle ignore the address, and the message is passed in the Data word. The transaction is performed as a Non-Posted transaction; however, the PCI target response (always Master Abort in this case) is not returned to PCI Express. After the Master Abort is detected on the PCI Bus, the successful completion TLP is returned to PCI Express.

8.7 PCI Express Enhanced Configuration Mechanisms

The PCI Express Enhanced Configuration Mechanism adds four extra bits to the *Register Address* field, to expand the space to 4,096 bytes. The PEX 8111 forwards Configuration transactions only when the Extended Register Address bits are all zeros (0h). This prevents address aliasing on the PCI Bus, which does not support Extended Register Addressing.

When a Configuration transaction targets the PCI Bus and contains a non-zero value in the *Extended Register Address* bits, the PEX 8111 treats the transaction as if it received a Master Abort on the PCI Bus.

The PEX 8111 performs the following:

1. Sets the appropriate status bits for the destination bus, as if the transaction had executed and received a Master Abort.
2. Generates a PCI Express completion with Unsupported Request status.
3. Indexed addressing of the Main Control Block registers.

8.7.1 Memory-Mapped Indirect (Reverse Bridge Mode Only)

In Reverse Bridge mode, the PEX 8111 provides the capability for a PCI host to access the downstream PCI Express Configuration registers, using PCI Memory transactions. The 4-KB region of the Memory range defined by the **PCI Base Address 0** register is used for this mechanism. Memory reads and writes to **PCI Base Address 0** register offsets 2000h to 2FFFh result in a PCI Express Configuration transaction. The Transaction address is determined by the **Enhanced Configuration Address** register. The format of this Address register is delineated in Table 8-5.

After the **Enhanced Configuration Address** register is programmed to point to a particular device, the entire PCI Express endpoint 4-KB Configuration space is directly accessed, using Memory Read and Write transactions. Only single DWORDs are transferred during Enhanced Configuration transactions.

Table 8-5. Address Register Format

31	30 28	27 20	19 15	14 12	11 0
Enhanced Enable	***Rsvd***	Bus Number	Device Number	Function Number	***Rsvd***

8.8 Configuration Retry Mechanism

8.8.1 Forward Bridge Mode

Bridges are required to return a completion for all Configuration Requests that cross the bridge from PCI Express-to-PCI, prior to expiration of the Root Complex's Completion Timeout Timer. This requires that bridges take ownership of all Configuration Requests forwarded across the bridge.

When the Configuration Request to PCI successfully completes prior to the bridge's CRS Timer (**CRS Timer** register, offset 1060h) expiration, the bridge returns a completion with Successful Status to PCI Express.

When the Configuration Request to PCI encounters an error condition prior to the CRS Timer expiration, the bridge returns an appropriate error completion to PCI Express.

When the Configuration Request to PCI does not complete successfully or with an error, prior to CRS Timer expiration, then the bridge returns a completion with Configuration Retry Status (CRS) to PCI Express.

Although the PEX 8111 returned a completion with CRS to PCI Express, the PEX 8111 continues to keep the Configuration transaction alive on the PCI Bus. The *PCI r3.0* states that after a PCI master detects a Target Retry, it must continue to Retry the transaction until at least one DWORD is transferred. The PEX 8111 Retries the transaction until it completes on the PCI Bus, or until the PCI Express-to-PCI Retry Timer expires.

When another PCI Express-to-PCI Configuration transaction is detected while the previous one is Retried, a completion with CRS is immediately returned.

When the Configuration transaction completes on the PCI Bus after the return of a completion with CRS on PCI Express, the PEX 8111 discards the completion information. Bridges that implement this option are also required to implement bit 15 of the **PCI Express Device Control** register as the *Bridge Configuration Retry Enable* bit.

When the *Bridge Configuration Retry Enable* bit is cleared, the bridge does not return a completion with CRS on behalf of Configuration Requests forwarded across the bridge. The lack of a completion results in eventual Completion Timeout at the Root Complex.

By default, bridges do not return CRS for Configuration Requests to a PCI device behind the bridge, which might result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

8.8.2 Reverse Bridge Mode

In Reverse Bridge mode, the PEX 8111 detects completion with CRS status from a downstream PCI Express device. The **Device-Specific Control** register *CRS Retry Control* field determines the PEX 8111 response in Reverse Bridge mode when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry Status.

Table 8-6. CRS Retry Control

CRS Retry Control	Response
00b	Retry one time after one second. When another CRS is received, Target Abort on the PCI Bus.
01b	Retry eight times, one time per second. When another CRS is received, Target Abort on the PCI Bus.
10b	Retry one time per second, until successful completion.
11b	***Reserved***

Chapter 9 Error Handling

9.1 Forward Bridge Error Handling

For all errors detected by the bridge, the bridge sets the appropriate error status bit [both legacy PCI error bit(s) and PCI Express error status bit(s)], and optionally generates an error message on PCI Express. Each error condition maintains a default error severity level, with a corresponding error message generated on PCI Express.

Error message generation on the PCI Express Bus is controlled by four Control bits:

- **PCI Command** register *SERR# Enable* bit
- **PCI Express Device Control** register *Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Correctable Error Reporting Enable* bit

PCI Express ERR_FATAL messages are enabled for transmission when the *SERR# Enable* or *Fatal Error Reporting Enable* bit is set. ERR_NONFATAL messages are enabled for transmission when either the *SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. ERR_COR messages are enabled for transmission when the *Correctable Error Reporting Enable* bit is set.

The **PCI Express Device Status** register *Fatal Error Detected*, *Non-Fatal Error Detected*, and *Correctable Error Detected* status bits are set for the corresponding errors on PCI Express, regardless of the *Error Reporting Enable* bits.

9.1.1 Forward Bridge PCI Express Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge when the originating side is the PCI Express interface, and the destination side is the PCI Bus. When a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction must be considered as corrupt. Invert the parity for all data when completing the transaction on the PCI Bus.

Table 9-1 provides the translation a bridge must perform when it forwards a non-posted PCI Express request (read or write) to the PCI Bus, and the request is immediately completed on the PCI Bus, either normally or with an error condition.

Table 9-1. Translation Performed when Bridge Forwards a Non-Posted PCI Express Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with Parity error (reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

9.1.1.1 Received Poisoned TLP

When a write request or read completion is received by the PCI Express interface, and the data is poisoned, the following occur:

- **PCI Status** register *Detected Parity Error* bit is set
- **PCI Status** register *Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PCI Command** register *Parity Error Response Enable* bit is set
- ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- Parity bit associated with each DWORD of data is inverted
- For a poisoned write request, the **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, and the bridge sees PERR# asserted when the inverted parity is detected by the PCI target device

9.1.1.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI Bus, and an Uncorrectable PCI error is detected.

Immediate Reads

When the PEX 8111 forwards a Read Request (I/O, Memory, or Configuration) from the PCI Express and detects an Uncorrectable Data error on the secondary bus while receiving an immediate response from the completer, the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- **Secondary Status** register *Secondary Detected Parity Error* bit is set
- PERR# is asserted on the secondary interface when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8111 continues to fetch data until the Byte Count is satisfied or the target ends the transaction. When the bridge creates the PCI Express completion, it forwards it with Successful Completion and poisons the TLP.

Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI secondary interface while forwarding a non-poisoned Posted Write transaction from PCI Express, the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- After the error is detected, the remainder of the data is forwarded

Non-Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI secondary interface while forwarding a non-poisoned non-posted write transaction from PCI Express, the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- PCI Express completion with Unsupported Request status is generated
- ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

9.1.1.3 PCI Address Errors

When the PEX 8111 forwards transactions from PCI Express-to-PCI, PCI Address errors are reported by SERR# assertion. When the PEX 8111 detects SERR# asserted, the following occur:

- **Secondary Status** register *Secondary Received System Error* bit is set
- ERR_FATAL message is generated on PCI Express, when the following conditions are met:
  - **Bridge Control** register *Secondary SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Secondary SERR# Enable* and *SERR# Enable* bits are set

9.1.1.4 PCI Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Secondary Status** register *Secondary Received Master Abort* bit is set
- ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
  - **Bridge Control** register *Master Abort Mode* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Master Abort Mode* and *SERR# Enable* bits are set

9.1.1.5 PCI Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Completion with Unsupported Request status is returned on PCI Express
- **Secondary Status** register *Secondary Received Master Abort* bit is set

9.1.1.6 PCI Target Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Secondary Status** register *Secondary Received Target Abort* bit is set
- ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

9.1.1.7 PCI Target Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Completion with Completer Abort status is returned on the PCI Express
- **Secondary Status** register *Secondary Received Target Abort* bit is set
- **PCI Status** register *Signaled Target Abort* bit is set
- ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

9.1.1.8 PCI Retry Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in the maximum number of PCI Retries (selectable in the **PCI Control** register), the following occur:

- Remaining data is discarded
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set

9.1.1.9 PCI Retry Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in the maximum number of PCI Retries (selectable in the **PCI Control** register), the following occur:

- Completion with the Completer Abort status is returned on PCI Express
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set
- **PCI Status** register *Signaled Target Abort* bit is set

9.1.2 Forward Bridge PCI Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge when the originating side is the PCI Bus, and the destination side is PCI Express. The PEX 8111 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on the PCI interface. Posted Write data received on the PCI interface with bad parity is forwarded to PCI Express as Poisoned TLPs.

Table 9-2 provides the error forwarding requirements for Uncorrectable data errors detected by the PEX 8111 when a transaction targets the PCI Express interface.

Table 9-2. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort Status

Table 9-3 describes the bridge behavior on a PCI Delayed transaction that is forwarded by a bridge to PCI Express as a Memory Read request or an I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 9-3. Bridge Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Target Abort	Normal completion
Completer Abort	Target Abort	

9.1.2.1 Received PCI Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted write is addressed such that it crosses the bridge, and the PEX 8111 detects an Uncorrectable Data error on the PCI interface, the following occur:

- **Secondary Status** register *Secondary Detected Parity Error* status bit is set.
- If the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, the transaction is discarded and is not forwarded to PCI Express. The PERR# signal is asserted on the PCI Bus.
- If the **Bridge Control** register *Secondary Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. Also, set the **PCI Status** register *Master Data Parity Error* bit when the **PCI Command** register *Parity Error Response Enable* bit is set. The PERR# signal is not asserted on the PCI Bus.

Uncorrectable Data Error on Posted Write

When the PEX 8111 detects an Uncorrectable Data error on the PCI secondary interface for a Posted Write transaction that crosses the bridge, the following occur:

- PCI PERR# signal is asserted when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- **Secondary Status** register *Secondary Detected Parity Error* status bit is set
- Posted Write transaction is forwarded to PCI Express as a poisoned TLP
- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8111 forwards a non-poisoned Read Completion from PCI Express-to-PCI, and it detects PERR# asserted by the PCI master, the remainder of the completion is forwarded.

When the PEX 8111 forwards a poisoned Read Completion from PCI Express-to-PCI, the PEX 8111 proceeds with the above mentioned actions when it detects the PERR# signal asserted by the PCI master; however, no error message is generated on PCI Express.

Uncorrectable Address Error

When an uncorrectable address error is detected by the PEX 8111, and parity error detection is enabled by way of the **Bridge Control** register *Secondary Parity Error Response Enable* bit, the following occur:

- Transaction is terminated with a Target Abort
- **Secondary Status** register *Secondary Detected Parity Error* status bit is set, independent of the setting of the **Bridge Control** register *Secondary Parity Error Response Enable* bit
- **Secondary Status** register *Secondary Signaled Target Abort* bit is set
- ERR_FATAL message is generated on PCI Express when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

9.1.2.2 Unsupported Request (UR) Completion Status

The PEX 8111 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the PCI interface. The response is controlled by the **Bridge Control** register *Master Abort Mode* bit. In either case, the **PCI Status** register *Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and an Unsupported Request is not considered to be an error.

When a Read transaction initiated on the PCI results in the return of a completion with Unsupported Request status, the PEX 8111 returns FFFFFFFFh to the originating master and terminates the Read transaction on the originating interface normally (by asserting TRDY#).

When a Non-Posted Write transaction results in a completion with Unsupported Request status, the PEX 8111 completes the Write transaction on the originating bus normally (by asserting TRDY#) and discards the Write data.

Master Abort Mode Bit Set

When the **Bridge Control** register *Master Abort Mode* bit is set, the PEX 8111 signals a Target Abort to the originating master of an Upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a completion with UR Status. In addition, the **Secondary Status** register *Secondary Signaled Target Abort* bit is set.

9.1.2.3 Completer Abort (CA) Completion Status

When the PEX 8111 receives a completion with Completer Abort status on the PCI Express primary interface in response to forwarded non-posted PCI transactions, the **PCI Status** register *Received Target Abort* bit is set. A CA response results in a Delayed Transaction Target Abort on the PCI Bus. The PEX 8111 provides data to the requesting PCI agent, up to the point where data was successfully returned from the PCI Express interface, then signals Target Abort. The **Secondary Status** register *Secondary Signaled Target Abort* bit is set when signaling Target Abort to a PCI agent.

9.1.3 Forward Bridge Timeout Errors

9.1.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout Mechanism allows requesters to abort a non-posted request when a completion does not arrive within a reasonable length of time. Bridges, when acting as initiators on PCI Express on behalf of internally generated requests or when forwarding requests from a secondary interface, behave as endpoints for requests of which they take ownership.

When a completion timeout is detected and the link is up, the PEX 8111 responds as if a completion with Unsupported Request status is received. The following action is taken:

- ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –OR–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

When the link is down, the **PCI Control** register *PCI-to-PCI Express Retry Count* field determines the number of PCI Retries before a Master Abort is returned to the PCI Bus.

9.1.3.2 PCI Delayed Transaction Timeout Errors

The PEX 8111 maintains Delayed Transaction Timers for each queued Delayed transaction. When a Delayed transaction timeout is detected, the following occur:

- ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
  - **Bridge Control** register *Discard Timer SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- **Bridge Control** register *Discard Timer Status* bit is set

9.1.4 Forward Bridge "Other" Errors

PCI devices assert SERR# when detecting errors that compromise system integrity. When the PEX 8111 detects SERR# asserted on the secondary (PCI) bus, the following occur:

- **Secondary Status** register *Secondary Received System Error* bit is set
- ERR_FATAL message is generated on PCI Express, when the following conditions are met:
  - **Bridge Control** register *Secondary SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Secondary SERR# Enable* and *SERR# Enable* bits are set

9.2 Reverse Bridge Error Handling

For all errors detected by the bridge, the bridge sets the appropriate error status bit [both legacy PCI error bit(s) and PCI Express error status bit(s)]. PCI Express Error messages are not generated in Reverse Bridge mode.

9.2.1 Reverse Bridge PCI Express Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge when the originating side is the PCI Express (secondary) interface, and the destination side is the PCI (primary) interface.

When a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction is considered corrupt. The PEX 8111 inverts the parity for all data when completing the transaction on the PCI Bus.

Table 9-4 provides the translation the PEX 8111 performs when it forwards a non-posted PCI Express request (read or write) to the PCI Bus, and the request is immediately completed on the PCI Bus, either normally or with an error condition.

Table 9-4. PEX 8111 Translation – Non-Posted PCI Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with Parity error (reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

9.2.1.1 Received Poisoned TLP

When a Write Request or Read Completion is received by the PCI Express interface, and the data is poisoned, the following occur:

- **Secondary Status** register *Secondary Detected Parity Error* bit is set
- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- Parity bit associated with each DWORD of data is inverted
- For a poisoned Write request, the **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set, and the bridge sees PERR# asserted when the inverted parity is detected by the PCI target device

9.2.1.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI Bus, and an Uncorrectable PCI error is detected.

Immediate Reads

When the PEX 8111 forwards a Read Request (I/O or Memory) from the PCI Express secondary interface and detects an Uncorrectable Data error on the PCI primary bus while receiving an immediate response from the completer, the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- **PCI Status** register *Detected Parity Error* bit is set
- PERR# is asserted on the PCI interface when the **PCI Command** register *Parity Error Response Enable* bit is set

After detecting an Uncorrectable Data error on the destination bus for an immediate Read transaction, the PEX 8111 continues to fetch data until the Byte Count is satisfied or the target ends the transaction.

When the bridge creates the PCI Express completion, it forwards it with Successful Completion status and poisons the TLP.

Non-Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI primary interface while forwarding a non-poisoned Non-Posted Write transaction from PCI Express, the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- PCI Express completion with Unsupported Request status is returned

Posted Writes

When the PEX 8111 detects PERR# asserted on the PCI primary interface while forwarding a non-poisoned Posted Write transaction from PCI Express, the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- After the error is detected, the remainder of the data is forwarded

9.2.1.3 PCI Address Errors

When the PEX 8111 forwards transactions from PCI Express-to-PCI, PCI Address errors are reported by SERR# assertion by the PCI target. The PEX 8111 ignores the SERR# assertion, and allows the PCI Central Resource Function to service the error.

9.2.1.4 PCI Master Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **PCI Status** register *Received Master Abort* bit is set

9.2.1.5 PCI Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- PCI Express completion with Unsupported Request status is returned
- **PCI Status** register *Received Master Abort* bit is set

9.2.1.6 PCI Target Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **PCI Status** register *Received Target Abort* bit is set

9.2.1.7 PCI Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- PCI Express completion with Completer Abort status is returned
- **PCI Status** register *Received Target Abort* bit is set

9.2.1.8 PCI Retry Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-PCI results in a Retry Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set

9.2.1.9 PCI Retry Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Retry Abort on the PCI Bus, the following occur:

- PCI Express completion with Completer Abort status is returned
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set
- **Secondary Status** register *Secondary Signaled Target Abort* bit is set

9.2.2 Reverse Bridge PCI Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge when the originating side is the PCI Bus, and the destination side is PCI Express. The PEX 8111 supports TLP poisoning as a transmitter, to permit proper forwarding of Parity errors that occur on the PCI interface. Posted Write data received on the PCI interface with bad parity is forwarded to PCI Express as Poisoned TLPs.

Table 9-5 provides the error forwarding requirements for Uncorrectable Data errors detected by the PEX 8111 when a transaction targets the PCI Express interface.

Table 9-6 describes the bridge behavior on a PCI Delayed transaction that is forwarded to PCI Express as a Memory Read request or an I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 9-5. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort Status

Table 9-6. Bridge Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Target Abort	Normal completion
Completer Abort	Target Abort	

9.2.2.1 Received PCI Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted write is addressed such that it crosses the bridge, and the PEX 8111 detects an uncorrectable data error on the PCI interface, the following occur:

- **PCI Status** register *Detected Parity Error* status bit is set.
- If the **PCI Command** register *Parity Error Response Enable* bit is set, the transaction is discarded and is not forwarded to PCI Express. The PCI PERR# signal is asserted.
- If the **PCI Command** register *Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. The **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set. The PCI PERR# signal is not asserted.

Uncorrectable Data Error on Posted Write

When the PEX 8111 detects an Uncorrectable Data error on the PCI interface for a Posted Write transaction that crosses the bridge, the following occur:

- PCI PERR# signal is asserted when the **PCI Command** register *Parity Error Response Enable* bit is set
- **PCI Status** register *Detected Parity Error* status bit is set
- Posted Write transaction is forwarded to PCI Express as a poisoned TLP
- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8111 forwards a non-poisoned or poisoned Read Completion from PCI Express-to-PCI, and PERR# is asserted by the PCI master, the following occur:

- Remainder of the completion is forwarded
- PCI Central Resource Function services the PERR# assertion

Uncorrectable Address Error

When an uncorrectable address error is detected by the PEX 8111 and Parity error detection is enabled by way of the **PCI Command** register *Parity Error Response Enable* bit, the following occur:

- Transaction is terminated with a Target Abort
- **PCI Status** register *Signaled Target Abort* bit is set
- **PCI Status** register *Detected Parity Error* status bit is set, independent of the setting of the **PCI Command** register *Parity Error Response Enable* bit
- SERR# is asserted, when enabled by way of the **PCI Command** register *SERR# Enable* bit
- **PCI Status** register *Signaled System Error* bit is set when SERR# is asserted

9.2.2.2 Unsupported Request (UR) Completion Status

The PEX 8111 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the PCI interface. The response is controlled by the **Bridge Control** register *Master Abort Mode* bit. In either case, the **Secondary Status** register *Secondary Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and an Unsupported Request is not considered to be an error. When a Read transaction initiated on the PCI results in the return of a completion with UR status, the PEX 8111 returns FFFFFFFFh to the originating master and terminates the Read transaction on the originating interface normally (by asserting TRDY#). When a Non-Posted Write transaction results in a completion with UR status, the PEX 8111 completes the Write transaction on the originating bus normally (by asserting TRDY#) and discards the Write data.

Master Abort Mode Bit Set

When the **Bridge Control** register *Master Abort Mode* bit is set, the PEX 8111 signals a Target Abort to the originating master of a downstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a completion with UR status. Moreover, the **PCI Status** register *Signaled Target Abort* bit is set.

9.2.2.3 Completer Abort (CA) Completion Status

When the PEX 8111 receives a completion with Completer Abort status on the PCI Express interface in response to Forwarded Non-Posted PCI transactions, the **Secondary Status** register *Secondary Received Target Abort* bit is set. A completion with CA status results in a Delayed Transaction Target Abort on the PCI Bus. The PEX 8111 provides data to the requesting PCI agent, up to the point where data was successfully returned from the PCI Express interface, then signals Target Abort. The **PCI Status** register *Signaled Target Abort* status bit is set when signaling Target Abort to a PCI agent.

9.2.3 Reverse Bridge Timeout Errors

9.2.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout Mechanism allows requesters to abort a non-posted request when a completion does not arrive within a reasonable length of time. Bridges, when acting as initiators on PCI Express on behalf of internally-generated requests and requests forwarded from a secondary interface, behave as endpoints for requests that they take ownership of. When a completion timeout is detected and the link is up, the PEX 8111 responds as when an unsupported request completion is received.

When the link is down, the **PCI Control** register *PCI-to-PCI Express Retry Count* field determines the number of PCI Retries before a Master Abort is returned to the PCI Bus.

9.2.3.2 PCI Delayed Transaction Timeout Errors

The PEX 8111 maintains Delayed Transaction Timers for each queued Delayed transaction. When a Delayed transaction timeout is detected, the following occur:

- **Bridge Control** register *Discard Timer Status* bit is set
- Delayed request is removed from the Non-Posted Transaction queue
- SERR# is asserted when the **PCI Command** register *SERR# Enable* bit is set

9.2.4 Reverse Bridge PCI Express Error Messages

When the PEX 8111 detects an ERR_FATAL, ERR_NONFATAL, or ERR_COR error, or receives an ERR_FATAL, ERR_NONFATAL, or ERR_COR message, the PCI SERR# signal is asserted when the corresponding Reporting Enable bit in the **Root Control** register is set. When an ERR_FATAL or ERR_NONFATAL message is received, the **Secondary Status** register *Secondary Received System Error* bit is set, independent of the reporting Enable bits in the **Root Control** register.

When an Unsupported Request is received by the PEX 8111, an **Interrupt Request Status** register interrupt status bit is set. This status bit is enabled to generate an INT*x*# or MSI interrupt.

9.2.5 Reverse Bridge “Other” Errors

PCI devices assert SERR# when detecting errors that compromise system integrity. The PEX 8111 never monitors the SERR# ball in Reverse Bridge mode; instead, it allows the PCI Central Resource Function to service the SERR# interrupt.

Chapter 10 Exclusive (Locked) Access

10.1 Forward Bridge Exclusive Accesses

The exclusive access mechanism allows non-exclusive accesses to proceed in the face of exclusive accesses. This allows a master to hold a hardware lock across several accesses without interfering with non-exclusive data transfers. Masters and targets not involved in the exclusive accesses are allowed to proceed with non-exclusive accesses while another master retains a bus lock.

Exclusive access support in the PEX 8111 is enabled by the **PCI Control** register *Locked Transaction Enable* bit. When this bit is cleared, PCI Express Memory Read Locked requests are terminated with a completion with UR status.

10.1.1 Forward Bridge Lock Sequence across PEX 8111

Locked transaction sequences are generated by the Host CPU as one or more reads followed by a number of writes to the same locations. In Forward Bridge mode, the PEX 8111 only supports Locked transaction in the downstream direction (PCI Express-to-PCI). Upstream Locked transactions are not allowed. The initiation of a Locked transaction sequence through the PEX 8111 is as follows:

- Locked transaction starts with a MRdLk Request.
- Successive reads for the Locked transaction also use MRdLk Requests.
- Completions for successful MRdLk requests use the CplDLk Completion type, or the CplLk Completion type for unsuccessful requests.
- When the Locked Completion for the first Locked Read Request is returned, the PEX 8111 does not accept new requests from the PCI Bus.
- Writes for the locked sequence use MWr Requests.
- PEX 8111 remains locked until it is unlocked by the PCI Express. Unlock is then propagated to the PCI Bus by terminating the locked sequence.
- PCI Express Unlock message is used to indicate the end of a locked sequence. Upon receiving an Unlock message, the PEX 8111 unlocks itself. When the PEX 8111 is not locked, it ignores the Unlock message.

When the locked read request is queued in the PCI Express-to-PCI Non-Posted Transaction queue, subsequent non-posted, non-locked requests from the PCI Express are completed with Unsupported Request status. Requests that were queued before the Locked Read Request are allowed to complete.

10.1.2 Forward Bridge PCI Master Rules for Supporting LOCK#

The PEX 8111 must obey the following rules when performing locked sequences on the PCI Bus:

- Master accesses only a single resource during a Lock operation.
- First transaction of a lock operation must be a Memory Read transaction.
- LOCK# must be asserted during the Clock cycle following the Address phase and remain asserted to maintain control.
- LOCK# must be released when the initial transaction of the lock request is terminated with Retry (Lock was not established).
- LOCK# must be released when an access is terminated by Target Abort or Master Abort.
- LOCK# must be de-asserted between consecutive lock operations for a minimum of one Clock cycle while the bus remains in the Idle state.

10.1.3 Forward Bridge Acquiring Exclusive Access across PEX 8111

When a PCI Express Locked Memory Read request appears at the output of the non-posted request queue, the locked request is performed on the PCI Bus. The PEX 8111 monitors the PCI LOCK# ball state when attempting to establish lock. When LOCK# is asserted, the PEX 8111 does not request the PCI Bus to start the transaction.

After LOCK# is de-asserted and the PCI Bus is idle, REQ# is asserted. While waiting for GNT#, the PEX 8111 continues to monitor LOCK#. When LOCK# is busy, the PEX 8111 de-asserts REQ# because another agent gained control of LOCK#.

When the PEX 8111 is granted the bus and LOCK# is not asserted, ownership of LOCK# is obtained. The PEX 8111 is free to perform an exclusive operation when the current transaction completes. LOCK# is de-asserted during the first Address phase, and then is asserted one Clock cycle later. A Locked transaction is not established on the bus until the first Data phase of the first transaction completes (IRDY# and TRDY# asserted).

When the target terminates the first transaction with Retry, the PEX 8111 terminates the transaction and releases LOCK#. After the first Data phase completes, the PEX 8111 holds LOCK# asserted until the Lock operation completes or a Master Abort or Target Abort causes an early termination.

10.1.4 Forward Bridge Non-Posted Transactions and Lock

The PEX 8111 must consider itself locked when a Locked Memory Read Request is detected on the output of the non-posted request queue, although no data is transferred. This condition is referred to as a *target-lock*. While in target-lock, the PEX 8111 does not process new requests on PCI Express.

The bridge locks the PCI bus when lock sequence on the PCI Bus completes. A target-lock becomes a full-lock when the locked request is completed on the PCI Express. At this point, the PCI Express master established the lock.

10.1.5 Forward Bridge Continuing Exclusive Access

When the PEX 8111 performs another transaction to a locked target, LOCK# is de-asserted during the Address phase. The locked target accepts and responds to the request. LOCK# is asserted one Clock cycle after the Address phase to keep the target in the locked state and allow the PEX 8111 to retain ownership of LOCK# beyond the end of the current transaction.

10.1.6 Forward Bridge Completing Exclusive Access

When the PEX 8111 receives an Unlock message from the PCI Express, it de-asserts LOCK# on the PCI Bus.

10.1.7 Forward Bridge Invalid PCI Express Requests while Locked

When the PEX 8111 is locked, it only accepts PCI Express Memory Read Lock or Memory Write transactions that are being forwarded to the PCI Bus. Other transaction types are terminated with a completion with Unsupported Request status, including Non-Posted accesses to internal Configuration registers and shared memory.

10.1.8 Forward Bridge Locked Transaction Originating on PCI Bus

Locked transactions originating on the secondary bus are not allowed to propagate to the primary bus. When a Locked transaction is performed on the PCI Bus and intended for the PEX 8111, the PEX 8111 ignores the transaction.

10.1.9 Forward Bridge PCI Bus Errors while Locked

10.1.9.1 PCI Master Abort during Posted Transaction

When a PCI Master Abort occurs during a PCI Express-to-PCI Locked Write transaction, the PEX 8111 de-asserts LOCK#, thereby releasing the PCI bus from the locked state. Also, the PCI Express bus is released from the locked state, although no Unlock Message is received. Write data is discarded.

Refer to Section 9.1.1.4, "PCI Master Abort on Posted Transaction," for additional details describing the action taken when a Master Abort is detected during a Posted transaction.

10.1.9.2 PCI Master Abort during Non-Posted Transaction

When a PCI Master Abort occurs during a PCI Express-to-PCI Locked Read transaction, the PEX 8111 de-asserts LOCK#, thereby releasing the PCI Bus from the locked state. Also, the PCI Express Bus is released from the locked state, although no Unlock Message is received. A CplLk with Unsupported Request status is returned to the PCI Express Bus.

Refer to Section 9.1.1.5, "PCI Master Abort on Non-Posted Transaction," for additional details describing the action taken when a Master Abort is detected during a Non-Posted transaction.

10.1.9.3 PCI Target Abort during Posted Transaction

When a PCI Target Abort occurs during a PCI Express-to-PCI Locked Write transaction, the PEX 8111 de-asserts LOCK#, thereby releasing the PCI bus from the locked state. Also, the PCI Express Bus is released from the locked state, although no Unlock message is received. Write data is discarded.

Refer to Section 9.1.1.6, "PCI Target Abort on Posted Transaction," for additional details describing the action taken when a Target Abort is detected during a Posted transaction.

10.1.9.4 PCI Target Abort during Non-Posted Transaction

When a PCI Target Abort occurs during a PCI Express-to-PCI Locked Read transaction, the PEX 8111 de-asserts LOCK#, thereby releasing the PCI Bus from the locked state. Also, the PCI Express bus is released from the locked state, although no Unlock Message is received. A CplLk with Completer Abort status is returned to the PCI Express Bus.

Refer to Section 9.1.1.7, "PCI Target Abort on Non-Posted Transaction," for additional details describing the action taken when a Target Abort is detected during a Non-Posted transaction.

10.2 Reverse Bridge Exclusive Accesses

A reverse bridge is allowed to pass Locked transactions from the primary interface (PCI Bus) to the secondary interface (PCI Express Bus). When a locked request (LOCK# asserted) is initiated on the PCI Bus, then a Memory Read Locked Request is issued to the PCI Express Bus. All subsequent Locked Read transactions targeting the PEX 8111 use the Memory Read Locked Request on the PCI Express Bus. All subsequent Locked Write transactions use the Memory Write Request on the PCI Express Bus. The PEX 8111 must transmit the Unlock message when PCI Lock sequence is complete.

Exclusive access support in the PEX 8111 is enabled by the **PCI Control** register *Locked Transaction Enable* bit. When this bit is cleared, the PCI LOCK# ball is ignored, and Locked transactions are treated as Unlocked transactions.

10.2.1 Reverse Bridge PCI Target Rules for Supporting LOCK#

- The PEX 8111, acting as a target of an access, locks itself when LOCK# is de-asserted during the Address phase and is asserted during the following Clock cycle.
- Lock is established when LOCK# is de-asserted during the Address phase, asserted during the following Clock cycle, and data is transferred during the current transaction.
- After lock is established, the PEX 8111 remains locked until both FRAME# and LOCK# are sampled de-asserted, regardless of how the transaction is terminated.
- The PEX 8111 is not allowed to accept new requests (from PCI or PCI Express) while it remains in a locked condition, except from the owner of LOCK#.

10.2.2 Reverse Bridge Acquiring Exclusive Access across PEX 8111

A PCI master attempts to forward a Locked Memory Read transaction to the PCI Express Bus. The transaction is terminated by the PEX 8111 with a Retry, and the locked request is written to the PCI-to-PCI Express Non-Posted Transaction queue. When this locked request reaches the top of the queue, the locked request is performed on the PCI Express bus as a Memory Read Lock Request. When the PCI Express responds with a locked completion, the locked request is updated with completion status. When the PCI master Retries the locked memory read request, the PEX 8111 responds with TRDY#, thereby completing the lock sequence.

When the PEX 8111 is locked, it only accepts PCI Locked transactions that are being forwarded to the PCI Express Bus. Other bus transactions are terminated with a Retry, including accesses to internal Configuration registers and shared memory. All PCI Express requests are terminated with a completion with Unsupported Request status.

10.2.3 Reverse Bridge Completing Exclusive Access

When the PEX 8111 detects LOCK# and FRAME# de-asserted, it transmits an Unlock message to the PCI Express Bus.

10.2.4 Reverse Bridge PCI Express Locked Read Request

When a Locked Read Request is performed on the PCI Express Bus, the PEX 8111 responds with a completion with Unsupported Request status.

10.2.5 Reverse Bridge Limitations

In a system with multiple PCI masters that perform exclusive transactions to the PCI Express Bus, the **PCI Control** register *Locked Transaction Enable* bit must be set.

Chapter 11 Power Management

11.1 Forward Bridge Power Management

PCI Express defines Link power management states, replacing the bus power management states that were defined by the *PCI Power Mgmt. r1.1*. Link states are not visible to *PCI Power Mgmt. r1.1* legacy-compatible software, and are derived from the power management D states or by Active State power management protocols.

11.1.1 Forward Bridge Link State Power Management

11.1.1.1 Link Power States

Table 11-1 delineates the link power states supported by the PEX 8111 in Forward Bridge mode.

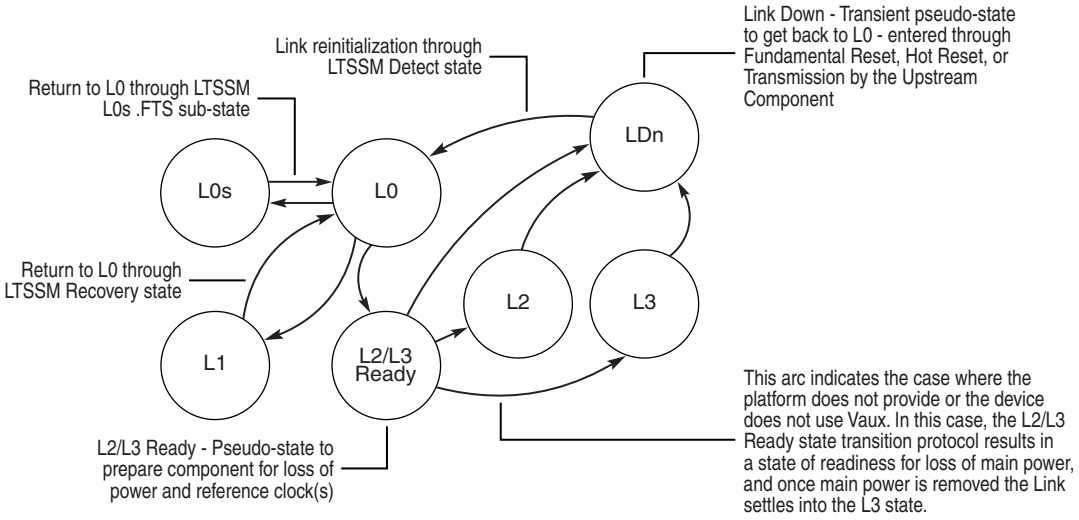
Table 11-1. Supported Link Power States (Forward Bridge)

Link Power State	Description
L0	Active state. All PCI Express operations are enabled.
L0s	A low resume latency, energy-saving "standby" state.
L1	Higher latency, lower power "standby" state. L1 support is required for *PCI Power Mgmt. r1.1*-compatible power management. L1 is optional for Active State Link power management. All platform provided main power supplies and component reference clocks must remain active at all times in L1. The component internal PLLs are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered when all functions of a downstream component on a given PCI Express Link are programmed to a D-state other than D0, or when the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by an upstream initiated transaction targeting the downstream component, or by the need of the downstream component to initiate a transaction heading upstream. Transition from L1 to L0 is typically a few microseconds. TLP and DLLP communication over a Link that remains in the L1 state is prohibited. The PEX 8111 only requests L1 entry for *PCI Power Mgmt. r1.1*-compatible power management. When PMEIN# is asserted, the PEX 8111 requests a transition from L1 to L0.
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to *PCI Power Mgmt. r1.1* D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for L2 or L3; however, not actually in either of those states until main power is removed. Depending upon the implementation choices of the platform with respect to providing a Vaux supply, after main power is removed, the Link settles into L2 (*that is*, Vaux is provided), or into a zero power "off" state (refer to L3). The PEX 8111 does ***not support*** L2; therefore, it settles into the L3 state. The L2/L3 Ready state entry transition process must start as soon as possible following the PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its transmit Port. TLP and DLLP communication over a Link that remains in L2/L3 Ready is prohibited. Exit from L2/L3 Ready to L0 is initiated only by an upstream-initiated transaction targeting the downstream component in the same manner that an upstream-initiated transaction triggers the transition from L1 returning to L0. In the case of an upstream-initiated exit from L2/L3 Ready occurring, corresponds to the scenario wherein some time following the transition of the Link to L2/L3 Ready, but before main power is removed, and the platform power manager decides not to enter the system sleep state. A Link's transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol, leading up to the platform entering into in a system sleep state wherein main power is shut off (*such as*, ACPI S3 or S4 sleep state).
L2	***Not supported.*** Auxiliary powered link deep energy-saving state. by PEX 8111.
L3	Link-off state. Power-off state.

11.1.1.2 Link State Transitions

Figure 11-1 highlights the L-state transitions which occur during the course of Link operations.

Figure 11-1. L-State Transitions during Link Operations



Note: *In this case, the L2/L3 Ready state transition protocol results in a state of readiness for loss of main power, and after removal, the Link settles into the L3 state.*

The arc indicated in Figure 11-1 indicates the case wherein the platform does not provide Vaux. Link PM Transitions from an L-state to another L-state pass through the L0 state during the transition process with the exception of the L2/L3 Ready to L2 or L3 transitions. In this case, the Link transitions from L2/L3 Ready directly to L2 or L3 when main power to the component is removed. (This follows along with a D-state transition from D3, for the corresponding component.)

The following sequence, leading up to entering a system sleep state, illustrates the multi-step Link state transition process:

1. System software directs all functions of a downstream component to D3hot.
2. The downstream component then initiates the transition of the Link to L1 as required.
3. System software then causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
4. This message causes the subject Link to transition (return) to L0 to transmit it, and enable the downstream component to respond with PME_TO_Ack.
5. After the PME_TO_Ack is transmitted, the downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

- L0 –> L1 –> L0 –> L2/L3 Ready
- L2/L3 Ready entry sequence is initiated at the completion of the PME_Turn_Off/PME_TO_Ack protocol handshake

It is also possible to remove power without first placing all devices into D3hot:

1. System software causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
2. The downstream components respond with PME_TO_Ack.
3. After the PME_TO_Ack is transmitted, the downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

- L0 –> L2/L3 Ready

11.1.2 Forward Bridge Power Management States

The PEX 8111 provides the Configuration registers and support hardware required by the *PCI Power Mgmt. r1.1*. The **PCI Capabilities Pointer** register points to the Base address of the Power Management registers (40h in the PEX 8111).

The PEX 8111 also supports the PCI Express Active State Link Power Management protocol, as described in Section 11.1.1.

11.1.2.1 Power States

Table 11-2 delineates the power states supported by the PEX 8111, selectable by way of the **Power Management Control/Status** register *Power State* field.

When transitioning from D0 to another state, the PCI Express link transitions to link state L1.

System software must allow a minimum recovery time following a D3hot to D0 transition of at least 10 ms, prior to accessing the function. *For example*, this recovery time is used by the D3hot to D0 transitioning component to bootstrap its component interfaces (*such as*, from serial ROM) prior to being accessible. Attempts to target the function during the recovery time (including configuration request packets) results in undefined behavior.

Table 11-2. Supported Power States (Forward Bridge)

Power State	Description
D0_uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Space Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0_active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Space Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. All PCI Express requests generated by the PEX 8111 are disabled except for PME messages.
D2	Heavy sleep. Same restrictions as D1.
D3hot	Function context not maintained. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. All PCI Express requests generated by the PEX 8111 are disabled except for PME messages. From this state, the next power state is D3cold or D0 uninitialized. When transitioning from D3hot to D0, the entire chip is reset.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold state to the D0 uninitialized state. At this point software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0 active state.

11.1.3 Forward Bridge Power Management Signaling

PCI devices assert PME# to signal a Power Management Event (PME). The PEX 8111 converts the PME# signal to PCI Express PME messages. There are no internal events that cause a PME message to transmit upstream.

Power Management messages are used to support Power Management Events signaled by devices downstream of the PEX 8111. System software must identify the source of a PCI Power Management Event that is reported by a PM_PME message. When the PME comes from an agent on a PCI Bus, then the PM_PME Message Requester ID reports the Bus Number from which the PME was collected, and the Device Number and Function Number reported must both be 0.

When the PME message is transmitted to the host, the **Power Management Control/Status** register *PME Status* bit is set and a 100 ms timer is started. When the status bit is not cleared within 100 ms, another PME message is transmitted.

When the upstream device is powering down the downstream devices, it first places all devices into the D3hot state. It then transmits a PCI Express PME_Turn_Off message. After the PEX 8111 receives this message, it does not transmit further PME messages upstream. The PEX 8111 then transmits a PME_TO_Ack message to the upstream device and places its link into the L2/L3 Ready state. It is now ready to be powered-down. When the upstream device returns the PEX 8111 power state to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8111, and is not communicated to the PCI devices. The PEX 8111 does not issue a PM_PME message on behalf of a downstream PCI device while its upstream Link remains in the L2/L3 non-communicating state.

To avoid loss of PCI backplane PME# assertions in the conversion of the level-sensitive PME# signal to the edge triggered PCI Express PM_PME message, the PCI PME# signal is polled every 256 ms by the PEX 8111 and a PCI Express PM_PME message is generated when PME# is asserted.

11.1.3.1 Wakeup

When the link remains in the L2 state, a device on the secondary (PCI) bus signals the Root Complex to wake up the link.

The PEX 8111 asserts the WAKEOUT# signal or transmits a PCI Express beacon for the following:

- PCI PME# signal is asserted while link remains in L2 state
- PCI Express beacon is received while link remains in L2 state
- PCI Express PM_PME Message is received

A beacon is transmitted when the following are true:

- PCI PME# signal is asserted while link remains in L2 state
- **Device-Specific Control** register *Beacon Generate Enable* bit is set
- **Power Management Control/Status** register *PME Enable* bit is set

11.1.4 Set Slot Power

When a PCI Express link first comes up, or the Root Complex **Slot Capabilities** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields are changed, the Root Complex transmits a Set Slot Power message.

When the PEX 8111 receives this message, it updates its **Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

When the available power indicated by the **Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields is greater than or equal to the power requirement indicated in the **Power** register, the PWR_OK signal is asserted.

11.2 Reverse Bridge Power Management

The PEX 8111 supports Active State Power Management (ASPM) in Reverse Bridge mode. The default is that L1 be enabled and L0s be disabled.

11.2.1 Reverse Bridge Active State Power Management (ASPM)

11.2.1.1 ASPM States

Table 11-3 delineates the link power states supported by the PEX 8111 in Reverse Bridge mode.

Table 11-3. Supported Link Power States (Reverse Bridge)

Link Power State	Description
L0	Active state. All PCI Express operations are enabled.
L0s	A low-resume latency, energy-saving "standby" state. when enabled by the serial EEPROM or external driver, the PEX 8111 transmitter transitions to L0s after a low resume latency, energy-saving "standby" state. L0s support is required for Active State Link power management. It is not applicable to *PCI Power Mgmt. r1.1*-compatible power management. All main power supplies, component reference clocks, and components' internal PLLs must be active at all times during L0s. TLP and DLLP communication over a Link that remains in L0s is prohibited. The L0s state is exclusively used for active-state power management. The PCI Express physical layer provides mechanisms for quick transitions from this state to the L0 state. When common (distributed) reference clocks are used on both sides of a given Link, the transition time from L0s to L0 is typically fewer than 100 symbol times.
L1	Higher-latency, lower-power "standby" state. L1 support is required for *PCI Power Mgmt. r1.1*-compatible power management. L1 is optional for Active State Link power management. All platform provided main power supplies and component reference clocks must remain active at all times in L1. A component's internal PLLs are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered when all functions of a downstream component on a given PCI Express Link are programmed to a D-state other than D0, or when the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by an upstream initiated transaction targeting the downstream component, or by the downstream component's need to initiate a transaction heading upstream. Transition from L1 to L0 is typically a few microseconds. TLP and DLLP communication over a Link that remains in the L1 state is prohibited.
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to *PCI Power Mgmt. r1.1* D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for L2 or L3; however, not actually in either of those states until main power is removed. Depending upon the platform's implementation choices with respect to providing a Vaux supply, after main power is removed, the Link either settles into L2 (*for example*, Vaux is provided), or into a zero power "off" state (refer to L3). The PEX 8111 does not maintain Vaux capability; however, it supports L2 when the system Vaux supply is used as the main power to the PEX 8111. The L2/L3 Ready state entry transition process must start as soon as possible following PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its transmit Port. TLP and DLLP communication over a Link that remains in L2/L3 Ready is prohibited. Exit from L2/L3 Ready returning to L0 is initiated only by an upstream-initiated transaction targeting the downstream component in the same manner that an upstream-initiated transaction triggers the transition from L1 returning to L0. In the case of an upstream-initiated exit from L2/L3 Ready occurring, corresponds to the scenario wherein some time following the transition of the Link to L2/L3 Ready, but before main power is removed, and the platform power manager decides not to enter the system sleep state. A Link's transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol leading up to the platform entering into in a system sleep state wherein main power is shut off (*for example*, ACPI S3 or S4 sleep state).
L2	Auxiliary-powered link deep energy-saving state.
L3	Link-off state. Power-off state.

11.2.2 Reverse Bridge Power Management States

The PEX 8111 provides the Configuration registers and support hardware required by the *PCI Power Mgmt. r1.1*. The **PCI Capabilities Pointer** register points to the Base address of the Power Management registers (40h in the PEX 8111).

11.2.2.1 Power States

Table 11-4 delineates the power states supported by the PEX 8111, selectable by way of the **Power Management Control/Status** register *Power State* field.

Table 11-4. Supported Power States (Reverse Bridge)

Power State	Description
D0 uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Space Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0 active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Space Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Configuration transactions are accepted. No Master cycles are allowed, and the INTx# interrupts are disabled. The PMEOUT# signal is asserted by the PEX 8111 and the PCI clock continues to run in this state.
D2	Heavy sleep. Same as D1, except that the PCI host stops the PCI clock.
D3hot	Function context not maintained. Only PCI Configuration transactions are accepted. From this state, the next power state is D3cold or D0 uninitialized. When transitioning from D3hot to D0, the entire chip is reset.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold state to the D0 uninitialized state. At this point software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0 active state.

11.2.3 Reverse Bridge Power Down Sequence

During a link power-down, the following sequence occurs:

1. PCI host places downstream PCI Express device in power state D3.
2. Downstream device initiates a transition to link state L1.
3. PCI host places PEX 8111 in power state D3.
4. PEX 8111 initiates a transition to L0 on the link.
5. PEX 8111 generates a PCI Express PME_Turn_Off message to the PCI Express downstream device.
6. Downstream device responds with a PME_TO_Ack message.
7. Downstream device transmits a DLLP to request transition to L2/L3 Ready state (L2.Idle link state).
8. PEX 8111 acknowledges the request, completing the transition to the L2.Idle link state.
9. PME# signal is asserted to the PCI host.
10. PCI host can now remove power from the PEX 8111.

11.2.4 Reverse Bridge PME# Signal

PME messages from the PCI Express interface are translated to the PCI backplane PME# signal. The **Power Management Control/Status** register *PME Status* bit is set when a PCI Express PME message is received, the WAKEIN# signal is asserted, a beacon is detected, or the link transitions to the L2/L3 Ready state. PME# is asserted when the *PME Status* bit is set and PME is enabled.

11.2.5 Reverse Bridge Set Slot Power

When a PCI Express link first comes up, or the PEX 8111 **Slot Capabilities** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields are changed, the PEX 8111 transmits a Set Slot Power message to the downstream PCI Express device.

When the downstream device receives this message, it updates the **Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

Chapter 12 PCI Express Messages

12.1 Forward Bridge PCI Express Messages

PCI Express defines a set of messages that are used as a method for in-band communication of events (*such as*, interrupts), generally replacing the need for sideband signals. These messages are also used for general-purpose messaging. PCI Express-to-PCI bridge support requirements for these messages are described in the following sections.

PCI Express messages are routed explicitly or implicitly depending on specific bit field encodings in the message request header. An explicitly routed message is routed based on a specific address or on an ID field contained within the message header. The destination of an implicitly routed message is inferred from the message *Type* field.

12.1.1 Forward Bridge INT*x*# Interrupt Signaling

INT*x*# Interrupt Signaling messages are used for in-band communication of the state of the PCI line-based interrupts INTA#, INTB#, INTC#, and INTD# for downstream devices. (Refer to Section 5.1, "Forward Bridge PCI Interrupts," for details.)

12.1.2 Forward Bridge Power Management Messages

Power Management Messages are used to support Power Management Events signaled by sources integrated into the bridge and for downstream devices. (Refer to Section 11.1, "Forward Bridge Power Management," for details.)

12.1.3 Forward Bridge Error Signaling Messages

Error Signaling messages are transmitted by the bridge on its PCI Express primary interface to signal an error for a particular transaction, for the link interface, for errors internal to the bridge, or for PCI-related errors detected on the secondary interface. The message types include ERR_COR, ERR_NONFATAL, and ERR_FATAL. The relevant Mask bits are located in the PCI Express Capability Structure. (Refer to Section 9.1, "Forward Bridge Error Handling," for details.)

12.1.4 Forward Bridge Locked Transactions Support

The PCI Express Unlock Message is used to support Locked Transaction sequences in the downstream direction. (Refer to Section 10.1, "Forward Bridge Exclusive Accesses," for details.)

12.1.5 Forward Bridge Slot Power Limit Support

The Set Slot Power Limit message is transmitted to endpoints, including bridges, by the Root Complex or a Switch. The PEX 8111 supports and complies with these messages. These messages are particularly relevant to bridges implemented on add-in boards. (Refer to Section 11.1, "Forward Bridge Power Management," for details.)

12.1.6 Forward Bridge Hot Plug Signaling Messages

The PEX 8111 does ***not support*** Hot Plug Signaling, and ignores the associated messages.

12.2 Reverse Bridge PCI Express Messages

12.2.1 Reverse Bridge INT*x*# Interrupt Message Support

The PEX 8111 controls the state of the corresponding PCI interrupt pins based on the Assert_INT*x* and Deassert_INT*x* messages received.

12.2.2 Reverse Bridge Power Management Message Support

The PEX 8111 generates a PME_Turn_Off message when placed into power state D3. The PEX 8111 then waits for the PME_TO_Ack message from the downstream device before proceeding with the power-down sequence.

12.2.2.1 PME Handling Requirements

The PEX 8111 translates PME messages from the PCI Express interface to the PCI backplane PME# signal. The PEX 8111 converts the edge triggered PME events on the PCI Express interface to the level triggered PME# signal on PCI. The PEX 8111 signals PME# on the PCI Bus for the following:

- PCI Express WAKEIN# signal is asserted while link remains in L2 state
- PCI Express beacon is received while link remains in L2 state
- PCI Express PM_PME message is received

For compatibility with existing software, the PEX 8111 does not signal PME# unless the PME signaling is enabled by the **Power Management Control/Status** register *PME Enable* bit. The PEX 8111 sets the **Power Management Control/Status** register *PME Status* bit when PME# is signaled and clears PME# when the *PME Status* or *PME Enable* bit is cleared. All PME messages received while the *PME Enable* bit is cleared are ignored and the *PME Status* bit is not set during this time.

12.2.3 Reverse Bridge Error Signaling Message Support

The PEX 8111 converts all ERR_COR, ERR_FATAL, and ERR_NONFATAL messages to SERR# on the PCI interface.

12.2.4 Reverse Bridge Locked Transaction Support

The PEX 8111 is allowed to pass Locked transactions from the primary interface to the secondary interface. The PEX 8111 uses the Memory Read Locked Request to initiate a locked sequence when a locked request is transmitted on the PCI Bus. All subsequent Locked Read transactions targeting the bridge use the Memory Read Locked request on PCI Express. All subsequent Locked Write transactions use the Memory Write request on PCI Express. The PEX 8111 transmits the Unlock Message when PCI Lock sequence is complete.

12.2.5 Reverse Bridge Slot Power Limit Support

The Set Slot Power Limit message is transmitted to endpoints, including bridges, by the Root Complex or a Switch. The PEX 8111 supports and complies with these messages. These messages are particularly relevant to bridges implemented on add-in boards. (Refer to Section 11.2, "Reverse Bridge Power Management," for details.)

Chapter 13 PCI Arbiter

13.1 Overview

A PCI system using the PEX 8111 utilizes an external bus arbiter, or the PEX 8111 internal arbiter. This internal arbiter accepts bus requests from up to four external PCI devices. The PCI Express-to-PCI bridge controller logic also requests control of the PCI Bus.

13.2 Internal Arbiter Mode

When the EXTARB signal is de-asserted, the PEX 8111 accepts and arbitrates PCI requests from up to four external devices. The PEX 8111 supports single and multi-level arbiter modes, selected by the **PCI Control** register *PCI Multi-Level Arbiter* bit.

13.2.1 Single-Level Mode

The four external requests and the PCI Express-to-PCI Bridge Controller request are placed into a single-level arbiter. After a device is granted the bus, it becomes the lowest level requester. All devices retain the same priority. *For example*, when all internal and external agents are requesting the bus, then the order of the agents granted the bus would be:

- PEX 8111 PCI Initiator
- External Requester 0
- External Requester 1
- External Requester 2
- External Requester 3
- Bridge

and so forth.

13.2.2 Multi-Level Mode

The four external requests are placed into a two-level Round Robin arbiter with the PCI Express-to-PCI Bridge Controller. Level 0 alternates between the PCI Express-to-PCI Bridge controller and level 1, guaranteeing that the PCI Express-to-PCI Bridge is granted up to 50% of the accesses. Level 1 consists of the four external PCI requesters.

For example, when all internal and external agents are requesting the bus, then the order of the agents that are granted the bus would be:

- PEX 8111 PCI Initiator
- External Requester 0
- PEX 8111 PCI Initiator
- External Requester 1
- PEX 8111 PCI Initiator
- External Requester 2
- PEX 8111 PCI Initiator
- External Requester 3

and so forth.

13.3 External Arbiter Mode

When the EXTARB signal is asserted, the PEX 8111 PCI request inputs to the internal arbiter are disabled. The PEX 8111 generates a PCI Request (REQ0#) to an external arbiter when it must use the PCI Bus. The PCI Grant input (GNT0#) to the PEX 8111 allows it to become the PCI Bus master.

13.4 Arbitration Parking

The PCI Bus is not allowed to float for more than eight Clock cycles. When there are no requests for the bus, the arbiter selects a device to drive the bus to a known state, by driving its GNT# ball active. When the EXTARB signal is de-asserted (Internal Arbiter mode), the PEX 8111 selects a PCI master to be parked on the bus during idle periods. The **PCI Control** register *PCI Arbiter Park Select* field determines which master is parked on the bus. When parked (GNT# driven during idle bus), the device drives AD[31:0], CBE[3:0]#, and PAR to a known state. The PEX 8111 drives AD[31:0], CBE[3:0]#, and PAR with the previous output value.

In Forward Bridge mode, the PEX 8111 parks on the PCI Bus during reset, independent of the EXTARB signal, and drives AD[31:0], CBE[3:0]#, and PAR low.

Chapter 14 Configuration Registers

14.1 Register Description

The PCI-Compatible Configuration registers are accessed by the PCI Express Root Complex (Forward Bridge mode) or PCI host (Reverse Bridge mode), using the PCI Configuration Address space. All Configuration registers are accessed from the PCI Express or PCI Bus, using the 64-KB memory space defined by **PCI Base Address 0**. Registers that are written by the Serial EEPROM Controller are also written using Memory writes through **PCI Base Address 0**.

In Reverse Bridge mode, a PCI master cannot access PCI Express Extended Capability registers using PCI Configuration transactions.

When the Configuration registers are accessed using Memory transactions to the **PCI Base Address 0** register, the address mapping delineated in Table 14-1 is used.

The Serial EEPROM Controller writes to Configuration registers. An upper Address bit is used to select one of two register spaces, as delineated in Table 14-2.

Each register is 32 bits wide, and is accessed one byte, word, or DWORD at a time. These registers utilize Little Endian byte ordering, which is consistent with the *PCI r3.0*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8111 is powered-up or reset, the registers are set to their default values. Writes to unused registers are ignored, and reads from unused registers return a value of 0.

Table 14-1. PCI Base Address 0 Register Address Mapping

Address Offset	Register Space
0000h - 0FFFh	PCI-Compatible Configuration registers
1000h - 1FFFh	Main Configuration registers
2000h - 2FFFh	Memory-Mapped indirect access to downstream PCI Express Endpoint registers (Reverse Bridge mode only)
8000h - 9FFFh	8-KB internal shared memory

Table 14-2. Selecting Register Space

AD12	Register Space
0	PCI-Compatible Configuration registers
1	Main Configuration registers

14.1.1 Indexed Addressing

In addition to Memory-Mapped accesses, the PEX 8111 **Main Configuration** registers can be accessed using the **Main Control Register Index** and **Main Control Register Data** registers. This method allows all Main Configuration registers to be accessed using Configuration transactions, rather than Memory transactions. First, the Main Configuration register offset is written to the **Main Control Register Index** register (offset 84h). Then, the Main Configuration register is written or read by accessing the **Main Control Register Data** register (offset 88h).

14.2 Configuration Access Types

Table 14-3 delineates configuration access types referenced by the registers in this chapter.

Table 14-3. Configuration Access Types

Access Type	Description
CFG	Initiated by PCI Configuration transactions on the primary bus.
MM	Initiated by PCI Memory transactions on the primary or secondary bus, using the address range defined by **PCI Base Address 0**.
EE	Initiated by the Serial EEPROM Controller during initialization.

14.3 Register Attributes

Table 14-3 delineates the register attributes used to indicate access types provided by each register bit.

Table 14-4. Access Provided by Register Bits

Register Attribute	Description
HwInit	**Hardware Initialized** Register bits are initialized by firmware or hardware mechanisms *such a*s ball strapping (on the BAR0ENB#, FORWARD, and EXTARB balls) or serial EEPROM. Bits are Read-Only after initialization and reset only with "Fundamental Reset."
RO	**Read-Only Register** Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8111 hardware initialization mechanism or PEX 8111 Serial EEPROM register initialization feature.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve value read for writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.
RW	**Read-Write Register** Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	**Read-Only Status** Write 1 to clear status register. Register bits indicate status when read; a set bit indicating a status event is cleared by writing 1. Writing 0 to RW1C bits has no effect.
WO	**Write-Only** Used to indicate that a register is written by the Serial EEPROM Controller.

14.4 Register Summary

Table 14-5. Register Summary

Register Group	PCI Space	Address Range
PCI-Compatible Configuration Registers (Type 1)	PCI Express Configuration (Forward Bridge mode); PCI Configuration (Reverse Bridge mode)	00h - 0FFh
	Memory-Mapped, BAR0	00h - 0FFh
PCI Express Extended Capability Registers	PCI Express Configuration (Forward Bridge mode)	100h - 1FFh
	Memory-Mapped, BAR0	100h - 1FFh
Main Control Registers	Memory-Mapped, BAR0	1000h - 10FFh
PCI Express Configuration Registers Using Enhanced Configuration Access	Memory-Mapped, BAR0	2000h - 2FFFh
8-KB Shared Memory instead of General Purpose Memory	Memory-Mapped, BAR0	8000h - 9FFFh

14.5 Register Mapping

14.5.1 PCI-Compatible Configuration Registers (Type 1)

Table 14-6. PCI-Compatible Configuration Registers (Type 1)

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
00h	PCI Device ID		PCI Vendor ID	
04h	PCI Status		PCI Command	
08h	PCI Class Code			PCI Device Revision ID
0Ch	PCI Built-In Self-Test	PCI Header Type	PCI Bus Latency Timer	PCI Cache Line Size
10h	PCI Base Address 0			
14h	PCI Base Address 1			
18h	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Memory Base Upper 32 Bits			
2Ch	Prefetchable Memory Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	***Reserved***			PCI Capabilities Pointer
38h	PCI Base Address for Expansion ROM (***Not Supported***)			
3Ch	Bridge Control		PCI Interrupt Pin	PCI Interrupt Line

14.5.2 PCI-Compatible Extended Capability Registers for PCI Express Bus

Table 14-7. PCI-Compatible Extended Capability Registers for PCI Express Bus

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
40h	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID
44h	Power Management Data	Power Management Bridge Support	Power Management Control/Status	
48h	Device-Specific Control			
4Ch	***Reserved***			
50h	Message Signaled Interrupts Control		Message Signaled Interrupts Next Capability Pointer	Message Signaled Interrupts Capability ID
54h	Message Signaled Interrupts Address			
58h	Message Signaled Interrupts Upper Address			
5Ch	***Reserved***		Message Signaled Interrupts Data	
60h	PCI Express Capabilities		PCI Express Next Capability Pointer	PCI Express Capability ID
64h	Device Capabilities			
68h	PCI Express Device Status		PCI Express Device Control	
6Ch	Link Capabilities			
70h	Link Status		Link Control	
74h	Slot Capabilities			
78h	Slot Status		Slot Control	
7Ch	***Reserved***		Root Control	
80h	Root Status			
84h	Main Control Register Index			
88h	Main Control Register Data			

14.5.3 PCI Express Extended Capability Registers

Table 14-8. Power Budgeting Capability and Device Serial Number Registers

PCI Express Configuration Register Offset	31 20	19 16	15 8	7 0
100h	Power Budgeting Next Capability Offset	Power Budgeting Capability Version	Power Budgeting PCI Express Extended Capability ID	
104h	***Reserved***			Power Budgeting Data Select
108h	Power Budgeting Data			
10Ch	***Reserved***			Power Budget Capability
110h	Serial Number Next Capability Offset	Serial Number Capability Version	Serial Number PCI Express Extended Capability ID	
114h	Serial Number Low (Lower DW)			
118h	Serial Number Hi (Upper DW)			

14.5.4 Main Control Registers

Table 14-9. 32-Bit Main Control Registers

PCI Express Configuration Register Offset	31 1
1000h	Device Initialization
1004h	Serial EEPROM Control
1008h	Serial EEPROM Clock Frequency
100Ch	PCI Control
1010h	PCI Express Interrupt Request Enable
1014h	PCI Interrupt Request Enable
1018h	Interrupt Request Status
101Ch	Power
1020h	General-Purpose I/O Control
1024h	General-Purpose I/O Status
1030h	Mailbox 0
1034h	Mailbox 1
1038h	Mailbox 2
103Ch	Mailbox 3
1040h	Chip Silicon Revision
1044h	Diagnostic Control (Factory Test Only)
1048h	TLP Controller Configuration 0
104Ch	TLP Controller Configuration 1
1050h	TLP Controller Configuration 2
1054h	TLP Controller Tag
1058h	TLP Controller Time Limit 0
105Ch	TLP Controller Time Limit 1
1060h	CRS Timer
1064h	Enhanced Configuration Address

14.6 PCI-Compatible Configuration Registers (Type 1)

Register 14-1. (Offset 00h; PCIVENDID) PCI Vendor ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID** Identifies device manufacturer. The PEX 8111 returns the PLX PCI SIG-assigned Vendor ID, 10B5h.	RO	RW	WO	10B5h

Register 14-2. (Offset 02h; PCIDEVID) PCI Device ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Device ID** Identifies particular device, as specified by the Vendor. The PEX 8111 returns the PLX-assigned Device ID, 8111h.	RO	RW	WO	8111h

Register 14-3. (Offset 04h; PCICMD) PCI Command (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Space Enable** Enables the PEX 8111 to respond to I/O Space accesses on the primary interface (PCI Express). These accesses must be directed to a target on the PCI Bus, because the PEX 8111 does not maintain internal I/O-mapped resources.	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8111 to respond to Memory Space accesses on the primary interface (PCI Express). These accesses are directed to a target on the PCI Bus, or to internal Memory-Mapped registers. When this bit is cleared, responds to all Memory Requests on the primary interface with an Unsupported Request completion.	RW	RW	WO	0
2	**Bus Master Enable** Enables the PEX 8111 to issue memory and I/O read/write requests on the primary interface (PCI Express). Requests other than Memory or I/O Requests are not controlled by this bit. When this bit is cleared, the bridge must disable response as a target to all Memory or I/O transactions on the PCI Bus secondary interface (they cannot be forwarded to the primary interface).	RW	RW	WO	0
3	**Special Cycle Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** When set, enables the PEX 8111 PCI Bus master logic to use the Memory Write and Invalidate command. When clear, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	**Parity Error Response Enable** Controls the response to Data Parity errors forwarded from the primary interface (*such as*, a poisoned TLP). When clear, the bridge must ignore (but records status *such as* setting the **PCI Status** register *Detected Parity Error* bit) Data Parity errors detected and continue normal operation. When set, the bridge must take its normal action when a Data Parity error is detected.	RW	RW	WO	0
7	**Address Stepping Enable** The PEX 8111 performs Address Stepping for PCI Configuration cycles; therefore this bit is read/write with an initial value of 1.	RW	RW	WO	1

Register 14-3. (Offset 04h; PCICMD) PCI Command (Forward Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**SERR# Enable** Enables reporting of Non-Fatal and Fatal errors to the Root Complex. ***Note:*** *Errors are reported when enabled through this bit or through the **PCI Express Device Control**, PCI Express-specific bits.*	RW	RW	WO	0
9	**Fast Back-to-Back Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** When set: • PEX 8111 is prevented from generating INT*x*# interrupt messages on behalf of functions integrated into the bridge • INT*x*# emulation interrupts previously asserted must be de-asserted There is no effect on INT*x*# messages generated on behalf of INT*x*# inputs associated with the PCI Bus secondary interface.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-4. (Offset 04h; PCICMD) PCI Command (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Space Enable** Enables the PEX 8111 to respond to I/O space accesses on the primary interface (PCI). These accesses are directed to a target on the PCI Express Bus, because the PEX 8111 does not maintain internal I/O-mapped devices. When this bit is cleared, PCI I/O accesses to the PEX 8111 result in a Master Abort.	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8111 to respond to Memory space accesses on the primary interface (PCI). These accesses are directed to a target on the PCI Express Bus, or to internal Memory-Mapped registers. When this bit is cleared, PCI Memory accesses to the PEX 8111 result in a Master Abort.	RW	RW	WO	0
2	**Bus Master Enable** When set, enables the PEX 8111 to perform Memory or I/O transactions on the PCI Bus. Configuration transactions are forwarded from the PCI Express Bus and performed on the PCI Bus, independent of this bit. When clear, the bridge must disable response as a target to all Memory or I/O transactions on the PCI Express Bus secondary interface (they cannot be forwarded to the primary interface). In this case, all Memory and I/O requests are terminated with an Unsupported Request completion.	RW	RW	WO	0
3	**Special Cycle Enable** A bridge does not respond to special cycle transactions; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** When set, enables the PEX 8111 PCI Bus master logic to use the Memory Write and Invalidate command. When clear, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop** When set, I/O writes in the first 64 KB of the I/O Address space with Address bits [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA aliases – AD[15:10] are not decoded and are of any value) must be positively decoded on the PCI interface and forwarded to the PCI Express Bus secondary interface.	RW	RW	WO	0
6	**Parity Error Response Enable** Enables PCI Parity checking.	RW	RW	WO	0
7	***Reserved***	RsvdP	RsvdP	–	0
8	**SERR# Enable** When asserted, enables the SERR# signal to assert.	RW	RW	WO	0
9	**Fast Back-to-Back Enable** The PEX 8111 PCI master interface does not perform Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** When set, the PEX 8111 is prevented from asserting INT*x*# signals on behalf of functions integrated into the bridge. There is no effect on INT*x*# signals asserted on behalf of INT*x*# messages associated with the PCI Express Bus secondary interface.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-5. (Offset 06h; PCISTAT) PCI Status (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** When set, indicates that an INT*x*# interrupt message is pending on behalf of functions integrated into the bridge. Does not reflect the status of INT*x*# inputs associated with the secondary interface.	RO	RO	–	0
4	**Capabilities List** Indicates when the **PCI Capabilities Pointer** at offset 34h is valid. Because all PCI Express devices are required to implement the PCI Express capability structure, this bit is hardwired to 1.	RO	RO	–	1
5	**66 MHz Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Used to report data parity error detection by the bridge. Set when the **PCI Command** register *Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked poisoned on primary interface • Bridge poisons a write request or read completion on primary interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	00b
11	**Signaled Target Abort** Set when the bridge completes a request as a transaction target on its primary interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on its primary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on its primary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the **PCI Command** register *SERR# Enable* bit is set. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the primary interface, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 14-6. (Offset 06h; PCISTAT) PCI Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** Reflects the PEX 8111 internal PCI interrupt status state. One of the INT*x*# signals is asserted when this bit is high, the **PCI Command** register *Interrupt Disable* bit is low, and the Power State is D0.	RO	RO	–	0
4	**Capabilities List** Indicates when the **PCI Capabilities Pointer** at offset 34h is valid.	RO	RO	–	1
5	**66 MHz Capable** Indicates whether the PEX 8111 is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the PEX 8111 is 66-MHz capable.	RO	RW	WO	1
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** The PEX 8111 does not accept Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Indicates that a data parity error occurred when this device was the PCI Bus master. The **PCI Command** register *Parity Error Response Enable* bit must be set for this bit to be set. Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Determines how quickly this device responds to a transaction with DEVSEL#. A value of 01b indicates a medium response.	RO	RO	–	01b
11	**Signaled Target Abort** Set when the device is acting as a PCI Bus target, and terminates its transaction with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction, which never occurs in the PEX 8111; therefore, a 0 is always returned.	RsvdZ	RsvdZ	–	0
12	**Received Target Abort** Set when the device is acting as a PCI Bus master, and its transaction terminated with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction. De-asserts DEVSEL# and asserts STOP# to signal the Target Abort. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the device is acting as a PCI Bus master, and its transaction terminated with a Master Abort. A Master Abort occurs when no target responds with a DEVSEL#. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the device asserts the SERR# signal. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set when the device detects a parity error on incoming addresses or data from the PCI Bus, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 14-7. (Offset 08h; PCIDEVREV) PCI Device Revision ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Device Revision ID** Identifies the device Silicon Revision. Bits [3:0] represent the minor revision number and bits [7:4] represent the major revision number.	RO	RO	–	21h

Register 14-8. (Offset 09h; PCICLASS) PCI Class Code

Bits	Description	CFG	MM	EE	Default
7:0	**Programming Interface**	RO	RW	WO	00h
15:8	**Sub Class Code**	RO	RW	WO	04h
23:16	**Base Class Code**	RO	RW	WO	06h

Register 14-9. (Offset 0Ch; PCICACHESIZE) PCI Cache Line Size

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size** Specifies the system Cache Line Size in DWORD units. The value in this register is used by PCI master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands for accessing memory. Supports Cache Line Sizes of 2, 4, 8, 16, or 32 DWORDs. Writes of values other than these result in a Cache Line Size of 0; however, the value written is nonetheless returned when this register is read.	RW	RW	WO	0h

Register 14-10. (Offset 0Dh; PCILATENCY) PCI Bus Latency Timer (Reverse Bridge Mode Only)

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Bus Latency Timer** Also referred to as *Primary Latency Timer* for Type 1 Configuration Space Header devices. The Primary/Master Latency Timer does not apply to PCI Express (Forward Bridge mode). In Reverse Bridge mode, this field specifies, in PCI Clock units, the value of the Latency Timer during Bus Master bursts. When the Latency Timer expires, the device must terminate its tenure on the bus.	RO (F) RW (R)	RO (F) RW (R)	– (F) WO (R)	0h

Register 14-11. (Offset 0Eh; PCIHEADER) PCI Header Type

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Header Type** Specifies the format of the second part of the pre-defined configuration header starting at offset 10h. For PCI Bridges, this field is forced to 1h.	RO	RO	–	1h

Register 14-12. (Offset 0Fh; PCIBIST) PCI Built-In Self-Test

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self-Test** ***Not supported***. Always returns a value of 0h.	RO	RO	–	0h

Register 14-13. (Offset 10h; PCIBASE0) PCI Base Address 0

Bits	Description	CFG	MM	EE	Default
0	**Space Type** When low, this space is accessed as memory. When high, this space is accessed as I/O. ***Note:*** *Hardwired to 0.*	RO	RO	–	0
2:1	**Address Type** Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space (default) 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = ***Reserved***	RO	RW	WO	10b
3	**Prefetch Enable** When set, indicates that prefetching has no side effects on reads.	RO	RW	WO	1
15:4	**Base Address** This section of the Base address is ignored for a 64-KB space. ***Note:*** *Hardwired to 0.*	RO	RO	–	0h
31:16	**Base Address** Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the PEX 8111 Configuration registers and shared memory.	RW	RW	WO	0h

Register 14-14. (Offset 14h; PCIBASE1) PCI Base Address 1

Bits	Description	CFG	MM	EE	Default
31:0	**Base Address 1** When **PCI Base Address 0** is configured for 64-bit addressing, this register determines the upper 32 bits of the address.	RW	RW	WO	0h

Register 14-15. (Offset 18h; PRIMBUSNUM) Primary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the primary interface of the bridge is connected.	RW	RW	WO	0h

Register 14-16. (Offset 19h; SECBUSNUM) Secondary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the bridge secondary interface is connected.	RW	RW	WO	0h

Register 14-17. (Offset 1Ah; SUBBUSNUM) Subordinate Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number** Used to record the Bus Number of the highest numbered PCI Bus segment which is behind (or subordinate to) the bridge.	RW	RW	WO	0h

Register 14-18. (Offset 1Bh; SECLATTIMER) Secondary Latency Timer (Forward Bridge Mode Only)

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Latency Timer** Valid only in Forward Bridge mode. Specifies, in PCI clock units, the value of the Latency Timer during secondary (PCI) bus master bursts. When the Latency Timer expires, the device must terminate its tenure on the bus.	RW	RW	WO	0h

Register 14-19. (Offset 1Ch; IOBASE) I/O Base

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values = ***Reserved***	RO	RW	WO	0000b
7:4	**I/O Base** Determines the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are zero (0h). Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB boundary, and the top is one less than a 4-KB boundary.	RW	RW	WO	0h

Register 14-20. (Offset 1Dh; IOLIMIT) I/O Limit

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values = ***Reserved*** The value returned in this field is derived from the **I/O Base** register *I/O Base Address Capability* field.	RO	RO	–	0000b
7:4	**I/O Limit** Determines the I/O Space range forwarded from the primary interface to the secondary interface. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary side of the bridge, the *I/O Limit* field is programmed to a value smaller than the **I/O Base** register *I/O Base* field. In this case, the bridge does not forward I/O transactions from the primary bus to the secondary bus; however, the bridge does forward all I/O transactions from the secondary bus to the primary bus.	RW	RW	WO	0h

Register 14-21. (Offset 1Eh; SECSTAT) Secondary Status (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable** Indicates whether the bridge secondary interface is capable of operating at 66 MHz.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Indicates whether the bridge secondary interface is capable of decoding Fast Back-to-Back transactions when the transactions are from the same master but to different targets. (A bridge is required to support fast back-to-back transactions from the same master.) The PEX 8111 does not support fast back-to-back decoding.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Reports data parity error detection by the bridge when it is the master of the transaction on the secondary interface. Set when the following three conditions are true: • Bridge is the bus master of the transaction on secondary interface • Bridge asserted PERR# (Read transaction) or detected PERR# asserted (Write transaction) • **Bridge Control** register *Secondary Parity Error Response Enable* bit is set Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Encodes the timing of the secondary interface DEVSEL#. The encoding must indicate the slowest response time that the bridge uses to assert DEVSEL# on its secondary interface when responding as a target to a transaction other than a Configuration Read or Configuration Write. Hardwired to a value of 01b, indicating medium DEVSEL# timing.	RO	RO	–	01b
11	**Secondary Signaled Target Abort** Reports Target Abort termination signaling by the bridge when it responds as the transaction target on its secondary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Reports Target Abort termination detection by the bridge when it is the master of a transaction on its secondary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Reports Master Abort termination detection by the bridge when it is the master of a transaction on its secondary interface. Also set for a PCI Express-to-PCI Configuration transaction with an extended address not equal to 0. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Reports the SERR# assertion direction on the bridge secondary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Reports Address or Data Parity error detection by the bridge on its secondary interface. Set when any of the following three conditions are true: • Bridge detects an Address Parity error as a potential target • Bridge detects a Data Parity error when a Write transaction target • Bridge detects a Data Parity error when Read transaction master Set irrespective of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 14-22. (Offset 1Eh; SECSTAT) Secondary Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable** Indicates whether the bridge secondary interface is capable of operating at 66 MHz. Not valid for PCI Express and is forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Indicates whether the bridge secondary interface is capable of decoding Fast Back-to-Back transactions when the transactions are from the same master but to different targets. Not valid for PCI Express and is forced to 0.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Used to report Data Parity error detection by the bridge. Set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked poisoned on the secondary interface • Bridge poisons a Write Request or Read Completion on the secondary interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Encodes the secondary interface DEVSEL# timing. Not valid for PCI Express and is forced to 00b.	RO	RO	–	00b
11	**Secondary Signaled Target Abort** Set when the bridge completes a request as a transaction target on its secondary interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on its secondary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on its secondary interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Set when the PEX 8111 receives an ERR_FATAL or ERR_NONFATAL message from the downstream PCI Express device. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the secondary interface, regardless of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 14-23. (Offset 20h; MEMBASE) Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Base** Determines the starting address at which Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are zero (0h). The bottom of the defined memory address range is aligned to a 1-MB boundary, and the top is one less than a 1-MB boundary.	RW	RW	WO	–

Register 14-24. (Offset 22h; MEMLIMIT) Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Limit** Determines the Memory Space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are FFFFFh. When there are no Memory-Mapped I/O addresses on the secondary side of the bridge, the *Memory Limit* field must be programmed to a value smaller than the **Memory Base** register *Memory Base* field. When there is no Prefetchable Memory, and no Memory-Mapped I/O on the secondary side of the bridge, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 14-25. (Offset 24h; PREBASE) Prefetchable Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values = ***Reserved***	RO	RW	WO	0000b
15:4	**Prefetchable Memory Base** Determines the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are zero (0h). The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB boundary, and the top is one less than a 1-MB boundary.	RW	RW	WO	–

Register 14-26. (Offset 26h; PRELIMIT) Prefetchable Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values = ***Reserved*** The value returned in this field is derived from the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field.	RO	RO	–	0000b
15:4	**Prefetchable Memory Limit** Determines the Prefetchable Memory space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are FFFFFh. When there is no prefetchable memory on the secondary side of the bridge, the *Prefetchable Memory Limit* field must be programmed to a value smaller than the **Prefetchable Memory Base** register *Prefetchable Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the bridge, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 14-27. (Offset 28h; PREBASEUPPER) Prefetchable Memory Base Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits** When the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	0h

Register 14-28. (Offset 2Ch; PRELIMITUPPER) Prefetchable Memory Limit Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits** When the **Prefetchable Memory Limit** register *Prefetchable Limit Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Limit Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the Prefetchable Memory range forwarded from the primary interface to the secondary interface.	RW	RW	WO	0h

Register 14-29. (Offset 30h; IOBASEUPPER) I/O Base Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits** When the **I/O Base** register *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface.	RW	RW	WO	–

Register 14-30. (Offset 32h; IOLIMITUPPER) I/O Limit Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits** When the **I/O Limit** register *I/O Limit Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Limit Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the I/O range forwarded from the primary interface to the secondary interface.	RW	RW	WO	–

Register 14-31. (Offset 34h; PCICAPPTR) PCI Capabilities Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Capabilities Pointer** Provides the configuration address of the first New Capabilities register.	RO	RW	WO	40h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-32. (Offset 3Ch; PCIINTLINE) PCI Interrupt Line

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Line** Indicates to which system interrupt controller input the device Interrupt pin is connected. Device drivers and operating systems use this field.	RW	RW	WO	0h

Register 14-33. (Offset 3Dh; PCIINTPIN) PCI Interrupt Pin

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Pin** For Forward Bridge mode, this register identifies the legacy interrupt message(s) that the device uses. Valid values are 1, 2, 3, and 4, which map to legacy interrupt messages for INTA#, INTB#, INTC#, and INTD#. A value of 0 indicates that the device uses no legacy interrupt message(s). For Reverse Bridge mode, this register selects which Interrupt pin the device uses.	RO	RW	WO	1h

Register 14-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the bridge response to Address and Data Parity errors on the PCI Bus secondary interface. When cleared, the bridge must ignore Parity errors detected and continue normal operation. A bridge must generate parity although the Parity error reporting is disabled. Also, the bridge must always forward Posted Write data with poisoning, from PCI-to-PCI Express on a PCI Data Parity error, regardless of this bit's setting. When set, the bridge must take its normal action when a Parity error is detected.	RW	RW	WO	0
1	**Secondary SERR# Enable** Controls the forwarding of PCI Bus secondary interface SERR# assertions to the primary interface (PCI Express). The bridge transmits an ERR_FATAL message on the primary interface when all of the following are true: • SERR# is asserted on the secondary interface • Bit is set • **PCI Command** register *SERR# Enable* bit is set or **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bits are set	RW	RW	WO	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. When set, the bridge blocks forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies bridge response to VGA-compatible addresses. When set, the bridge positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A0000h to 000BFFFFh • I/O address in the first 64 KB of the I/O Address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] remains in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] possesses any value and is not used in decoding) When the *VGA Enable* bit is set, VGA address forwarding is independent of the *ISA Enable* bit value, and the I/O Address range and Memory Address ranges defined by the **I/O Base** and **I/O Limit**, **Memory Base** and **Memory Limit**, and **Prefetchable Memory Base** and **Prefetchable Memory Limit** registers. VGA address forwarding is qualified by the **PCI Command** register *I/O Space Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Space Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 14-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. Retains meaning only when bit 3 (*VGA Enable*) of this register is also set to 1, enabling VGA I/O decoding and bridge forwarding. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the PCI bus or an Unsupported Request on PCI Express. • 0 = Do not report Master Aborts If PCI Express UR is received: – Return FFFFFFFFh to PCI Bus for reads – Complete Non-Posted write normally on PCI Bus (assert TRDY#) and – Discard the Write data – Discard Posted PCI-to-PCI Express Write data If PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-PCI • 1 = Report Master Aborts If PCI Express UR is received: – Complete reads and Non-Posted writes with PCI Target Abort – Discard Posted PCI-to-PCI Express Write data If PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-PCI – Transmit ERR_NONFATAL message for Posted writes	RW	RW	WO	0
6	**Secondary Bus Reset** When set, forces RST# assertion on the secondary bus. Additionally, the bridge secondary bus interface and buffers between the two interfaces (primary and secondary) must be initialized to their default state. The primary bus interface and all Configuration Space registers must not be affected by setting this bit. Because RST# is asserted when this bit is set, software must observe proper PCI reset timing requirements.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported***. Controls bridge ability to generate Fast Back-to-Back transactions to various secondary interface devices.	RO	RO	–	0

Register 14-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Forward Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** In Forward Bridge mode, this bit does not apply and is forced to 0.	RO	RO	–	0
9	**Secondary Discard Timer** Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a Delayed Transaction request. The counter starts after completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the downstream queue of the bridge (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed transaction with the originating master on the secondary bus). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed transaction from its queue and sets the *Discard Timer Status* bit. 0 = Secondary Discard Timer counts 2^{15} PCI clock periods 1 = Secondary Discard Timer counts 2^{10} PCI clock periods	RW	RW	WO	0
10	**Discard Timer Status** Set to 1 when the *Secondary Discard Timer* expires and a Delayed Completion is discarded from a queue in the bridge. Writing 1 clears this bit.	RW1C	RW1C	WO	0
11	**Discard Timer SERR# Enable** When set to 1, enables the bridge to generate an ERR_NONFATAL Message on the primary interface when the *Secondary Discard Timer* expires and a Delayed transaction is discarded from a queue in the bridge. 0 = Do not generate ERR_NONFATAL message on the primary interface as a result of the expiration of the *Secondary Discard Timer* 1 = Generate ERR_NONFATAL message on the primary interface when the *Secondary Discard Timer* expires and a Delayed transaction is discarded from a queue in the bridge	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls bridge response to data parity errors forwarded from the primary interface (*such as*, a poisoned TLP). When clear, the bridge must ignore data parity errors detected and continue normal operation. When set, the bridge must take its normal action when a data parity error is detected.	RW	RW	WO	0
1	**Secondary SERR# Enable** No effect in Reverse Bridge mode. Secondary bus error reporting using SERR# is controlled by the **Root Control** register.	RW	RW	WO	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. When set, the bridge blocks forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies bridge response to VGA-compatible addresses. When this bit is set, the bridge positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A0000h to 000BFFFFh • I/O address in the first 64 KB of the I/O Address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] remains in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] possesses any value and is not used in decoding) When the *VGA Enable* bit is set, VGA address forwarding is independent of the *ISA Enable* bit value, and the I/O Address range and Memory Address ranges defined by the **I/O Base** and **I/O Limit**, **Memory Base** and **Memory Limit**, and **Prefetchable Memory Base** and **Prefetchable Memory Limit** registers. VGA address forwarding is qualified by the **PCI Command** register *I/O Space Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Space Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 14-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. Retains meaning only when bit 3 (*VGA Enable)* of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the PCI Bus or an Unsupported Request on PCI Express. • 0 = Do not report Master Aborts If PCI Express UR is received: – Return FFFFFFFFh to PCI bus for reads – Complete non-posted write normally on PCI Bus (assert TRDY#) and discard the Write data – Discard posted PCI-to-PCI Express Write data If PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-PCI • 1 = Report Master Aborts If PCI Express UR is received: – Complete reads and Non-Posted writes with PCI Target Abort – Discard Posted PCI-to-PCI Express Write data If PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-PCI – Transmit ERR_NONFATAL message for Posted writes	RW	RW	WO	0
6	**Secondary Bus Reset** When set, causes a Hot Reset to be communicated on the secondary bus. Additionally, the bridge secondary bus interface and buffers between the two interfaces (primary and secondary) must be initialized to their default state. The primary bus interface and all Configuration Space registers are not affected by setting this bit.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported***. Controls bridge ability to generate Fast Back-to-Back transactions to different devices on the secondary interface.	RO	RO	–	0

Register 14-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Reverse Bridge Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** Selects the number of PCI clocks that the bridge waits for a master on the primary interface to repeat a Delayed Transaction request. The counter starts after the completion (PCI Express Completion associated with the Delayed Transaction request) reached the head of the downstream queue of the bridge (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed transaction with the originating master on the secondary bus). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed transaction from its queue and sets the *Discard Timer Status* bit. 0 = Secondary Discard Timer counts 2^{15} PCI clock periods 1 = Secondary Discard Timer counts 2^{10} PCI clock periods	RW	RW	WO	0
9	**Secondary Discard Timer** In Reverse Bridge mode, this bit does not apply and is forced to 0.	RO	RO	–	0
10	**Discard Timer Status** Set to 1 when the *Primary Discard Timer* expires and a Delayed Completion is discarded from a queue in the bridge.	RW1C	RW1C	–	0
11	**Discard Timer SERR# Enable** When set to 1, enables the bridge to assert SERR# on the primary interface when the *Primary Discard Timer* expires and a Delayed transaction is discarded from a queue in the bridge. 0 = Do not assert SERR# on the primary interface as a result of the *Primary Discard Timer* expiration 1 = Generate SERR# on the primary interface when the *Primary Discard Timer* expires and a Delayed transaction is discarded from a queue in the bridge	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	–	0h

14.7 PCI-Compatible Extended Capability Registers for PCI Express Bus

Register 14-36. (Offset 40h; PWRMNGID) Power Management Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID** Specifies the Power Management Capability ID.	RO	RO	–	1h

Register 14-37. (Offset 41h; PWRMNGNEXT) Power Management Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, Message Signaled Interrupts.	RO	RW	WO	50h

Register 14-38. (Offset 42h; PWRMNGCAP) Power Management Capabilities (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version** Specifies the revision of the *PCI Power Mgmt. r1.1* to which this device complies.	RO	RW	WO	2h
3	**PME Clock** For Forward Bridge mode, does not apply to PCI Express; therefore, must always retain a value of 0.	RO	RO	–	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the device requires special initialization following a transition to the D0 uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PCI backplane PME# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the device supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the device supports the D2 state.	RO	RW	WO	0
15:11	**PME Support** Indicates the power states in which the device transmits a PME message. **Value** **Description** XXXX1b Asserted from D0 XXX1Xb Asserted from D1 XX1XXb Asserted from D2 X1XXXb Asserted from D3hot 1XXXXb Asserted from D3cold	RO	RW	WO	0Bh (D0, D1, D3hot)

Register 14-39. (Offset 42h; PWRMNGCAP) Power Management Capabilities (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version** Specifies the *PCI Power Mgmt. r1.1* revision to which this device complies.	RO	RW	WO	2h
3	**PME Clock** When low, indicates that no PCI clock is required to generate PME#. When high, indicates that a PCI clock is required to generate PME#.	RO	RW	WO	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the device requires special initialization following a transition to the D0 uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PME# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the device supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the device supports the D2 state.	RO	RW	WO	0
15:11	**PME Support** Indicates the power states in which the device transmits a PME message. **Value** **Description** XXXX1b Asserted from D0 XXX1Xb Asserted from D1 XX1XXb Asserted from D2 X1XXXb Asserted from D3hot 1XXXXb Asserted from D3cold	RO	RW	WO	0Bh (D0, D1, D3hot)

Register 14-40. (Offset 44h; PWRMNGCSR) Power Management Control/Status (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. **Value** **State** 00b D0 01b D1 10b D2 11b D3hot A transition from state D3 to state D0 causes a soft reset to occur. In states D1 and D2, when the corresponding *D1 Support* and *D2 Support* bits are set, PCI memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables a PME message to transmit upstream.	RW	RW	WO	0
12:9	**Data Select** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported.*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** Indicates that a PME message was transmitted upstream. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 14-41. (Offset 44h; PWRMNGCSR) Power Management Control/Status (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. **Value** **State** 00b D0 01b D1 10b D2 11b D3hot A transition from state D3 to state D0 causes a soft reset to occur. In states D1 and D2, when the corresponding *D1 Support* and *D2 Support* bits are set, PCI memory and I/O accesses are disabled, as well as the PCI interrupt; however, Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables the PMEOUT# signal to assert.	RW	RW	WO	0
12:9	**Data Select** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported.*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** When the *PME Enable* bit is set high, indicates that PMEOUT# is being driven. Writing 1 from the PCI Bus clears this bit.	RW1C	RW1C	–	0

Register 14-42. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support (Forward Bridge Mode)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** ***Not supported*** in Forward Bridge mode; therefore, bit is forced to 0. When clear, indicates that, when the bridge function is programmed to D3hot, its secondary bus has its power removed (B3). Retains meaning only when bit 7 is set. When set, indicates that, when the bridge function is programmed to D3hot, its secondary bus PCI clock is stopped (B2).	RO	RO	–	0
7	**Bus Power/Clock Control Enable** ***Not supported*** in Forward Bridge mode; therefore, bit is forced to 0. When set, indicates that the bus power/clock control mechanism (as defined in the *PCI-to-PCI Bridge r1.1*, Section 4.7.1) is enabled.	RO	RO	–	0

Register 14-43. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support (Reverse Bridge Mode)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** When clear, indicates that, when the bridge function is programmed to D3hot, its secondary bus has its power removed (B3). Retains meaning only when bit 7 is set. When set, indicates that, when the bridge function is programmed to D3hot, its secondary bus PCI clock is stopped (B2).	RO	RW	WO	0
7	**Bus Power/Clock Control Enable** When set, indicates that the bus power/clock control mechanism (as defined in the *PCI-to-PCI Bridge r1.1*, Section 4.7.1) is enabled.	RO	RW	WO	0

Register 14-44. (Offset 47h; PWRMNGDATA) Power Management Data

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Data** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h

Register 14-45. (Offset 48h; DEVSPECCTL) Device-Specific Control

Bits	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable** When clear, a Memory Read command on the PCI Bus that targets the PCI Express memory space causes only 1 word to be read from PCI Express Bus. When set, a Memory Read command on the PCI Bus that targets the PCI Express Memory space causes a cache line to be read from PCI Express Bus.	RW	RW	WO	0
1	**PCI Base Address 0 Enable** When set, enables the **PCI Base Address 0** space for Memory-Mapped access to the Configuration registers and shared memory. **PCI Base Address 0** is also enabled when the BAR0ENB# ball is low.	RW	RW	WO	0
2	**L2 Enable** Valid only for Reverse Bridge mode. When clear, a power state change to D3 does not cause the PEX 8111 to change the link state to L2. When set, a power state change to D3 causes the PEX 8111 to change the link state to L2.	RW	RW	WO	0
3	**PMU Power Off** When set, the link transitioned to the L2/L3 Ready state, and is ready to power-down.	RO	RO	–	0
7:4	**PMU Link State** Indicates the link state, as follows. **Value** **State** 0001b L0 0010b L0s 0100b L1 1000b L2	RO	RO	–	–
9:8	**CRS Retry Control** Determines the response of the PEX 8111 in Reverse Bridge Mode when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry Status. **Value** **Response** 00b Retry one time after one second. When another CRS is received, Target Abort on the PCI Bus. 01b Retry eight times, one time per second. When another CRS is received, Target Abort on the PCI Bus. 10b Retry one time per second until successful completion. 11b ***Reserved***	RW	RW	WO	00b
10	**WAKE Out Enable** Valid only in Forward Bridge mode. When set, the WAKEOUT# signal is asserted when PMEIN# is asserted and the link remains in the L2 state.	RW	RW	WO	0
11	**Beacon Generate Enable** Valid only in Forward Bridge mode. When set, a beacon is generated when PMEIN# is asserted and the link remains in the L2 state.	RW	RW	WO	0

Register 14-45. (Offset 48h; DEVSPECCTL) Device-Specific Control *(Cont.)*

Bits	Description	CFG	MM	EE	Default
12	**Beacon Detect Enable** Valid only in Reverse Bridge mode. When set, a beacon detected while the link remains in the L2 state causes the **Power Management Control/Status** register *PME Status* bit to be set.	RW	RW	WO	0
13	**PLL Locked** High when internal PLL is locked.	RO	RO	–	–
15:14	***Reserved***	RsvdP	RsvdP	–	00b
20:16	**Link Training and Status State Machine** ***For internal use only.***	RO	RO	–	–
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-46. (Offset 50h; MSIID) Message Signaled Interrupts Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID** Specifies the Message Signaled Interrupts Capability ID.	RO	RO	–	5h

Register 14-47. (Offset 51h; MSINEXT) Message Signaled Interrupts Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, PCI Express Capability.	RO	RW	WO	60h

Register 14-48. (Offset 52h; MSICTL) Message Signaled Interrupts Control

Bits	Description	CFG	MM	EE	Default
0	**MSI Enable** When set: • Enables the PEX 8111 to use MSI to request service • Virtual interrupt support for internal interrupt sources are disabled for Forward Bridge mode • INT*x*# outputs are disabled in Reverse Bridge mode	RW	RW	WO	0
3:1	**Multiple Message Capable** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four). The encoding is defined as: **Value** **Number of Messages Requested** 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b, 111b ***Reserved***	RO	RO	–	000b
6:4	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. The encoding is defined as: **Value** **Number of Messages Requested** 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b, 111b ***Reserved***	RW	RW	WO	000b
7	**MSI 64-Bit Address Capable** When set, the PEX 8111 is capable of generating a 64-bit message address.	RO	RW	WO	1 (Fwd) 0 (Rev)
8	**Per Vector Masking Capable** ***Not supported.*** Forced to 0.	RO	RO	–	0
15:9	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-49. (Offset 54h; MSIADDR) Message Signaled Interrupts Address

Bits	Description	CFG	MM	EE	Default
1:0	***Reserved***	RsvdP	RsvdP	–	00b
31:2	**MSI Address** When the **Message Signaled Interrupts Control** register *MSI Enable* bit is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits 1 and 0 are driven to zero (00b) during the Address phase.	RW	RW	WO	0h

Register 14-50. (Offset 58h; MSIUPPERADDR) Message Signaled Interrupts Upper Address

Bits	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address** Optionally implemented only when the device supports a 64-bit message address when the **Message Signaled Interrupts Control** register *MSI 64-Bit Address Capable* bit is set. When the **Message Signaled Interrupts Control** register *MSI Enable* bit is set, the register contents specify a 64-bit message address upper 32 bits. When the register contents are zero (0h), the PEX 8111 uses the 32-bit address specified by the **Message Signaled Interrupts Address** register.	RW	RW	WO	0h

Register 14-51. (Offset 5Ch; MSIDATA) Message Signaled Interrupts Data

Bits	Description	CFG	MM	EE	Default
15:0	**MSI Data** When the **Message Signaled Interrupts Control** register *MSI Enable* bit is set, the Message data is driven onto the lower word (AD[15:0]) of the Memory Write Transaction Data phase.	RW	RW	WO	0h
31:16	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-52. (Offset 60h; PCIEXID) PCI Express Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID** Specifies the PCI Express Capability ID.	RO	RW	–	10h

Register 14-53. (Offset 61h; PCIEXNEXT) PCI Express Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List.	RO	RW	WO	0h

Register 14-54. (Offset 62h; PCIEXCAP) PCI Express Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Capability Version** Indicates the PCI Express capability structure version number.	RO	RW	WO	1h
7:4	**Device/Port Type** Indicates the type of PCI Express logical device. Device encodings are as follows: **Value** – **Device/Port Type** 0000b – PCI Express Endpoint Device 0001b – Legacy PCI Express Endpoint Device 0100b – Root Port of PCI Express Root Complex 0101b – Upstream Port of PCI Express Switch 0110b – Downstream Port of PCI Express Switch 0111b – PCI Express-to-PCI/PCI-X Bridge 1000b – PCI/PCI-X-to-PCI Express Bridge All other values – ***Reserved***	RO	RW	WO	0111b (Forward Bridge) 1000b (Reverse Bridge)
8	**Slot Implemented** When set, indicates that the PCI Express Link associated with this port is connected to a slot.	RO	RW	WO	0
13:9	**Interrupt Message Number** When this function is allocated more than one MSI interrupt number, this field must contain the offset between the Base Message data and the MSI message generated when status bits in the **Slot Status** or **Root Status** register of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the device changes.	RO	RO	–	0h
15:14	***Reserved***	RsvdP	RsvdP	–	00b

Register 14-55. (Offset 64h; DEVCAP) Device Capabilities

Bits	Description	CFG	MM	EE	Default
2:0	**Maximum Payload Size Supported** Indicates the maximum payload size that the device supports for TLPs. Defined encodings are as follows: **Value** — **Maximum Payload Size** 000b — 128 bytes 001b — 256 bytes 010b — 512 bytes 011b — 1,024 bytes 100b — 2,048 bytes 101b — 4,096 bytes 110b, 111b — ***Reserved*** ***Note:*** *Because the PEX 8111 only supports a Maximum Payload Size of 128 bytes, this field is hardwired to 000b.*	RO	RO	–	000b
4:3	**Phantom Functions Supported** ***Not supported.*** Hardwired to 00b. This field indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called Phantom Functions) with the Tag identifier.	RO	RO	–	00b
5	**Extended Tag Field Supported** Indicates the maximum supported size of the Tag field. When clear, a 5-bit Tag field is supported. When set, an 8-bit Tag field is supported. ***Note:*** *8-bit Tag field support must be enabled by the corresponding Control field in the* ***PCI Express Device Control*** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L0s entry are used with no loss of performance. Defined encodings are as follows: **Value** — **Latency** 000b — Less than 64 ns 001b — 64 ns to less than 128 ns 010b — 128 ns to less than 256 ns 011b — 256 ns to less than 512 ns 100b — 512 ns to 1 µs 101b — 1 µs to less than 2 µs 110b — 2 to 4 µs 111b — More than 4 µs	RO	RW	WO	000b

Register 14-55. (Offset 64h; DEVCAP) Device Capabilities *(Cont.)*

Bits	Description	CFG	MM	EE	Default
11:9	**Endpoint L1 Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Acceptable Latency number to compare against the L1 exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L1 entry is used with no loss of performance. Defined encodings are as follows: **Value** **Latency** 000b Less than 1 µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 to 64 µs 111b More than 64 µs	RO	RW	WO	000b
12	**Attention Button Present** ***Not supported.*** Forced to 0.	RO	RO	–	0
13	Attention Indicator Present. ***Not supported.*** Forced to 0.	RO	RO	–	0
14	**Power Indicator Present** ***Not supported.*** Forced to 0.	RO	RO	–	0
17:15	***Reserved***	RsvdP	RsvdP	–	000b
25:18	**Captured Slot Power Limit Value** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Value is set by the Set Slot Power Limit message.	RO	RW	WO	0h
27:26	**Captured Slot Power Limit Scale** Specifies the scale used for the *Slot Power Limit Value.* Range of values: **Value** **Scale** 00b 1.0x 01b 0.1x 10b 0.01x 11b 0.001x Value is set by the Set Slot Power Limit message.	RO	RW	WO	00b
31:28	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-56. (Offset 68h; DEVCTL) PCI Express Device Control

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable** Valid only in Forward Bridge mode. Controls Correctable error reporting. When an ERR_COR is detected in Forward Bridge mode and this bit is set, an ERR_COR message is transmitted to the Root Complex.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable** Valid only in Forward Bridge mode. Controls Non-Fatal error reporting. When a non-fatal error is detected in Forward Bridge mode and this bit is set, an ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
2	**Fatal Error Reporting Enable** Valid only in Forward Bridge mode. Controls Fatal error reporting. When a fatal error is detected in Forward Bridge mode and this bit is set, an ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable** Valid only in Forward Bridge mode. Controls Unsupported Request reporting. When an Unsupported Request response is received from the PCI Express in Forward Bridge mode and this bit is set, a non-ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
4	**Enable Relaxed Ordering** ***Not supported***. When set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Forced to 0.	RO	RO	–	0
7:5	**Maximum Payload Size** Sets the maximum TLP payload size for the device. As a receiver, the device must handle TLPs as large as the set value; as transmitter, the device must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the **Device Capabilities** register *Maximum Payload Size Supported* field. Defined encodings are as follows: **Value** – **Maximum Payload Size** 000b – 128 bytes 001b – 256 bytes 010b – 512 bytes 011b – 1,024 bytes 100b – 2,048 bytes 101b – 4,096 bytes 110b, 111b – ***Reserved***	RW	RW	WO	000b

Register 14-56. (Offset 68h; DEVCTL) PCI Express Device Control *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable** When clear, the device is restricted to a 5-bit Tag field. When set, enables a device to use an 8-bit Tag field as a requester. Forced to 0 when the **Device Capabilities** register *Extended Tag Field Supported* bit is cleared.	RW	RW	WO	0
9	**Phantom Function Enable** ***Not supported.*** Hardwired to 0.	RO	RO	–	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported.*** Hardwired to 0. When set, enables a device to draw AUX power independent of PME AUX power. Devices that require AUX power on legacy operating systems must continue to indicate PME AUX power requirements. AUX power is allocated as requested in the **Power Management Capabilities** register *AUX Current* field, independent of the **Power Management Control/Status** register *PME Enable* bit.	RO	RO	–	0
11	**Enable No Snoop** ***Not supported.*** Hardwired to 0. When set, the device is permitted to set the *No Snoop* bit in the Requester Attributes of transactions it initiates that do not require hardware-enforced cache coherency. Setting this bit to 1 does not cause a device to blindly set the *No Snoop* attribute on all transactions that it initiates. Although set to 1, a device only sets the *No Snoop* attribute on a transaction when it can guarantee that the transaction address is not stored in a system cache. PEX 8111 never sets the *No Snoop* attribute; therefore, this bit is forced to 0.	RO	RO	–	0
14:12	**Maximum Read Request Size** The value specified in this register is the upper boundary of the **PCI Express Device Control** register *Maximum Read Request Size* field if the **Device-Specific Control** register *Blind Prefetch Enable* bit is set. Sets the Maximum Read Request size for the Device as a Requester. The Device must not generate read requests with size exceeding the set value. Defined encodings are as follows: **Value** — **Maximum Payload Size** 000b — 128 bytes 001b — 256 bytes 010b — 512 bytes 011b — 1,024 bytes 100b — 2,048 bytes 101b — 4,096 bytes 110b, 111b — ***Reserved***	RW	RW	WO	010b
15	**Bridge Configuration Retry Enable** When clear, the PEX 8111 does not generate completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. When set, the PEX 8111 generates completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. Occurs after a delay determined by the **CRS Timer** register.	RW	RW	WO	0

Register 14-57. (Offset 6Ah; DEVSTAT) PCI Express Device Status

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Detected** Indicates correctable errors detected status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
1	**Non-Fatal Error Detected** Indicates non-fatal errors detected status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
2	**Fatal Error Detected** Indicates fatal errors detected status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
3	**Unsupported Request Detected** Indicates that the device received an Unsupported Request. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
4	**AUX Power Detected** Devices that require AUX power report this bit as set when AUX power is detected by the device.	RO	RO	–	0
5	**Transactions Pending** Because the PEX 8111 does not internally generate Non-Posted transactions, this bit is forced to 0.	RO	RO	–	0
15:6	***Reserved***	RsvdZ	RsvdZ	–	0h

Register 14-58. (Offset 6Ch; LINKCAP) Link Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed** Indicates the maximum Link speed of the given PCI Express Link. Defined encodings are as follows: **Value** **Maximum Link Speed** 0001b 2.5 Gbps Link All other values ***Reserved***	RO	RO	–	0001b
9:4	**Maximum Link Width** Indicates the maximum width of the given PCI Express Link. By default, the PEX 8111 has an x1 link; therefore, this field is hardwired to 000001b. All other values are ***not supported***.	RO	RO	–	000001b
11:10	**Active State Link PM Support** Indicates the level of active state power management supported on the given PCI Express Link. Defined encodings are as follows: **Value** **Latency** 00b ***Reserved*** 01b L0s Entry Supported 10b ***Reserved*** 11b L0s and L1 Supported	RO	RW	WO	11b
14:12	**L0s Exit Latency** Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. Defined encodings are as follows: **Value** **Latency** 000b Less than 64 ns 001b 64 ns to less than 128 ns 010b 128 ns to less than 256 ns 011b 256 ns to less than 512 ns 100b 512 ns to 1 µs 101b 1 µs to less than 2 µs 110b 2 to 4 µs 111b More than 4 µs	RO	RW	WO	100b
17:15	**L1 Exit Latency** Indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L1 to L0. Defined encodings are as follows: **Value** **Latency** 000b Less than 1 µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 to 64 µs 111b More than 64 µs	RO	RW	WO	100b
23:18	***Reserved***	RsvdP	RsvdP	–	0h
31:24	**Port Number** Indicates the PCI Express port number for the given PCI Express Link.	RO	RW	WO	0h

Register 14-59. (Offset 70h; LINKCTL) Link Control

Bits	Description	CFG	MM	EE	Default
1:0	**Active State Link PM Control** Controls the level of active state PM supported on the given PCI Express Link. Defined encodings are as follows: **Value** **PM Control** 00b Disabled 01b L0s Entry Supported 10b ***Reserved*** 11b L0s and L1 Entry Supported ***Note:*** *"L0s Entry Enabled" indicates the Transmitter entering L0s.*	RW	RW	WO	00b
2	***Reserved***	RsvdP	RsvdP	–	0
3	**Read Completion Boundary (RCB) Control** When clear, the read completion boundary is 64 bytes. When set, the read completion boundary is 128 bytes.	RW (Fwd) RO (Rev)	RW	WO	0
4	**Link Disable** Valid only in Reverse Bridge mode. Disables the Link when set to 1. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RO (Fwd) RW (Rev)	RO (Fwd) RW (Rev)	– (Fwd) WO (Rev)	0
5	**Retrain Link** Valid only in Reverse Bridge mode. Initiates Link retrain when set. Always returns 0 when read.	RO (Fwd) RW (Rev)	RO (Fwd) RW (Rev)	– (Fwd) WO (Rev)	0
6	**Common Clock Configuration** When set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.	RW	RW	WO	0
7	**Extended Sync** When set forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication.	RW	RW	WO	0
15:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-60. (Offset 72h; LINKSTAT) Link Status

Bits	Description	CFG	MM	EE	Default
3:0	**Link Speed** Indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are as follows: **Value** **Maximum Link Speed** 0001b 2.5 Gbps Link All other values ***Reserved***	RO	RO	–	0001b
9:4	**Negotiated Link Width** Indicates the negotiated width of the given PCI Express Link. By default, the PEX 8111 has an x1 link; therefore, this field is hardwired to 000001b. All other values are ***not supported***.	RO	RO	–	000001b
10	**Link Training Error** Indicates that a Link training error occurred. Only applicable in Reverse Bridge mode. Cleared by hardware upon successful training of the Link to the L0 Link state.	RO	RO	–	0
11	**Link Training** Indicates that Link training remains in progress; hardware clears this bit after Link training is complete. Only applicable in Reverse Bridge mode.	RO	RO	–	0
12	**Slot Clock Configuration** Indicates that the component uses the same physical reference clock that the platform provides on the connector. When the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	HwInit	RW	WO	0
15:13	***Reserved***	RsvdZ	RsvdZ	–	000b

Register 14-61. (Offset 74h; SLOTCAP) Slot Capabilities

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Present** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
1	**Power Controller Present** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
2	**MRL Sensor Present** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
3	**Attention Indicator Present** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
4	**Power Indicator Present** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
5	**Hot Plug Surprise** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
6	**Hot Plug Capable** Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
14:7	**Slot Power Limit Value** Valid only in Reverse Bridge mode. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot. The Power Limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Writes to this register cause the PEX 8111 to transmit the Set Slot Power Limit message downstream in Reverse Bridge mode.	RO	RW	WO	25d
16:15	**Slot Power Limit Scale** Valid only in Reverse Bridge mode. Specifies the scale used for the *Slot Power Limit Value*. Writes to this register cause the PEX 8111 to transmit the Set Slot Power Limit message downstream in Reverse Bridge mode. Defined encodings are as follows: **Value** **Scale** 00b 1.0x 01b 0.1x 10b 0.01x 11b 0.001x	RO	RW	WO	00b
18:17	***Reserved***	RsvdP	RsvdP	–	00b
31:19	**Physical Slot Number** ***Not supported.*** Forced to 0h.	RO	RO	–	0h

Register 14-62. (Offset 78h; SLOTCTL) Slot Control

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
1	**Power Fault Detected Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
2	**MRL Sensor Changed Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
3	**Presence Detect Changed Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
4	**Command Completed Interrupt Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
7:6	**Attention Indicator Control** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	00b
9:8	**Power Indicator Control** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	00b
10	**Power Controller Control** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-63. (Offset 7Ah; SLOTSTAT) Slot Status

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
1	**Power Fault Detected** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
2	**MRL Sensor Changed** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
3	**Presence Detect Changed** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
4	**Command Completed** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
5	**MRL Sensor State** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 0.	RO	RO	–	0
6	**Presence Detect State** Hot Plug-related setting. Hot Plug is ***not supported***; therefore, forced to 1.	RO	RO	–	1
15:7	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-64. (Offset 7Ch; ROOTCTL) Root Control (Reverse Bridge Mode Only)

Bits	Description	CFG	MM	EE	Default
0	**System Error on Correctable Error Enable** When set, a system error (SERR#) is generated when an ERR_COR is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
1	**System Error on Non-Fatal Error Enable** When set, a system error (SERR#) is generated when an ERR_NONFATAL is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
2	**System Error on Fatal Error Enable** When set, a system error (SERR#) is generated when an ERR_FATAL is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
3	**PME Interrupt Enable** When set, enables PME interrupt generation upon PME message receipt as reflected in the **Root Status** register *PME Status* bit. A PME interrupt is also generated when the *PME Status* bit is set when this bit is set from a cleared state.	RW	RW	WO	0
31:4	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-65. (Offset 80h; ROOTSTAT) Root Status (Reverse Bridge Mode Only)

Bits	Description	CFG	MM	EE	Default
15:0	**PME Requester ID** Indicates the PCI Requester ID of the last PME requester.	RO	RO	–	–
16	**PME Status** Indicates that PME was asserted by the Requester ID indicated in the *PME Requester ID* field. Subsequent PMEs remain pending until this bit is cleared by software, by writing 1.	RW1C	RW1C	–	0
17	**PME Pending** Indicates that another PME is pending when the *PME Status* bit is set. When the *PME Status* bit is cleared by software, the PME is delivered by hardware by setting the *PME Status* bit again and updating the Requester ID appropriately. The *PME Pending* bit is cleared by hardware when no further PMEs are pending.	RO	RO	–	–
31:18	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-66. (Offset 84h; MAININDEX) Main Control Register Index

Bits	Description	CFG	MM	EE	Default
11:0	**Main Control Register Index** Selects a **Main Control** register that is accessed by way of the **Main Control Register Data** register.	RW	RW	WO	0h
31:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-67. (Offset 88h; MAINDATA) Main Control Register Data

Bits	Description	CFG	MM	EE	Default
31:0	**Main Control Register Data** Writes to and reads from this register are mapped to a **Main Control** register selected by the **Main Control Register Index** register.	RW	RW	WO	0h

14.8 PCI Express Extended Capability Registers

14.8.1 PCI Express Power Budgeting Registers

Register 14-68. (Offset 100h; PWRCAPHDR) Power Budgeting Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI SIG-defined ID Number that indicates the nature and format of the extended capability.	RO	RW	WO	4h
19:16	**Capability Version** PCI SIG-defined Version Number that indicates the version of the capability structure present.	RO	RW	WO	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express capability structure or 000h when no other items exist in the New Capabilities Linked List. Set this field to 110h when Serial Number Capability must be enabled.	RO	RW	WO	000h

Register 14-69. (Offset 104h; PWRDATASEL) Power Budgeting Data Select

Bits	Description	CFG	MM	EE	Default
7:0	**Data Select Register** Indexes the Power Budgeting Data reported through the **Power Budgeting Data** register. Selects the DWORD of Power Budgeting Data that is to appear in the **Power Budgeting Data** register. The PEX 8111 supports values from 0 to 31 for this field. For values greater than 31, a value of 0h is returned when the **Power Budgeting Data** register is read.	RW	RW	WO	0h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-70 returns the DWORD of Power Budgeting Data selected by the **Power Budgeting Data Select** register. When the **Power Budgeting Data Select** register contains a value greater than or equal to the number of operating conditions for which the device provides power information, this register to return all zeros (0). The PEX 8111 supports 32 operating conditions.

Register 14-70. (Offset 108h; PWRDATA) Power Budgeting Data

Bits	Description	CFG	MM	EE	Default
7:0	**Base Power** Specifies, in Watts, the base power value in the given operating condition. This value must be multiplied by the *Data Scale*, to produce the actual power consumption value.	RO	RW	WO	0h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. Defined encodings are as follows: **Value** — **Scale Factor** 00b — 1.0x 01b — 0.1x 10b — 0.01x 11b — 0.001x	RO	RW	WO	00b
12:10	**PM Sub-State** Specifies the power management sub-state of the operating condition being described. Defined encodings are as follows: **Value** — **Sub-State** 000b — Default Sub-State All other values — Device Specific Sub-State	RO	RW	WO	000b
14:13	**PM State** Specifies the power management state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in the *PM Type* field to specify the D3cold PM State. An encoding of 11b along with any other *PM Type* field value specifies the D3hot state. Defined encodings are as follows: **Value** — **PM State** 00b — D0 01b — D1 10b — D2 11b — D3	RO	RW	WO	00b

Register 14-70. (Offset 108h; PWRDATA) Power Budgeting Data *(Cont.)*

Bits	Description	CFG	MM	EE	Default
17:15	**PM Type** Specifies the type of operating condition being described. Defined encodings are as follows: **Value** **PM Type** 000b PME Aux 001b Auxiliary 010b Idle 011b Sustained 111b Maximum All other values ***Reserved***	RO	RW	WO	000b
20:18	**Power Rail** Specifies the power rail of the operating condition being described. Defined encodings are as follows: **Value** **Power Rail** 000b Power (12V) 001b Power (3.3V) 010b Power (1.8V) 111b Thermal All other values ***Reserved***	RO	RW	WO	000b
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 14-71. (Offset 10Ch; PWRBUDCAP) Power Budget Capability

Bits	Description	CFG	MM	EE	Default
0	**System Allocated** When set, indicates that the device power budget is included within the system power budget. When set, software to ignore Reported Power Budgeting Data for power budgeting decisions.	RO	RW	WO	0
31:1	***Reserved***	RsvdP	RsvdP	–	0h

14.8.2 PCI Express Serial Number Registers

Register 14-72. (Offset 110h; SERCAPHDR) Serial Number Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI SIG-defined ID Number that indicates the nature and format of the extended capability. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	3h
19:16	**Capability Version** PCI SIG-defined Version Number that indicates the version of the capability structure present. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express capability structure or 000h when no other items exist in the New Capabilities Linked List.	RO	RO	–	000h

Register 14-73. (Offset 114h; SERNUMLOW) Serial Number Low

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the lower DWORD of the IEEE defined 64-bit extended unique identifier. Includes a 24-bit company identifier value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0, when Serial Number Capability is disabled.	RO	RW	WO	0h

Register 14-74. (Offset 118h; SERNUMHI) Serial Number Hi

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the upper DWORD of the IEEE defined 64-bit extended unique identifier. Includes a 24-bit company identifier value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0 when Serial Number Capability is disabled.	RO	RW	WO	0h

14.9 Main Control Registers

Register 14-75. (Offset 1000h; DEVINIT) Device Initialization

Bits	Description	Access	Default
3:0	**PCLKO Clock Frequency** Controls the PCLKO ball frequency. When cleared to 0000b, the clock is stopped and remains at a logic low (0V) DC value. Non-zero values represent divisors of the 100-MHz REFCLK. The default value is 0011b, representing a frequency of 66 MHz. **Value** **Frequency (MHz)** 0000b 0 0001b 100 0010b 50 0011b 33.3/66 (When M66EN is high, PCLKO frequency is 66 MHz) 0100b 25 0101b 20 0110b 16.7 0111b 14.3 1000b 12.5 1001b 11.1 1010b 10 1011b 9.1 1100b 8.3 1101b 7.7 1110b 7.1 1111b 6.7	RW	0011b
4	**PCI Express Enable** When clear, all configuration accesses to the PEX 8111 result in a completion status of Configuration Request Retry Status. When set, the PEX 8111 responds normally to PCI Express configuration accesses. When no valid serial EEPROM is detected, this bit is automatically set.	RW	0
5	**PCI Enable** When clear, all PCI accesses to the PEX 8111 result in a Target Retry response. When set, the PEX 8111 responds normally to PCI accesses. When no valid serial EEPROM is detected, this bit is automatically set.	RW	0
31:6	***Reserved***	RsvdP	0h

Register 14-76. (Offset 1004h; EECTL) Serial EEPROM Control

Bits	Description	Access	Default
7:0	**Serial EEPROM Write Data** Determines the byte written to the serial EEPROM when the *Serial EEPROM Byte Write Start* bit is set. Represents an opcode, address, or data being written to the serial EEPROM.	RW	0h
15:8	**Serial EEPROM Read Data** Determines the byte read from the serial EEPROM when the *Serial EEPROM Byte Read Start* bit is set.	RO	–
16	**Serial EEPROM Byte Write Start** When set, the value in the *Serial EEPROM Write Data* field is written to the serial EEPROM. Automatically cleared when the Write operation is complete.	RW	0
17	**Serial EEPROM Byte Read Start** When set, a byte is read from the serial EEPROM, and accessed using the *Serial EEPROM Read Data* field. Automatically cleared when the Read operation is complete.	RW	0
18	**Serial EEPROM Chip Select Enable** When set, the Serial EEPROM Chip Select is enabled.	RW	0
19	**Serial EEPROM Busy** When set, the Serial EEPROM Controller is busy performing a Byte Read or Write operation. An interrupt is generated when this bit goes false.	RO	0
20	**Serial EEPROM Valid** A serial EEPROM with 5Ah in the first byte is detected.	RO	–
21	**Serial EEPROM Present** Set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the PEX 8111.	RO	–
22	**Serial EEPROM Chip Select Active** Set when the EECS# ball to the serial EEPROM is active. The Chip Select is active across multiple byte operations.	RO	–
24:23	**Serial EEPROM Address Width** Reports the installed serial EEPROM's addressing width. When the addressing width cannot be determined, 0 is returned. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. **Value** – **Address Width** 00b – Undetermined 01b – 1 byte 10b – 2 bytes 11b – 3 bytes	RO	–
30:25	***Reserved***	RsvdP	0h
31	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the serial EEPROM. Reading this bit returns 0 while initialization is in progress, and 1 when initialization is complete.	RW	0

Register 14-77. (Offset 1008h; EECLKFREQ) Serial EEPROM Clock Frequency

Bits	Description	Access	Default
2:0	**Serial EEPROM Clock Frequency** Controls the EECLK ball frequency. **Value** **Frequency** 000b 2 MHz 001b 5 MHz 010b 8.3 MHz 011b 10 MHz 100b 12.5 MHz 101b 16.7 MHz 110b 25 MHz 111b ***Reserved***	RW	000b
31:3	***Reserved***	RsvdP	0h

Register 14-78. (Offset 100Ch; PCICTL) PCI Control

Bits	Description	Access	Default
0	**PCI Multi-Level Arbiter** When clear, all PCI requesters are placed into a single-level Round-Robin arbiter, each with equal access to the PCI Bus. When set, a two-level arbiter is selected.	RW	0
3:1	**PCI Arbiter Park Select** Determines which PCI master controller is granted the PCI bus when there are no pending requests. **Value** **Park** 000b Last Grantee 001b PCI Express Bus 010b, 011b ***Reserved*** 100b External Requester 0 101b External Requester 1 110b External Requester 2 111b External Requester 3	RW	000b
4	**Bridge Mode** Reflects the FORWARD ball status. When low, the device operates as a Reverse Bridge (PCI-to-PCI Express). When high, the device operates as a Forward Bridge (PCI Express-to-PCI).	RO	–
5	**PCI External Arbiter** Reflects the EXTARB ball state. When low, the PEX 8111 enables its internal arbiter. It then expects external requests on REQ[3:0]# and issues bus grants on GNT[3:0]#. When high, the PEX 8111 asserts REQ0# and expects GNT0# from an external arbiter.	RO	–
6	**Locked Transaction Enable** When clear, PCI Express Memory Read Lock requests are completed with UR status, and the PCI LOCK# ball is not driven in Forward Bridge mode. In Reverse Bridge mode, the PCI LOCK# ball is ignored. When set, Locked transactions are propagated through the bridge from the primary to secondary bus.	RW	0
7	**M66EN** Reflects the M66EN ball state. When low, the PEX 8111 PCI Bus is operating at 33 MHz. When high, the PEX 8111 PCI Bus is operating at 66 MHz.	RO	0

Register 14-78. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bits	Description	Access	Default
15:8	**PCI-to-PCI Express Retry Count** Valid only in Reverse Bridge mode when the PCI Express link is down. Determines number of times to Retry a PCI Type 1 Configuration transaction to PCI Express before aborting the transfer, in units of 2^{14} Retries. A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry count of 2^{24}. When the timer times out, a Master Abort is returned to the PCI Bus.	RW	80h
23:16	**PCI Express-to-PCI Retry Count** Determines number of times to Retry a PCI Express-to-PCI transaction before aborting the transfer, in units of 2^{4} Retries. A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry count of 2^{24}.	RW	0h
24	**Memory Read Line Enable** When clear, the PEX 8111 issues a Memory Read command for transactions that do not start on a cache boundary. When set, a Memory Read Line command is issued when a transaction is not aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst is stopped at the cache line boundary when the burst transfer size is less than one cache line of data or when a Memory Read Multiple command is started.	RW	1
25	**Memory Read Multiple Enable** When clear, the PEX 8111 issues a Memory Read command for transactions that start on a cache boundary. When set, a Memory Read Multiple command is issued when a transaction is aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst continues when the Burst Transfer size remains greater than or equal to one cache line of data.	RW	1
26	**Early Byte Enables Expected** When clear, the PEX 8111 accepts PCI Bytes Enables that are not valid until IRDY# is asserted. When set, the PEX 8111 expects the PCI Byte Enables to be valid in the clock tick following the Address phase. For maximum compatibility with non-compliant PCI devices, clear this bit to 0. For maximum performance, set this bit to 1.	RW	0
29:27	**Programmed Prefetch Size** Determines the byte number requested from the PCI Express bus as a result of a PCI-to-PCI Express read. Enable feature only when the PCI initiator reads all requested data without disconnecting. Otherwise, performance is impacted. Valid only for Memory Read Line and Memory Read Multiple transactions, or Memory Read transactions with the **Device-Specific Control** register *Blind Prefetch Enable* bit set. The Prefetch Size is limited by the **PCI Express Device Control** register *Maximum Read Request Size* field. **Value** — **Prefetch Size** 000b — Disabled 001b — 64 bytes 010b — 128 bytes 011b — 256 bytes 100b — 512 bytes 101b — 1,024 bytes 110b — 2,048 bytes 111b — 4,096 bytes (refer to Note) ***Note:*** *If the Programmed Prefetch Size is 4 KB, the* **TLP Controller Configuration 0** *register Limit Completion Flow Control Credit bit must be set.*	RW	000b
31:30	***Reserved***	RsvdP	00b

Register 14-79. (Offset 1010h; PCIEIRQENB) PCI Express Interrupt Request Enable

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** When set, enables a PCI Express interrupt to generate when a Serial EEPROM Read or Write transaction completes. (Refer to Section 5.1, "Forward Bridge PCI Interrupts," for further details.)	RW	0
1	**GPIO Interrupt Enable** When set, enables a PCI Express interrupt to generate when an interrupt is active from one of the GPIO balls.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** When set, enables a PCI Express interrupt to generate when the PCI Express-to-PCI Retry count is reached.	RW	0
4	**Mailbox 0 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 3 is written.	RW	0
30:8	***Reserved***	RsvdP	0h
31	**PCI Express Internal Interrupt Enable** When set, enables a PCI Express interrupt to generate as a result of an internal PEX 8111 interrupt source. The internal interrupt is serviced as a Message Signaled Interrupt (MSI) or a virtual wire interrupt. (Refer to Section 5.1, "Forward Bridge PCI Interrupts," for further details.)	RW	1 (Fwd) 0 (Rev)

Register 14-80. (Offset 1014h; PCIIRQENB) PCI Interrupt Request Enable

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** When set, enables a PCI interrupt to generate when a Serial EEPROM Read or Write transaction completes. (Refer to Section 5.2, "Reverse Bridge PCI Interrupts," for further details.)	RW	0
1	**GPIO Interrupt Enable** When set, enables a PCI interrupt to generate when an interrupt is active from one of the GPIO balls.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** When set, enables a PCI interrupt to generate when the PCI Express-to-PCI Retry count is reached.	RW	0
4	**Mailbox 0 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 3 is written.	RW	0
8	**Unsupported Request Interrupt Enable** When set, enables a PCI interrupt to generate when an Unsupported Request Completion response is received from the PCI Express.	RW	0
30:9	***Reserved***	RsvdP	0h
31	**PCI Internal Interrupt Enable** When set, enables a PCI interrupt to generate as a result of an internal PEX 8111 interrupt source. (Refer to Section 5.2, "Reverse Bridge PCI Interrupts," for further details.)	RW	0 (Fwd) 1 (Rev)

Register 14-81. (Offset 1018h; IRQSTAT) Interrupt Request Status

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt** Set when a Serial EEPROM Read or Write transaction completes. Writing 1 clears this status bit.	RW1C	0
1	**GPIO Interrupt** Conveys the interrupt status for the four GPIO balls. When set, the **General-Purpose I/O Status** register is read to determine the cause of the interrupt. Set independently of the *GPIO Interrupt Enable* bits. This bit is an OR of the four individual GPIO status bits.	RO	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt** Set when the PCI Express-to-PCI Retry count is reached. Writing 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt** Set when Mailbox 0 is written. Writing 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt** Set when Mailbox 1 is written. Writing 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt** Set when Mailbox 2 is written. Writing 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt** Set when Mailbox 3 is written. Writing 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt** Set when an Unsupported Request Completion is received from the PCI Express. Writing 1 clears this bit	RW1C	0
31:9	***Reserved***	RsvdZ	0h

Register 14-82. (Offset 101Ch; POWER) Power (Forward Bridge Mode Only)

Bits	Description	Access	Default
7:0	**Power Compare 0** Specifies the power required for this device and downstream PCI devices in Forward Bridge mode. It is compared with the **Device Capabilities** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capabilities** register *Captured Slot Power Limit Scale* field is 00b (scale = 1.0x).	RW	0h
15:8	**Power Compare 1** Specifies the power required for this device and downstream PCI devices in Forward Bridge mode. It is compared with the **Device Capabilities** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capabilities** register *Captured Slot Power Limit Scale* field is 01b (scale = 0.1x).	RW	0h
23:16	**Power Compare 2** Specifies the power required for this device and downstream PCI devices in Forward Bridge mode. It is compared with the **Device Capabilities** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capabilities** register *Captured Slot Power Limit Scale* field is 10b (scale = 0.01x).	RW	0h
31:24	**Power Compare 3** Specifies the power required for this device and downstream PCI devices in Forward Bridge mode. It is compared with the **Device Capabilities** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capabilities** register *Captured Slot Power Limit Scale* field is 11b (scale = 0.001x).	RW	0h

Register 14-83. (Offset 1020h; GPIOCTL) General-Purpose I/O Control

Bits	Description	Access	Default
0	**GPIO0 Data** When programmed as an output, values written to this bit appear on the GPIO0 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 ball.	RW	0
1	**GPIO1 Data** When programmed as an output, values written to this bit appear on the GPIO1 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 ball.	RW	0
2	**GPIO2 Data** When programmed as an output, values written to this bit appear on the GPIO2 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 ball.	RW	0
3	**GPIO3 Data** When programmed as an output, values written to this bit appear on the GPIO3 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 ball.	RW	0
4	**GPIO0 Output Enable** When clear, the GPIO0 ball is an input. When set, the GPIO0 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	1
5	**GPIO1 Output Enable** When clear, the GPIO1 ball is an input. When set, the GPIO1 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
6	**GPIO2 Output Enable** When clear, the GPIO2 ball is an input. When set, the GPIO2 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
7	**GPIO3 Output Enable** When clear, the GPIO3 ball is an input. When set, the GPIO3 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
8	**GPIO0 Interrupt Enable** When set, changes on the GPIO0 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
9	**GPIO1 Interrupt Enable** When set, changes on the GPIO1 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
10	**GPIO2 Interrupt Enable** When set, changes on the GPIO2 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
11	**GPIO3 Interrupt Enable** When set, changes on the GPIO3 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0

Register 14-83. (Offset 1020h; GPIOCTL) General-Purpose I/O Control *(Cont.)*

Bits	Description	Access	Default
13:12	**GPIO Diagnostic Select** Selects diagnostic signals that are output on the GPIO balls. **Value** **Description** 00b Normal GPIO operation 01b GPIO0 driven high when Link is up. GPIO[3:1] operate according to the configuration specified by bits [7:5] of this register. 10b GPIO[3:0] driven with lower four bits of the LTSSM state machine for twos (2), alternating with GPIO[1:0] driven with the upper two bits of the LTSSM state machine for ones (1) 11b GPIO[3:0] driven with PMU Linkstate (L2, L1, L0s, and L0) **LTSSM Codes** 00h – L3_L2 (Fundamental Reset) 01h – Detect 02h – Polling.Active 03h – Polling.Configuration 04h – Polling.Compliance 05h – Configuration.Linkwidth.Start & Accept (Reverse Bridge Mode) 06h – Configuration.Lanenum.Wait & Accept (Reverse Bridge Mode) 07h – Configuration.Complete (Reverse Bridge Mode) 08h – Configuration.Idle (Reverse Bridge Mode) 09h – Configuration.Linkwidth.Start (Forward Bridge Mode) 0Ah – Configuration.Linkwidth.Accept (Forward Bridge Mode) 0Bh – Configuration.Lanenum.Wait & Accept (Forward Bridge Mode) 0Ch – Configuration.Complete (Forward Bridge Mode) 0Dh – Configuration.Idle (Forward Bridge Mode) 0Eh – L0 0Fh – L0 (Transmit E.I.Ordered-set) 10h – L0 (Wait E.I.Ordered-set) 12h – L1.Idle 14h – L2.Idle 15h – Recovery.Rcvrlock (Extended Sync enabled) 16h – Recovery.Rcvrlock 17h – Recovery.RcvrCfg 18h – Recovery.Idle 19h – Disabled (Transmit TS1) 1Ah – Disabled (Transmit E.I.Ordered-set) 1Dh – Disabled (Wait Electrical Idle) 1Eh – Disabled (Disable) 1Fh – Loopback.Entry 20h – Loopback.Active 21h – Loopback.Exit 22h – Hot Reset (Wait TS1 with Hot Reset, Reverse Bridge Mode) 23h – Hot Reset (Reset Active) 24h – Loopback.Actice (Transmit E.I.Ordered-set) 25h – Loopback.Active (Wait Electrical Idle)	RW	01b
31:14	***Reserved***	RsvdP	0h

Register 14-84. (Offset 1024h; GPIOSTAT) General-Purpose I/O Status

Bits	Description	Access	Default
0	**GPIO0 Interrupt** Set when the GPIO0 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt** Set when the GPIO1 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt** Set when the GPIO2 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt** Set when the GPIO3 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
31:4	***Reserved***	RsvdZ	0h

Register 14-85. (Offset 1030h; MAILBOX0) Mailbox 0

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express or PCI Bus. Interrupts are generated to either of the buses when this register is written.	RW	FEEDFACEh

Register 14-86. (Offset 1034h; MAILBOX1) Mailbox 1

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express or PCI Bus. Interrupts are generated to either of the buses when this register is written.	RW	0h

Register 14-87. (Offset 1038h; MAILBOX2) Mailbox 2

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express or PCI Bus. Interrupts are generated to either of the buses when this register is written.	RW	0h

Register 14-88. (Offset 103Ch; MAILBOX3) Mailbox 3

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express or PCI Bus. Interrupts are generated to either of the buses when this register is written.	RW	0h

Register 14-89. (Offset 1040h; CHIPREV) Chip Silicon Revision

Bits	Description	Access	Default
15:0	**Chip Revision** Returns the PEX 8111 current Silicon Revision number.	RO	Current Revision
31:16	***Reserved***	RsvdP	0h

Note: ***CHIPREV*** *is the Silicon Revision, encoded as a 4-digit BCD value. The* ***CHIPREV*** *value for the third release of the chip (Rev. BB) is 0201h. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*

Register 14-90. (Offset 1044h; DIAGCTL) Diagnostic Control (*Factory Test Only*)

Bits	Description	Access	Default
0	**Fast Times** When set, internal timers and counters operate at a fast time for factory chip testing.	RW	0
1	**Force PCI Interrupt** When set, forces the PCI INT*x*# interrupt signal to assert. The **PCI Interrupt Pin** register determines which INT*x*# signal is asserted. Effective only when the **PCI Command** register *Interrupt Disable* bit is low.	RW	0
2	**Force PCI SERR** When set, forces the PCI SERR# interrupt signal to assert when the **PCI Command** register *SERR# Enable* bit is set (Reverse Bridge mode). In Forward Bridge mode, the **Bridge Control** register *Secondary SERR# Enable* bit must be set.	RW	0
3	**Force PCI Express Interrupt** When set, forces an interrupt to the PCI Express Root Complex using Message Signaled Interrupts or virtual INT*x*# interrupts.	RW	0
31:4	***Reserved***	RsvdP	0h

Register 14-91. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0

Bits	Description	Access	Default
7:0	**CFG_NUM_FTS** Forced NUM_FTS signal. NUM_FTS represents the number of Fast Training sequence (0 to 255). Refer to the *PCI Express r1.0a*, Section 4.2.4.3, for detailed information.	RW	20h
8	**CFG_ACK_FMODE** PCI Express interface ACK_DLLP transmitting interval mode. 0 = PCI Express interface uses own interval value 1 = PCI Express interface uses *CFG_ACK_COUNT* as interval value	RW	0
9	**CFG_TO_FMODE** PCI Express interface Timeout detection mode for replay timer. 0 = PCI Express interface uses own timer value 1 = PCI Express interface uses *CFG_TO_COUNT* as timer value	RW	0
10	**CFG_PORT_DISABLE** When set, the SERDES in PCI Express interface is disabled. This allows the endpoint to disable the PCI Express connection when power up or before the configuration is completed.	RW	0
11	**CFG_RCV_DETECT** Asserted when the PCI Express interface establishes the PCI Express connection.	RO	0
12	**CFG_LPB_MODE** Link Loop-Back mode. When set, the PEX8111 changes its LTSSM state to the Loop-Back state, becomes the Loop-Back master, and starts transmitting packets of pseudo random numbers.	RW	0
13	**CFG_PORT_MODE** When clear, Link PCI Express interface is configured as an upstream port (Endpoint). When set, Link PCI Express interface is configured as a downstream port (Root Complex).	RW	F(0) R(1)
14	***Reserved***	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE** When set, link is allowed generate ECRC. The PEX 8111 does not support ECRC; therefore, this bit is cleared to 0.	RW	0
16	**TLB_CPLD_NOSUCCESS_MALFORM_ENABLE** When clear, received completion is retained. When set, completion received when completion timeout expired is treated as a malformed TLB and is discarded.	RW	1
17	**Scrambler Disable** When clear, data scrambling is enabled. When set, data scrambling is disabled. Set only when testing and debugging.	RW	0
18	**Delay Link Training** When clear, link training is allowed to commence immediately after PEX_PERST# is de-asserted. When set, link training is delayed for 12 ms after Reset is de-asserted. Automatically set when GPIO3 is low during reset.	RW	0
19	**Decode Primary Bus Number** When clear, the PEX 8111 ignores the Primary Bus Number in a PCI Express Type 0 Configuration Request. When set, the PEX 8111 compares the Primary Bus Number in a PCI Express Type 0 Configuration Request with the **Primary Bus Number** register. When they match, the request is accepted. Otherwise, an Unsupported Request is returned. This comparison occurs only after the first Type 0 Configuration write occurs.	RW	0

Register 14-91. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0 *(Cont.)*

Bits	Description	Access	Default
20	**Ignore Function Number** When clear, the PEX 8111 only responds to Function Number 0 during a Type 0 Configuration transaction. Accesses to other function numbers result in an Unsupported Request (PCI Express) or Master Abort (PCI). When set, the PEX 8111 ignores the Function Number in a PCI or PCI Express Type 0 Configuration request, and responds to all eight functions.	RW	0
21	**Check RCB Boundary** When clear, the PEX 8111 ignores Read Completion Boundary (RCB) Violations. When set, the PEX 8111 checks for RCB violations. When detected, the PEX 8111 treats it as a malformed TLP (packet is dropped and a non-fatal error message is transmitted).	RW	0
22	**Limit Completion Flow Control Credit** When clear, the PEX 8111 advertises infinite flow control credits for completions. When set, the PEX 8111advertises completion flow control credits, based on available FIFO storage. Must be set when the **PCI Control** register *Programmed Prefetch Size* field is set to 4 KB. When GPIO2 is low during reset, this bit is automatically set. Because this bit is used during link training, it must be set by driving GPIO2 low during reset.	RW	0
23	**L2 Secondary Bus Reset** When clear and the PEX 8111 remains in the L2/L3 Ready state in Reverse Bridge mode, PCI-to-PCI Express Configuration transactions are Retried until the **PCI Control** register *PCI-to-PCI Express Retry Count* expires. The PEX 8111 responds with a Master Abort. When set, and the PEX 8111 remains in the L2/L3 Ready state in Reverse Bridge mode, PCI-to-PCI Express Configuration transactions result in a secondary bus reset. After the link training completes, the PCI-to-PCI Express Configuration transaction completes normally.	RW	1
31:24	***Reserved***	RsvdP	0h

Register 14-92. (Offset 104Ch; TLPCFG1) TLP Controller Configuration 1

Bits	Description	Access	Default
20:0	**CFG_TO_COUNT** PCI Express interface Replay Timer timeout value when *CFG_TO_FMODE* is set to 1.	RW	D4h
30:21	**CFG_ACK_COUNT** PCI Express interface ACK DLLP transmitting interval value when *CFG_ACK_FMODE* is set to 1.	RW	0h
31	***Reserved***	RsvdP	0

Register 14-93. (Offset 1050h; TLPCFG2) TLP Controller Configuration 2

Bits	Description	Access	Default
15:0	**CFG_COMPLETER_ID0** Bits [15:8] = Bus Number Bits [7:3] = Device Number Bits [2:0] = Function Number The Bus, Device, and Function Numbers of a Configuration transaction to the PEX 8111 are latched in this register. The latched values are then used when generating the completion.	RW	0h
26:16	**Update Credit FC** Controls a counter that determines the gap between UpdateFC DLLPs, in units of 62.5 MHz clocks = 16 ns = 4 symbol times. When data or headers are read from the TLP Controller, the Credit Allocation Manager transmits a set of UpdateFC DLLPs; posted, non-posted, and completion when the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. While transmitting the set of DLLPs, the Credit Allocation Manager uses the counter value to insert gaps between the DLLPs. The Bus, Device, and Function Numbers of a Configuration transaction to the PEX 8111 are latched in this register. The latched values are then used when generating the completion.	RW	1h
31:27	***Reserved***	RsvdP	0h

Register 14-94. (Offset 1054h; TLPTAG) TLP Controller Tag

Bits	Description	Access	Default
7:0	**TAG BME1** Message Request tag field.	RW	0h
15:8	**TAG ERM** Error Manager tag field.	RW	0h
23:16	**TAG PME** Power Manager tag field.	RW	0h
31:24	***Reserved***	RsvdP	0h

Register 14-95. (Offset 1058h; TLPTIMELIMIT0) TLP Controller Time Limit 0

Bits	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT** Bus master engine completion timeout in PCI clock units. The default value produces a 10-ms timeout.	RW	51615h (M66EN low) A2C2Ah (M66EN high)
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT** Determines length of time before power is removed after entering the L2 state. Value to be at least 100 ns. Contains PCI clock units.	RW	4h (M66EN low) 8h (M66EN high)
31:28	***Reserved***	RsvdP	0h

Register 14-96. (Offset 105Ch; TLPTIMELIMIT1) TLP Controller Time Limit 1

Bits	Description	Access	Default
10:0	**ASPM_LI_DLLP_INTERVAL_TIME_LIMIT** Determines time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions. The default is 10 µs for both 14Dh and 29Ah. Allow at least 10 µs spent in LTSSM L0 and L0s state before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP is transmitted. Refer to the *PCI Express r1.0a Errata,* page 19, for detailed information. Contains PCI clock units.	RW	14Dh (M66EN low) 29Ah (M66EN high)
31:11	***Reserved***	RsvdP	0h

Register 14-97. (Offset 1060h; CRSTIMER) CRS Timer (Forward Bridge Mode Only)

Bits	Description	Access	Default
15:0	**CRS Timer** Valid only in Forward Bridge mode when the **PCI Express Device Control** register *Bridge Configuration Retry Enable* bit is set. Determines number of microseconds to wait before returning a completion with CRS status in response to a PCI Express-to-PCI Configuration transaction. When the timer times out and the completion with CRS status is returned, the transaction is discarded from the Non-Posted Transaction queue.	RW	25d
31:16	***Reserved***	RsvdP	0h

Register 14-98. (Offset 1064h; ECFGADDR) Enhanced Configuration Address

Bits	Description	Access	Default
11:0	***Reserved***	RsvdP	0h
14:12	**Configuration Function Number** Provides the Function Number for an enhanced Configuration transaction.	RW	000b
19:15	**Configuration Device Number** Provides the Device Number for an enhanced Configuration transaction.	RW	0h
27:20	**Configuration Bus Number** Provides the Bus Number for an enhanced Configuration transaction.	RW	0h
30:28	***Reserved***	RsvdP	000b
31	**Enhanced Configuration Enable** Used only in Reverse Bridge mode. When clear, accesses to the **Base Address 0** register, offset 2000h, are not responded to by the PEX 8111. When set, accesses to the **Base Address 0** register, offset 2000h, are forwarded to the PCI Express Bus as a Configuration Request.	RW	0

Chapter 15 Shared Memory

15.1 Overview

The PEX 8111 contains a 2 KB x 32-bit (8-KB) memory block that is accessed from the serial EEPROM, PCI Express Bus, or PCI Bus.

15.2 Serial EEPROM Accesses

When the *Shared Memory Load* bit in the Serial EEPROM Format Byte is set, the shared memory is loaded from the serial EEPROM starting at location REG BYTE COUNT + 6. The byte number to load is determined by the value in serial EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5. The serial EEPROM data is always loaded into the shared memory starting at Address 0. Data is transferred from the serial EEPROM to the shared memory in DWORD units. Refer to Chapter 6, "Serial EEPROM Controller," for details.

15.3 PCI Express Accesses

The shared memory is accessed using the 64-KB address space defined by the **Base Address 0** register. The shared memory is located at Address offset 8000h in this space. PCI Express posted writes are used to write data to the shared memory. Single or Burst writes are accepted, and PCI Express first and last Byte Enables are supported. When shared memory write data is poisoned, the data is discarded and an ERR_NONFATAL message is generated when enabled. PCI Express Non-Posted reads are used to read data from the shared memory. Single or Burst reads are accepted. When the 8-KB boundary of the shared memory is reached during a Burst write or read, the address wraps around to the start of memory.

15.4 PCI Accesses

The shared memory is accessed using the 64-KB address space defined by the **Base Address 0** register. The shared memory is located at Address offset 8000h in this space. PCI single or Burst writes are used to write data to the shared memory. PCI Byte Enables are supported for each DWORD transferred. PCI Single or Burst reads are used to read data from the shared memory. When the 8-KB boundary of the shared memory is reached during a Burst write or read, a PCI Disconnect is generated.

Chapter 16 Testability and Debug

16.1 Joint Test Action Group (JTAG) Interface

The PEX 8111 provides a JTAG Boundary Scan interface, which is utilized to debug board connectivity for each ball.

16.1.1 IEEE Standard 1149.1 Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG* debug port, is an architectural standard described in the *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*. This standard describes a method for accessing internal chip facilities, using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG debug port implements the four required JTAG signals (TCK, TDI, TDO, TMS) and the optional TRST# signal
- JTAG Clock Requirements – TCK signal frequency range from DC to 10 MHz
- JTAG Reset Requirements – Refer to Section 16.1.4, "JTAG Reset Input TRST#"

16.1.2 JTAG Instructions

The JTAG debug port provides the *IEEE standard 1149.1* EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE instructions, as listed in Table 16-1. ***PRIVATE instructions are for PLX use only.*** Invalid instructions behave as the BYPASS instruction. Table 16-1 lists the JTAG instructions, along with their input codes. The PEX 8111 returns the IDCODE values listed in Table 16-2.

Table 16-1. EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE Instructions

Instruction	Input Code	Comments
EXTEST	00000b	*IEEE Standard 1149.1-1990*
IDCODE	00001b	
SAMPLE/PRELOAD	00011b	
BYPASS	11111b	
PRIVATE[a]	00011b	
	00100b	
	00101b	
	00110b	
	00111b	
	01000b	
	01001b	
	01010b	

*a. **Warning: Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.***

Table 16-2. PEX 8111 JTAG IDCODE Values

PEX 8111	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0001b	1000_0001_1101_0010	000_0001_0000	1
Hex	1h	81D2h	10h	1h
Decimal	1	33234	16	1

16.1.3 JTAG Boundary Scan Boundary

Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture. BSDL*, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, which allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. *BSDL* supports robust extensions that are used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of *BSDL* include the logical port description, physical ball map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the PEX 8111 balls. Each ball contains a logical type of In, Out, In Out, Buffer, or Linkage that defines the logical direction of signal flow.

The physical ball map correlates the chip logical ports to the physical balls of a specific package. A *BSDL* description maintains several physical ball maps; each map is given a unique name. (Refer to Section 2.3.1, "Physical Ball Assignment – 144-Ball PBGA Package" and Section 2.4.1, "Physical Ball Assignment – 161-Ball FBGA Package.")

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the chip in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the chip.

The boundary register description lists each cell or shift stage of the Boundary register. Each cell contains a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

16.1.4 JTAG Reset Input TRST#

The TRST# input ball is the asynchronous JTAG logic reset. When TRST# is asserted, it causes the PEX 8111 TAP controller to initialize. In addition, when the TAP controller is initialized, it selects the PEX 8111 normal logic path (PCI Express interface-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  - TRST# input signal uses a low-to-high transition one time during the PEX 8111 boot-up, along with the RST# signal
  - Hold the PEX 8111 TMS ball high while transitioning the PEX 8111 TCK ball five times
- If JTAG functionality is not required, the TRST# signal must be directly connected to ground

Chapter 17 Electrical Specifications

17.1 Power-Up Sequence

Apply power supply voltages in the following sequence:

1. VDD5
2. 3.3V
3. 1.5V

When the VDD5 balls are connected to the same 3.3V power supply used by the VDD3.3 and VDDQ balls, power can be applied at the same time to the VDD5, VDD3.3, and VDDQ balls.

17.2 Power-Down Sequence

Remove power supply voltages in the following sequence:

1. 1.5V
2. 3.3V
3. VDD5

When the VDD5 balls are connected to the same 3.3V power supply used by the VDD3.3 and VDDQ balls, power can be removed at the same time from the VDD5, VDD3.3, and VDDQ balls.

17.3 Absolute Maximum Ratings

Caution: ***Conditions that exceed the Absolute Maximum limits can destroy the device.***

Table 17-1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Power Supply Voltages	With Respect to Ground	-0.5	+1.8	V
VDD3.3, VDDQ	3.3V Power Supply Voltages	With Respect to Ground	-0.5	+4.6	V
VDD5	5V Power Supply Voltage	With Respect to Ground	-0.5	+6.6	V
V_I	DC Input Voltage	3.3V buffer	-0.5	+4.6	V
		5V Tolerant buffer (PCI)	-0.5	+6.6	V
I_{OUT}	DC Output Current, per ball	3 mA Buffer	-10	+10	mA
		6 mA Buffer	-20	+20	mA
		12 mA Buffer	-40	+40	mA
		24 mA Buffer (PCI)	-70	+70	mA
T_{STG}	Storage Temperature	No bias	-65	+150	°C
V_{ESD}	ESD Rating	R = 1.5K, C = 100 pF	–	2	KV

17.4 Recommended Operating Conditions

Caution: ***Conditions that exceed the Operating limits can cause the device to malfunction.***

Table 17-2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Power Supply Voltages		1.4	1.6	V
VDD3.3, VDDQ	3.3V Power Supply Voltages		3.0	3.6	V
VDD5	5V Power Supply Voltage	Note 1	4.75	5.25	V
V_N	Negative Trigger Voltage	3.3V buffer	0.8	1.7	V
		5V tolerant buffer (PCI)	0.8	1.7	V
V_P	Positive Trigger Voltage	3.3V buffer	1.3	2.4	V
		5V tolerant buffer (PCI)	1.3	2.4	V
V_{IL}	Low Level Input Voltage	3.3V buffer	0	0.7	V
		5V tolerant buffer (PCI)	0	0.8	V
V_{IH}	High Level Input Voltage	3.3V buffer	1.7	VDD3	V
		5V tolerant buffer (PCI)	2.0	VDD5 + 0.5	V
I_{OL}	Low Level Output Current	3 mA buffer (V_{OL} = 0.4)		3	mA
		6 mA buffer (V_{OL} = 0.4)		6	mA
		12 mA buffer (V_{OL} = 0.4)		12	mA
		24 mA buffer (V_{OL} = 0.4) (PCI)		24	mA
I_{OH}	High Level Output Current	3 mA buffer (V_{OH} = 2.4)		-3	mA
		6 mA buffer (V_{OH} = 2.4)		-6	mA
		12 mA buffer (V_{OH} = 2.4)		-12	mA
		24 mA buffer (V_{OH} = 2.4) (PCI)		-24	mA
T_A	Operating Temperature		0	70	°C
t_R	Input Rise Times	Normal input	0	200	ns
t_F	Input Fall Time		0	200	ns
t_R	Input Rise Times	Schmitt input	0	10	ms
t_F	Input Fall Time		0	10	ms

Notes:

1. *In a 3.3V-only system, the VDD5 balls can be connected to the 3.3V power supply (3.0 to 3.6V).*

17.5 DC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = 0 to 70°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 17-3. PCI Express Interface DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDD1.5}$	VDD1.5 Supply Current	VDD1.5 = 1.5V		180	207	mA
$I_{VDDSERDES}$	VDD_P, VDD_R, VDD_T, AVDD, Supply Currents	VDD_P, VDD_R, VDD_T, AVDD = 1.5V				
$I_{VDD3.3}$	VDD3.3 Supply Current	VDD3.3 = 3.3V		19	22	mA
I_{VDDQ}	VDDQ Supply Current	VDDQ= 3.3V				
I_{VDD5}	VDD5 Supply Current	VDD5= 5.0V		.003	.004	mA

17.5.1 PCI Bus DC Specification

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = 0 to 70°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 17-4. PCI Bus DC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHd}	PCI 3.3V Input High Voltage		0.5 * VDD3.3		VDD3.3	V
V_{ILd}	PCI 3.3V Input Low Voltage		0		0.7	V
V_{IH}	PCI 5.0V Input High Voltage		2.0		5.5	V
V_{IL}	PCI 5.0V Input Low Voltage		0		0.8	V
I_{IL}	Input Leakage	$0V < V_{IN} < VDD5$	-10		+10	µA
I_{OZ}	Hi-Z State Data Line Leakage	$0V < V_{IN} < VDD5$			10	µA
V_{OH3}	PCI 3.3V Output High Voltage	I_{OUT} = -500 µA	0.9 * VDD3.3			V
V_{OL3}	PCI 3.3V Output Low Voltage	I_{OUT} = 1500 µA			0.1 * VDD3.3	V
V_{OH}	PCI 5.0V Output High Voltage	I_{OUT} = -12 mA	2.4			V
V_{OL}	PCI 5.0V Output Low Voltage	I_{OUT} = 12 mA			0.4	V
C_{IN}	Input Capacitance	Ball to GND			10	pF
C_{CLK}	CLK Ball Capacitance	Ball to GND	5		12	pF
C_{IDSEL}	IDSEL Ball Capacitance	Ball to GND			8	pF

17.6 AC Specifications

17.6.1 PCI Bus 33-MHz AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = 0 to 70°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 17-5. PCI Bus 33-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		30	∞	ns	
T_{VAL}	CLK to Signal Valid Delay – Bused Signals		2	11	ns	2, 3
T_{VAL}(ptp)	CLK to Signal Valid Delay – Point-to-Point		2	12	ns	2, 3
T_{ON}	Float to Active Delay		2		ns	7
T_{OFF}	Active to Float Delay			28	ns	7
T_{SU}	Input Setup to CLK – Bused Signals		6		ns	3, 8
T_{SU}(ptp)	Input Setup to CLK – Point-to-Point		10,12		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset Active Time after Power Stable		1		ms	5
$T_{RST-CLK}$	Reset Active Time after CLK Stable		100		µs	5
$T_{RST-OFF}$	Reset Active to Output Float Delay			40	ns	5, 6, 7
T_{RHFA}	RST# High to First Configuration Access		2^{25}		clocks	9
T_{RHFF}	RST# High to First FRAME# Assertion		5		clocks	

Notes:

2. *For parts compliant to the 5V signaling environment:*

   Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance varies; however, results must be correlated to these specifications.

   Faster buffers can exhibit ring back when attached to a 50 pF lump load but should be of no consequence when the output buffers are in full compliance with slew rate and V/I curve specifications.

   For parts compliant to the 3.3V signaling environment:

   Minimum times are evaluated with the same load used for slew rate measurement; maximum times are evaluated with a parallel RC load of 25 Ohms and 10 pF.

3. *REQ# and GNT# are point-to-point signals and maintain different output valid delay and input setup times than bused signals. The setup for REQ# is 12. The setup for GNT# is 10. All other signals are bused.*
5. *CLK is stable when it meets the PCI CLK specifications. RST# is asserted and de-asserted asynchronously with respect to CLK.*
6. *All output drivers must be asynchronously floated when RST# is active.*
7. *For Active/Float timing measurement purposes, the Hi-Z or "off" state is defined as "total current delivered through the component ball is less than or equal to the leakage current specification."*
8. *Setup time applies only when the device is not driving the ball. Devices cannot drive and receive signals at the same time.*
9. *At 33 MHz, the device must be ready to accept a configuration access within 1s after RST# is high.*

17.6.2 PCI Bus 66-MHz AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = 0 to 70°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 17-6. PCI Bus 66-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		15	∞	ns	
T_{VAL}	CLK to Signal Valid Delay – Bused Signals		2	6	ns	3, 8
T_{VAL}(ptp)	CLK to Signal Valid Delay – Point-to-Point		2	6	ns	3, 8
T_{ON}	Float to Active Delay		2		ns	8, 9
T_{OFF}	Active to Float Delay			14	ns	9
T_{SU}	Input Setup to CLK – Bused Signals		3		ns	3, 10
T_{SU}(ptp)	Input Setup to CLK – Point-to-Point		5		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset Active Time after Power Stable		1		ms	5
$T_{RST-CLK}$	Reset Active Time after CLK Stable		100		µs	5
$T_{RST-OFF}$	Reset Active to Output Float Delay			40	ns	5, 6
T_{RHFA}	RST# High to First Configuration Access		2^{25}		clocks	9
T_{RHFF}	RST# High to First FRAME# Assertion		5		clocks	

Notes:

3. *REQ# and GNT# are point-to-point signals and maintain different input setup times than bused signals. The setup for REQ# and GNT# is 5 ns at 66 MHz. All other signals are bused.*
5. *When M66EN is asserted, CLK is stable when it meets the requirements in the PCI r3.0, Section 7.6.4.1. RST# is asserted and de-asserted asynchronously with respect to CLK. Refer to the PCI r3.0, Section 4.3.2, for further details.*
6. *All output drivers must be floated when RST# is active.*
8. *When M66EN is asserted, the minimum specification for Tval(min), Tval(ptp)(min), and Ton are reduced to 1 ns when a mechanism is provided to guarantee a minimum value of 2 ns when M66EN is de-asserted.*
9. *For Active/Float timing measurement purposes, the Hi-Z or "off" state is defined as "total current delivered through the component ball is less than or equal to the leakage current specification."*
10. *Setup time applies only when the device is not driving the signal. Devices cannot drive and receive signals at the same time. Refer to the PCI r3.0, Section 3.10, item 9, for further details.*

Chapter 18 Physical Specifications

18.1 PEX 8111 Package Specifications

The PEX 8111 is offered in two package types:

- 13-mm square 144-ball PBGA (Plastic BGA) package (refer to Table 18-1)
- 10-mm square 161-Ball FBGA (Fine-Pitch BGA) package (refer to Table 18-2)

Table 18-1. PEX 8111 144-Ball PBGA Package Specifications

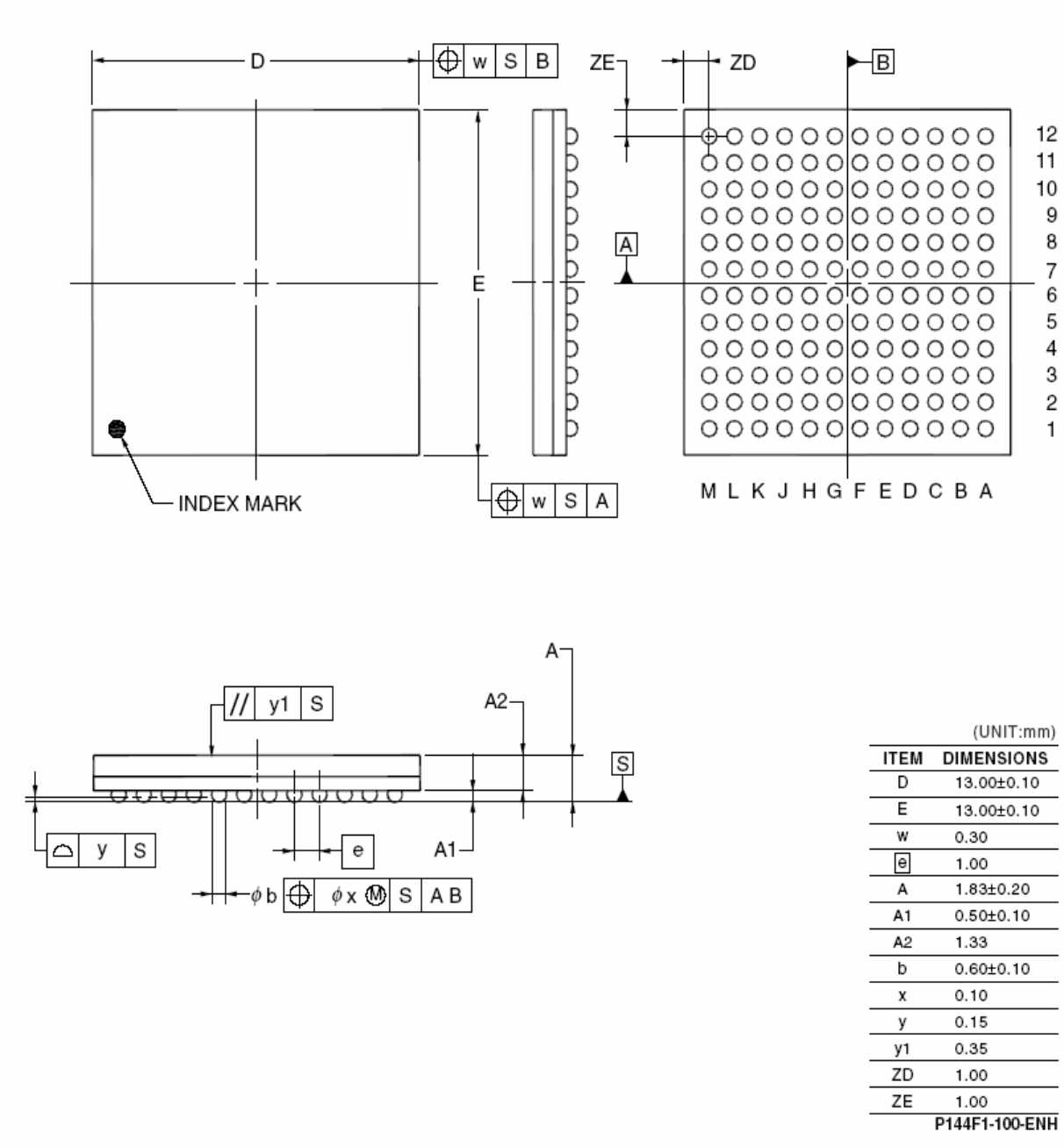
Parameter	Specification
Package Type	Plastic Ball Grid Array
Package Dimensions	13 x 13 mm (approximately 1.83 mm high)
Ball matrix pattern	12 x 12 mm
Ball pitch	1.00 mm
Ball diameter	0.60 ±0.15 mm
Ball spacing	0.40 mm

Table 18-2. PEX 8111 161-Ball FBGA Package Specifications

Parameter	Specification
Package Type	Fine-Pitch Ball Grid Array
Package Dimensions	10 x 10 mm (approximately 1.43 mm high)
Ball matrix pattern	9 x 9 mm
Ball pitch	0.65 mm
Ball diameter	0.60 ±0.15 mm
Ball spacing	0.40 mm

18.2 Mechanical Drawings

Figure 18-1. 144-Ball PBGA Mechanical Drawing

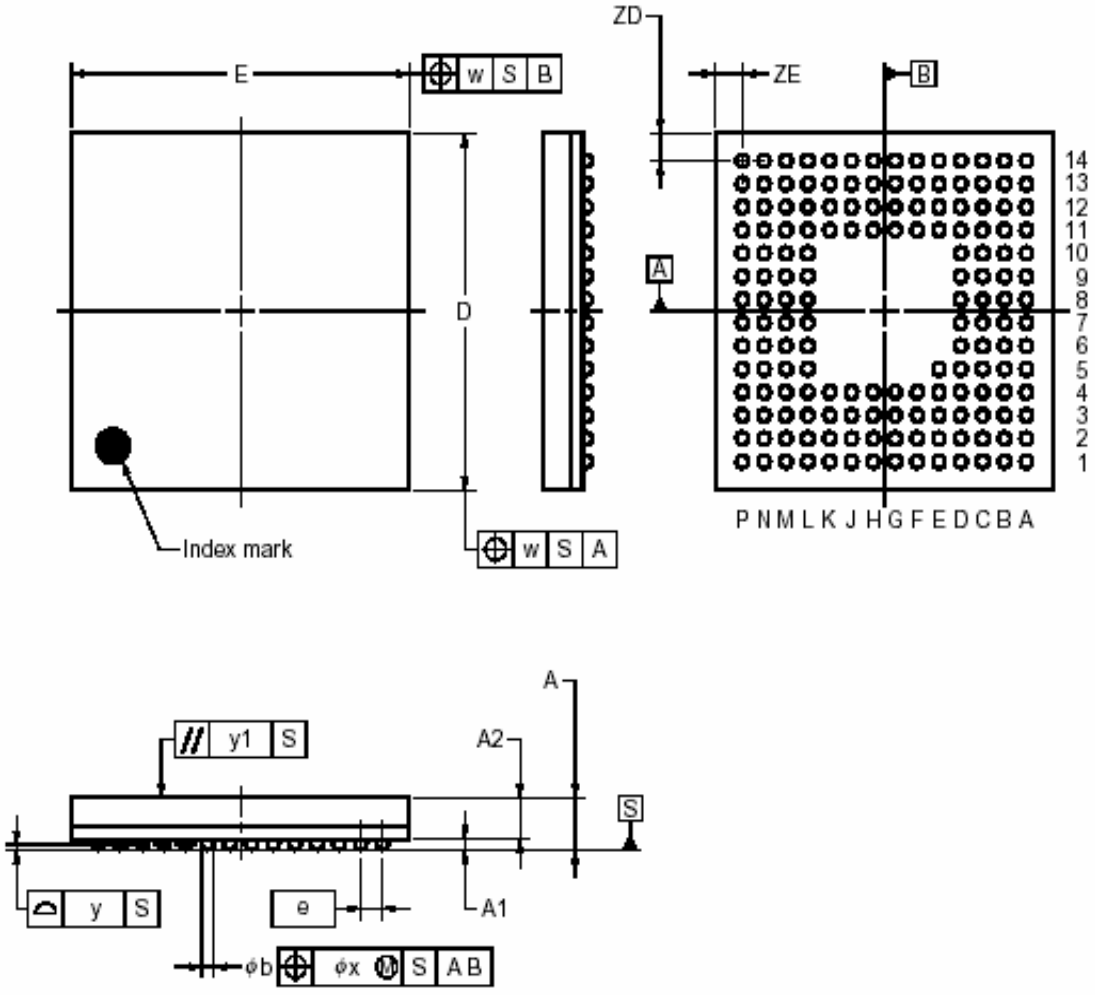


(UNIT:mm)

ITEM	DIMENSIONS
D	13.00±0.10
E	13.00±0.10
w	0.30
e	1.00
A	1.83±0.20
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P144F1-100-ENH

Figure 18-2. 161-Ball FBGA Mechanical Drawing

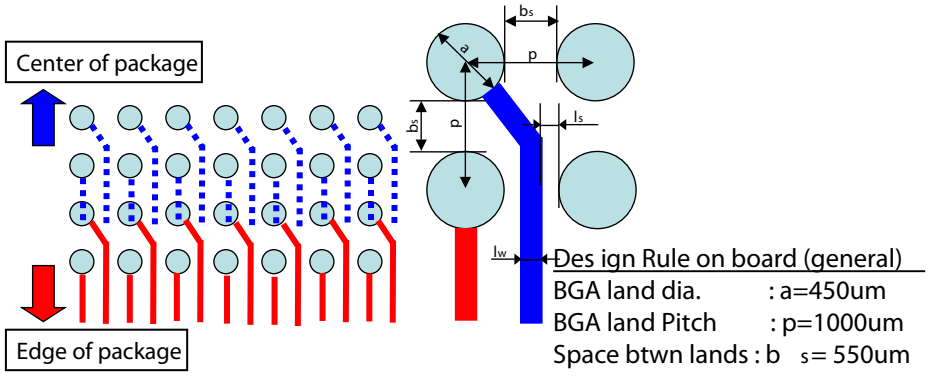


ITEM	MILLIMETERS
D	10.00±0.10
E	10.00±0.10
w	0.20
A	1.43±0.10
A1	0.30±0.05
A2	1.13
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.775
ZE	0.775

P161F1-65-DA1

18.3 PCB Layouts

Figure 18-3. 144-Ball PBGA PCB Layout

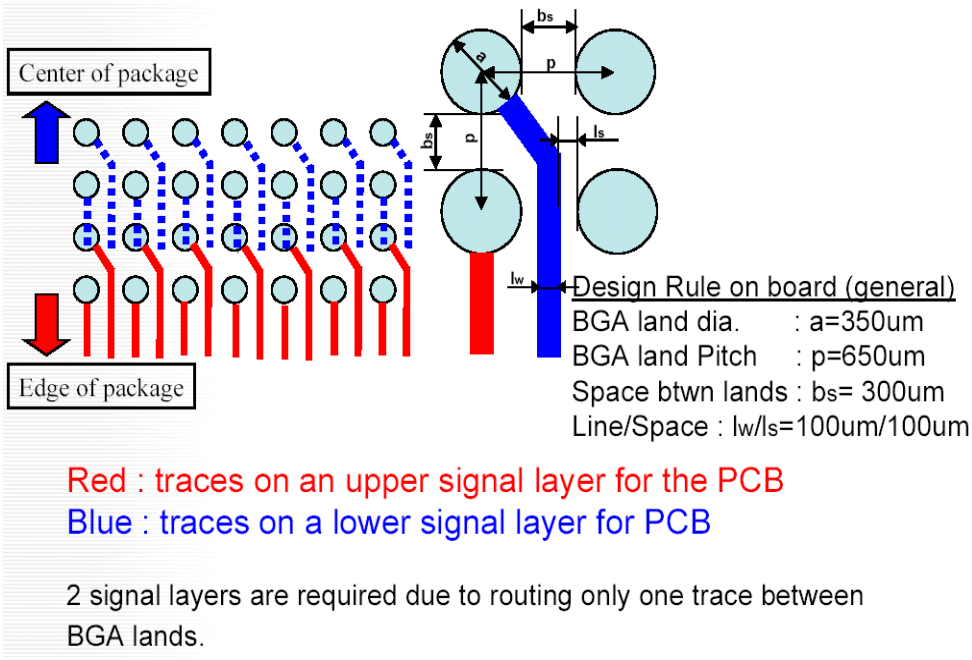


Red : traces on an upper signal layer for the PCB
Blue : traces on a lower signal layer for PCB

2 signal layers are required due to routing only one trace between BGA lands.

Note: *Refer to the PEX 8111 Quick Start Design Guide for the trace lengths and a detailed description of the PCI Express layout considerations.*

Figure 18-4. 161-Ball FBGA PCB Layout



Note: *Refer to the PEX 8111 Quick Start Design Guide for the trace lengths and a detailed description of the PCI Express layout considerations.*

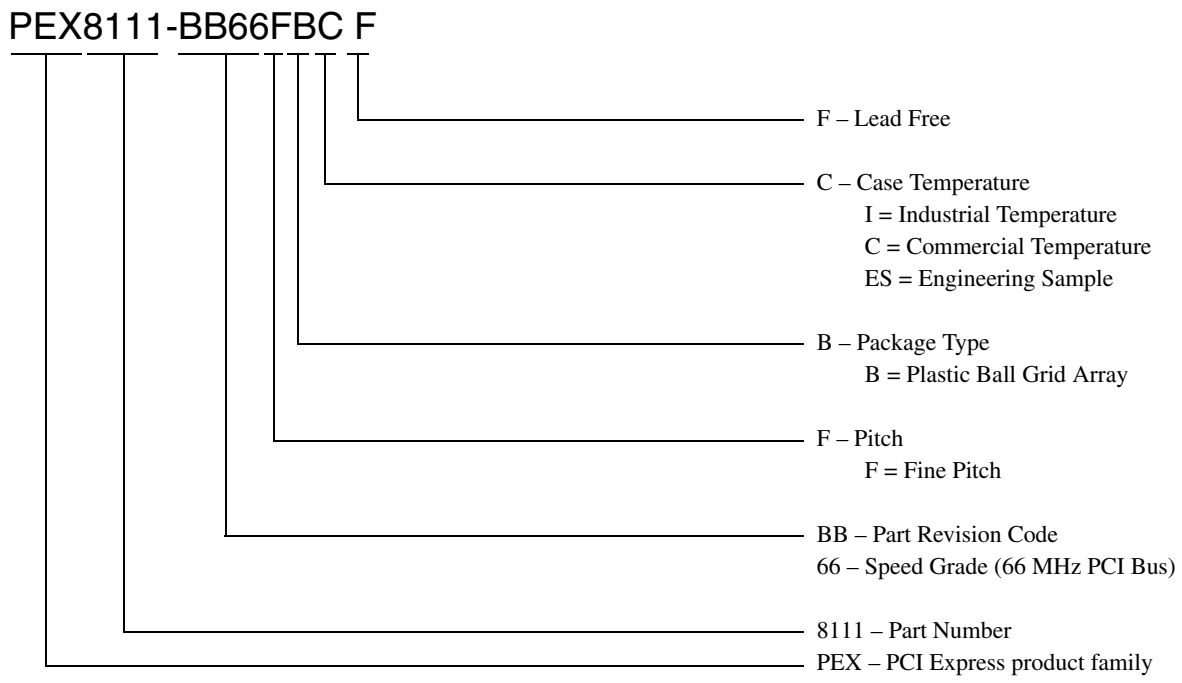
Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX sales representative for ordering information.

Table A-1. Product Ordering Information

Part Number	Description
PEX8111-BB66BC	PCI Express-to-PCI Bridge, Standard BGA Package (144-Ball, 13 x 13 mm)
PEX8111-BB66FBC	PCI Express-to-PCI Bridge, Fine-Pitch BGA Package (161-Ball, 10 x 10 mm)
PEX8111-BB66BC F	PCI Express-to-PCI Bridge, Standard BGA Package (144-Ball, 13 x 13 mm), Lead Free
PEX8111-BB66FBC F	PCI Express-to-PCI Bridge, Fine-Pitch BGA Package (161-Ball, 10 x 10 mm), Lead Free
PEX8111RDK-F	Forward Bridge Reference Design Kit
PEX8111RDK-R	Reverse Bridge Reference Design Kit



A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support/, or call 408 774-9060 or 800 759-3735.