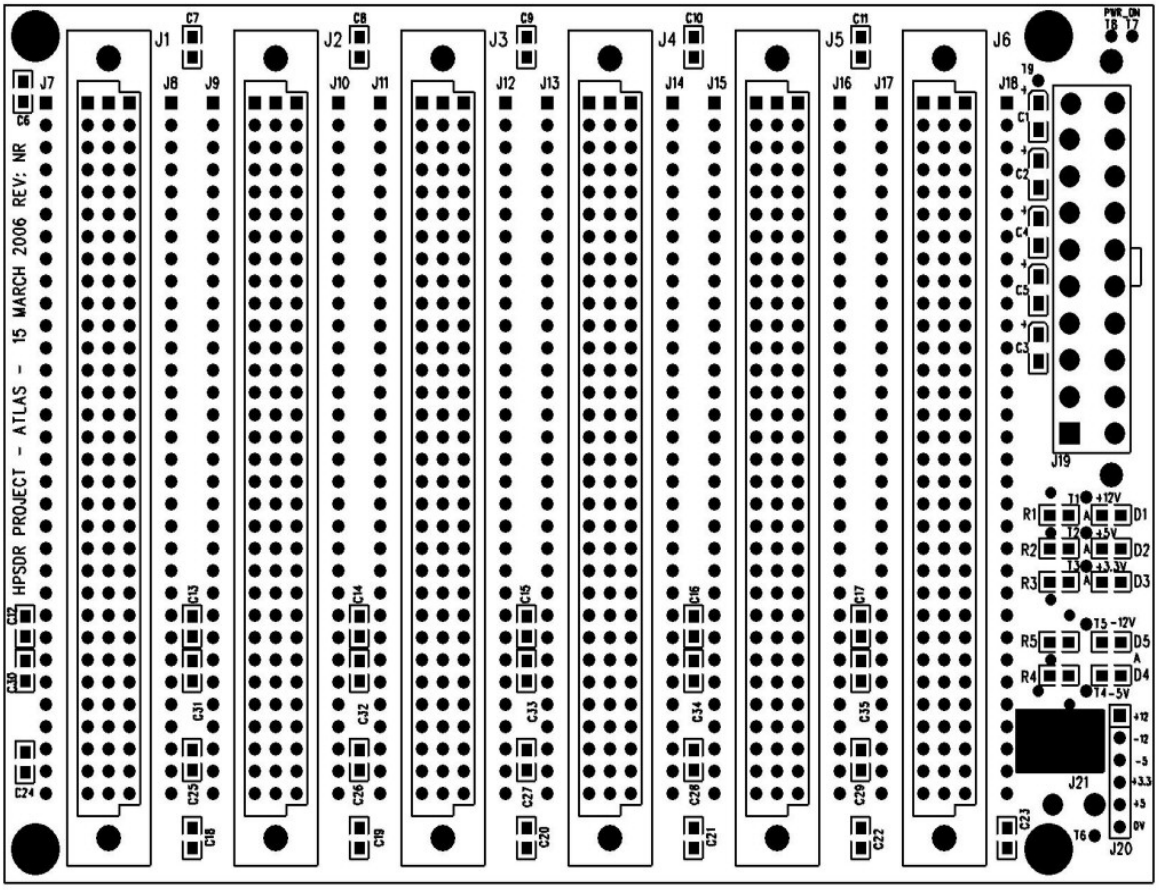
HIGH PERFORMANCE SOFTWARE DEFINED RADIO PROJECT

ATLAS BUS PHYSICAL DESCRIPTION



BOARD: 4 LAYER , 5.500" X 3.940", J1-J6 slots spaced at 0.800"

STACKUP:

- **GROUND PLANE (TOP LAYER)**
- **YBUS**
- **POWER PLANES**
- **XBUS (BOTTOM LAYER)**

POWER:

- **+12VDC, -12VDC, +5VDC, -5VDC, +3.3VDC**

STANDARD CONNECTORS:

- **96 pin DIN41612 (J1-J6) - BUS**
- **20 pin ATX PS (J15) - POWER**
- **PS LOAD (J21) - LOAD**
- **6 pin 0.100 SIP (J20) - POWER**
- **T1-T6 for external LEDs**
- **T7-T8 for remote ATX power on switch.**
- **T9 for ATX_PWR_OK.**

OPTIONAL CONNECTORS:

- **64 pin DIN41612 (using XBUS only)**
- **32x2 0.100 HEADER (using XBUS only)**

MISC FEATURES:

- **Each pin of the slot connectors can be isolated from the bus and then jumpered to another bus pin or signal. J7-J18 are provided for optional 32 pin SIP headers or wire-wrap pins. This allows re-routing the bus as needed.**
- **The user can decide to use the XBUS only by populating J1-J6 with DIN41612 64 pin "Type B" connectors or 32 pin dual 0.100 headers.**
- **J21 allows for an optional load resistor to be placed on the +5V bus when using an ATX power supply. The load resistor should be mounted to a proper heatsink.**
- **D1-D5 are SMT LEDs connected to the power bus (+12, -12, +5, -5, +3.3) through dropping resistors R1-R5.**
- **T1-T6 allow panel mounting of LEDs instead of SMT.**
- **All supplies bypassed.**

NOTES:

1. **The buses are separated into the XBUS and YBUS, with 24 lines each.**
2. **The XBUS is routed on the bottom layer of the PCB.**
3. **The YBUS is routed between the top ground plane layer and the power plane layer.**
4. **The XBUS is divided into the subgroups XA0-XA7, XB0-XB7, XC0-XC7, XDC.**
5. **The YBUS is divided into the subgroups YA0-YA7, YB0-YB7, YC0-YC7, YDC.**
6. **XDC and YDC are daisy chained between slots (see schematic).**
7. **The XBUS and YBUS subgroup divisions are for physical naming purposes only.**
8. **Since the YBUS is sandwiched in between two plane layers, it should be used to route medium speed signals or clocks between boards. While not intended to be a LVDS bus, it should be adequate for clock speeds up to 20-25 MHz.**
9. **J7, J9, J11, J13, J15, J17 are connected to the XBUS. J8, J10, J12, J14, J16, J18 are connected to the YBUS. On the bottom side of the Atlas board, J7-J18 are then connected by traces to J1-J6. This allows you to isolate pins on the J1-J6 connectors by cutting the connecting trace. See 9 below.**
10. **If an application requires re-routing signals on the bus, a possible solution is to populate the related pin on connectors J7-J18 with wire wrap pins. The signal then can be routed on top of the Atlas board with wire wrap wire. Since the top of the board is a ground plane, the wire wrap wire should lay directly on the board surface to minimize crosstalk/noise.**
11. **An alternative to wire wrap is to place jumper wires between the rerouted bus signals on the J7-J18 pads.**
12. **See physical bus pinout below.**

DIN41612 96 PIN

PIN	NAME	PIN	NAME	PIN	NAME
A1	**+12VDC**	**B1**	**+12VDC**	**C1**	**+12VDC**
A2	X0A0	B2	GND	C2	Y0A0
A3	X1A1	B3	GND	C3	Y1A1
A4	X2A2	B4	GND	C4	Y2A2
A5	X3A3	B5	GND	C5	Y3A3
A6	X4A4	B6	GND	C6	Y4A4
A7	X5A5	B7	GND	C7	Y5A5
A8	X6A6	B8	GND	C8	Y6A6
A9	X7A7	B9	GND	C9	Y7A7
A10	X8B0	B10	GND	C10	Y8B0
A11	X9B1	B11	GND	C11	Y9B1
A12	X10B2	B12	GND	C12	Y10B2
A13	X11B3	B13	GND	C13	Y11B3
A14	X12B4	B14	GND	C14	Y12B4
A15	X13B5	B15	GND	C15	Y13B5
A16	X14B6	B16	GND	C16	Y14B6
A17	X15B7	B17	GND	C17	Y15B7
A18	X16C0	B18	GND	C18	Y16C0
A19	X17C1	B19	GND	C19	Y17C1
A20	X18C2	B20	GND	C20	Y18C2
A21	X19C3	B21	GND	C21	Y19C3
A22	X20C4	B22	GND	C22	Y20C4
A23	X21C5	B23	GND	C23	Y21C5
A24	X22C6	B24	GND	C24	Y22C6
A25	X23C7	B25	GND	C25	Y23C7
A26	**-12VDC**	**B26**	**-12VDC**	**C26**	**-12VDC**
A27	X24DC	B27	GND	C27	Y24DC
A28	**-5VDC**	**B28**	**-5VDC**	**C28**	**-5VDC**
A29	X25DC	B29	GND	C29	Y25DC
A30	**+3.3VDC**	**B30**	**+3.3VDC**	**C30**	**+3.3VDC**
A31	X26DC	B31	GND	C31	Y26DC
A32	**+5VDC**	**B32**	**+5VDC**	**C32**	+5VDC