# TS5A3159A
# 1-Ω SPDT ANALOG SWITCH
# 5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

SCDS200–AUGUST 2005

## FEATURES

- **Isolation in Power-Down Mode, $V_+$ = 0**
- **Pin Compatible With TS5A3159**
- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (1 Ω)**
- **Control Inputs Are 5.5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

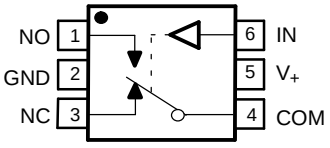
## APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio and Video Signal Routing**
- **Low-Voltage Data Acquisition Systems**
- **Communication Circuits**
- **Modems**
- **Hard Drives**
- **Computer Peripherals**
- **Wireless Terminals and Peripherals**

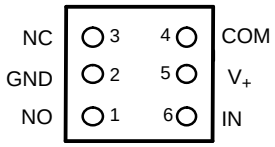
## DESCRIPTION

The TS5A3159A is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

**SOT-23 OR SC-70 PACKAGE (TOP VIEW)**




**YEA, YEP, YZA, OR YZP PACKAGE (BOTTOM VIEW)**




**FUNCTION TABLE**

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|---|---|---|
| L | ON | OFF |
| H | OFF | ON |

## SUMMARY OF CHARACTERISTICS

$V_+$ = 5 V, $T_A$ = 25°C

| | |
|---|---|
| Configuration | 2:1 Multiplexer/ Demultiplexer (1 × SPDT) |
| Number of channels | 1 |
| ON-state resistance ($r_{on}$) | 1.1 Ω |
| ON-state resistance match ($\Delta r_{on}$) | 0.1 Ω |
| ON-state resistance flatness ($r_{on(flat)}$) | 0.15 Ω |
| Turn-on/turn-off time ($t_{ON/tOFF}$) | 20 ns/15 ns |
| Break-before-make time ($t_{BBM}$) | 12 ns |
| Charge injection ($Q_C$) | –20 pC |
| Bandwidth (BW) | 100 MHz |
| OFF isolation ($O_{ISO}$) | –65 dB at 1 MHz |
| Crosstalk ($X_{TALK}$) | –66 dB at 1 MHz |
| Total harmonic distortion (THD) | 0.01% |
| Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$) | ±20 nA |
| Power-supply current ($I_+$) | 0.1 µA |
| Package options | 6-pin DBV, DCK, YEP, YZA, or YZP |

## ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(2) |
|---|---|---|---|---|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | | TS5A3159AYEPR | ___JJ_ |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Tape and reel | TS5A3159AYZPR | |
| | SOT (SOT-23) – DBV | Tape and reel | TS5A3159ADBVR | JAJ_ |
| | SOT (SC-70) – DCK(2) | Tape and reel | TS5A3159ADCKR | JJ_ |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, · = Pb-free).

## Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_+$ | Supply voltage range(3) | | –0.5 | 6.5 | V |
| $V_{NO}$<br>$V_{NC}$<br>$V_{COM}$ | Analog voltage range(3)(4)(5) | | –0.5 | $V_+$ + 0.5 | V |
| $I_K$ | Analog port diode current | $V_{NC}$, $V_{NO}$, $V_{COM}$ < 0 | –50 | | mA |
| $I_{NO}$,<br>$I_{NC}$,<br>$I_{COM}$ | On-state switch current | $V_{NO}$, $V_{NC}$, $V_{COM}$ = 0 to $V_+$ | –200 | 200 | mA |
| | On-state peak switch current(6) | | –400 | 400 | |
| $V_I$ | Digital input voltage range(3)(4) | | –0.5 | 6.5 | V |
| $I_{IK}$ | Digital input clamp current | $V_I$ < 0 | –50 | | mA |
| $I_+$ | Continuous current through $V_+$ | | | 100 | mA |
| $I_{GND}$ | Continuous current through GND | | –100 | 100 | mA |
| $\theta_{JA}$ | Package thermal impedance(7) | DBV package | | 165 | °C/W |
| | | DCK package | | 259 | |
| | | YEA/YEP/YZA/YZP package | | 123 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply(1)

$V_+$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Peak ON resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 0.8 | 1.1 | Ω |
| | | | | Full | | | | 1.5 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2.5 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 0.7 | 0.9 | Ω |
| | | | | Full | | | | 1.1 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2.5 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 0.05 | 0.1 | Ω |
| | | | | Full | | | | 0.1 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 0.15 | | Ω |
| | | $V_{NO}$ or $V_{NC}$ = 1 V, 1.5 V, 2.5 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | | | 0.1 | 0.25 | |
| | | | | Full | | | | 0.25 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = 1 V to 4.5 V, or $V_{NC}$ or $V_{NO}$ = 4.5 V, $V_{COM}$ = 1 V to 4.5 V, | Switch OFF, See Figure 14 | 25°C | 5.5 V | –20 | 2 | 20 | nA |
| | | | | Full | | –100 | | 100 | |
| | $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 5.5 V, $V_{COM}$ = 5.5 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.2 | 1 | µA |
| | | | | Full | | –20 | | 20 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = Open, or $V_{NC}$ or $V_{NO}$ = 4.5 V, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 5.5 V | –20 | 2 | 20 | nA |
| | | | | Full | | –100 | | 100 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 5.5 V, $V_{COM}$ = 5.5 V to 0, | Switch OFF, See Figure 14 | 25° | 0 V | –1 | 0.1 | 1 | µA |
| | | | | Full | | –20 | | 20 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 1 V, or $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 4.5 V, | Switch ON, See Figure 15 | 25°C | 5.5 V | –20 | 2 | 20 | nA |
| | | | | Full | | –100 | | 100 | |
| **Digital Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | 2.4 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | 0.8 | |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 5.5 V | –2 | | 2 | nA |
| | | | | Full | | –100 | | 100 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 5-V Supply(1) (Continued)

$V_+$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 5 V | 1 | 12 | 30 | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 35 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 5 V | 1 | 5 | 20 | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 30 | |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 18 | 25°C | 5 V | | 6 | | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 20 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 1 nF, See Figure 22 | 25°C | 5 V | | –20 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 5 V | | 18 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 5 V | | 55 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 5 V | | 55 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 5 V | | 2 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 19 | 25°C | 5 V | | 100 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch OFF, See Figure 20 | 25°C | 5 V | | –64 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch ON, See Figure 21 | 25°C | 5 V | | –64 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 200 Hz to 20 kHz, See Figure 23 | 25°C | 5 V | | 0.004 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 5.5 V | | 10 | 50 | nA |
| | | | | Full | | | | 500 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 3.3-V Supply[1]

$V_+$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Peak ON resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 1.3 | 1.6 | Ω |
| | | | | Full | | | | 2 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 1.2 | 1.5 | Ω |
| | | | | Full | | | | 1.7 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2 V, 0.8 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 0.1 | 0.15 | Ω |
| | | | | Full | | | | 0.15 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 0.2 | | Ω |
| | | $V_{NO}$ or $V_{NC}$ = 2 V, 0.8 V, $I_{COM}$ = –100 mA, | Switch ON, See Figure 13 | 25°C | | | 0.15 | 0.3 | |
| | | | | Full | | | | 0.3 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = 1 V to 3 V, or $V_{NC}$ or $V_{NO}$ = 3 V, $V_{COM}$ = 1 V to 3 V, | Switch OFF, See Figure 14 | 25°C | 3.6 V | –20 | 2 | 20 | nA |
| | | | | Full | | –50 | | 50 | |
| | $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 3.6 V, $V_{COM}$ = 3.6 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.2 | 1 | µA |
| | | | | Full | | –15 | | 15 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = Open, or $V_{NC}$ or $V_{NO}$ = 3 V, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 3.6 V | –10 | 2 | 10 | nA |
| | | | | Full | | –20 | | 20 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 3.6 V to 0, $V_{COM}$ = 0 to 3.6 V, | Switch OFF, See Figure 14 | 25° | 0 V | –1 | 0.2 | 1 | µA |
| | | | | Full | | –15 | | 15 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 1 V, or $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 3 V, | Switch ON, See Figure 15 | 25°C | 3.6 V | –10 | 2 | 10 | nA |
| | | | | Full | | –20 | | 20 | |
| **Digital Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | 2.4 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | 0.8 | |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 3.6 V | –2 | | 2 | nA |
| | | | | Full | | –100 | | 100 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 3.3-V Supply[1] (Continued)

$V_+$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 3.3 V | 5 | 16 | 35 | ns |
| | | | | Full | 3 V to 3.6 V | 3 | | 50 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 3.3 V | 1 | 9 | 20 | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 30 | |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 18 | 25°C | 3.3 V | | 9 | | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 40 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 1 nF, See Figure 22 | 25°C | 3.3 V | | –11 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 3.3 V | | 18 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 3.3 V | | 55 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 3.3 V | | 55 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 3.3 V | | 2 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 19 | 25°C | 3.3 V | | 100 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch OFF, See Figure 20 | 25°C | 3.3 V | | –64 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch ON, See Figure 21 | 25°C | 3.3 V | | –64 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 23 | 25°C | 3.3 V | | 0.01 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 3.6 V | | 10 | 25 | nA |
| | | | | Full | | | | 100 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 2.5-V Supply(1)

$V_+$ = 2.3 V to 2.7, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Peak ON resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 1.8 | 2.5 | Ω |
| | | | | Full | | | | 2.7 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.8 V, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 1.5 | 2 | Ω |
| | | | | Full | | | | 2.4 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.8 V, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 0.15 | 0.2 | Ω |
| | | | | Full | | | | 0.2 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 0.6 | | Ω |
| | | $V_{NO}$ or $V_{NC}$ = 0.8 V, 1.8 V, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | | | 0.6 | 1 | |
| | | | | Full | | | | 1 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0.5 V, $V_{COM}$ = 0.5 V to 2.3 V, or $V_{NC}$ or $V_{NO}$ = 2.3 V, $V_{COM}$ = 0.5 V to 2.3 V, | Switch OFF, See Figure 14 | 25°C | 2.7 V | –20 | 2 | 20 | nA |
| | | | | Full | | –50 | | 50 | |
| | $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 3.6 V, $V_{COM}$ = 3.6 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.1 | 1 | µA |
| | | | | Full | | –10 | | 10 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0.5 V, $V_{COM}$ = Open, or $V_{NC}$ or $V_{NO}$ = 2.2 V, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 2.7 V | –10 | 2 | 10 | nA |
| | | | | Full | | –20 | | 20 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 2.7 V to 0, $V_{COM}$ = 0 to 2.7 V, | Switch OFF, See Figure 14 | 25° | 0 V | –1 | 0.1 | 10 | µA |
| | | | | Full | | –10 | | 20 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0.5 V, or $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 2.2 V, | Switch ON, See Figure 15 | 25°C | 2.7 V | –10 | 2 | 10 | nA |
| | | | | Full | | –20 | | 20 | |
| **Digital Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | 1.8 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | 0.6 | |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 2.7 V | –2 | | 2 | nA |
| | | | | Full | | 20 | | 20 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 2.5-V Supply[1] (Continued)

$V_+$ = 2.3 V to 2.7, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 2.5 V | 5 | 22 | 40 | ns |
| | | | | Full | 2.3 V to 2.7 V | 5 | | 50 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 2.5 V | 2 | 6 | 35 | ns |
| | | | | Full | 2.3 V to 2.7 V | 2 | | 50 | |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 18 | 25°C | 2.5 V | 2 | 13 | 35 | ns |
| | | | | Full | 2.3 V to 2.7 V | 2 | | 45 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 1 nF, See Figure 22 | 25°C | 2.5 V | | –7 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 2.5 V | | 18 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 2.5 V | | 55 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 2.5 V | | 55 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 2.5 V | | 2 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 19 | 25°C | 2.5 V | | 100 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch OFF, See Figure 20 | 25°C | 2.5 V | | –64 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch ON, See Figure 21 | 25°C | 2.5 V | | –64 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 23 | 25°C | 2.5 V | | 0.02 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 2.7 V | | 10 | 20 | nA |
| | | | | Full | | | | 50 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 1.8-V Supply[1]

$V_+$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Peak ON resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –2 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 5 | | Ω |
| | | | | Full | | | | 15 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.5 V, $I_{COM}$ = –2 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 2 | 2.5 | Ω |
| | | | | Full | | | | 3.5 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.5 V, $I_{COM}$ = –2 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 0.15 | 0.4 | Ω |
| | | | | Full | | | | 0.4 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 5 | | Ω |
| | | $V_{NO}$ or $V_{NC}$ = 0.6 V, 1.5 V, $I_{COM}$ = –2 mA, | Switch ON, See Figure 13 | 25°C | | | 4.5 | | |
| | | | | Full | | | | | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0.3 V, $V_{COM}$ = 0.3 V to 1.65 V, or $V_{NC}$ or $V_{NO}$ = 1.65 V, $V_{COM}$ = 0.3 V to 1.65 V, | Switch OFF, See Figure 14 | 25°C | 1.95 V | –5 | 2 | 5 | nA |
| | | | | Full | | –20 | | 20 | |
| | $I_{NC(PWROFF)}$ $I_{NO(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 1.95 V, $V_{COM}$ = 1.95 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 V | –1 | 0.1 | 1 | µA |
| | | | | Full | | –5 | | 5 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0.3 V, $V_{COM}$ = Open, or $V_{NC}$ or $V_{NO}$ = 1.65 V, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 1.95 V | –5 | 2 | 5 | nA |
| | | | | Full | | –20 | | 20 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 1.95 V to 0, $V_{COM}$ = 0 to 1.95 V, | Switch OFF, See Figure 14 | 25° | 0 V | –1 | 0.1 | 7 | µA |
| | | | | Full | | –5 | | 5 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0.3 V, or $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 1.65 V, | Switch ON, See Figure 15 | 25°C | 1.95 V | –5 | 2 | 5 | nA |
| | | | | Full | | –20 | | 20 | |
| **Digital Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | 1.5 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | 0.6 | |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 1.95 V | –2 | | 2 | nA |
| | | | | Full | | 20 | | 20 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 1.8-V Supply(1) (Continued)

$V_+$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 1.8 V | 10 | 35 | 70 | ns |
| | | | | Full | 1.65 V to 1.95 V | 10 | | 75 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 17 | 25°C | 1.8 V | 2 | 15 | 40 | ns |
| | | | | Full | 1.65 V to 1.95 V | 2 | | 50 | |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$, $R_L$ = 50 Ω, | $C_L$ = 35 pF, See Figure 18 | 25°C | 1.8 V | | 22 | | ns |
| | | | | Full | 1.65 V to 1.95 V | 2 | | 70 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 1 nF, See Figure 22 | 25°C | 1.8 V | | –4 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 1.8 V | | 18 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 1.8 V | | 55 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 1.8 V | | 55 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 1.8 V | | 2 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 19 | 25°C | 1.8 V | | 105 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch OFF, See Figure 20 | 25°C | 1.8 V | | 64 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 1 MHz, | Switch ON, See Figure 21 | 25°C | 1.8 V | | 64 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 23 | 25°C | 1.8 V | | 0.06 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 1.95 V | | 5 | 15 | μA |
| | | | | Full | | | | 50 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## TYPICAL PERFORMANCE

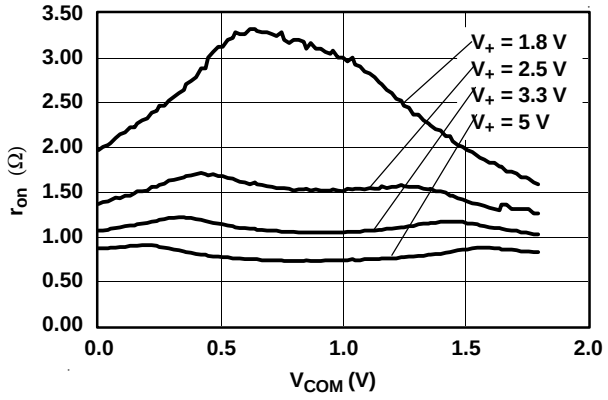



Figure 1. $r_{on}$ vs $V_{COM}$

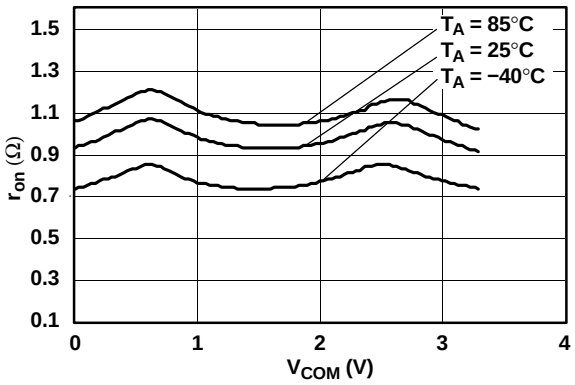



Figure 2. $r_{on}$ vs $V_{COM}$ ($V_+$ = 3.3 V)

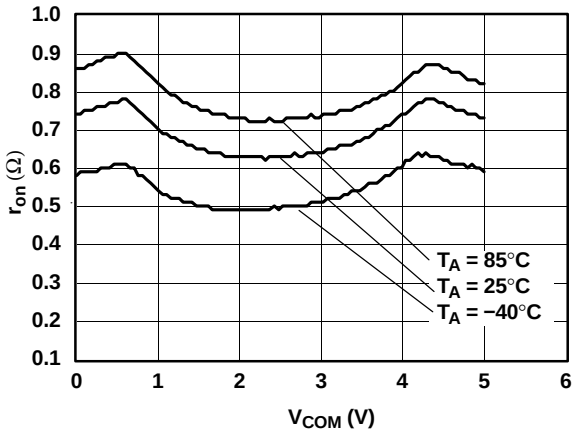



Figure 3. $r_{on}$ vs $V_{COM}$ ($V_+$ = 5 V)

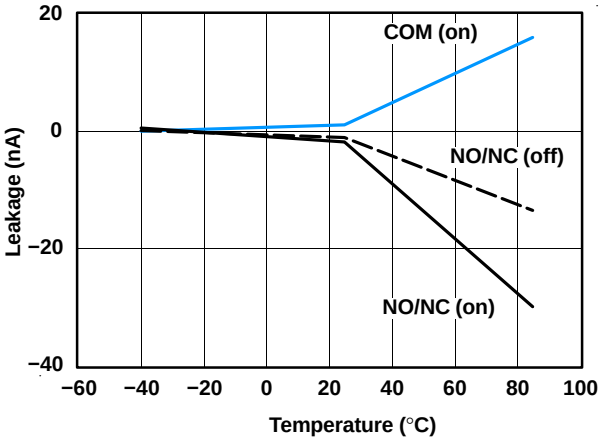



Figure 4. Leakage Current vs Temperature ($V_+$ = 3.3 V)

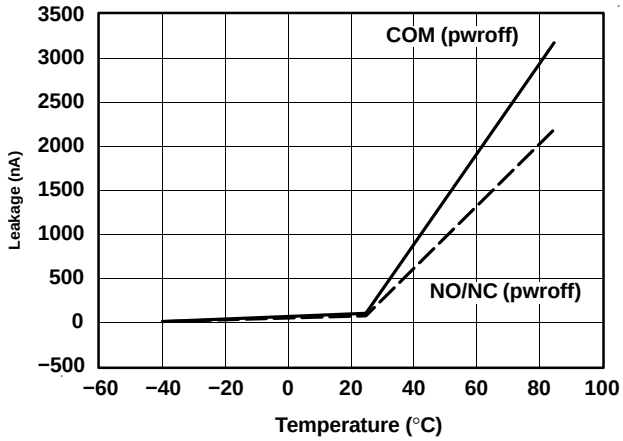



Figure 5. Leakage Current vs Temperature ($V_+$ = 5 V)

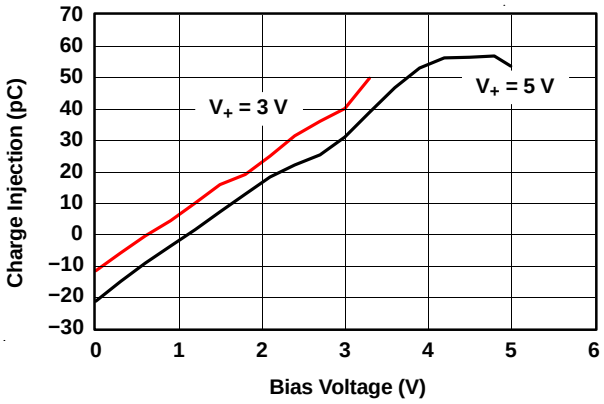



Figure 6. Charge Injection ($Q_C$) vs $V_{COM}$

## TYPICAL PERFORMANCE (continued)

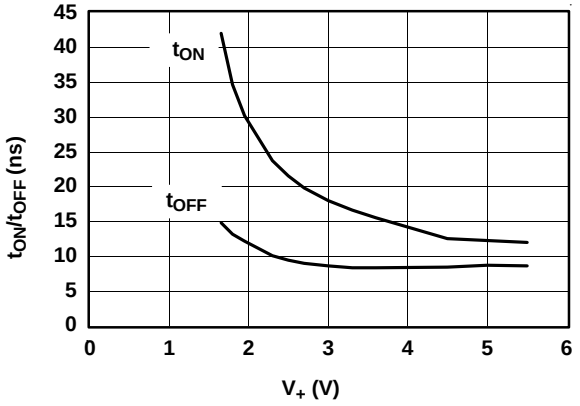



Figure 7. $t_{ON}$ and $t_{OFF}$ vs Supply Voltage

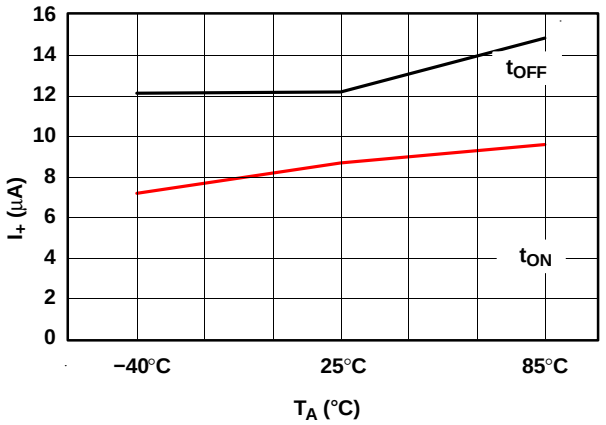



Figure 8. $t_{ON}$ and $t_{OFF}$ vs Temperature

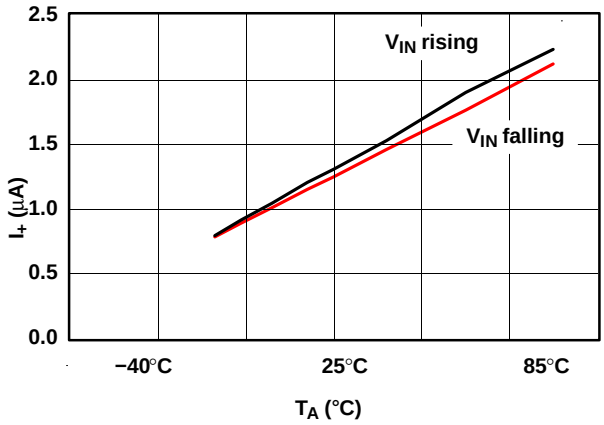



Figure 9. $t_{ON}$ and $t_{OFF}$ vs Temperature

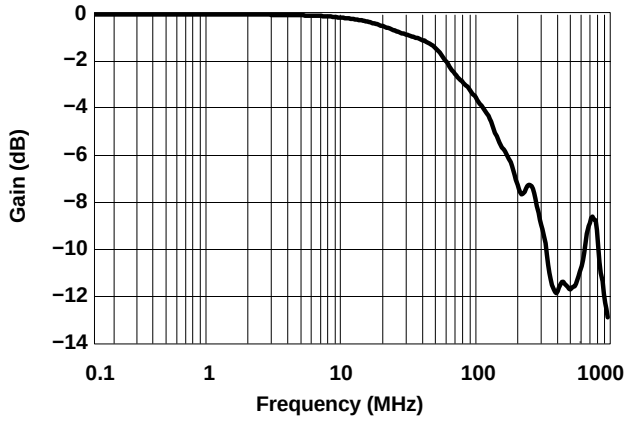



Figure 10. Bandwidth ($V_+$ = 5 V)

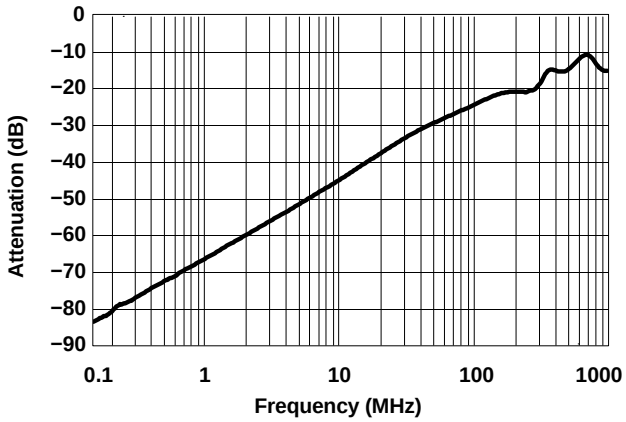



Figure 11. OFF Isolation vs Frequency

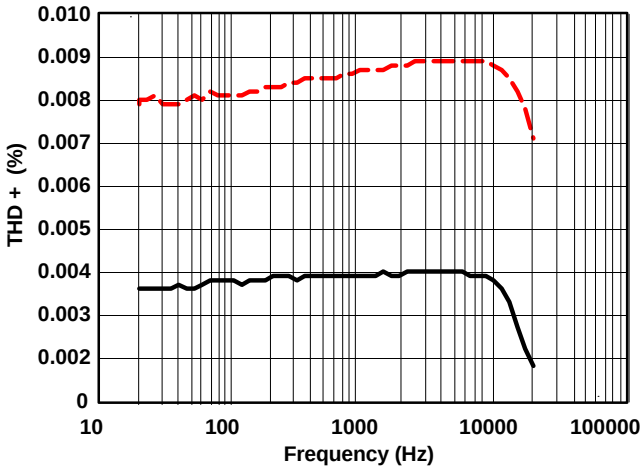



Figure 12. Total Harmonic Distortion vs Frequency ($V_+$ = 5 V)

## TYPICAL PERFORMANCE (continued)

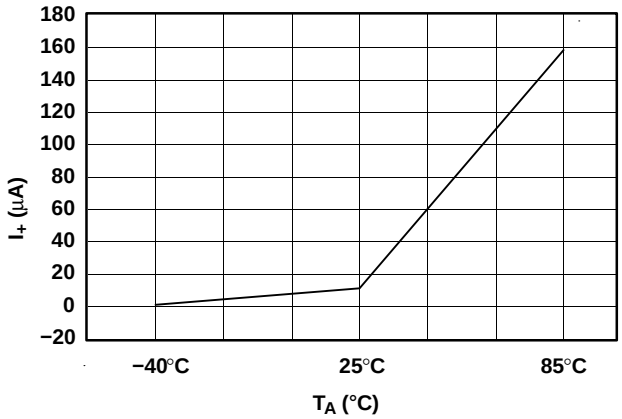



**Figure 13. Power-Supply Current vs Temperature ($V_+$ = 5 V)**

## PIN DESCRIPTION

| PIN NUMBER | NAME | DESCRIPTION |
|---|---|---|
| 1 | NO | Normally-open |
| 2 | GND | Digital ground |
| 3 | NC | Normally closed |
| 4 | COM | Common |
| 5 | $V_+$ | Power supply |
| 6 | IN | Digital control pin to connect COM to NO |

## PARAMETER DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| $V_{COM}$ | Voltage at COM |
| $V_{NC}$ | Voltage at NC |
| $V_{NO}$ | Voltage at NO |
| $r_{on}$ | Resistance between COM and NC or COM and NO ports when the channel is ON |
| $r_{peak}$ | Peak ON-state resistance over a specified voltage range |
| $\Delta r_{on}$ | Difference of $r_{on}$ between channels |
| $r_{on(flat)}$ | Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions |
| $I_{NC(OFF)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions |
| $I_{NC(PWROFF)}$ | Leakage current measured at the NC port during the power-down condition, $V_+ = 0$ |
| $I_{NO(OFF)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions |
| $I_{NO(PWROFF)}$ | Leakage current measured at the NO port during the power-down condition, $V_+ = 0$ |
| $I_{NC(ON)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open |
| $I_{NO(ON)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open |
| $I_{COM(ON)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open |
| $I_{COM(PWROFF)}$ | Leakage current measured at the COM port during the power-down condition, $V_+ = 0$ |
| $V_{IH}$ | Minimum input voltage for logic high for the control input (IN) |
| $V_{IL}$ | Maximum input voltage for logic low for the control input (IN) |
| $V_I$ | Voltage at (IN) |
| $I_{IH}$, $I_{IL}$ | Leakage current measured at (IN) |
| $t_{ON}$ | Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning ON. |
| $t_{OFF}$ | Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning OFF. |
| $t_{BBM}$ | Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state. |
| $Q_C$ | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, $C_L$ is the load capacitance and $\Delta$VO is the change in analog output voltage. |
| $C_{NC(OFF)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF |
| $C_{NO(OFF)}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is OFF |
| $C_{NC(ON)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON |
| $C_{NO(ON)}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is ON |
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON |
| $C_{IN}$ | Capacitance of (IN) |
| OISO | OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. |
| $X_{TALK}$ | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain. |
| THD | Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio or root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic. |
| $I_+$ | Static power supply current with the control (IN) pin at $V_+$ or GND |

## PARAMETER MEASUREMENT INFORMATION

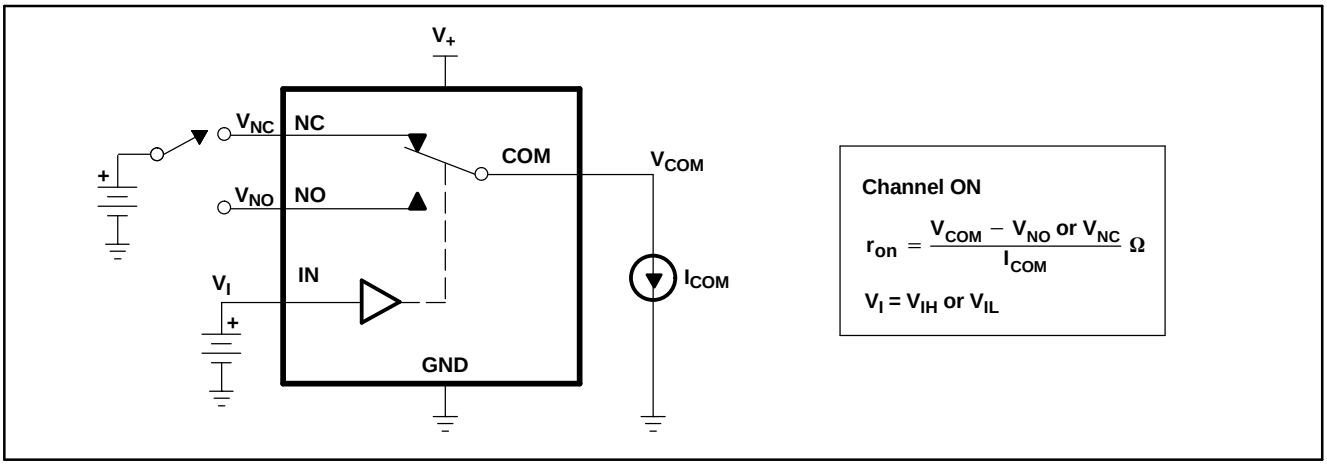



**Figure 14. ON-State Resistance ($r_{on}$)**

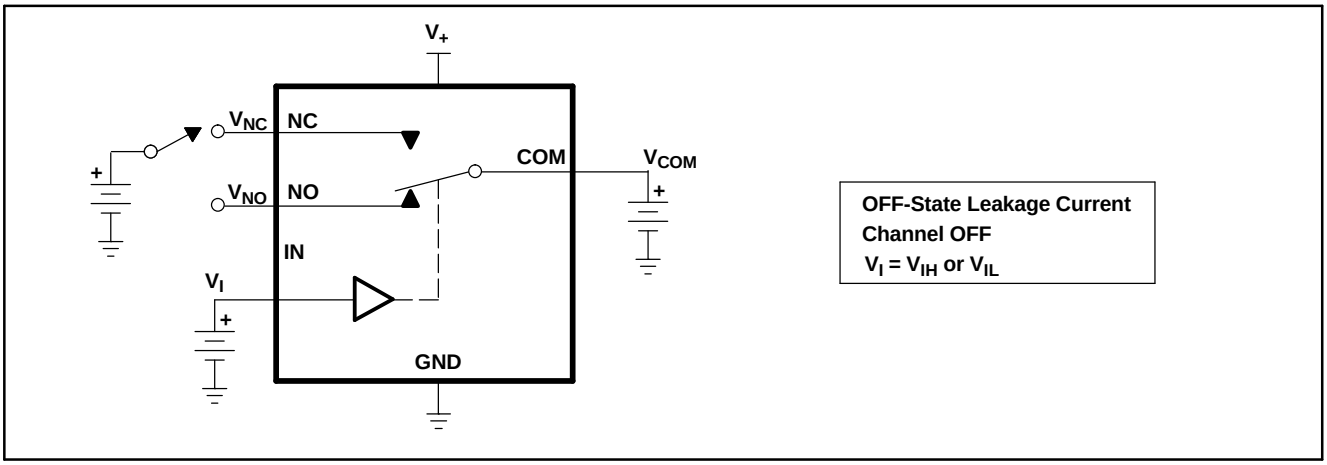



**Figure 15. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)**

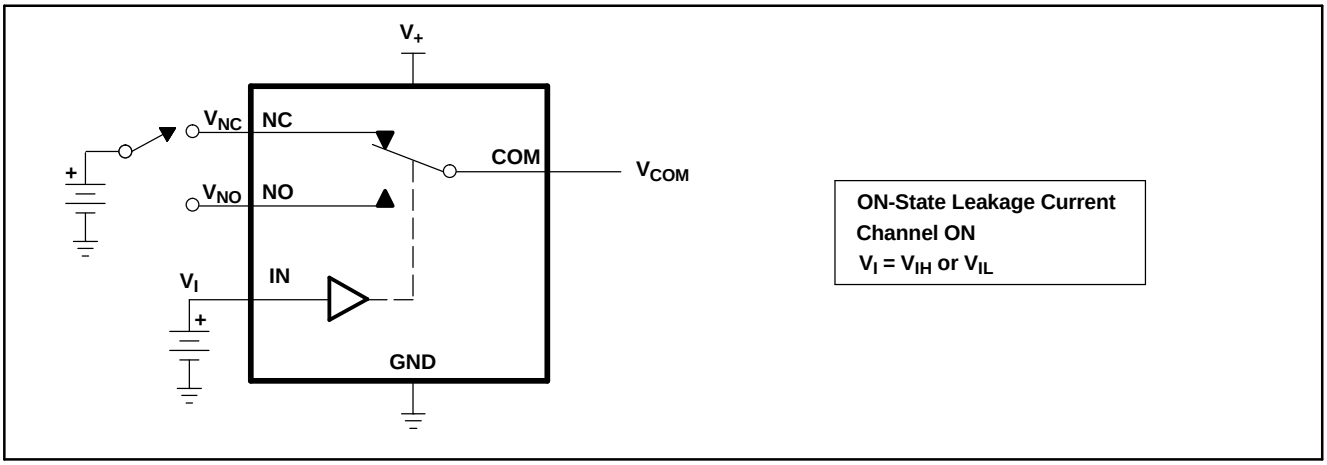



**Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)**

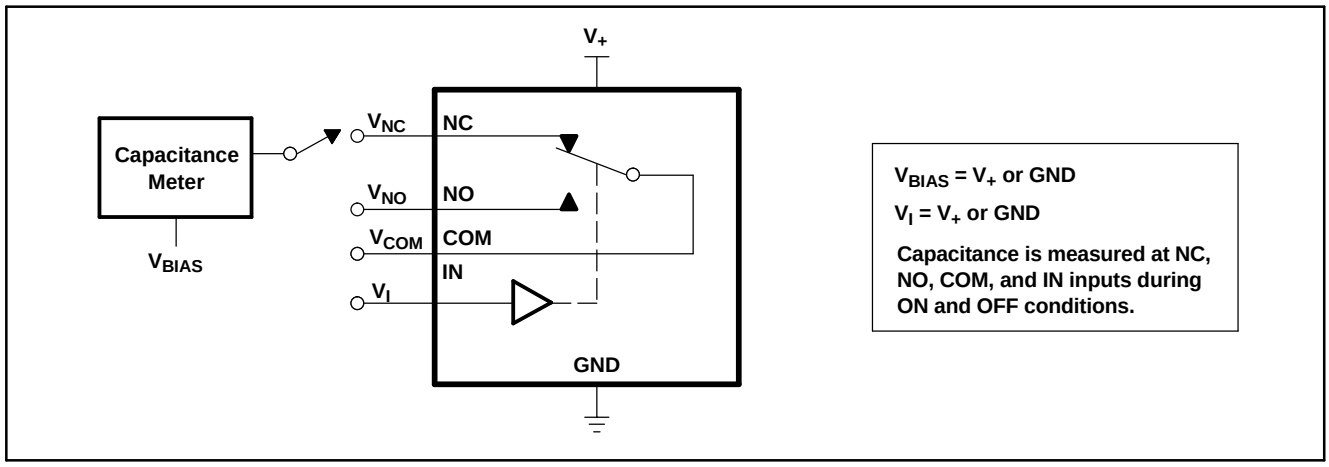
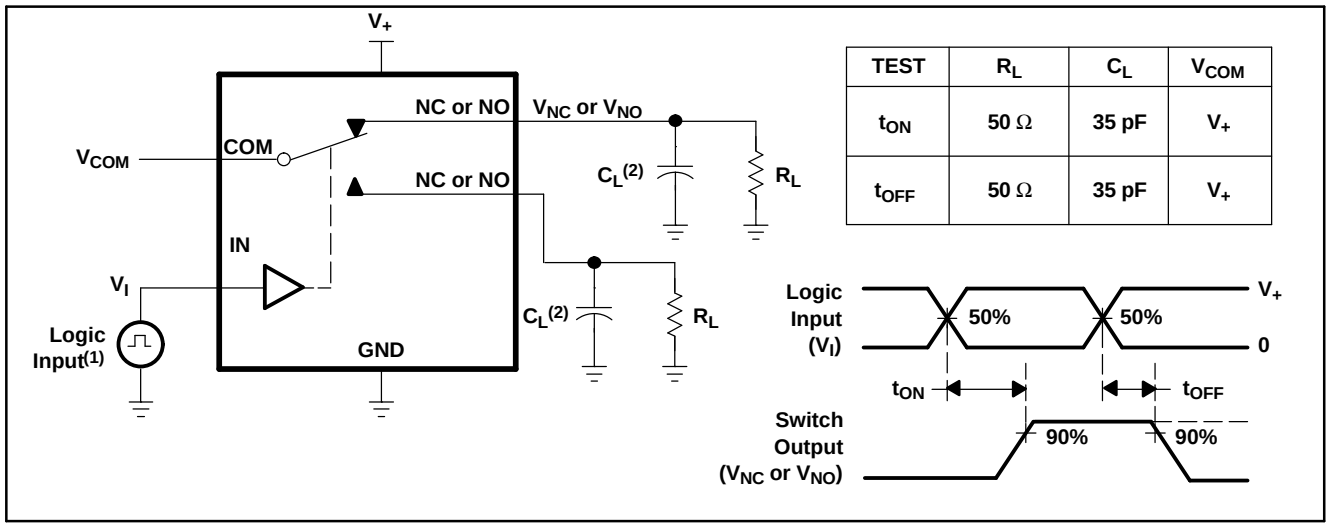



**Figure 17. Capacitance ($C_I$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)**

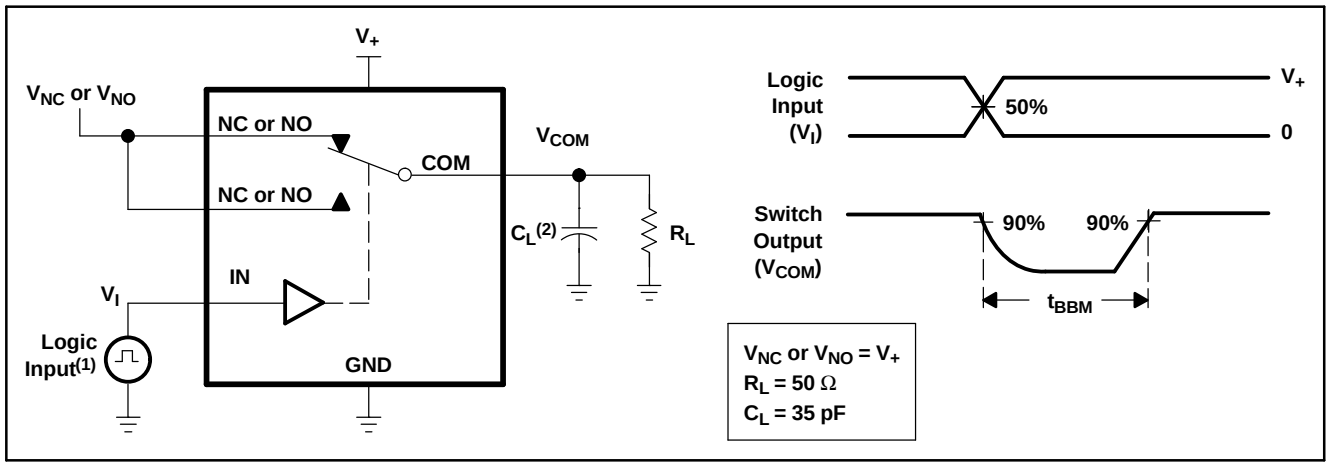



| TEST | $R_L$ | $C_L$ | $V_{COM}$ |
|---|---|---|---|
| $t_{ON}$ | 50 Ω | 35 pF | $V_+$ |
| $t_{OFF}$ | 50 Ω | 35 pF | $V_+$ |

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 18. Turn-On ($t_{ON}$) and Turn-Off Time ($t_{OFF}$)**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 19. Break-Before-Make Time ($t_{BBM}$)**

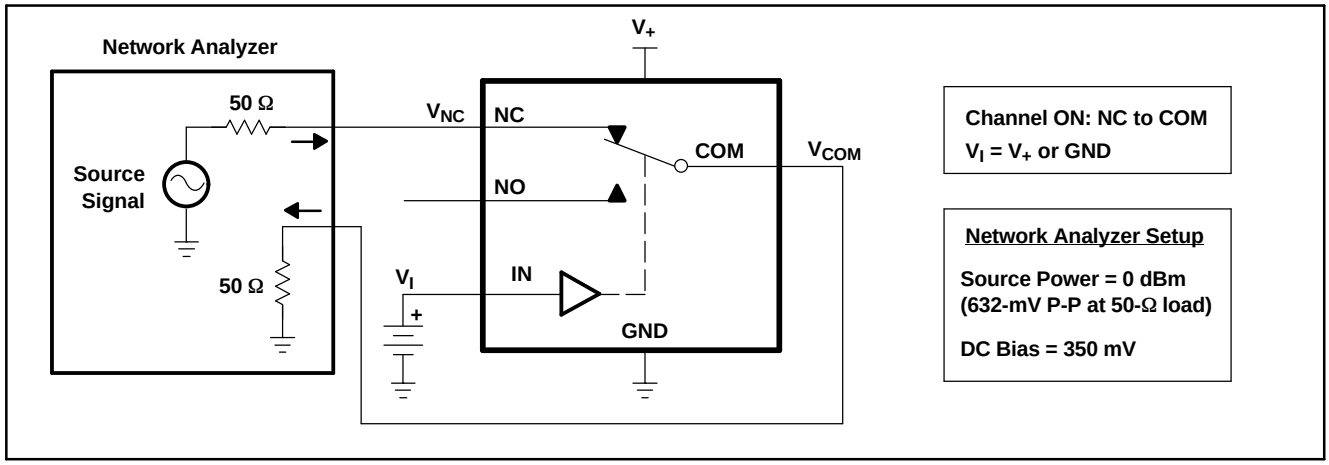



**Figure 20. Bandwidth (BW)**

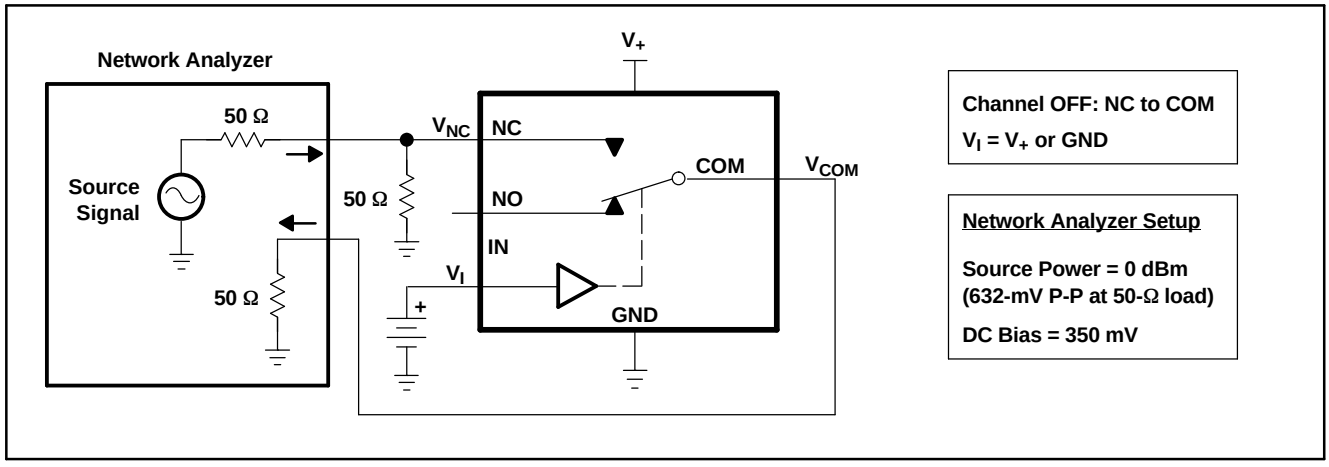



**Figure 21. OFF Isolation (OISO)**

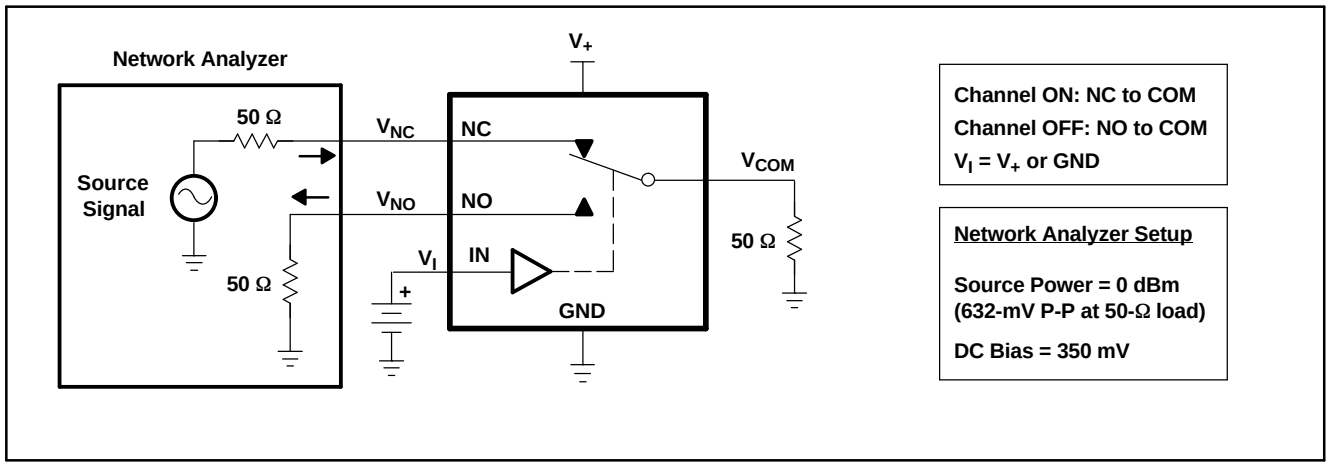
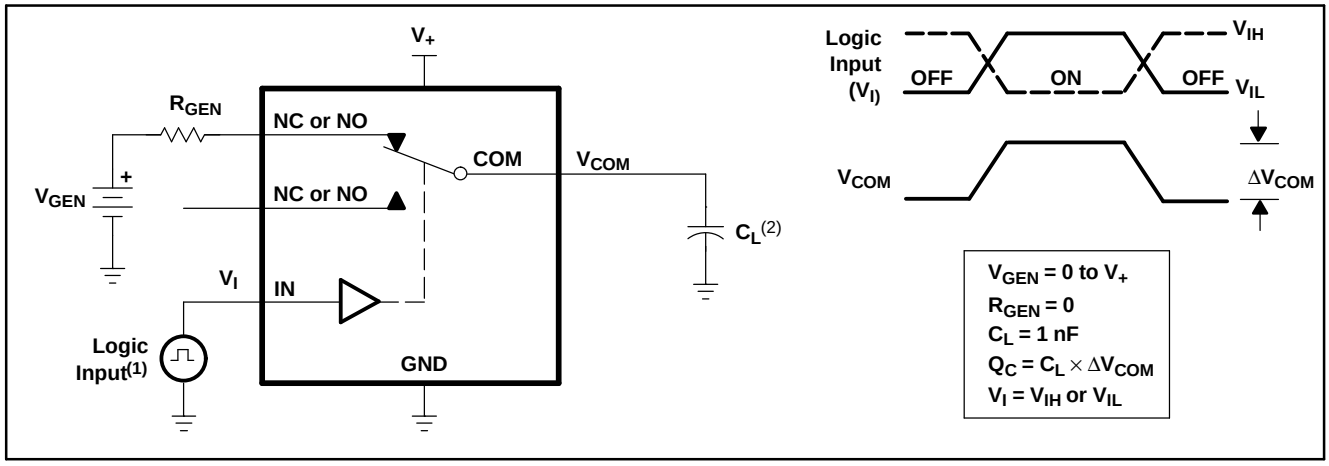


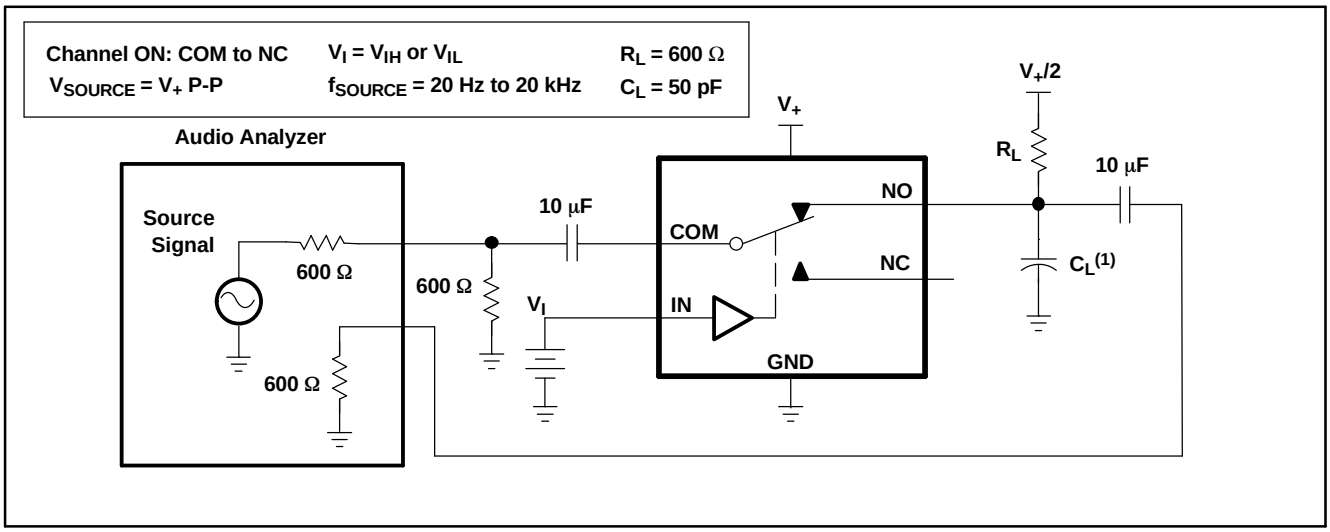

**Figure 22. Crosstalk ($X_{TALK}$)**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 23. Charge Injection ($Q_C$)**




A. $C_L$ includes probe and jig capacitance.

**Figure 24. Total Harmonic Distortion (THD)**

## PACKAGING INFORMATION

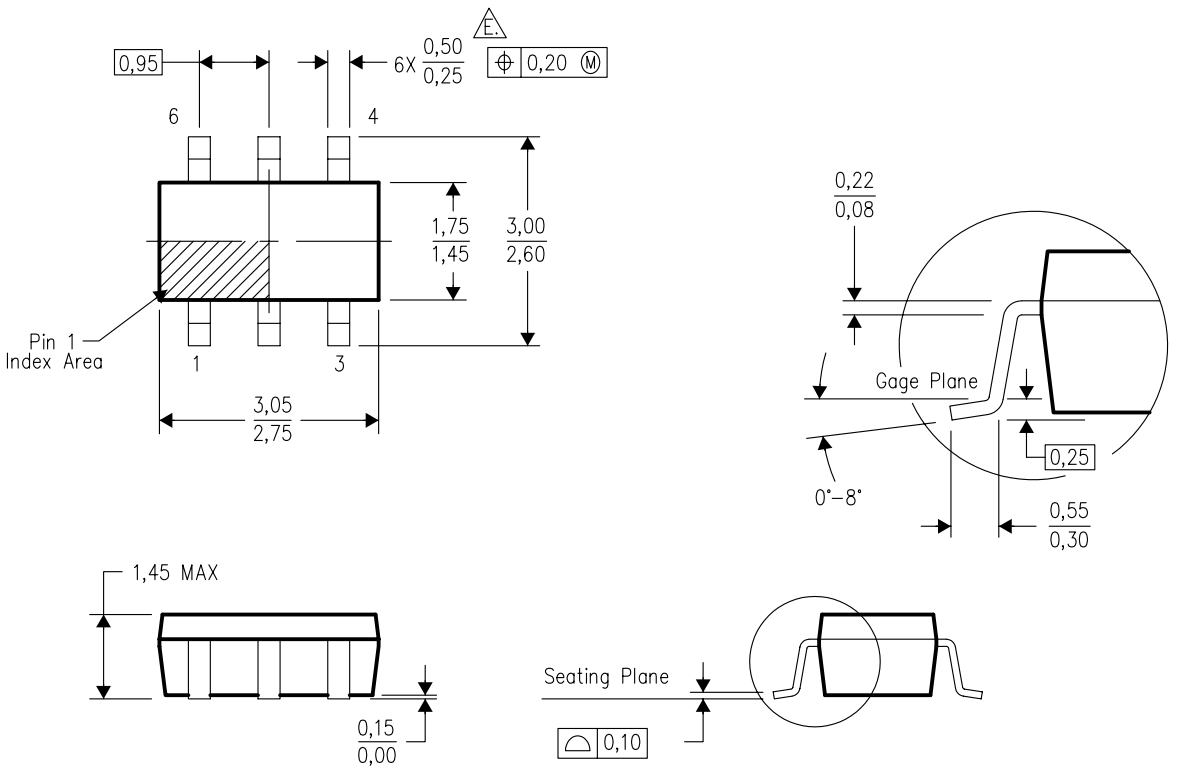
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TS5A3159ADBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADBVRE4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADBVTE4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159ADCKTE4 | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS5A3159AYZPR | ACTIVE | WCSP | YZP | 6 | 3000 | Pb-Free (RoHS) | SNAGCU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

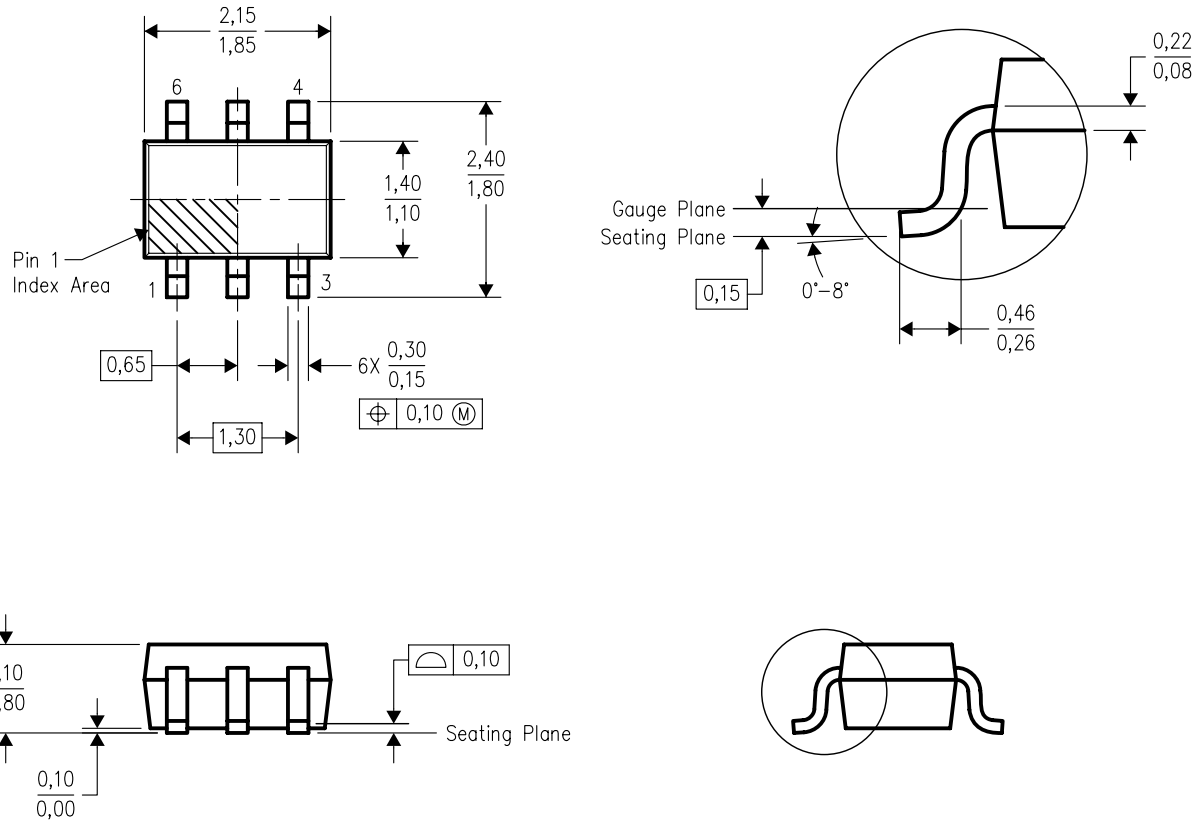
## DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

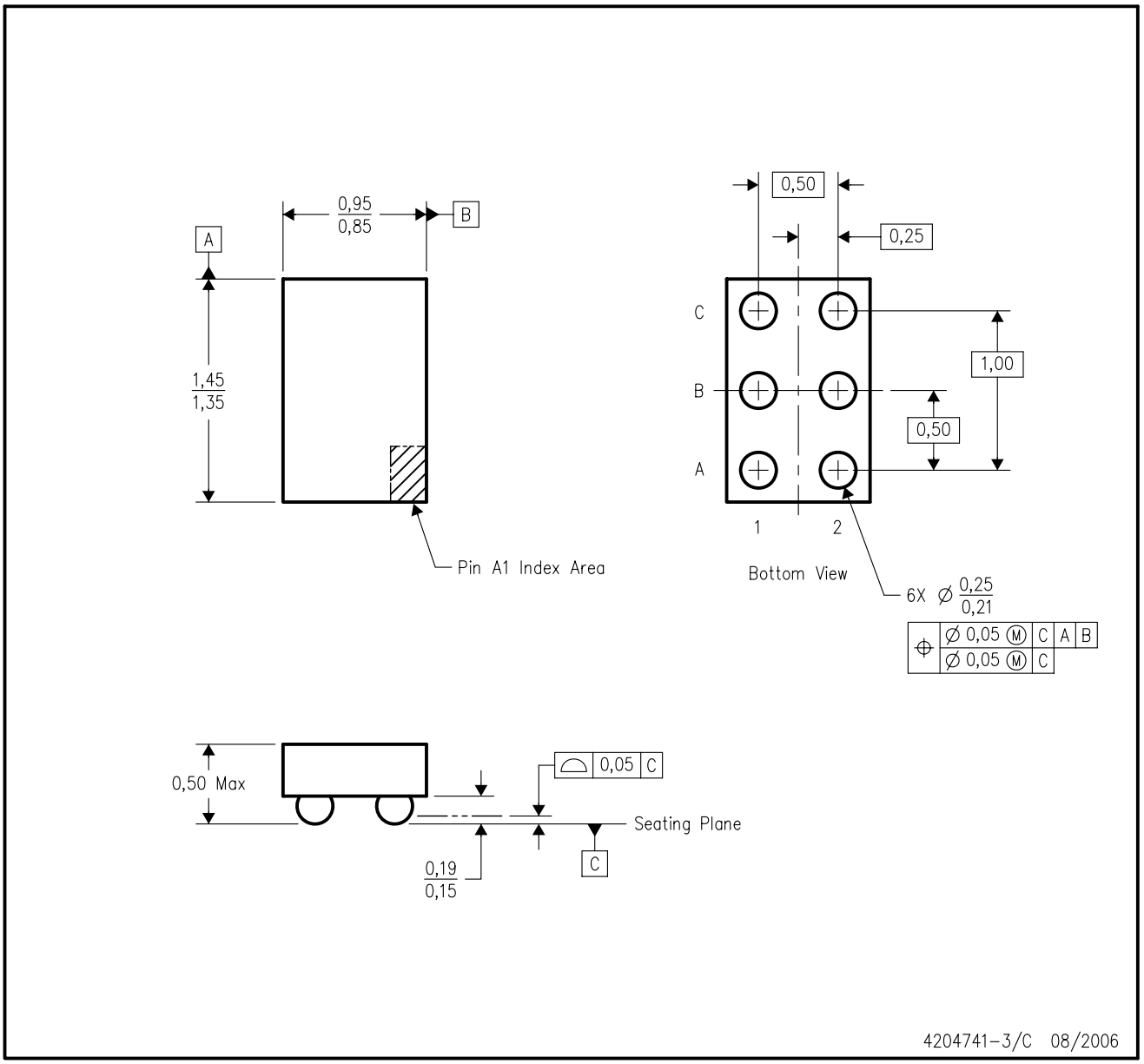
## DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/F 07/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 6 YEP package (drawing 4204725) for tin–lead (SnPb).

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