PATP – operations for example 1

CS132 T6H6

Initialisation: load example 1 program into memory, set PC to 00000, then start machine execution with the first fetch.

MS address	Mnemonic	Data
0 (=00000)	CLEAR	000 00000
1 (=00001)	ADD# 9	010 01001
2 (=00010)	DEC1	011 00000

(NB I've changed example 1: last time this was ADD# 3 but now it is ADD# 9)

Macro step	Mnemonic	Macro operation	Micro step	Micro operations	MAR IN 0:4	IR IN 0:7, OUT 0:4	PC IN 0:4, OUT 0:4	D0 IN 0:7, OUT 0:7	ALU(P) IN 0:7	ALU(Q) IN 0:7	ALU(F) IN F_1, F_2	ALUreg IN 0:7, OUT 0:7
(initialisation)							00000					
fetch	(fetch step A)	[IR] ← [MS(PC)]	1	[MAR] ← [PC]	00000							
			2	[IR(0:7)] ← [MS(MAR)]		000 00000						
	(fetch step B)	[PC] ← [PC] + 1	3	[ALU(Q)] ← [PC]						… 00000		
			4	[ALU(F)] ← 01 ("Q+1")							01 (“Q+1”)	
			5	[ALUreg] ← [ALU]								… 00001
			6	[PC] ← [ALUreg]			00001					
1	CLEAR	[D0] ← 0	7	[ALU(F)] ← 00 ("Zero")							00 (“Zero”)	
			8	[ALUreg] ← [ALU]								0000 0000
			9	[D0] ← [ALUreg]				0000 0000				
fetch	**(fetch step A)**	**[IR] ← [MS(PC)]**	10	**[MAR] ← [PC]**	**00001**							
			11	**[IR(0:7)] ← [MS(MAR)]**		**010 01001**						
	(fetch step B)	**[PC] ← [PC] + 1**	12	**[ALU(Q)] ← [PC]**						**… 00001**		
			13	**[ALU(F)] ← 01 ("Q+1")**							**01 (“Q+1”)**	
			14	**[ALUreg] ← [ALU]**								**… 00010**
			15	**[PC] ← [ALUreg]**			**00010**					
2	**ADD# 9**	**[D0] ← [D0] + v**	16	**[ALU(P)] ← [D0]**					**0000 0000**			
			17	**[ALU(Q)] ← [IR(0:4)]**						**(000) 01001**		
			18	**[ALU(F)] ← 10 ("Q+P")**							**10 (“Q+P”)**	
			19	**[ALUreg] ← [ALU]**								**0000 1001**
			20	**[D0] ← [ALUreg]**				**0000 1001**				
fetch	**(fetch step A)**	**[IR] ← [MS(PC)]**	21	**[MAR] ← [PC]**	**00010**							
			22	**[IR(0:7)] ← [MS(MAR)]**		**011 00000**						
	(fetch step B)	[PC] ← [PC] + 1	23	[ALU(Q)] ← [PC]							01 (“Q+1”)	
			24	[ALU(F)] ← 01 ("Q+1")								… 00011
			25	[ALUreg] ← [ALU]			00011					
			26	[PC] ← [ALUreg]						0000 1001		
3	DEC1	[D0] ← [D0] - 1	27	[ALU(Q)] ← [D0]							11 (“Q-1”)	
			28	[ALU(F)] ← 11 ("Q-1")								0000 1000
			29	[ALUreg] ← [ALU]				0000 1000				
			30	[D0] ← [ALUreg]								