PATP – operations for instructions and fetch

CS132 T6H5

Opcode	Mnemonic	Macro operation	Micro step	Micro operations	Control step	Control actions
	(fetch step A)	[IR] ← [MS(PC)]	1	[MAR] ← [PC]	1	E_{PC}, C_{MAR}
			2	[IR(0:7)] ← [MS(MAR)]	2	R, E_{MS}, C_{IR}
	(fetch step B)	[PC] ← [PC] + 1	3	[ALU(Q)] ← [PC]	3	E_{PC}
			4	[ALU(F)] ← 01 ("Q+1")	3	F_1=0 & F_2=1
			5	[ALUreg] ← [ALU]	3	C_{ALUR}
			6	[PC] ← [ALUreg]	4	E_{ALUR}, C_{PC}
000	CLEAR	[D0] ← 0	1	[ALU(F)] ← 00 ("Zero")	1	F_1=0 & F_2=0
			2	[ALUreg] ← [ALU]	1	C_{ALUR}
			3	[D0] ← [ALUreg]	2	E_{ALUR}, C_{D0}
001	INC1	[D0] ← [D0] + 1	1	[ALU(Q)] ← [D0]	1	E_{D0}
			2	[ALU(F)] ← 01 ("Q+1")	1	F_1=0 & F_2=1
			3	[ALUreg] ← [ALU]	1	C_{ALUR}
			4	[D0] ← [ALUreg]	2	E_{ALUR}, C_{D0}
010	ADD# n	[D0] ← [D0] + v	1	[ALU(P)] ← [D0]	1	No control actions required
			2	[ALU(Q)] ← [IR(0:4)]	1	E_{IR}
			3	[ALU(F)] ← 10 ("Q+P")	1	F_1=1 & F_2=0
			4	[ALUreg] ← [ALU]	1	C_{ALUR}
			5	[D0] ← [ALUreg]	2	E_{ALUR}, C_{D0}
011	DEC1	[D0] ← [D0] - 1	1	[ALU(Q)] ← [D0]	1	E_{D0}
			2	[ALU(F)] ← 11 ("Q-1")	1	F_1=1 & F_2=1
			3	[ALUreg] ← [ALU]	1	C_{ALUR}
			4	[D0] ← [ALUreg]	2	E_{ALUR}, C_{D0}
100	JMP loc	[PC] ← loc	1	[PC] ← [IR(0:4)]	1	E_{IR}, C_{PC}
101	BUZ loc / BNZ loc / BZC loc / BNE loc	If Z is not 0 then [PC] ← loc	1	If Z is not 0 then [PC] ← [IR(0:4)]	1	If Z is not 0 then E_{IR}, C_{PC}
110	LOAD loc	[D0] ← [MS(loc)]	1	[MAR] ← [IR(0:4)]	1	E_{IR}, C_{MAR}
			2	[D0] ← [MS(MAR)]	2	R, E_{MS}, C_{D0}
111	STORE loc	[MS(loc)] ← [D0]	1	[MAR] ← [IR(0:4)]	1	E_{IR}, C_{MAR}
			2	[MS(MAR)] ← [D0]	2	E_{D0}, W