Signal Name	Pin Type	Pin Number	Pin Mode	TOP_LEVEL		
				Entity	External IO Index	Internal IO Index
ClockFPGA	in	128	LVCMOS33	ClockFPGA		
FPGA_nReset	in	126	LVCMOS33	FPGA_nReset		
SPI0_MOSI	in	133	LVCMOS33	SPI0_MOSI		
SPI0_SCLK	in	138	LVCMOS33	SPI0_SCLK		
SPI0_nCE0	in	127	LVCMOS33	SPI0_nCE0		
SPI0_nCE1	in	132	LVCMOS33	SPI0_nCE1		
SPI0_MISO	out	139	LVCMOS33	SPI0_MISO		
GPIO0	inout	125	LVCMOS33	IN_OUT_DATA[0]	0	0
GPIO1	inout	122	LVCMOS33	IN_OUT_DATA[1]	1	1
InXLeft	inout	83	LVCMOS33	IN_OUT_DATA[2]	2	2
InXRight	inout	84	LVCMOS33	IN_OUT_DATA[3]	3	3
InXRef	inout	85	LVCMOS33	IN_OUT_DATA[4]	4	4
InYBack	inout	87	LVCMOS33	IN_OUT_DATA[5]	5	5
InYFront	inout	86	LVCMOS33	IN_OUT_DATA[6]	6	6
InYRef	inout	89	LVCMOS33	IN_OUT_DATA[7]	7	7
InZBottom	inout	92	LVCMOS33	IN_OUT_DATA[8]	8	8
InZTop	inout	91	LVCMOS33	IN_OUT_DATA[9]	9	9
InProximity	inout	99	LVCMOS33	IN_OUT_DATA[10]	10	10
InIncX_A	inout	93	LVCMOS33	IN_OUT_DATA[11]	11	11
InIncX_B	inout	94	LVCMOS33	IN_OUT_DATA[12]	12	12
InIncX_I	inout	95	LVCMOS33	IN_OUT_DATA[13]	13	13
InIncY_A	inout	96	LVCMOS33	IN_OUT_DATA[14]	14	14
InIncY_B	inout	97	LVCMOS33	IN_OUT_DATA[15]	15	15
InIncY_I	inout	98	LVCMOS33	IN_OUT_DATA[16]	16	16
EnableDCX	inout	100	LVCMOS33	IN_OUT_DATA[17]	17	17
OutDCX_A	inout	103	LVCMOS33	IN_OUT_DATA[18]	18	18
OutDCX_B	inout	104	LVCMOS33	IN_OUT_DATA[19]	19	19
EnableDCY	inout	112	LVCMOS33	IN_OUT_DATA[20]	20	20
OutDCY_A	inout	111	LVCMOS33	IN_OUT_DATA[21]	21	21
OutDCY_B	inout	113	LVCMOS33	IN_OUT_DATA[22]	22	22
EnableDCZ	inout	105	LVCMOS33	IN_OUT_DATA[23]	23	23
OutDCZ_A	inout	106	LVCMOS33	IN_OUT_DATA[24]	24	24
OutDCZ_B	inout	107	LVCMOS33	IN_OUT_DATA[25]	25	25
EnableMagnet	inout	109	LVCMOS33	IN_OUT_DATA[26]	26	26
OutMagnet	inout	110	LVCMOS33	IN_OUT_DATA[27]	27	27
LEDPowerR	inout	141	LVCMOS33	IN_OUT_DATA[28]	28	28
LEDPowerG	inout	140	LVCMOS33	IN_OUT_DATA[29]	29	29
LightRed	inout	10	LVCMOS33	IN_OUT_DATA[30]	30	30
LightWhite	inout	11	LVCMOS33	IN_OUT_DATA[31]	31	31
LightGreen	inout	12	LVCMOS33	IN_OUT_DATA[32]	32	32
External 0	inout	73	LVCMOS33	IN_OUT_DATA[33]	33	41
External 1	inout	74	LVCMOS33	IN_OUT_DATA[34]	34	41
External 2	inout	75	LVCMOS33	IN_OUT_DATA[35]	35	41
External 3	inout	76	LVCMOS33	IN_OUT_DATA[36]	36	41
External 4	inout	77	LVCMOS33	IN_OUT_DATA[37]	37	41
External 5	inout	78	LVCMOS33	IN_OUT_DATA[38]	38	41
External 6	inout	81	LVCMOS33	IN_OUT_DATA[39]	39	41
External 7	inout	82	LVCMOS33	IN_OUT_DATA[40]	40	41

Notes:	
1	LVCMOS33 was used given that the mayority of pins use this standard. The pins are distributed only across bank 1 and 0 and this forces all pins to the same standard. LVCMOS22 could also be used for all pins
2	Internal IO Pin 41 is grounded and configured as input. The data is not used
3	The external IO and internal IO are related through the default layout of the IO_CROSSBAR. This can be changed by either modifying the original definition in the GOLDI_MODULE_CONFIG package or enabling the dynamic mode. Use first option in case of using External # pins

Register Map

Document Version   1
Hardware Version   V1.00.00
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All registers have a base address located on the package GOLDI_MODULE_CONFIG. This can be changed to move the modules in case the configuration word width is changed.

Register Name	Address (Dec)	Address (Hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System configuration	1	0x01	0x00							ENC_rst	BUS_sel
Sensor IO high	2	0x02	0x00								InProximity
Sensor IO low	3	0x03	0x00	InZTop	InZBottom	InYRef	InYFront	InYBack	InXRef	InXRight	InXLeft
Error list 1	4	0x04	0x00	error_7	error_6	error_5	error_4	error_3	error_2	error_1	error_0
Error list 2	5	0x05	0x00	error_15	error_14	error_13	error_12	error_11	error_10	error_9	error_8
Error list 3	6	0x06	0x00		error_22	error_21	error_20	error_19	error_18	error_17	error_16
GPIO0 Driver	7	0x07	0x00							out_enb	data
GPIO1 Driver	8	0x08	0x00							out_enb	data
X Encoder low	9	0x09	0x00	X_VAL[7:0]							
X Encoder high	10	0x0A	0x00	X_VAL[15:8]							
Y Encoder low	11	0x0B	0x00	Y_VAL[7:0]							
Y Encoder high	12	0x0C	0x00	Y_VAL[15:8]							
X Motor Direction	13	0x0D	0x00							X_Right	X_Left
X Motor Speed	14	0x0E	0x00	PWM[7:0]							
Y Motor Direction	15	0x0F	0x00							Y_Front	Y_Back
Y Motor Speed	16	0x10	0x00	PWM[7:0]							
Z Motor Direction	17	0x11	0x00							Z_Top	Z_Bottom
Z Motor Speed	18	0x12	0x00	PWM[7:0]							
Electromagnet Power	19	0x13	0x00								mag_pow
Power LED Red	20	0x14	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Power LED Green	21	0x15	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Light Red	22	0x16	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Light White	23	0x17	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Light Green	24	0x18	0x00	on/off	Blink_enb	Delay_on			Delay_off		

Error code	Error definition
error_0	Sensors X_left and X_right triggered
error_1	Sensors X_left and X_ref triggered
error_2	Sensors X_right and X_ref triggered
error_3	Sensors Y_back and Y_front triggered
error_4	Sensors Y_back and Y_ref triggered
error_5	Sensors Y_front and Y_ref triggered
error_6	Sensors Z_bottom and Z_top
error_7	X_right and X_left simultaneously on
error_8	Y_back and Y_front simultaneously on
error_9	Z_bottom and Z_top simultaneously on
error_10	X motor actuated left while crane not in top position
error_11	X motor actuated right while crane not in top position
error_12	Y motor actuated back while crane not in top position
error_13	Y motor actuated front while crane not in top position
error_14	Portal at outermost position and X_left
error_15	Portal at outermost position and X_right
error_16	Portal at outermost position and Y_back
error_17	Portal at outermost position and Y_front
error_18	Portal at outermost position and Z_bottom
error_19	Portal at outermost position and Z_top
error_20	X DC motor out channels inverted
error_21	Y DC motor out channels inverted
error_22	Z DC motor out channels inverted

Communication Protocol

Configuration Word - Byte 1								Data Word - Byte 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WE	REGISTER ADDRESS							REGISTER DATA [MSBF]							
0	ADDRESS[6:0]							[MOSI: don't care] / [MISO: Register data]							
1	ADDRESS[6:0]							[MOSI:New register data] / [MISO: Old register data]							

Configuration Word - Byte 1								Data Word - Byte 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WE	EXTERNAL IO ADDRESS [IO_INDEX + 2]							INTERNAL IO INDEX [MSBF]							
0	EXTERNAL_IO_ADDRESS[6:0]							[MOSI: don't care] / [MISO: Internal IO Index]							
1	EXTERNAL_IO_ADDRESS[6:0]							[MOSI: New Internal IO Index] / [MISO: Old Internal IO Index]							

Notes:	
1	Register 1 [SYSTEM_CONFIGURATION] is addressable from both buses; this explains the codification of the External IO Address as "Index + 2". Register follows the "System Communication Mode Protocol" independent of content.
2	Multi-word spi transactions follow MSBF order. The second data word is stored in the lower address accessed. The SPI transfer "ADDRESS[6:0]/DATA_1[7:0]/DATA_2[7:0]" is equivalent to "ADDRESS[6:0] / DATA_1[7:0] ADDRESS[6:0]-1 / DATA_2[7:0]"

SPI Protocol:

CPOL	Initial clock state during idle cycle	1	logic high
CPHA	Clock transition vs data transitoin	1	Data shifted out on the falling edge and registered on the rising edge