High-Bay Warehouse Pinout							
Hardware Pinout					FPGA System		
Signal Name	Schematic Name	Pin Type	Pin Number	Pin Mode	Entity	Crossbar Right/External IO	Default Crossbar Left/Internal IO
Clock FPGA	ClockFPGA	in	128	LVCMOS33	ClockFPGA	-	-
Reset	FPGA_nReset	in	126	LVCMOS33	FPGA_nReset	-	-
SCLK	SPI0_SCLK	out	138	LVCMOS33	SPI0_SCLK	-	-
MOSI	SPI0_MOSI	out	133	LVCMOS33	SPI0_MOSI	-	-
MISO	SPI0_MISO	in	139	LVCMOS33	SPI0_MISO	-	-
nCE	SPI0_nCE0	out	127	LVCMOS33	SPI0_nCE0	-	-
GPIO0	CMGPIO0	inout	125	LVCMOS33	IO_DATA[0]	0	0
GPIO1	CMGPIO1	inout	122	LVCMOS33	IO_DATA[1]	1	1
X-Axis Limit Left	Stepper0_LSDir0	inout	84	LVCMOS33	IO_DATA[2]	2	2
X-Axis Limit Right	Stepper0_LSDir1	inout	85	LVCMOS33	IO_DATA[3]	3	3
Y-Axis Limit Outside	HBridge0A_LS	inout	15	LVCMOS33	IO_DATA[4]	4	4
Y-Axis Limit Inside	HBridge0B_LS	inout	17	LVCMOS33	IO_DATA[5]	5	5
Z-Axis Limit Bottom	Stepper1_LSDir1	inout	92	LVCMOS33	IO_DATA[6]	6	6
Z-Axis Limit Top	Stepper1_LSDir0	inout	91	LVCMOS33	IO_DATA[7]	7	7
Inductive sensor signal	Input7	inout	57	LVCMOS33	IO_DATA[8]	8	8
Encoder X Channel A	Stepper0_EncA	inout	87	LVCMOS33	IO_DATA[9]	9	9
Encoder X Channel B	Stepper0_EncB	inout	89	LVCMOS33	IO_DATA[10]	10	10
Encoder X Channel I	Stepper0_EncI	inout	86	LVCMOS33	IO_DATA[11]	11	11
Encoder Z Channel A	Stepper1_EncA	inout	104	LVCMOS33	IO_DATA[12]	12	12
Encoder Z Channel B	Stepper1_EncB	inout	105	LVCMOS33	IO_DATA[13]	13	13
Encoder Z Channel I	Stepper1_EncI	inout	106	LVCMOS33	IO_DATA[14]	14	14
X Motor Clock	Stepper0_CLK	inout	78	LVCMOS33	IO_DATA[15]	15	15
X Motor Enable	Stepper0_ENN	inout	77	LVCMOS33	IO_DATA[16]	16	16
X Motor Stall Guard	Stepper0_SG	inout	83	LVCMOS33	IO_DATA[17]	17	17
X Motor Step	Stepper0_STEP	inout	81	LVCMOS33	IO_DATA[18]	18	18
X Motor Direction	Stepper0_DIR	inout	82	LVCMOS33	IO_DATA[19]	19	19
X Motor Spi nCS	Stepper0_nCS	inout	76	LVCMOS33	IO_DATA[20]	20	20
X Motor Spi SCLK	Stepper0_SCK	inout	75	LVCMOS33	IO_DATA[21]	21	21
X Motor Spi MOSI	Stepper0_MOSI	inout	74	LVCMOS33	IO_DATA[22]	22	22
X Motor Spi MISO	Stepper0_MISO	inout	73	LVCMOS33	IO_DATA[23]	23	23
Y Motor Enable	HBridge0AB_Enable	inout	1	LVCMOS33	IO_DATA[24]	24	24
Y Motor Out Left	HBridge0A_PWM	inout	2	LVCMOS33	IO_DATA[25]	25	25
Y Motor Out Right	HBridge0B_PWM	inout	6	LVCMOS33	IO_DATA[26]	26	26
Z Motor Clock	Stepper1_CLK	inout	103	LVCMOS33	IO_DATA[27]	27	27
Z Motor Enable	Stepper1_ENN	inout	100	LVCMOS33	IO_DATA[28]	28	28
Z Motor Stall Guard	Stepper1_SG	inout	95	LVCMOS33	IO_DATA[29]	29	29
Z Motor Step	Stepper1_STEP	inout	93	LVCMOS33	IO_DATA[30]	30	30
Z Motor Direction	Stepper1_DIR	inout	94	LVCMOS33	IO_DATA[31]	31	31
Z Motor Spi nCS	Stepper1_nCS	inout	99	LVCMOS33	IO_DATA[32]	32	32
Z Motor Spi SCLK	Stepper1_SCK	inout	98	LVCMOS33	IO_DATA[33]	33	33
Z Motor Spi MOSI	Stepper1_MOSI	inout	97	LVCMOS33	IO_DATA[34]	34	34
Z Motor Spi MISO	Stepper1_MISO	inout	96	LVCMOS33	IO_DATA[35]	35	35
LED Power Red	LEDPowerR	inout	141	LVCMOS33	IO_DATA[36]	36	36
LED Power Green	LEDPowerG	inout	140	LVCMOS33	IO_DATA[37]	37	37
Environment Light Red	LightRed	inout	33	LVCMOS33	IO_DATA[38]	38	38
Environment Light White	LightWhite	inout	34	LVCMOS33	IO_DATA[39]	39	39
Environment Light Green	LightGreen	inout	35	LVCMOS33	IO_DATA[40]	40	40

Register Map

Document Version	1
Hardware Version	V2.00.00
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All registers have a base address located on the package GOLDI_MODULE_CONFIG. This can be changed to move the modules in case the configuration word width is changed.

Register Name	Address (Dec)	Address (Hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System Configuration	1	0x01	0x00							ENC_rst	BUS_sel
Sensors: model	2	0x02	0x00		inductive	z_top	z_bottom	y_inside	y_outside	x_right	x_left
Sensors: virtual low	3	0x03	0x00	virtual_x[8]	virtual_x[7]	virtual_x[6]	virtual_x[5]	virtual_x[4]	virtual_x[3]	virtual_x[2]	virtual_x[1]
Sensors: virtual high	4	0x04	0x00		virtual_z[5]	virtual_z[4]	virtual_z[3]	virtual_z[2]	virtual_z[1]	virtual_x[10]	virtual_x[9]
Error list 1	5	0x05	0x00								error_0
Error list 2	6	0x06	0x00								
GPIO0 Driver	7	0x07	0x00							Out_enb	Data
GPIO1 Driver	8	0x08	0x00							Out_enb	Data
X Encoder low	9	0x09	0x00	X_VAL[7:0]							
X Encoder high	10	0x0A	0x00	X_VAL[15:8]							
Z Encoder low	11	0x0B	0x00	Z_VAL[7:0]							
Z Encoder high	12	0x0C	0x00	Z_VAL[15:8]							
X Motor Control	13	0x0D	0x00	Pow_off					Stall	Dir1	Dir0
X Motor Speed	14	0x0E	0x00	FRQ_VAL[7:0]							
X Motor Speed	15	0x0F	0x00	FRQ_VAL[15:8]							
X Motor SPI 0	16	0x10	0x07	CONFIG_WORD[7:0]							
X Motor SPI 1	17	0x11	0x00	CONFIG_WORD[15:8]							
X Motor SPI 2	18	0x12	0x00	CONFIG_WORD[23:16]							
Y Motor Direction	19	0x13	0x00							Y_Inside	Y_Outside
Y Motor Speed	20	0x14	0x00	PWM[7:0]							
Z Motor Control	21	0x15	0x00	Pow_off					Stall	Dir1	Dir0
Z Motor Speed	22	0x16	0x00	FRQ_VAL[7:0]							
Z Motor Speed	23	0x17	0x00	FRQ_VAL[15:8]							
Z Motor SPI 0	24	0x18	0x07	CONFIG_WORD[7:0]							
Z Motor SPI 1	25	0x19	0x00	CONFIG_WORD[15:8]							
Z Motor SPI 2	26	0x20	0x00					CONFIG_WORD[19:16]			
Power LED Red	27	0x21	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Power LED Green	28	0x22	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Environment Light Red	29	0x23	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Environment Light White	30	0x24	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Environment Light Green	31	0x25	0x00	on/off	Blink_enb	Delay_on			Delay_off		

Error code	Error definition
error_0	Limit sensors left and right active
error_1	Limit sensors y-Outside and y-Inside active
error_2	Limit sensors bottom and top active
error_3	Motor x drive to left active and limit left active
error_4	Motor x drive to right active and limit right active
error_5	Motor y drive to outside active and limit outside active
error_6	Motor y drive to inside active and limit inside active
error_7	Motor z drive to bottom active and limit bottom active
error_8	Motor z drive to top active and limit top active
error_9	Crane out of the horizontal virtual box in the left limit
error_10	Crane out of the horizontal virtual box in the right limit
error_11	Crane out of the vertical virtual box in the bottom limit
error_12	Crane out of the vertical virtual box in the top limit

Communication Protocol

The *GOLDI_ControlUnit_IO_FPGA* requires configuration parameters through the SPI interface to operate. The SPI interface allows reading and writing values into the dynamic registers of the model.

Bus Signals

The *GOLDI_ControlUnit_IO_FPGA* has four signals:

SPI0_SCLK: bus clock input
SPI0_MOSI: serial data input
SPI0_MISO: serial data output
SPI0_nCE0: chip select input (active low)

The module is enabled for an SPI transaction by a low on the chip select input nCE0. Bit transfer is synchronous to the bus clock SCLK, with the slave latching the data from MOSI on the rising edge of SCLK and driving data to MISO on the falling edge. The most significant bit is sent first. A minimum of 16 SCLK clock cycles is required for a bus transaction (CONFIGURATION_WORD[7:0]+DATA_WORD[7:0].

If more than 16 clocks are driven, the additional bits shifted into MOSI are assigned to increasing lower addresses. If a read transaction with 16 + n*8 clocks is performed then the MISO shifts the data of the selected register and the registers with the address (adr-n). If a write transaction with 16 + n*8 clocks is performed the MOSI shifts the data to the selected registers and the registers with the address (adr-n).

nCE0 must be low during the whole bus transaction. When nCE0 goes high, the unfinished transaction is discarded. The MOSI data is latched once the DATA_WORD is transfered

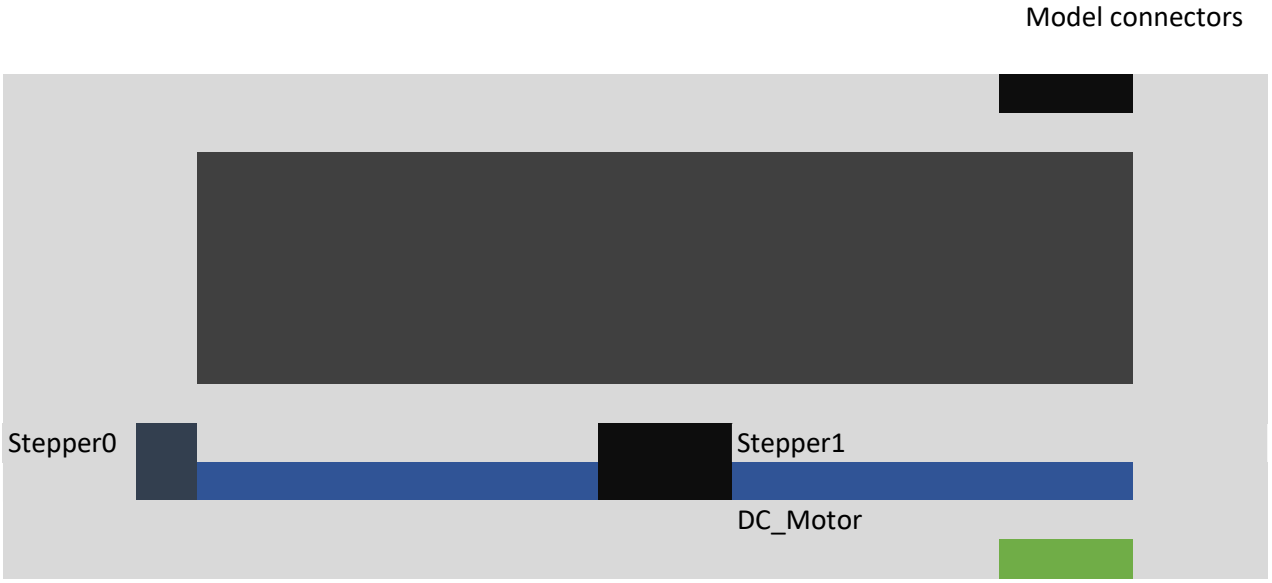
The configuration word length is based on the value "BUS_ADDRESS_WIDTH" in the GOLDI_COMM_STANDARD package. This corresponds to the address width + 1 bit for write enable. The data word length is based on the value "SYSTEM_DATA_WIDTH" in the GOLDI_COMM_STANDARD package. This value corresponds to the number of data bits

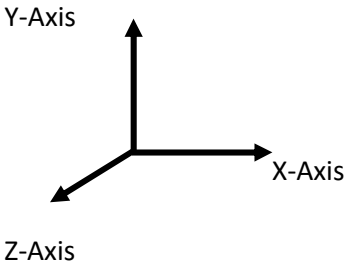
Default configuration for the *GOLDI_ControlUnit_IO_FPGA* model

BUS_ADDRESS_WIDTH	7
SYSTEM_DATA_WIDTH	8

Configuration Word [7:0]								Data Word[7:0]
Bit7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Byte 0**
WE	REGISTER_ADDRESS							DATA[MSBF]
0	READ_ADDRESS[6:0]							[MOSI: dc] | [MISO: Register data]
1	WRITE_ADDRESS[6:0]							[MOSI: New data] | [MISO: Register data]

Physical model reference map





Actuation Map	
Direction	**Condition**
x_neg | left	Stepper0 -> Dir0
x_pos | right	Stepper0 -> Dir1
y_neg | Outside	DC -> Outside
y_pos | Inside	DC -> Inside
z_neg | bottom	Stepper1 -> Dir0
z_pos | top	Stepper1 -> Dir1