#### **GOLDI Axis Portal V1**

**Document version:** 2

**Release date:** 25.05.2023

#### Overview:

The GOLDI Axis Portal V1 is an FPGA-driven unit used to control the GOLDI Axis Portal V1 model. The FPGA system provides a standard interface for a microcontroller to control the model by writing data to the FPGA registers.

## Calibration procedure:

The GOLDI Axis Portal V1 does not have an initialization or calibration process needed to operate correctly. The system can be used directly after initialization. However, it is recommended to drive the crane to the utmost left and back position and reset the encoders using the control register to get a reproducible encoder position value.

### Operation:

The GOLDI Axis Portal V1 is operated by writing the corresponding values into the FPGA registers (See Register Table)

## **SPI Communication Protocol**

The GOLDI Axis Portal V1 is configured through an SPI interface. The SPI interface allows the independent reading and writing of values from and into the registers of the model.

#### **SPI Signals**

0010 00114

The GOLDI Axis Portal V1 has four signals:

SPI0_SCLK	SPI clock
SPI0_MOSI	SPI serial data input
SPI0_MISO	SPI serial data output
SPI0_nCE0	SPI chip select input (active low)

The module is enabled for an SPI transaction by a logic low on the chip select input nCE0. Bit transfer is synchronous to the bus clock SCLK, with the slave latching the data from MOSI on the rising edge of SCLK and driving data to MISO on the falling edge. The most significant bit is sent first. A minimum of 24 SCLK clock cycles is required for a bus transaction.

(CONFIGURATION WORD[15:0] + DATA WORD[7:0])

If more than 24 clocks are driven, the additional bits shifted into MOSI are assigned to increasing lower addresses. If a read transaction with 24+n\*8 clocks is performed then the MISO shifts the data of the selected register and the registers with the addesses (adr-n). If a write transaction with 24+n\*8 clocks is performed the MOSI shifts the data to the selected registers and the registers with the address (adr-n)

nCE0 must be low during the whole SPI transaction. When nCE0 goes high, the unfinished transaction is discarded. The MOSI data is latched once the DATA WORD is transferred

The configuration word length is based on the value "BUS ADDRESS WIDTH" in the GOLDI COMM STANDARD package. This corresponds to the address width + 1 bit for the write enable flag. The data word length is based on the value "SYSTEM DATA WIDTH" in the GOLDI COMM STANDARD package. This value corresponds to the number of data bits

#### Default configuration for the GOLDI Axis Portal V1 model

BUS ADDRESS WIDTH 15 SYSTEM DATA WIDTH

	Configuration Word [15:0]	Data Word[7:0]
Bit 15	Bit [14:8] Bit [7:0]	Bit [7:0]
WE	REGISTER_ADDRESS	DATA[MSBF]
0	READ_ADDRESS[15:0]	[MOSI: dc]   [MISO: Register data]
1	WRITE_ADDRESS[15:0]	[MOSI: New data]   [MISO: Register data]

8

# GOLDI Axis Portal V1 hardware pinout

Control Unit Pinout							
Hardware	Pinout	FPGA System					
		Pin Type	e Pin Number Pin Mo		Entity name		
External FPGA Clock	ClockFPGA	in 128		LVCMOS33	ClockFPGA		
Reset	FPGA_nReset	in	126	LVCMOS33	FPGA_nReset		
SCLK	SPI0_SCLK	in	138	LVCMOS33	SPI0_SCLK		
MOSI	SPI0_MOSI	in	133	LVCMOS33	SPI0_MOSI		
MISO	SPI0_MISO	out	139	LVCMOS33	SPI0_MISC		
nCE	SPI0_nCE0	in	127	LVCMOS33	SPI0_nCE0		
Multi-purpose GPIO0	GPIO0	inout	125	LVCMOS33	IO_DATA[0]		
Multi-purpose GPIO1	GPIO1	inout	122	LVCMOS33	IO_DATA[1]		
X-axis sensor left	InXLeft	inout	83	LVCMOS33	IO_DATA[2]		
X-axis sensor right	InXRight	inout	84	LVCMOS33	IO_DATA[3]		
X-axis sensor reference	InXRef	inout	85	LVCMOS33	IO_DATA[4]		
Y-axis sensor back	InYBack	inout	87	LVCMOS33	IO_DATA[5]		
Y-axis sensor front	InYFront	inout	86	LVCMOS33	IO_DATA[6]		
Y-axis sensor reference	InYRef	inout	89	LVCMOS33	IO_DATA[7]		
Z-axis sensor bottom	InZBottom	inout	92	LVCMOS33	IO_DATA[8]		
Z-axis sensor top	InZTop	inout	91	LVCMOS33	IO_DATA[9]		
Z-axis sensor proximity	InProximity	inout	99	LVCMOS33	IO_DATA[10]		
Encoder X channel A	InIncX_A	inout	93	LVCMOS33	IO_DATA[11]		
Encoder X channel B	InIncX_B	inout	94	LVCMOS33	IO_DATA[12]		
Encoder X channel I	InIncX_I	inout	95	LVCMOS33	IO_DATA[13]		
Encoder Y channel A	InIncY_A	inout	96	LVCMOS33	IO_DATA[14]		
Encoder Y channel B	InIncY_B	inout	97	LVCMOS33	IO_DATA[15]		
Encoder Y channel I	InIncY_I	inout	98	LVCMOS33	IO_DATA[16]		
X-axis motor enable	EnableDCX	inout	100	LVCMOS33	IO_DATA[17]		
X-axis motor out 1	OutDCX_A	inout	103	LVCMOS33	IO_DATA[18]		
X-axis motor out 2	OutDCX_B	inout	104	LVCMOS33	IO_DATA[19]		
Y-axis motor enable	EnableDCY	inout	112	LVCMOS33	IO_DATA[20]		
Y-axis motor out 1	OutDCY_A	inout	111	LVCMOS33	IO_DATA[21]		
Y-axis motor out 2	OutDCY_B	inout	113	LVCMOS33	IO_DATA[22]		
Z-axis motor enable	EnableDCZ	inout	105	LVCMOS33	IO_DATA[23]		
Z-axis motor out 1	OutDCZ_A	inout	106	LVCMOS33	IO_DATA[24]		
Z-axis motor out 2	OutDCZ_B	inout	107	LVCMOS33	IO_DATA[25]		
E-Magnet power on/off	EnableMagnet	inout	109	LVCMOS33	IO_DATA[26]		
E-Magnet out 1	OutMagnet	inout	110	LVCMOS33	IO_DATA[27]		
Power LED Red	LEDPowerR	inout	141	LVCMOS33	IO_DATA[28]		
Power LED Green	LEDPowerG	inout	140	LVCMOS33	IO_DATA[29]		
Environment LED Red	LightRed	inout	10	LVCMOS33	IO_DATA[30]		
Environment LED White	LightWhite	inout	11	LVCMOS33	IO_DATA[31]		
Environment LED Green	LightGreen	inout	12	LVCMOS33	IO_DATA[32]		
Multi-purpose pin 0	External 0	inout	73	LVCMOS33	IO_DATA[33]		

Multi-purpose pin 1	External 1	inout	74	LVCMOS33	IO_DATA[34]
Multi-purpose pin 2	External 2	inout	75	LVCMOS33	IO_DATA[35]
Multi-purpose pin 3	External 3	inout	76	LVCMOS33	IO_DATA[36]
Multi-purpose pin 4	External 4	inout	77	LVCMOS33	IO_DATA[37]
Multi-purpose pin 5	External 5	inout	78	LVCMOS33	IO_DATA[38]
Multi-purpose pin 6	External 6	inout	81	LVCMOS33	IO_DATA[39]
Multi-purpose pin 7	External 7	inout	82	LVCMOS33	IO_DATA[40]

# Register Map

 Document Version
 2

 Hardware Version
 V3.00.00

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 25.05.2023

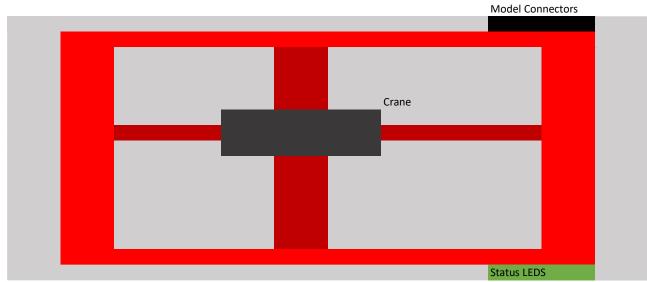
All registers have a base address located on the package GOLDI\_MODULE\_CONFIG. This can be changed to move the modules in case the configuration word width is changed.

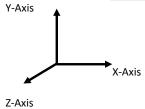
Register Name	Address (Dec)	Address (Hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System Configuration	1	0x01	0x00								ENC_rst
Sensor IO high	2	0x02	0x00	InZFront	InZBottom	InYRef	InYFront	InYBack	InXRef	InXRight	InXLeft
Sensor IO low	3	0x03	0x00								InProximity
Error list 1	4	0x04	0x00	error_7	error_6	error_5	error_4	error_3	error_2	error_1	error_0
Error list 2	5	0x05	0x00	error_15	error_14	error_13	error_12	error_11	error_10	error_9	error_8
Error list 3	6	0x06	0x00		error_22	error_21	error_20	error_19	error_18	error_17	error_16
GPIO0 Driver	7	0x07	0x00							Out_enb	Data
GPIO1 Driver	8	0x08	0x00							Out_enb	Data
X Encoder low	9	0x09	0x00	X_VAL[7:0]				•			
X Encoder high	10	0x0A	0x00		X_VAL[15:8]						
Z Encoder low	11	0x0B	0x00		Y_VAL[7:0]						
Z Encoder high	12	0x0C	0x00				Y_VA	AL[15:8]			
X Motor Direction	13	0x0D	0x00							right	left
X Motor Speed	14	0x0E	0x00		•	•	PW	M[7:0]	-	-	
Y Motor Direction	15	0x0F	0x00							front	back
Y Motor Speed	16	0x10	0x07		•		PW	M[7:0]	•	•	-
Z Motor Direction	17	0x11	0x00							top	bottom
Z Motor Speed	18	0x12	0x00	PWM[7:0]				•			
Electromagnet Power	19	0x13	0x00								mag_pwr
Power LED Red	20	0x14	0x00	on/off	Blink_enb		Delay_on	-		Delay_off	
Power LED Green	21	0x15	0x00	on/off	Blink_enb		Delay_on			Delay_off	
Light Red	22	0x16	0x00	on/off	Blink_enb		Delay_on			Delay_off	
Light White	23	0x17	0x00	on/off	Blink_enb		Delay_on			Delay_off	
Light Green	24	0x18	0x00	on/off	Blink_enb		Delay_on			Delay_off	

## **Error List**

Error code	Error definition	
error_0	Sensors X_left and X_right triggered	
error_1	Sensors X_left and X_ref triggered	
error_2	Sensors X_right and X_ref triggered	
error_3	Sensors Y_back and Y_front triggered	
error_4	Sensors Y_back and Y_ref triggered	
error_5	Sensors Y_front and Y_ref triggered	
error_6	Sensors Z_bottom and Z_top	
error_7	X_right and X_left simultaneously on	
error_8	Y_back and Y_front simultaneously on	
error_9	Z_bottom and Z_top simultaneously on	
error_10	X motor actuated left while crane not in top position	
error_11	X motor actuated right while crane not in top position	
error_12	Y motor actuated back while crane not in top position	
error_13	Y motor actuated front while crane not in top position	
error_14	Portal at outermost position and X_left	
error_15	Portal at outermost position and X_right	
error_16	Portal at outermost position and Y_back	
error_17	Portal at outermost position and Y_front	
error_18	Portal at outermost position and Z_bottom	
error_19	Portal at outermost position and Z_top	
error_20	X DC motor out channels inverted	
error_21	Y DC motor out channels inverted	
error_22	Z DC motor out channels inverted	

# Physical model reference map





Actuation Map				
Direction	Condition			
x_neg   left	X Motor -> Out2/left			
x_pos   right	X Motor -> Out1/right			
y_neg   back	Y Motor -> Out2/back			
y_pos   front	Y Motor -> Out1/front			
z_neg   bottom	Z Motor -> Out2/bottom			
z_pos   top	Z Motor -> Out1/top			