GOLDI Control Unit IO

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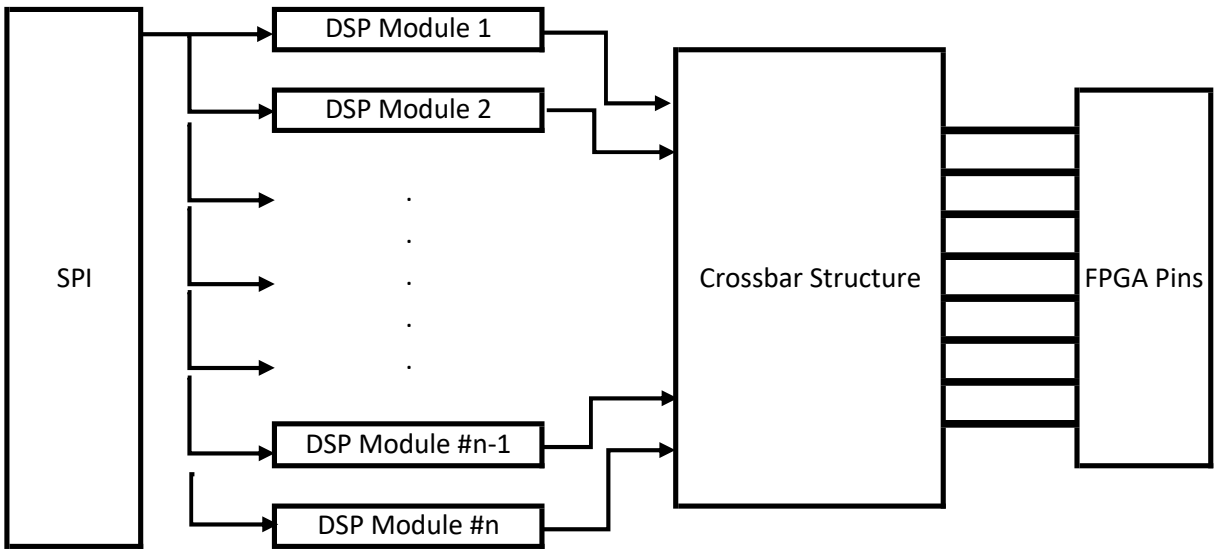
Overview:
The GOLDI Control Unit IO is an FPGA-driven unit used to emulate the normal functions found in a microcontroller. The current version of the Control Unit implements the IO functions of a microcontroller: input mode, output mode, and analog output (PWM). An SPI interface is used to interact with the system and provide the configuration needed to drive the output modes. Additionally, the system uses crossbar structures to multiplex and demultiplex IO DSP modules.

Architecture:
Pin Bank diagramm



The Control Unit is distributed into IO banks which consist of 8 IO pins from the FPGA, a crossbar structure and a number of modules used to generate and process the IO signals. The modules are configured through the SPI interface. The crossbar structure allows the FPGA pins to perform multiple functions by multiplexing and demultiplexing the modules inputs and outputs associated with the bank. The control unit has a total of 8 banks and a total of 64 pins.

SPI Communication Protocol

The GOLDI Control Unit IO is configured through an SPI interface. The SPI interface allows the reading and writing of values form and into the dynamic registers of the model.

SPI Signals
The GOLDI Control Unit has four signals:

SPI0_SCLK	SPI clock
SPI0_MOSI	SPI serial data input
SPI0_MISO	SPI serial data output
SPI0_nCE0	SPI chip select input (active low)

The module is enabled for an SPI transaction by a logic low on the chip select input nCE0. Bit transfer is synchronous to the bus clock SCLK, with the slave latching the data from MOSI on the rising edge of SCLK and driving data to MISO on the falling edge. The most significant bit is sent first. A minimum of 24 SCLK clock cycles is required for a bus transaction.
(CONFIGURATION_WORD[15:0] + DATA_WORD[7:0])

If more than 24 clocks are driven, the additional bits shifted into MOSI are assigned to increasing lower addresses. If a read transaction with 24+n*8 clocks is performed then the MISO shifts the data of the selected register and the registers with the addesses (adr-n). If a write transaction with 24+n*8 clocks is performed the MOSI shifts the data to the selected registers and the registers with the address (adr-n)

nCE0 must be low during the whole SPI transaction. When nCE0 goes high, the unfinished transaction is discarded. The MOSI data is latched once the DATA_WORD is transferred

The configuration word length is based on the value "BUS_ADDRESS_WIDTH" in the GOLDI_COMM_STANDARD package. This corresponds to the address width + 1 bit for the write enable flag. The data word length is based on the value "SYSTEM_DATA_WIDTH" in the GOLDI_COMM_STANDARD package. This value corresponds to the number of data bits

Default configuration for the GOLDI Control Unit model

BUS_ADDRESS_WIDTH	15
SYSTEM_DATA_WIDTH	8

Configuration Word [15:0]			**Data Word[7:0]**
Bit 15	**Bit [14:8]**	**Bit [7:0]**	**Bit [7:0]**
WE	REGISTER_ADDRESS		DATA[MSBF]
0	READ_ADDRESS[15:0]		[MOSI: dc] | [MISO: Register data]
1	WRITE_ADDRESS[15:0]		[MOSI: New data] | [MISO: Register data]

GOLDI Control Unit hardware pinout

Control Unit Pinout						
Hardware Pinout		FPGA System				
Signal Name	Schematic Name	Pin Type	Pin Number	Pin Mode	Entity name	Bank Number
System clock	ClockFPGA	in	128	LVCMOS33	ClockFGPA	
FPGA reset	FPGA_nReset	in	3	LVCMOS33	FPGA_nReset	
FPGA SCLK	SPI0_SCLK	in	9	LVCMOS33	SPI0_SCLK	
FPGA nCS	SPI0_nCE0	in	4	LVCMOS33	SPI0_nCE0	
FPGA MOSI	SPI0_MOSI	in	6	LVCMOS33	SPI0_MOSI	
FPGA MISO	SPI0_MISO	out	10	LVCMOS33	SPI0_MISO	
Control Unit IO Pin 0	IO_0	inout	14	LVCMOS33	IO_DATA[1]	
Control Unit IO Pin 1	IO_1	inout	13	LVCMOS33	IO_DATA[2]	
Control Unit IO Pin 2	IO_2	inout	20	LVCMOS33	IO_DATA[3]	
Control Unit IO Pin 3	IO_3	inout	19	LVCMOS33	IO_DATA[4]	
Control Unit IO Pin 4	IO_4	inout	32	LVCMOS33	IO_DATA[5]	Bank 1
Control Unit IO Pin 5	IO_5	inout	31	LVCMOS33	IO_DATA[6]	
Control Unit IO Pin 6	IO_6	inout	26	LVCMOS33	IO_DATA[7]	
Control Unit IO Pin 7	IO_7	inout	25	LVCMOS33	IO_DATA[8]	
Control Unit IO Pin 8	IO_8	inout	17	LVCMOS33	IO_DATA[9]	
Control Unit IO Pin 9	IO_9	inout	15	LVCMOS33	IO_DATA[10]	
Control Unit IO Pin 10	IO_10	inout	22	LVCMOS33	IO_DATA[11]	
Control Unit IO Pin 11	IO_11	inout	21	LVCMOS33	IO_DATA[12]	
Control Unit IO Pin 12	IO_12	inout	28	LVCMOS33	IO_DATA[13]	Bank 2
Control Unit IO Pin 13	IO_13	inout	27	LVCMOS33	IO_DATA[14]	
Control Unit IO Pin 14	IO_14	inout	24	LVCMOS33	IO_DATA[15]	
Control Unit IO Pin 15	IO_15	inout	23	LVCMOS33	IO_DATA[16]	
Control Unit IO Pin 16	IO_16	inout	34	LVCMOS33	IO_DATA[17]	
Control Unit IO Pin 17	IO_17	inout	33	LVCMOS33	IO_DATA[18]	
Control Unit IO Pin 18	IO_18	inout	40	LVCMOS33	IO_DATA[19]	
Control Unit IO Pin 19	IO_19	inout	39	LVCMOS33	IO_DATA[20]	
Control Unit IO Pin 20	IO_20	inout	61	LVCMOS33	IO_DATA[21]	Bank 3
Control Unit IO Pin 21	IO_21	inout	60	LVCMOS33	IO_DATA[22]	
Control Unit IO Pin 22	IO_22	inout	44	LVCMOS33	IO_DATA[23]	
Control Unit IO Pin 23	IO_23	inout	45	LVCMOS33	IO_DATA[24]	
Control Unit IO Pin 24	IO_24	inout	38	LVCMOS33	IO_DATA[25]	
Control Unit IO Pin 25	IO_25	inout	35	LVCMOS33	IO_DATA[26]	
Control Unit IO Pin 26	IO_26	inout	42	LVCMOS33	IO_DATA[27]	
Control Unit IO Pin 27	IO_27	inout	41	LVCMOS33	IO_DATA[28]	
Control Unit IO Pin 28	IO_28	inout	59	LVCMOS33	IO_DATA[29]	Bank 4
Control Unit IO Pin 29	IO_29	inout	58	LVCMOS33	IO_DATA[30]	
Control Unit IO Pin 30	IO_30	inout	47	LVCMOS33	IO_DATA[31]	
Control Unit IO Pin 31	IO_31	inout	48	LVCMOS33	IO_DATA[32]	
Control Unit IO Pin 32	IO_32	inout	69	LVCMOS33	IO_DATA[33]	
Control Unit IO Pin 33	IO_33	inout	68	LVCMOS33	IO_DATA[34]	

Control Unit IO Pin 34	IO_34	inout	63	LVCMOS33	IO_DATA[35]	Bank 5
Control Unit IO Pin 35	IO_35	inout	62	LVCMOS33	IO_DATA[36]	
Control Unit IO Pin 36	IO_36	inout	83	LVCMOS33	IO_DATA[37]	
Control Unit IO Pin 37	IO_37	inout	82	LVCMOS33	IO_DATA[38]	
Control Unit IO Pin 38	IO_38	inout	93	LVCMOS33	IO_DATA[39]	
Control Unit IO Pin 39	IO_39	inout	92	LVCMOS33	IO_DATA[40]	
Control Unit IO Pin 40	IO_40	inout	71	LVCMOS33	IO_DATA[41]	Bank 6
Control Unit IO Pin 41	IO_41	inout	70	LVCMOS33	IO_DATA[42]	
Control Unit IO Pin 42	IO_42	inout	67	LVCMOS33	IO_DATA[43]	
Control Unit IO Pin 43	IO_43	inout	65	LVCMOS33	IO_DATA[44]	
Control Unit IO Pin 44	IO_44	inout	81	LVCMOS33	IO_DATA[45]	
Control Unit IO Pin 45	IO_45	inout	78	LVCMOS33	IO_DATA[46]	
Control Unit IO Pin 46	IO_46	inout	91	LVCMOS33	IO_DATA[47]	
Control Unit IO Pin 47	IO_47	inout	89	LVCMOS33	IO_DATA[48]	
Control Unit IO Pin 48	IO_48	inout	95	LVCMOS33	IO_DATA[49]	Bank 7
Control Unit IO Pin 49	IO_49	inout	94	LVCMOS33	IO_DATA[50]	
Control Unit IO Pin 50	IO_50	inout	85	LVCMOS33	IO_DATA[51]	
Control Unit IO Pin 51	IO_51	inout	84	LVCMOS33	IO_DATA[52]	
Control Unit IO Pin 52	IO_52	inout	103	LVCMOS33	IO_DATA[53]	
Control Unit IO Pin 53	IO_53	inout	100	LVCMOS33	IO_DATA[54]	
Control Unit IO Pin 54	IO_54	inout	107	LVCMOS33	IO_DATA[55]	
Control Unit IO Pin 55	IO_55	inout	106	LVCMOS33	IO_DATA[56]	
Control Unit IO Pin 56	IO_56	inout	97	LVCMOS33	IO_DATA[57]	Bank 8
Control Unit IO Pin 57	IO_57	inout	96	LVCMOS33	IO_DATA[58]	
Control Unit IO Pin 58	IO_58	inout	87	LVCMOS33	IO_DATA[59]	
Control Unit IO Pin 59	IO_59	inout	86	LVCMOS33	IO_DATA[60]	
Control Unit IO Pin 60	IO_60	inout	99	LVCMOS33	IO_DATA[61]	
Control Unit IO Pin 61	IO_61	inout	98	LVCMOS33	IO_DATA[62]	
Control Unit IO Pin 62	IO_62	inout	105	LVCMOS33	IO_DATA[63]	
Control Unit IO Pin 63	IO_63	inout	104	LVCMOS33	IO_DATA[64]	
Power LED Red	LEDPowerR	out	109	LVCMOS33	IO_DATA[65]	
Power LED Green	LEDPowerG	out	110	LVCMOS33	IO_DATA[66]	

Control Unit Register Map

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Release date	12.05.2023

base address located

Register Name	Address (Dec)	Address (Hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System Configuration	1	0x01	0x30								
GPIO Driver 0	2	0x02	0x00							Out_enb	Data
GPIO Driver 1	3	0x03	0x00							Out_enb	Data
	.						.				
	.						.				
	.						.				
GPIO Driver 63	65	0x41	0x00							Out_enb	Data
PWM Driver 0	66	0x42	0x00	PWM[7:0]							
PWM Driver 1	67	0x43	0x00	PWM[7:0]							
	.						.				
	.						.				
	.						.				
PWM Driver 15	81	0x51	0x00	PWM[7:0]							
Power LED Red	82	0x52	0x00	on/off	Blink_enb	Delay_on			Delay_off		
Power LED Green	83	0x53	0x00	on/off	Blink_enb	Delay_on			Delay_off		

Crossbar Operation

The GOLDI Control Unit IO uses a crossbar structure associated with each bank to multiplex and demultiplex the IO signals from and into different modules. This increases the functionality of the board and provides each pin with multiple modes. The crossbar structure uses the SPI interface to configure the pins.

Crossbar selection

The GOLDI Control Unit has a total of 8 crossbar structures corresponding to each pin bank. The "selected_bus" byte in the control register 0x01 must be selected to choose a crossbar structure to read or modify. Once a structure is selected the SPI-transmitted data is interpreted differently.

READ_ADDRESS	Read right crossbar pin address #Pin+2 configuration
WRITE_ADDRESS	Write right crossbar pin address #Pin+2 configuration
READ_DATA	Associated left crossbar pin read
WRITE_DATA	New associated left crossbar pin written

The module is enabled for an SPI transaction by a logic low on the chip select input nCE0. Bit transfer is synchronous to the bus clock SCLK, with the slave latching the data from MOSI on the rising edge of SCLK and driving data to MISO on the falling edge. The most significant bit is sent first. A minimum of 24 SCLK clock cycles is required for a bus transaction.

(CONFIGURATION_WORD[15:0] + DATA_WORD[7:0])

If more than 24 clocks are driven, the additional bits shifted into MOSI are assigned to increasing lower pins. If a read transaction with 24+n*8 clocks is performed then the MISO shifts the data of the selected pins and the pins (#Pin - n). If a write transaction with 24+n*8 clocks is performed the MOSI shifts the data to the selected pin and the pins (#Pin - n)

nCE0 must be low during the whole SPI transaction. When nCE0 goes high, the unfinished transaction is discarded. The MOSI data is latched once the DATA_WORD is transferred

The configuration word length is based on the value "BUS_ADDRESS_WIDTH" in the GOLDI_COMM_STANDARD package. This corresponds to the address width + 1 bit for the write enable flag. The data word length is based on the value "SYSTEM_DATA_WIDTH" in the GOLDI_COMM_STANDARD package. This value corresponds to the number of data bits

Default configuration for the GOLDI Control Unit model

BUS_ADDRESS_WIDTH	15
SYSTEM_DATA_WIDTH	8

Crossbar default dimensions

Left crossbar size	10
Right crossbar size	8

Configuration Word [15:0]			Data Word[7:0]
Bit 15	**Bit [14:8]**	**Bit [7:0]**	**Bit [7:0]**
WE	RIGHT_PIN_ADDRES		DATA[MSBF]
0	RIGHT_PIN_NUMBER + 2		[MOSI: dc] | [MISO: Left pin associated]
1	RIGHT_PIN_NUMBER + 2		[MOSI: New left pin] | [MISO: Left pin associated]

Example:

To change the right pin #7 in bank 1 originally associated with the GPIO Driver 7 module to the PWM Driver 0 the following steps are needed

1. Select bank 1 crossbar by writing x"01" to the control register -> SPI [x"0001" / x"01"]
2. Calculate pin address by adding 2 to the right crossbar pin number -> #Pin(7) + 2 = 9
3. Look up left crossbar pin in bank 1 associated with PWM Driver 0 -> #Pin(8)
4. SPI write transaction with the right pin address and left pin number -> SPI [x"0009" / x"08"]
5. Select normal operation by writing x"00" to the control register -> SPI [x"0001" / x"00"]

Bank Pinout

Bank 1 [selected_bus = x"1"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 0	2	0x02	0	0	0
GPIO Driver 1	3	0x03	1	1	1
GPIO Driver 2	4	0x04	2	2	2
GPIO Driver 3	5	0x05	3	3	3
GPIO Driver 4	6	0x06	4	4	4
GPIO Driver 5	7	0x07	5	5	5
GPIO Driver 6	8	0x08	6	6	6
GPIO Driver 7	9	0x09	7	7	7
PWM Driver 0	66	0x42	8	-	
PWM Driver 1	67	0x43	9	-	

Bank 2 [selected_bus = x"2"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 8	10	0x0A	0	0	8
GPIO Driver 9	11	0x0B	1	1	9
GPIO Driver 10	12	0x0C	2	2	10
GPIO Driver 11	13	0x0D	3	3	11
GPIO Driver 12	14	0x0E	4	4	12
GPIO Driver 13	15	0x0F	5	5	13
GPIO Driver 14	16	0x10	6	6	14
GPIO Driver 15	17	0x11	7	7	15
PWM Driver 2	68	0x44	8	-	
PWM Driver 3	69	0x45	9	-	

Bank 3 [selected_bus = x"3"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 16	18	0x12	0	0	16
GPIO Driver 17	19	0x13	1	1	17
GPIO Driver 18	20	0x14	2	2	18
GPIO Driver 19	21	0x15	3	3	19
GPIO Driver 20	22	0x16	4	4	20
GPIO Driver 21	23	0x17	5	5	21
GPIO Driver 22	24	0x18	6	6	22
GPIO Driver 23	25	0x19	7	7	23
PWM Driver 4	70	0x46	8	-	
PWM Driver 5	71	0x47	9	-	

Bank 4 [selected_bus = x"4"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 24	26	0x1A	0	0	24
GPIO Driver 25	27	0x1B	1	1	25
GPIO Driver 26	28	0x1C	2	2	26
GPIO Driver 27	29	0x1D	3	3	27

GPIO Driver 28	30	0x1E	4	4	28
GPIO Driver 29	31	0x1F	5	5	29
GPIO Driver 30	32	0x20	6	6	30
GPIO Driver 31	33	0x21	7	7	31
PWM Driver 6	72	0x48	8	-	
PWM Driver 7	73	0x49	9	-	

Bank 5 [selected_bus = x"5"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 32	34	0x22	0	0	32
GPIO Driver 33	35	0x23	1	1	33
GPIO Driver 34	36	0x24	2	2	34
GPIO Driver 35	37	0x25	3	3	35
GPIO Driver 36	38	0x26	4	4	36
GPIO Driver 37	39	0x27	5	5	37
GPIO Driver 38	40	0x28	6	6	38
GPIO Driver 39	41	0x29	7	7	39
PWM Driver 8	74	0x4A	8	-	
PWM Driver 9	75	0x4B	9	-	

Bank 6 [selected_bus = x"6"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 40	42	0x2A	0	0	40
GPIO Driver 41	43	0x2B	1	1	41
GPIO Driver 42	44	0x2C	2	2	42
GPIO Driver 43	45	0x2D	3	3	43
GPIO Driver 44	46	0x2E	4	4	44
GPIO Driver 45	47	0x2F	5	5	45
GPIO Driver 46	48	0x30	6	6	46
GPIO Driver 47	49	0x31	7	7	47
PWM Driver 10	76	0x4C	8	-	
PWM Driver 11	77	0x4D	9	-	

Bank 7 [selected_bus = x"7"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 48	50	0x32	0	0	48
GPIO Driver 49	51	0x33	1	1	49
GPIO Driver 50	52	0x34	2	2	50
GPIO Driver 51	53	0x35	3	3	51
GPIO Driver 52	54	0x36	4	4	52
GPIO Driver 53	55	0x37	5	5	53
GPIO Driver 54	56	0x38	6	6	54
GPIO Driver 55	57	0x39	7	7	55
PWM Driver 12	78	0x4E	8	-	
PWM Driver 13	79	0x4F	9	-	

Bank 8 [selected_bus = x"8"]					
Module Name	**Address (Dec)**	**Address (Hex)**	**CB - Left pin**	**CB - Right Pin**	**FPGA Pin**
GPIO Driver 56	58	0x3A	0	0	56
GPIO Driver 57	59	0x3B	1	1	57
GPIO Driver 58	60	0x3C	2	2	58
GPIO Driver 59	61	0x3D	3	3	59
GPIO Driver 60	62	0x3E	4	4	60
GPIO Driver 61	63	0x3F	5	5	61
GPIO Driver 62	64	0x40	6	6	62
GPIO Driver 63	65	0x41	7	7	63
PWM Driver 12	80	0x50	8	-	
PWM Driver 13	81	0x51	9	-	