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| **Partner 3** | **Organisation name / Department:**  **UJF-VERIMAG** |  |
| **Expertise:** UJF-VERIMAG - Université Joseph Fourier Grenoble 1: UJF-VERIMAG is one of the main European labs in embedded systems. It develops theory, methods and tools for safety critical and embedded systems. It has been established in 1993. It is a research lab associated with the CNRS, Université Joseph Fourier, and the INPG Technical University. Currently, it has a total staff of 90 persons including 30 permanent researchers, 15 researchers under contract and 40 Ph.D. students. UJF-VERIMAG carries out research in the area of embedded systems design. It aims to produce theoretical and practical tools for the cost-effective development of embedded systems of guaranteed quality. Quality includes dependability properties such as security, safety, availability and performance.  UJF-VERIMAG’s results have given rise to transfer and to numerous contractual relations implying Verilog, Schneider Electric (nuclear plants), EADS for the development of safety critical systems in Airbus, Prover-Technology for a verification tool dedicated to Lustre, and Esterel-Technologies. Other industrial partners of UJF-VERIMAG are STMicroelectronics, Alcatel, CS-Transport, EDF, France Telecom, IBM, Intrasoft, ISD, Leti/CEA, Prover Technology, RATP, Silicomp, Trusted Logic.  UJF-VERIMAG has well-recognised competences in synchronous languages, validation and verification with focus on security and safety, modelling and temporal and hybrid systems analysis. It plays a significant role in real-time embedded systems. UJF- VERIMAG has been and is currently involved in many European projects: LTR VIRES (Verification of Real time systems), IST Crisys, IST Interval, IST SafeAir I & II (Advanced Design Tools for Aircraft Systems and Airborne Software) and Agedis IST Next-TTA (01-03), RISE, AMETIST, ASSERT, SPEEDS, PRO3D, CERTAINTY, D-MILS, ASCENS, SMECY, CyPhERS, and ACROSS. VERIMAG coordinated the projects OMEGA (Correct Development of Real-Time Embedded Systems) CC, COMBEST. VERIMAG coordinated the IST-004527 ARTIST2 NoE on Embedded Systems (http://www.artist-embedded.org). The NoE includes 35 partners representing the top research teams in embedded systems design.  **Prof Saddek Bensalem** is Professor in Computer Science. His research is centered around the design of computer systems, notably embedded systems, with emphasis on the formalization of design processes and techniques that ensure correction by construction.  **Dr Marius Bozga** is research at VERIMAG laboratory. He has conducted research and tool development for modelling and verification of distributed real-time systems. His work focuses actually on modelling, analysis and efficient implementation of Embedded systems.   1. N. Ben Said, T. Abdellatif, S. Bensalem, M. Bozga Model-driven Information Flow Security for Component-Based Systems In *FPS'14 ETAPS Workshop.* 2. S. Bensalem, M. Bozga, J. Quilbeuf and J. Sifakis Optimized Distributed Implementation of Multiparty Interactions with Restriction In *Science of Computer Programming*, 2014. 3. A. Basu, S. Bensalem, M. Bozga, J. Combaz, M. Jaber, T-H. Nguyen, J. Sifakis Rigorous Component-Based System Design Using the BIP Framework In *IEEE Software*, 28(3): 41-48 (2011). 4. S. Bensalem, A. Legay, M. Bozga Rigorous embedded design: challenges and perspectives In *Software Tools for Technology Transfer (STTT)* 15(3):149-154(2013). 5. A. Basu, S. Bensalem, M. Bozga, B. Delahaye, A. Legay Statistical abstraction and model-checking of large heterogeneous systems In *Software Tools for Technology Transfer (STTT)* 14(1):53-72(2012). | | |
| **Role in project:** UJF-VERIMAG will contribute across the full project and particularly we will coordinate WP2 System Design and Implementation which is at the core of the project, and will contribute to all other work packages. | | |